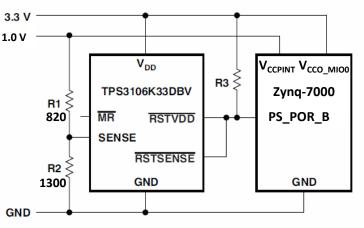
Example PS_POR_B Supervisor Circuit (Just one example of many possible implementations)

- An example device is the TI TPS3106K33DBV with an input sense threshold of 0.551V and valid reset assertion with a minimum V_{DD} of 0.4V
 - This device is appropriate for V_{DD} powering from 3.3V $V_{\text{CCO}_\text{MIO0}}$ and sensing of a second power supply
 - Powering V_{DD} from V_{CCPINT} is not recommended for this device
- The key criteria for selecting a supervisor circuit is the minimum V_{DD} level that will guarantee a valid assertion of PS_POR_B to GND
 - The minimum V_{DD} level should be 0.60V when powered by V_{CCPAUX} or 0.80V when powered by V_{CCO_MIO0} to ensure that either the external supervisor circuit or the internal POR monitor is asserting reset within the device.



Note: R1 and R2 were selected to create 0.551V at the sense pin when V_{CCPINT} has dropped to ${\sim}0.90V$

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Additional PS_POR_B Supervisor Circuit Guidelines

> For any new designs review the customer systems to ensure

- PS_POR_B is held low during power-on until the PS power supplies reach minimum levels as required by the datasheets and TRM
- PS_POR_B is asserted low during the power-off sequence, before V_{CCPINT} reaches 0.80V and held asserted low until V_{CCPINT} is lower than 0.40V or V_{CCPAUX} is lower than 0.70V or V_{CCO_MIO0} is lower than 0.90V
- If PS_POR_B is driven by a supervisor circuit it must guarantee assertion to GND when its V_{DD} supply is 0.30V if powered by V_{CCPINT}, 0.60V if powered by V_{CCPAUX} or 0.80V if powered by V_{CCO_MIO0}
 - If another supply is used then it must be guaranteed to be valid for the entire power-on and power-off phase