## AR#58873 - MIG 7 Series DDR3 - Automated Trace Matching

## **Checker against MIG 7 Series DDR3 Requirements**

## Quick User Guide

## Introduction

This document describes how to use the automatic tool to verify the matching rules for the DDR3 MIG IP.

First, please read the Notes and "How to use the tool" sections in the Answer Record or on the first sheet of the tool.

The Notes are listed below.

#### Notes

- 1. This Checker only works on Windows.
- 2. Macros must be enabled in Excel.
- The ISE or Vivado executable path must be defined in the environment variable "PATH". For example:

Set PATH=c:\Work\program\145\14.5\ISE\_DS\ISE\bin\nt64; %PATH% Set PATH=C:\Work\program\20134\Vivado\2013.4\bin; %PATH%

- Stripline is used for all signals. V=C \* Sqr(Er) is used to calculate flight time on the PCB. Here C = 3 E-10 cm/s.
- 5. In the FPGA Rating list, "HP/HR" is the bank type. "2.0/1.8" is the Vccaux\_io power. "L" means an FBG package. For an FFG package use the options without "L".
- 6. In the FPGA Working mode list, "4:1/2:1" means memory/user clock ratio. "1.5V/1.35V" means DDR3 or DDR3L. "L" means the Vccint is 0.9V. For Vccint with 1.0V use the options without "L".
- 7. In the Design Flow list, "ISE" means an ISE flow. "Vivado" means a Vivado Flow. "Bypass" means no PKG file is generated. If "Bypass" is selected, the user should find all information.
- 8. When this check is used to get package delay automatically, all DDR3 signals must use the default MIG output signal name.
- 9. The UCF/XDC file MUST be MIG within the default output. Use "Board File" to select the PCB layout length file.
- 10. If Board File is Selected, the signal name of DDR3 MUST use the default MIG signal name.
- 11. "Adherence to Rule" in the TotalDelay table means the length relationship between CK/Addr or DQS/DQ BEFORE PCB layout. This can help PCB layout constraint.

- 12. The current table can only support verification of address/control signals for one component. If other address/control skew is required, please enter new values for the new component.
- The "Use DM" option is used when ECC is enabled and DM is ignored. "NO" means no DM is used.
- 14. The Board\_File\_Example sheet shows an example file format. The first column MUST be the signal name and the second column must be the route length (mil).
- 15. A positive Adherence value means that the signal should be longer than CK or DQS. A negative value means the signal should be shorter than CK or DQS on the board.
- 16. A value of zero in the Derating Table means that the value in the Overview option is not valid.
- 17. Matching length for differential pins (CK/CK#, DQS/DQS#) is added for the adherence column. The differential I/O should be same length including Flight time and route length.

# Guideline

Detailed steps to use the tool are described below:

1. When a standard flight time file is generated already, select "Bypass" in the Design Flow drop-down.

This will not involve ISE/Vivado in generating the flight time file.

Only address, control and data information will be generated in the TotalDelay sheet.

If flight time is not ready, please select "Vivado/ISE" for the Design Flow.

2. Select FPGA Type, FPGA Part, Packaging Type, FPGA Speed and FPGA Rating for the FPGA settings. These parameters will contribute to the maximum speed of DDR3 and the derating value.

3. Set MIG IP Settings.

Fill in the DQS group number, Rank Number and Address Number.

Also select the Target DDR3 Speed, DDR3 component Speed Grade and FPGA working Mode. These options will generate the proper DDR3 controller information and contribute to the derating value.

If DM is not used on the board, select "NO" for the "USE DM" option.

4. To select I/O location automatically, choose the XDC file of the default MIG example design or user design for a Vivado flow. For an ISE flow choose the UCF file of the default MIG example design or user design.

5. To find the route length information automatically, choose a Board file. The board file format must be the same as in the Board\_File\_Example sheet.

6. Fill in the PCB dielectric Constant. This will define the relationship between route length and route time.

After all options are selected, the tool will look like figure 1.

	11 1/10	Artix-7, Kintex-7, Virtex-7		Version 1.1
Series	MIG DDR3 PCB I	ayout Requriement: Pleas	<u>se see "Design Guidl</u>	ines'' on UG586
FPG4	A Settings	MIG IP Set	tings	PCB Settings
esign Flow	Vivado 🔻	DQS group number	2	PCB dielectric constant 4.5
PGA Type	Kintex7 -	Rank Number	1	
GA Part	XC7K325T -	Address Number	14	
ckaging Type	FFG900 -	Target DDR3 Speed(Mbps)	1334~1600 🚽	
GA speed	-2 -	DDR3 component Speed grade(Mbps)	1866 👻	
PGA Rating	HP_2.0 •	FPGA Working Mode	4:1 1.57	
		Use DM?	YES -	
True de				P
Envi	ronment Settings			Kun
JCF/XDC Fil	e C:\Work\project\MIG\prj	<pre>\pcbskew\m1g_(s_ddr), xdc</pre>		Generate PKG
Board File	C:\work\project\miG\prj	<pre>\pcbskew\iraceLengtnExample.xis</pre>		Upen PKG

Figure 1 - Vivado Flow option example

7. Click the Generate PKG button. A command line window will open as shown in figure 2.



Figure 2 - Flight time generation

This window shows the process of flight time file generation. After the file generation is done, the window will close automatically. If "Bypass" is selected in Design flow, this window will not appear. The flight time file is generated in the TMP folder defined in the Windows Environment.

8. DDR3 and derating information will be generated in the TotalDelay sheet as shown in figure 3.

Memory Total	Delay Calcula	tion															
				_		_											
10 pins	PCB Route length(mil)	PCB Route Delay(ps)	Package Min Delay(ps)	Package Max Delay(ps)	Total Min Delay(ps)	Total Max Delay(ps)	Addr/Ctrl Pass?	DQ/DQS Pass?	CK/DQS Pass?	Adherance to Rule BEFORE Layout(ps)	Adherance to Rule AFTER Layout(ps)	Calcul	ate Tota	l Delay			
																Derating T	able
ddr3_ba[2]															DQS/DQ	Addr/CK	DQS/CK (ps)
ddr3_ba[1]													Verify		49.5	114.1	1600
ddr3_ba[0]																	
ddr3_ras_n																	
ddr3_cas_n																	
ddr3_we_n												R	eset Tabl	les			
ddr3_reset_n												<u></u>			1		
ddr3_cke[0]																	
ddr3_odt[0]																	
ddr3_cs_n[0]																	
ddr3_ck_p[U]																	
ddr3_ck_n[U]																	
ddr3_addr[0]																	
ddr3_addr[1]																	
ddr3_addr[2]												Notes					
ddr3_addr[4]												1 Boritivo	Adherance	volue mean	e cienol che	uld he les	near than CK or DO
ddr3_addr[4]												Negative v	Autoriatice	signal shou	id he short	erthan CK	or DOS on baard
ddr3_addr[6]												2 Zero in l	Derating Tall	o means th	e value in	Overview	nion is not valid
ddr3_addr[7]												please ma	ke sure tare	et rating and	1 compome	nt rating a	re valid.
ddr3_addr[8]												3. The colo	r field shou	ld not be me	odified by	user.	
ddr3_addr[9]																	
ddr3 addr[10]																	
ddr3 addr[11]																	
ddr3 addr[12]																	
ddr3_addr[13]																	
ddr3_dq[0]																	
ddr3_dq[1]																	
ddr3_dq[2]																	
ddr3_dq[3]																	
ddr3_dq[4]																	
ddr3_dq[5]																	
ddr3_dq[6]																	

Figure 3 - DDR3 and derating information

Address, control and DQ/DQS are all generated. Derating values for DQS/DQ, ADDR/CK and CK/DQS are also generated.

9. Click the Open PKG button.

XDC/UCF, Board File and flight time files will be opened in a new Excel window.

Flight time and route length will be filled into the TotalDelay sheet automatically as in figure 4.

If PCB route information and constraint information are required automatically, Vivado or ISE must be selected in the Design Flow list. For Vivado the XDC file format will be executed and for ISE the UCF file format will be executed for the constraint file.

10 pins	PCB Route length(mil)	PCB Route Delay(ps)	Package Min Delay(ps)	Package Max Delay(ps)	Total Min Delay(ps)	Total Max Delay(ps)	Addr/Ctrl Pass?	DQ/DQS Pass?	CK/DQS Pass?	Adherance to Rule BEFORE Layout(ps)	Adherance to Rule AFTER Layout(ps)	Calcul	ate Tota	l Delay			
																Derating T	able
ddr3_ba[2]	2278.8284		123.657	124.899											DQS/DQ	Addr/CK	DQS/CK (ps)
ddr3_ba[1]	2241.4827	1	135.142	136.5	1								verily		49.5	114.1	1600
ddr3_ba[0]	2251.9287		120.774	121.988	1												
ddr3_ras_n	2317.7391		123.379	124.615	-												
ddr3_cas_n	2284.785		129.264	130.564	1												
ddr3_we_n	2293.0299		131.704	133.028	1							Re	eset Tab	les			
ddr3_reset_n	2121.5951		147.818	149.304	1												
ddr3_cke[0]	2275,7535		160.652	162.266	-												
ddr3_odt[0]	2370.9198		171.037	172.755	i												
ddr3_cs_n[0]	1485.8741		160.151	. 161.761	_												
ddr3_ck_p[0]	2295.1286		142.592	144.026													
ddr3_ck_n[0]	2295.4249		147.635	149.115	-												
ddr3_addr[0]	2183.2557		144.011	. 145.459													
ddr3_addr[1]	2132.4689		140.613	142.021	-												
ddr3_addr[2]	2235.7497		157.554	159.138													
ddr3_addr[3]	2159.3866		144.703	146.15								Note:					
ddr3_addr[4]	2269,4446		148.294	149.784								1. Positive	Adherance	value mean	s signal sho	ould be lo	nger than CK or D
ddr3_addr[5]	2069.7289		139.095	140.493								Negative	alue means	signal shou	Id be short	er than CK	or DQS on baord.
ddr3_addr[6]	2193.6347		120.027	121.235	-							2. zero in L	Derating Tal	be means th	e value in i	overview	opion is not valid.
ddr3_addr[7]	2068.5446		120.649	121.861	-							please ma	ke sure targ	et rating and	1 compome	ent rating a	re valid.
ddr3_addr[8]	2114.7961		120.901	122.117								3. The colo	or field shou	ld not be m	dified by a	user.	
ddr3_addr[9]	2052.9443		122.596	123.828													
ddr3_addr[10]	2148.7151	-	118.682	119.874	-												
ddr3_addr[11]	2200.8613		149.31	150.81	-												
ddr3_addr[12]	2180.5319		148.897	150.393													
ddr3_addr[13]	2209.7485		129.334	130.634													
ddr2 do[0]	1917 7702		119 736	119.93													
ddr3_dq[0]	1762 8071		110.730	120.273													
ddr3_do[2]	1864 787		139.946	140.241													
ddr3_dd[3]	1928 7946		142 446	143.879													
ddr3_dq[4]	1720.958		140.076	141.494													
ddr3_dq[4]	1929.2763		140.564	141.976													
ddr3_dq[6]	1790.8215		155.088	156.646													
amo_ad[o]	1750.0215		155.086	136.646	-												

Figure 4 - Flight time and route delay loaded

10. In the TotalDelay sheet, click the Calculate Total Delay button. This function will use the PCB electronic constant to transfer route length to route time on the PCB. The route time will appear in the PCB Route Delay column in ps.

Minimum and maximum Flight time plus the PCB route delay are filled into the Total Min/Max column. Figure 5 shows this step.

Memory Total	Delay Calcula	tion															
10 pins	PCB Route length(mil)	PCB Route Delay(ps)	Package Min Delay(ps)	Package Max Delay(ps)	Total Min Delay(ps)	Total Max Delay(ps)	Addr/Ctrl Pass?	DQ/DQS Pass?	CK/DQS Pass?	Adherance to Rule BEFORE Layout(ps)	Adherance to Rule AFTER Layout(ps)	Calcul	ate Tota	l Delay			
																Derating T	ible
ddr3_ba[2]	2278.8284	410.900629	123.657	124.899	534.55763	535.79963									DQS/DQ	Addr/CK	DQS/CK (ps)
ddr3_ba[1]	2241.4827	484.166742	135.142	136.5	539.30874	540.66674							verity		49.5	114.1	1600
ddr3_ba[0]	2251.9287	406.050284	120.774	121.988	526.82428	528.03828											
ddr3_ras_n	2317.7391	417.916704	123.379	124.619	541.2957	542.5357											
ddr3_cas_n	2284.785	411.974677	129.264	130.564	541.23868	542.53868						Pe	ant Tabl				
ddr3_we_h	2121 5051	413.461333	131.704	133.020	545.16533	546.46333						Reset Tables					
ddr3_reset_n	2121.0901	410 246107	147.818	149.304	570 99919	572 61219											
ddr3_odt[0]	2270.9198	427,505834	171.037	172.755	598 54283	600.26083											
ddr3 cs n[0]	1485.8741	267.921271	160.151	161.761	428.07227	429,68227											
ddr3 ck p[0]	2295,1286	413,839754	142.592	144.026	556.43175	557.86575											
ddr3 ck n[0]	2295.4249	413.893181	147.635	149.119	561.52818	563.01218											
ddr3_addr[0]	2183.2557	393.667702	144.011	145.459	537.6787	539.1267											
ddr3_addr[1]	2132.4689	384.510221	140.613	142.027	525.12322	526.53722											
ddr3_addr[2]	2235.7497	403.133012	157.554	159.138	560.68701	562.27101											
ddr3_addr[3]	2159.3866	389.363812	144.703	146.157	534.06681	535.52081						Note:					
ddr3_addr[4]	2269.4446	409.208615	148.294	149.784	557.50261	558.99261						1. Positive	Adherance	value mean:	s signal sho	uld be lor	ger than CK or DQS.
ddr3_addr[5]	2069.7289	373.197432	139.095	140.493	512.29243	513.69043						Negative v	alue means	signal shoul	d be short	er than CK	or DQS on baord.
ddr3_addr[6]	2193.6347	395.539163	120.027	121.233	515.56616	516.77216						2. Zero in D	Derating Tall	e means th	e value in C	Overview o	pion is not valid.
ddr3_addr[7]	2068.5446	372.983888	120.649	121.861	493.63289	494.84489						please mai	ke sure targe	t rating and	compome	nt rating a	/e valid.
ddr3_addr[8]	2114.7961	381.323599	120.901	122.117	502.2246	503.4406						3. The colo	r field shoul	d not be mo	dified by u	iser.	
ddr3_addr[9]	2052.9443	370.170963	122.596	123.828	492.76696	493.99896											
ddr3_addr[10]	2148.7151	387.43961	118.682	119.874	505.12151	507.31361											
ddr3_addr[11]	2100.0013	330.042207	149.51	150.00	540.15221	547.65221											
ddr3_addr[13]	2209.7485	398.444678	129.334	130.634	527,77868	529.07868											
						027101000											
ddr3_dq[0]	1917.7702	345.79742	118.736	119.93	464.53342	465.72742											
ddr3_dq[1]	1762.8071	317.855678	119.081	120.277	436.93668	438.13268											
ddr3_dq[2]	1864.787	336.243901	138.846	140.242	475.0899	476.4859											
ddr3_dq[3]	1928.7946	347.785254	142.446	143.878	490.23125	491.66325											
ddr3_dq[4]	1720.958	310.309773	140.076	141.484	450.38577	451.79377											
ddr3_dq[5]	1929.2763	347.87211	140.564	141.976	488.43611	489.84811											
ddr3_dq[6]	1790.8215	322.907017	155.088	156.646	477.99502	479.55302											

Figure 5 - Route delay and total delay time generation

11. Click the Verify button on the TotalDelay sheet. Matching rules will be applied and checked. Results are filled into the corresponding columns as in figures 6 and 7.

Memory rota	Delay Calcula	uon									
IO pins	PCB Route length(mil)	PCB Route Delay(ps)	Package Min Delay(ps)	Package Max Delay(ps)	Total Min Delay(ps)	Total Max Delay(ps)	Addr/Ctrl Pass?	DQ/DQS Pass?	CK/DQS Pass?	Adherance to Rule BEFORE Layout(ps)	Adherance to Rule AFTER Layout(ps)
ddr3_ba[2]	2278.8284	410.900629	123.657	124.899	534.55763	535.79963	YES			-88.6379984741211~136.836	-85.6454202169961~139.828550386081
ddr3_ba[1]	2241.4827	404.166742	135.142	136.5	539.30874	540.66674	YES			-100.122998474121~125.235	-90.3965337988657~134.961436804212
ddr3_ba[0]	2251.9287	406.050284	120.774	121.988	526.82428	528.03828	YES			-85.7549984741211~139.747	-77.9120753451157~147.589895257962
ddr3_ras_n	2317.7391	417.916704	123.379	124.619	541.2957	542.5357	YES			-88.3599984741211~137.116	-92.3834952738284~133.092475329249
ddr3_cas_n	2284.785	411.974677	129.264	130.564	541.23868	542.53868	YES			-94.2449984741211~131.171	-92.3264680414641~133.089502561613
ddr3_we_n	2293.0299	413.461333	131.704	133.028	545.16533	546.48933	YES			-96.6849984741211~128.707	-96.2531243400164~129.138846263061
ddr3_reset_n	2121.5951	382.549542	147.818	149.304	530.36754	531.85354	YES			-112.798998474121~112.431	-81.4553333891197~143.774637213958
ddr3_cke[0]	2275.7535	410.346187	160.652	162.266	570.99819	572.61219	YES			-125.632998474121~99.469	-122.085978143421~103.015992459656
ddr3_odt[0]	2370.9198	427.505834	171.037	172.755	598.54283	600.26083	YES			-136.017998474121~88.98	-149.630625841382~75.3673447616959
ddr3_cs_n[0]	1485.8741	267.921271	160.151	161.761	428.07227	429.68227	NO			-125.131998474121~99.974	20.839937271767~245.945907874845
ddr3_ck_p[0]	2295.1286	413.839754	142.592	144.026	556.43175	557.86575	NA			5.04299999999998*5.09299999999999	5.0964265135126~5.14642651351267
ddr3_ck_n[0]	2295.4249	413.893181	147.635	149.119	561.52818	563.01218	NA				
ddr3_addr[0]	2183.2557	393.667702	144.011	145.459	537.6787	539.1267	YES			-108.991998474121~116.276	-88.7664936290877*136.50147697399
ddr3_addr[1]	2132.4689	384.510221	140.613	142.027	525.12322	526.53722	YES			-105.593998474121~119.708	-76.2110125070226~149.090958096055
ddr3_addr[2]	2235.7497	403.133012	157.554	159.138	560.68701	562.27101	YES			-122.534998474121~102.597	-111.774803788847~113.35716681423
ddr3_addr[3]	2159.3866	389.363812	144.703	146.157	534.06681	535.52081	YES			-109.683998474121~115.578	-85.1546029990285~140.107367604049
ddr3_addr[4]	2269.4446	409.208615	148.294	149.784	557.50261	558.99261	YES			-113.274998474121~111.951	-108.590406320605~116.635564282473
ddr3_addr[5]	2069.7289	373.197432	139.095	140.493	512.29243	513.69043	YES			-104.075998474121~121.242	-63.3802232468533~161.937747356224
ddr3_addr[6]	2193.6347	395.539163	120.027	121.233	515.56616	516.77216	YES			-85.0079984741211~140.502	-66.6539542559811~158.856016347096
ddr3_addr[7]	2068.5446	372.983888	120.649	121.861	493.63289	494.84489	YES			-85.6299984741211~139.874	-44.7206794738088~180.783291129269
ddr3_addr[8]	2114.7961	381.323599	120.901	122.117	502.2246	503.4406	YES			-85.8819984741211~139.618	-53.3123905427714~172.187580060306
ddr3_addr[9]	2052.9443	370.170963	122.596	123.828	492.76696	493.99896	YES			-87.5769984741211~137.907	-43.85475460458~181.629215998498
ddr3_addr[10]	2148.7151	387.43961	118.682	119.874	506.12161	507.31361	YES			-83.6629984741211~141.861	-57.2094010450933~168.314569557984
ddr3_addr[11]	2200.8613	396.842207	149.31	150.81	546.15221	547.65221	YES			-114.290998474121~110.925	-97.2399986115364~127.975971991541
ddr3_addr[12]	2180.5319	393.176568	148.897	150.393	542.07357	543.56957	YES			-113.877998474121~111.342	-93.1613591791856~132.058611423892
ddr3_addr[13]	2209.7485	398.444678	129.334	130.634	527.77868	529.07868	YES			-94.3149984741211~131.101	-78.8664694549054~146.549501148172

Figure 6 - Addr/Ctrl with CK matching results

If there is any violation, it will be highlighted in red. Green means the check has been passed. In the "Adherence to Rule BEFORE Layout" and "Adherence to Rule AFTER Layout" columns, there is chance that negative values will be displayed. A negative value means that Addr/Ctrl should be shorter than CK on board.

Figure 7 shows the matching results of DQS/DQ and DQs/CK. Similar to figure 6, green indicates a pass but red indicates failure. A negative value means that DQ should be shorter than DQS on board.

ddr3_dq[0]	1917.7702	345.79742	118.736	119.93	464.53342	465.72742	YES		-33.0030002593994~63.457	-66.2904947267551~30.1695052732449
ddr3_dq[1]	1762.8071	317.855678	119.081	120.277	436.93668	438.13268	YES		-33.3479995727539~63.11	-38.6937527216144~57.7642472783857
ddr3_dq[2]	1864.787	336.243901	138.846	140.242	475.0899	476.4859	YES		-53.1129999160767~43.145	-76.8469758244696~19.4110241755305
ddr3_dq[3]	1928.7946	347.785254	142.446	143.878	490.23125	491.66325	YES		-56.7129998207092~39.509	-91.9883288663759~4.23367113362411
ddr3_dq[4]	1720.958	310.309773	140.076	141.484	450.38577	451.79377	YES		-54.3429999351501~41.903	-52.1428482104931~44.1031517895069
ddr3_dq[5]	1929.2763	347.87211	140.564	141.976	488.43611	489.84811	YES		-54.8309998512268~41.411	-90.1931852671827°6.04881473281722
ddr3_dq[6]	1790.8215	322.907017	155.088	156.646	477.99502	479.55302	YES		-69.3549995422363~26.741	-79.7520916353869~16.3439083646131
ddr3_dq[7]	1783.0067	321.497913	162.023	163.651	483.52091	485.14891	YES		-76.2900009155273~19.736	-85.2779876266146~10.7480123733854
ddr3_dqs_p[0]	1724.7369	310.991155	133.17	134.508	444.16116	445.49916	NA	YES	.71700000000013~.724999999999994	2.23576990657324~2.24376990657328
ddr3_dqs_n[0]	1733.1599	312.509925	133.887	135.233	446.39693	447.74293	NA	YES		
ddr3_dm[0]	1813.0007	326.906198	122.884	124.12	449.7902	451.0262	YES		-37.1510000228882~59.267	-51.5472726293165~44.8707273706835
ddr3_dq[8]	1815.2178	327.305968	64.567	65.215	391.87297	392.52097	YES		-37.9860000610352~59.609	-35.9306389305428~61.6643610694571
ddr3_dq[8] ddr3_dq[9]	1815.2178 1984.5193	327.305968 357.833099	64.567 93.071	65.215 94.006	391.87297 450.9041	392.52097 451.8391	YES YES		-37.9860000610352**59.609 -66.4899997711182**30.818	-35.9306389305428~61.6643610694571 -94.9617698028817~2.34623019711825
ddr3_dq[8] ddr3_dq[9] ddr3_dq[10]	1815.2178 1984.5193 1829.8038	327.305968 357.833099 329.936002	64.567 93.071 97.274	65.215 94.006 98.252	391.87297 450.9041 427.21	392.52097 451.8391 428.188	YES YES YES		-37.9860000610352**59.609 -66.4899997711182**30.818 -70.693000793457**26.572	-35.9306389305428°61.6643610694571 -94.9617698028817°2.34623019711825 -71.2676731056915°25.9973268943085
ddr3_dq[8] ddr3_dq[9] ddr3_dq[10] ddr3_dq[11]	1815.2178 1984.5193 1829.8038 1987.9894	327.305968 357.833099 329.936002 358.4588	64.567 93.071 97.274 55.544	65.215 94.006 98.252 56.102	391.87297 450.9041 427.21 414.0028	392.52097 451.8391 428.188 414.5608	YES YES YES YES		-37.9860000610352*59.609 -66.4899997711182*30.818 -70.693000793457*26.572 -28.9629993438721*68.722	-35.9306389305428°61.6643610694571 -94.9617698028817°2.34623019711825 -71.2676731056915°25.9973268943085 -58.0604712694375°39.6245287305625
ddr3_dq[8] ddr3_dq[9] ddr3_dq[10] ddr3_dq[11] ddr3_dq[12]	1815.2178 1984.5193 1829.8038 1987.9894 1822.4564	327.305968 357.833099 329.936002 358.4588 328.611176	64.567 93.071 97.274 55.544 57.292	65.215 94.006 98.252 56.102 57.867	391.87297 450.9041 427.21 414.0028 385.90318	392.52097 451.8391 428.188 414.5608 386.47818	YES YES YES YES		-37.9860000610352*59.609 -66.4899997711182*30.818 -70.6930007934726.572 -28.9629993438721*68.722 -30.711004425049*66.957	-35,9306389305428*61.6643610694571 -94,9617698028817*2.34623019711825 -71,2676731056915*25,9973268943085 -58,0604712544375*39.6245287305625 -29,9608470328486*67.7071529671514
ddr3_dq[8] ddr3_dq[9] ddr3_dq[10] ddr3_dq[11] ddr3_dq[12] ddr3_dq[13]	1815.2178 1984.5193 1829.8038 1987.9894 1822.4564 1884.5049	327.305968 357.833099 329.936002 358.4588 328.611176 339.799279	64.567 93.071 97.274 55.544 57.292 51.852	65.215 94.006 98.252 56.102 57.867 52.373	391.87297 450.9041 427.21 414.0028 385.90318 391.65128	392.52097 451.8391 428.188 414.5608 386.47818 392.17228	YES YES YES YES YES		-37,9860000610352*59,609 -66,4899997711182*30,818 -70,69300079345*26,572 -28,96299993438721*68,722 -30,7110004425049*66,557 -25,2709999084473*72,451	-35.9306389305426*61.6643610694571 -94.9617699028817*2.34623019711825 -71.2676731056915*75.9973268943085 -58.0604712694375*39.6245287305625 -29.9608470328486*57.771525671514 -35.7089503865242*62.0130496134758
ddr3_dq[8] ddr3_dq[9] ddr3_dq[10] ddr3_dq[11] ddr3_dq[12] ddr3_dq[13] ddr3_dq[14]	1815.2178 1984.5193 1829.8038 1987.9894 1822.4564 1884.5049 1857.9627	327.305968 357.833099 329.936002 358.4588 328.611176 339.799279 335.013396	64.567 93.071 97.274 55.544 57.292 51.852 53.811	65.215 94.006 98.252 56.102 57.867 52.373 54.352	391.87297 450.9041 427.21 414.0028 385.90318 391.65128 388.8244	392.52097 451.8391 428.188 414.5608 386.47818 392.17228 389.3654	YES YES YES YES YES YES		-37.966000610852*59.609 -66.48999771182*30.818 -70.6930073945*726.572 -28.9629993438721*68.722 -30.711000425049*66.957 -25.2709999084473*72.451 -27.229999522263*70.472	-35.9306389305428*61.6643610694571 -44.961759802817*2.4623019711825 -71.267672165515*25.997326943005 -58.0604712694375*39.6245287305625 -29.960470328486*67.7071529671514 -35.7089503865242*62.0130496134758 -22.82067136538*64.813928654162
ddr3_dq[8] ddr3_dq[9] ddr3_dq[10] ddr3_dq[11] ddr3_dq[12] ddr3_dq[13] ddr3_dq[14] ddr3_dq[15]	1815.2178 1984.5193 1829.8038 1987.9894 1822.4564 1884.5049 1857.9627 1863.5047	327.305968 357.833099 329.936002 358.4588 328.611176 339.799279 335.013396 336.012687	64.567 93.071 97.274 55.544 57.292 51.852 53.811 72.051	65.215 94.006 98.252 56.102 57.867 52.373 54.352 72.775	391.87297 450.9041 427.21 414.0028 385.90318 391.65128 388.8244 408.06369	392.52097 451.8391 428.188 414.5608 386.47818 392.17228 389.3654 408.78769	YES YES YES YES YES YES YES		-37.966000610352759.609 -66.499999771102730.818 -70.653000793457726.572 -28.9629993438721766.722 -0.711000429049765.957 -25.7709999084473772.451 -27.239955422685770.472 -45.463993701317752.043	-55.93063930542°61.664361064471 -94.9617639028017°2.34623019711025 -71.2676731056315°25.9973263943085 -58.06471269437°39.6245287305625 -29.560470228446°67.072152671514 -55.7089503865242°62.0130496134758 -32.862067136538°64.8139328634162 -52.121357180244°45.3976424891756
ddr3_dq[8] ddr3_dq[9] ddr3_dq[10] ddr3_dq[11] ddr3_dq[12] ddr3_dq[13] ddr3_dq[14] ddr3_dq[15] ddr3_dqs_p[1]	1815.2178 1984.5193 1829.8038 1987.9894 1822.4564 1884.5049 1857.9627 1863.5047 1808.4408	327.305968 357.833099 329.936002 358.4588 328.611176 339.799279 335.013396 336.012687 326.083992	64.567 93.071 97.274 55.544 57.292 51.852 53.811 72.051 70.943	65.215 94.006 98.252 56.102 57.867 52.373 54.352 72.775 71.656	391.87297 450.9041 427.21 414.0028 385.90318 391.65128 388.8244 408.06369 397.02699	392.52097 451.8391 428.188 414.5608 386.47818 392.17228 389.3654 408.78769 397.73999	YES YES YES YES YES YES YES	YES	-37.566000610352753.609 -66.489999771182730.818 -70.6930073367726.572 -38.652993438721766.722 -30.711000442504766.957 -25.270999964473772.451 -37.229995422365770.472 -45.46999959730151752.049 -4381*4.425	- 35.390639930542°F1.664361065471 -94.961759028817°2.34633019711825 -71.2676731056915°725.97326934085 -56.060471264375°38.6245287305655 -29.9600470328486°67.7071529671514 -35.7089530865242°F2.0130495134758 -32.8820671365838°F4.8199328654162 -52.1213575108244°45.3976424891756 -7.65833704676294°7.70233704675292
ddr3_dq[8] ddr3_dq[9] ddr3_dq[10] ddr3_dq[11] ddr3_dq[12] ddr3_dq[13] ddr3_dq[14] ddr3_dq[15] ddr3_dq5_p[1] ddr3_dq5_n[1]	1815.2178 1984.5193 1829.8038 1987.9894 1822.4564 1884.5049 1857.9627 1863.5047 1808.4408 1826.6167	327.305968 357.833099 329.936002 358.4588 328.611176 339.799279 335.013396 336.012687 326.083992 329.361329	64.567 93.071 97.274 55.544 57.292 51.852 53.811 72.051 70.943 75.324	65.215 94.006 98.252 56.102 57.867 52.373 54.352 72.775 71.656 76.081	391.87297 450.9041 427.21 414.0028 385.90318 391.65128 388.8244 408.06369 397.02699 404.68533	392.52097 451.8391 428.188 414.5608 386.47818 392.17228 389.3654 408.78769 397.73999 405.44233	YES YES YES YES YES YES NA NA	YES	-37.966000610852*59.609 -66.489997711182*30.818 -70.6390073945*726.572 -28.9629993438721*68.722 -30.711000425049*66.957 -52.7299995422363*70.451 -27.229995422363*70.472 -45.4699997301917*52.043 4.381*4.425	-35.9306309305428*61.6643610694571 -44.961759602817*2.34623013711825 -71.2675731056515*75.937250934085 -58.0604712694375*39.6245287305625 -29.96047022848*67.7071529671514 -35.708570365242**6213049513475 -32.8920671365838*64.8199328634162 -52.121357510824**45.3976424891756 7.65833704676294**7.70233704676292
ddr3_dq[8] ddr3_dq[9] ddr3_dq[10] ddr3_dq[11] ddr3_dq[12] ddr3_dq[12] ddr3_dq[14] ddr3_dq[15] ddr3_dq5_p[1] ddr3_dm[1]	1815.2178 1984.5193 1829.8038 1987.9894 1822.4564 1884.5049 1857.9627 1863.5047 1808.4408 1826.6167 1937.852	327.305968 357.833099 329.936002 358.4588 328.611176 339.799279 335.013396 336.012687 326.083992 329.361329 349.418414	64.567 93.071 97.274 55.544 57.292 51.852 53.811 72.051 70.943 75.324 66.566	65.215 94.006 98.252 55.102 57.867 52.373 54.352 72.775 71.656 76.081 67.235	391.87297 450.9041 427.21 414.0028 385.90318 391.65128 388.8244 408.06369 397.02699 404.68533 415.98441	392.52097 451.8391 428.188 414.5608 386.47818 392.17228 389.3654 408.78769 397.73999 405.44233 416.65341	YES YES YES YES YES YES YES NA NA YES	YES YES	-77.960000610352759.609 -70.63900793457726.572 -28.9629993437726.572 -29.962999343721766.722 -0.711004245049765.957 -25.2709999084473772.451 -27.2299956422365770.472 -45.4639995790191752.043 4.381*4.425	-55.93063930542°61.664351064471 -94.961769028817°2.34623013711025 -71.267631056315°25.9973268943065 -58.060471264337°39.6245287305655 -29.950847024846°57.771252671514 -35.7089503865242°62.0130496134756 -32.802671365838°64.8199326634162 -52.1213575108244°5.39724424891756 7.65833704676294°7.70233704676292 -60.0420849090166°37.5319150909834

Figure 7 - DQS/DQ and DQS/CK matching results

12. If some options need to be changed, click "Reset Tables" to remove all information on the TotalDelay Sheet. The next check can then be executed.

Tips:

1. When Flight time, constraint files, and Board files are already opened, it is not necessary to select "Vivado/ISE". Just select Bypass. This will save on the time taken to reproduce the files.

2. When MIG IP Settings or PCB Settings are changed, select "Bypass" in the Design Flow to bypass Flight time generation to save time.

3. Make sure that the correct flow is selected when Open PKG is clicked.