XILINX®

Xilinx Answer 53786
7-Series Integrated Block for PCI Express in Vivado

Important Note: This downloadable PDF of an Answer Record is provided to enhance its usability and readability. It is important to note that Answer Records are Web-based content that are frequently updated as new information becomes available. You are reminded to visit the Xilinx Technical Support Website and review (Xilinx Answer 53786) for the latest version of this Answer.

Introduction

This document illustrates the things a user needs to know to use 7 Series Xilinx Integrated PCI Express Block core v1.8 in Vivado 2012.4. All the steps are illustrated with screenshots without minimal description. The provided screenshots and the captions are self-descriptive. This should help users to get quickly familiar with the tool flow while using 7 Series Xilinx Integrated PCI Express Block core v1.8 in their design.

Along with the core output products generation, simulation and debugging of the hardware using Chipscope have also been described. Users who are familiar with generating the core in Coregen will find this document helpful in quick migration from Coregen to Vivado platform.

PCIe Core Output Products Generation (Generate Example Design)

After creating a Vivado project and generating the core as described in PG054, the example design files have to be generated separately by clicking on ‘Generate Output Products’ as show in Figure 1.

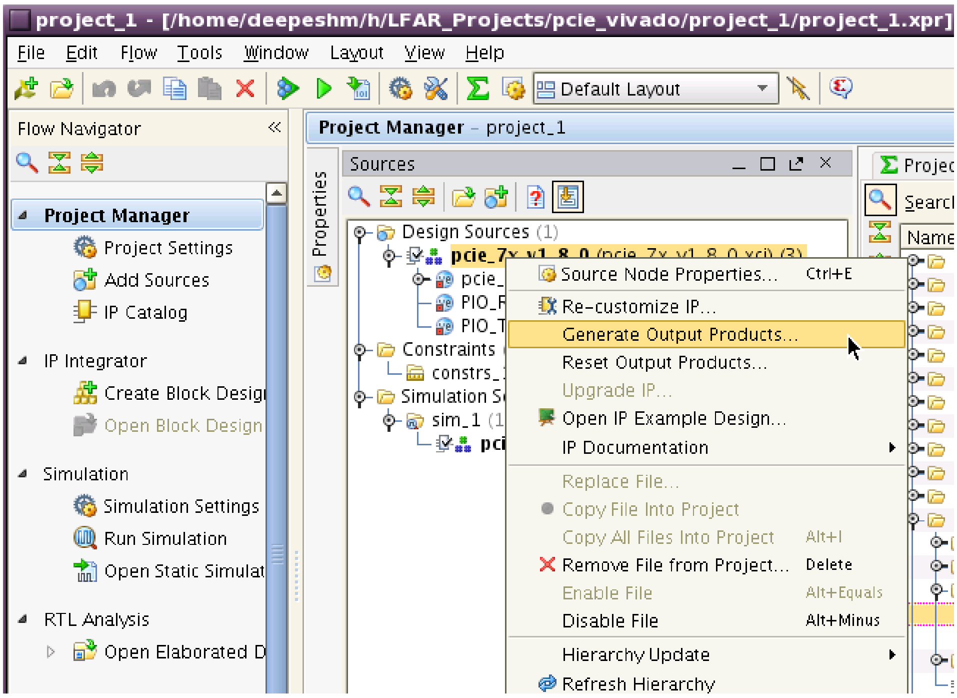
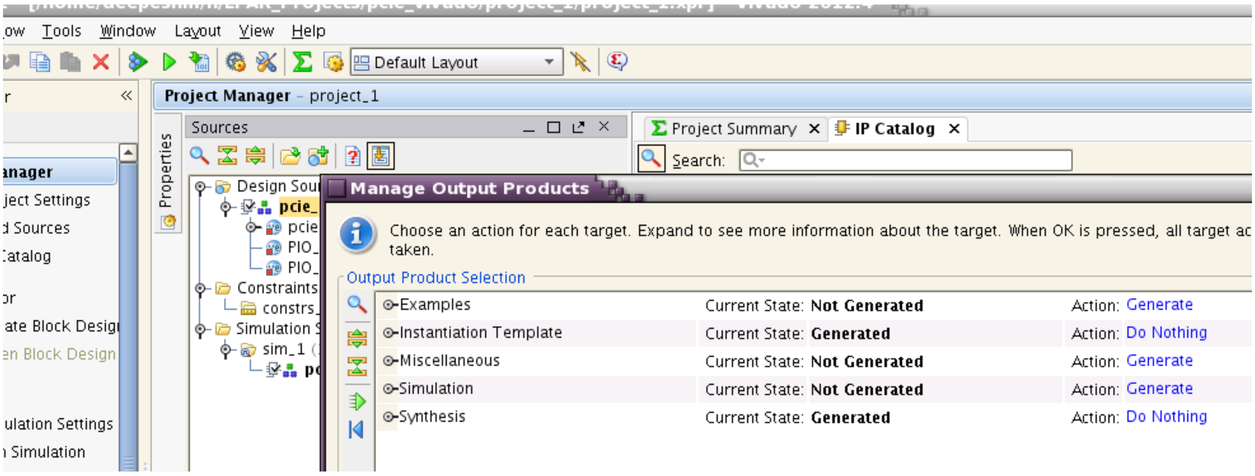


Figure 1 – Generate PCIe Output Products



Choose an action for each target. Expand to see more information about the target. When OK is pressed, all target ac taken.

Examples	Current State: **Not Generated**	Action: Generate
Instantiation Template	Current State: **Generated**	Action: Do Nothing
Miscellaneous	Current State: **Not Generated**	Action: Generate
Simulation	Current State: **Not Generated**	Action: Generate
Synthesis	Current State: **Generated**	Action: Do Nothing

Figure 2 – List of PCIe Output Products

After the example design files have been generated, open the example design project as shown in Figure 3. This opens a separate Vivado project. The example design project location is shown in Figure 5.

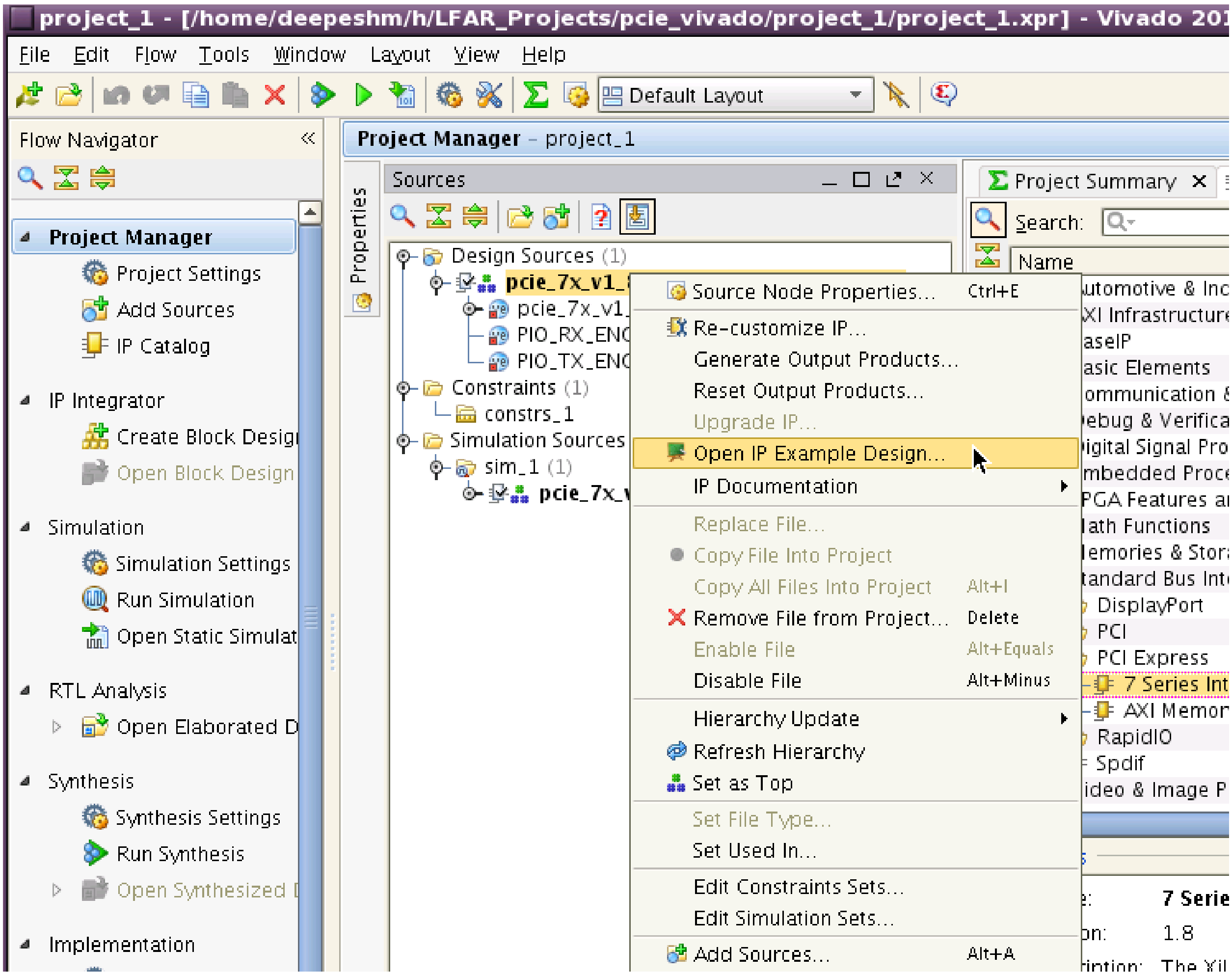

project_1 - [/home/deepeshm/h/LFAR_Projects/pcie_vivado/project_1/project_1.xpr] - Vivado 201

Figure 3 – Open PCIe IP Example Design

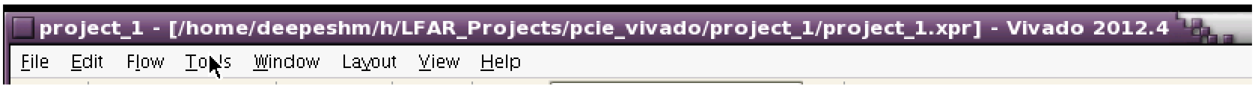
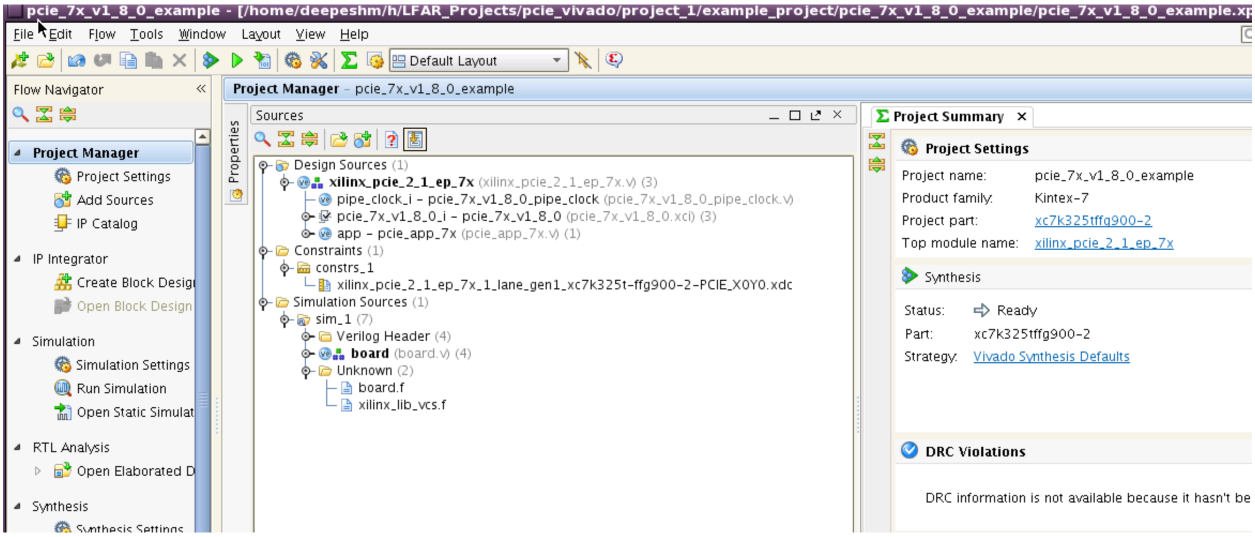

project_1 - [/home/deepeshm/h/LFAR_Projects/pcie_vivado/project_1/project_1.xpr] - Vivado 2012.4

Figure 4 – PCIe Core Vivado Project

/LFAR_Projects/pcie_vivado/project_1/example_project/pcie_7x_v1_8_0_example/pcie_7x_v1_8_0_example.xpr] - Vivado 2012.4

Figure 5 – PCIe Core Example Design Vivado Project



pcie_7x_v1_8_0_example - [/home/deepeshm/h/LFAR_Projects/pcie_vivado/project_1/example_project/pcie_7x_v1_8_0_example/pcie_7x_v1_8_0_example.xp

Project Manager - pcie_7x_v1_8_0_example

```
Design Sources (1)
    xilinx_pcie_2_1_ep_7x (xilinx_pcie_2_1_ep_7x.v) (3)
        pipe_clock_i - pcie_7x_v1_8_0_pipe_clock (pcie_7x_v1_8_0_pipe_clock.v)
        pcie_7x_v1_8_0_i - pcie_7x_v1_8_0 (pcie_7x_v1_8_0.xci) (3)
        app - pcie_app_7x (pcie_app_7x.v) (1)
Constraints (1)
    constrs_1
        xilinx_pcie_2_1_ep_7x_1_lane_gen1_xc7k325t-ffg900-2-PCIE_X0Y0.xdc
Simulation Sources (1)
    sim_1 (7)
        Verilog Header (4)
        board (board.v) (4)
        Unknown (2)
            board.f
            xilinx_lib_vcs.f
```

Project Settings

Project name: pcie_7x_v1_8_0_example
Product family: Kintex-7
Project part: xc7k325tffg900-2
Top module name: xilinx_pcie_2_1_ep_7x

Synthesis

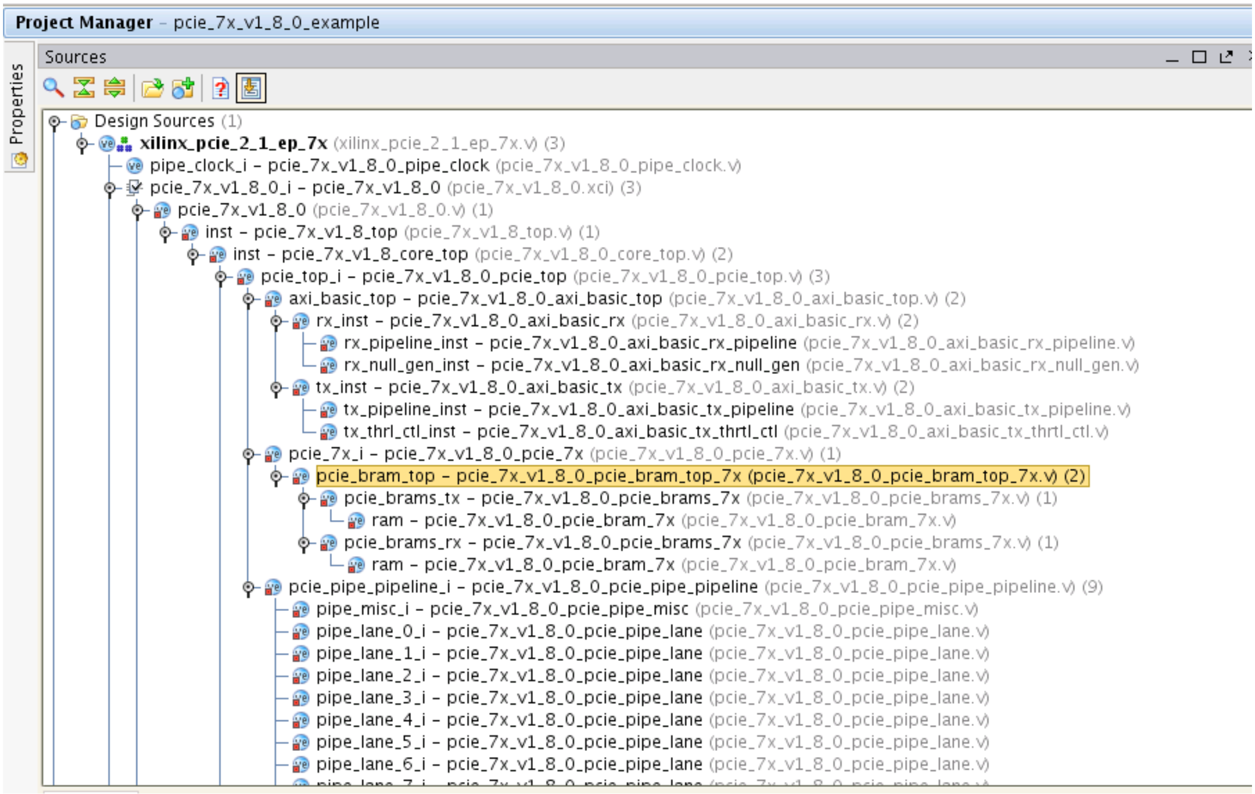
Status: Ready
Part: xc7k325tffg900-2
Strategy: Vivado Synthesis Defaults

DRC Violations

DRC information is not available because it hasn't be

Figure 6 – PCIe Example Design Vivado Project GUI

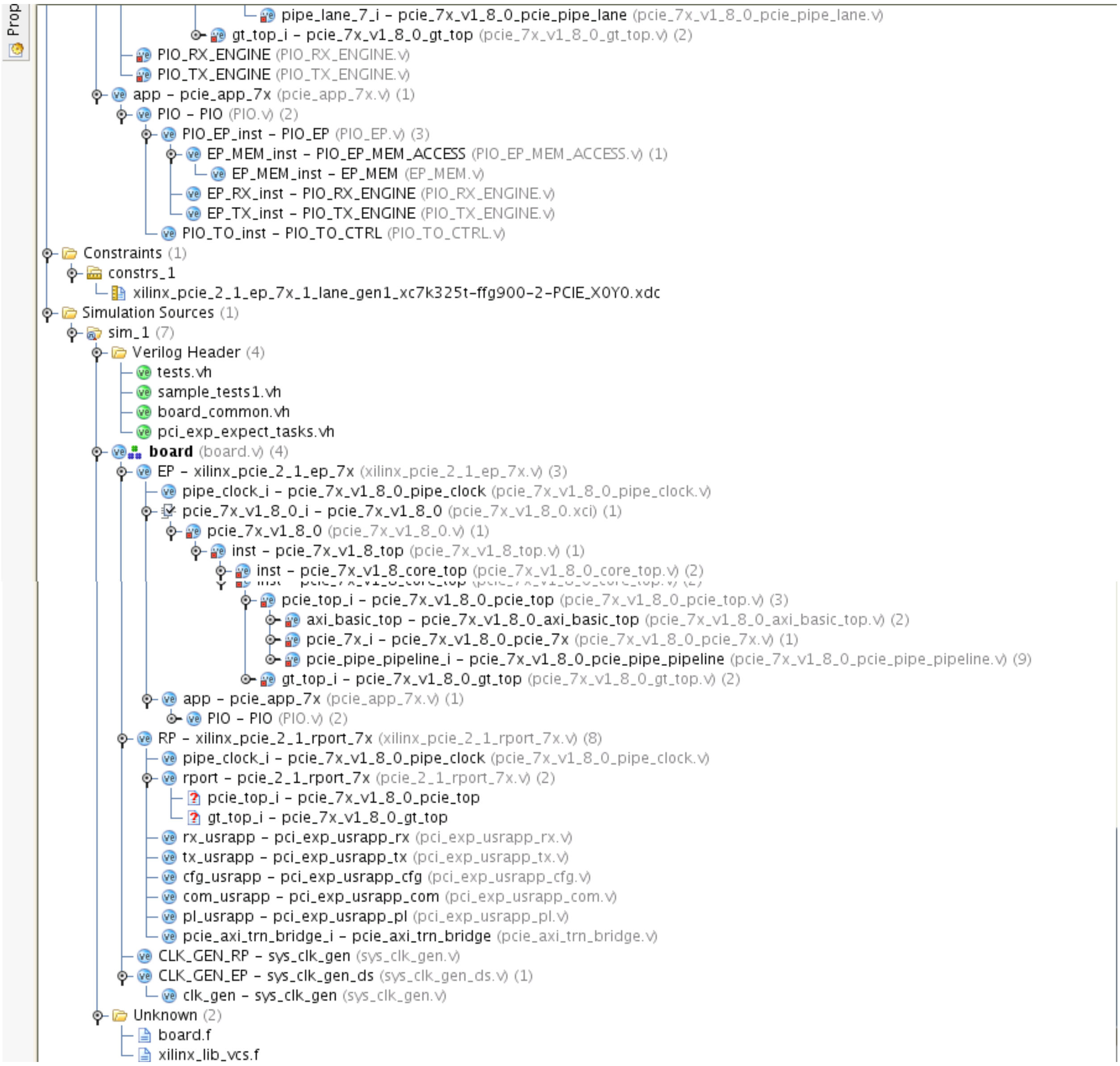
PCIe Example Design Hierarchy



Project Manager - pcie_7x_v1_8_0_example

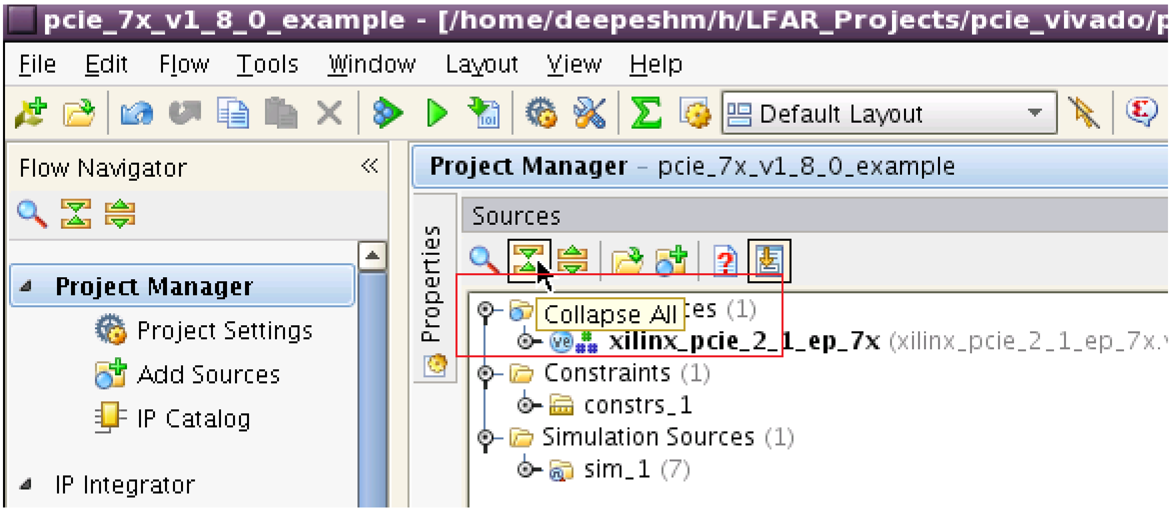
```
Design Sources (1)
    xilinx_pcie_2_1_ep_7x (xilinx_pcie_2_1_ep_7x.v) (3)
        pipe_clock_i - pcie_7x_v1_8_0_pipe_clock (pcie_7x_v1_8_0_pipe_clock.v)
        pcie_7x_v1_8_0_i - pcie_7x_v1_8_0 (pcie_7x_v1_8_0.xci) (3)
            pcie_7x_v1_8_0 (pcie_7x_v1_8_0.v) (1)
                inst - pcie_7x_v1_8_top (pcie_7x_v1_8_top.v) (1)
                    inst - pcie_7x_v1_8_core_top (pcie_7x_v1_8_0_core_top.v) (2)
                        pcie_top_i - pcie_7x_v1_8_0_pcie_top (pcie_7x_v1_8_0_pcie_top.v) (3)
                            axi_basic_top - pcie_7x_v1_8_0_axi_basic_top (pcie_7x_v1_8_0_axi_basic_top.v) (2)
                                rx_inst - pcie_7x_v1_8_0_axi_basic_rx (pcie_7x_v1_8_0_axi_basic_rx.v) (2)
                                    rx_pipeline_inst - pcie_7x_v1_8_0_axi_basic_rx_pipeline (pcie_7x_v1_8_0_axi_basic_rx_pipeline.v)
                                    rx_null_gen_inst - pcie_7x_v1_8_0_axi_basic_rx_null_gen (pcie_7x_v1_8_0_axi_basic_rx_null_gen.v)
                                tx_inst - pcie_7x_v1_8_0_axi_basic_tx (pcie_7x_v1_8_0_axi_basic_tx.v) (2)
                                    tx_pipeline_inst - pcie_7x_v1_8_0_axi_basic_tx_pipeline (pcie_7x_v1_8_0_axi_basic_tx_pipeline.v)
                                    tx_thrl_ctl_inst - pcie_7x_v1_8_0_axi_basic_tx_thrtl_ctl (pcie_7x_v1_8_0_axi_basic_tx_thrtl_ctl.v)
                            pcie_7x_i - pcie_7x_v1_8_0_pcie_7x (pcie_7x_v1_8_0_pcie_7x.v) (1)
                                pcie_bram_top - pcie_7x_v1_8_0_pcie_bram_top_7x (pcie_7x_v1_8_0_pcie_bram_top_7x.v) (2)
                                    pcie_brams_tx - pcie_7x_v1_8_0_pcie_brams_7x (pcie_7x_v1_8_0_pcie_brams_7x.v) (1)
                                        ram - pcie_7x_v1_8_0_pcie_bram_7x (pcie_7x_v1_8_0_pcie_bram_7x.v)
                                    pcie_brams_rx - pcie_7x_v1_8_0_pcie_brams_7x (pcie_7x_v1_8_0_pcie_brams_7x.v) (1)
                                        ram - pcie_7x_v1_8_0_pcie_bram_7x (pcie_7x_v1_8_0_pcie_bram_7x.v)
                            pcie_pipe_pipeline_i - pcie_7x_v1_8_0_pcie_pipe_pipeline (pcie_7x_v1_8_0_pcie_pipe_pipeline.v) (9)
                                pipe_misc_i - pcie_7x_v1_8_0_pcie_pipe_misc (pcie_7x_v1_8_0_pcie_pipe_misc.v)
                                pipe_lane_0_i - pcie_7x_v1_8_0_pcie_pipe_lane (pcie_7x_v1_8_0_pcie_pipe_lane.v)
                                pipe_lane_1_i - pcie_7x_v1_8_0_pcie_pipe_lane (pcie_7x_v1_8_0_pcie_pipe_lane.v)
                                pipe_lane_2_i - pcie_7x_v1_8_0_pcie_pipe_lane (pcie_7x_v1_8_0_pcie_pipe_lane.v)
                                pipe_lane_3_i - pcie_7x_v1_8_0_pcie_pipe_lane (pcie_7x_v1_8_0_pcie_pipe_lane.v)
                                pipe_lane_4_i - pcie_7x_v1_8_0_pcie_pipe_lane (pcie_7x_v1_8_0_pcie_pipe_lane.v)
                                pipe_lane_5_i - pcie_7x_v1_8_0_pcie_pipe_lane (pcie_7x_v1_8_0_pcie_pipe_lane.v)
                                pipe_lane_6_i - pcie_7x_v1_8_0_pcie_pipe_lane (pcie_7x_v1_8_0_pcie_pipe_lane.v)
                                pipe_lane_7_i - pcie_7x_v1_8_0_pcie_pipe_lane (pcie_7x_v1_8_0_pcie_pipe_lane.v)
```

Figure 7 – PCIe IP Example Design Hierarchy (Part-1)



```
Prop
                        └ pipe_lane_7_i - pcie_7x_v1_8_0_pcie_pipe_lane (pcie_7x_v1_8_0_pcie_pipe_lane.v)
                    gt_top_i - pcie_7x_v1_8_0_gt_top (pcie_7x_v1_8_0_gt_top.v) (2)
          ├ PIO_RX_ENGINE (PIO_RX_ENGINE.v)
          └ PIO_TX_ENGINE (PIO_TX_ENGINE.v)
      app - pcie_app_7x (pcie_app_7x.v) (1)
        PIO - PIO (PIO.v) (2)
          PIO_EP_inst - PIO_EP (PIO_EP.v) (3)
            EP_MEM_inst - PIO_EP_MEM_ACCESS (PIO_EP_MEM_ACCESS.v) (1)
              └ EP_MEM_inst - EP_MEM (EP_MEM.v)
            ├ EP_RX_inst - PIO_RX_ENGINE (PIO_RX_ENGINE.v)
            └ EP_TX_inst - PIO_TX_ENGINE (PIO_TX_ENGINE.v)
          └ PIO_TO_inst - PIO_TO_CTRL (PIO_TO_CTRL.v)
Constraints (1)
  constrs_1
    └ xilinx_pcie_2_1_ep_7x_1_lane_gen1_xc7k325t-ffg900-2-PCIE_X0Y0.xdc
Simulation Sources (1)
  sim_1 (7)
    Verilog Header (4)
      ├ tests.vh
      ├ sample_tests1.vh
      ├ board_common.vh
      └ pci_exp_expect_tasks.vh
    board (board.v) (4)
      EP - xilinx_pcie_2_1_ep_7x (xilinx_pcie_2_1_ep_7x.v) (3)
        ├ pipe_clock_i - pcie_7x_v1_8_0_pipe_clock (pcie_7x_v1_8_0_pipe_clock.v)
        pcie_7x_v1_8_0_i - pcie_7x_v1_8_0 (pcie_7x_v1_8_0.xci) (1)
          pcie_7x_v1_8_0 (pcie_7x_v1_8_0.v) (1)
            inst - pcie_7x_v1_8_top (pcie_7x_v1_8_top.v) (1)
              inst - pcie_7x_v1_8_core_top (pcie_7x_v1_8_0_core_top.v) (2)
                pcie_top_i - pcie_7x_v1_8_0_pcie_top (pcie_7x_v1_8_0_pcie_top.v) (3)
                  axi_basic_top - pcie_7x_v1_8_0_axi_basic_top (pcie_7x_v1_8_0_axi_basic_top.v) (2)
                  pcie_7x_i - pcie_7x_v1_8_0_pcie_7x (pcie_7x_v1_8_0_pcie_7x.v) (1)
                  pcie_pipe_pipeline_i - pcie_7x_v1_8_0_pcie_pipe_pipeline (pcie_7x_v1_8_0_pcie_pipe_pipeline.v) (9)
                gt_top_i - pcie_7x_v1_8_0_gt_top (pcie_7x_v1_8_0_gt_top.v) (2)
        app - pcie_app_7x (pcie_app_7x.v) (1)
          PIO - PIO (PIO.v) (2)
      RP - xilinx_pcie_2_1_rport_7x (xilinx_pcie_2_1_rport_7x.v) (8)
        ├ pipe_clock_i - pcie_7x_v1_8_0_pipe_clock (pcie_7x_v1_8_0_pipe_clock.v)
        rport - pcie_2_1_rport_7x (pcie_2_1_rport_7x.v) (2)
          ├ pcie_top_i - pcie_7x_v1_8_0_pcie_top
          └ gt_top_i - pcie_7x_v1_8_0_gt_top
        ├ rx_usrapp - pci_exp_usrapp_rx (pci_exp_usrapp_rx.v)
        ├ tx_usrapp - pci_exp_usrapp_tx (pci_exp_usrapp_tx.v)
        ├ cfg_usrapp - pci_exp_usrapp_cfg (pci_exp_usrapp_cfg.v)
        ├ com_usrapp - pci_exp_usrapp_com (pci_exp_usrapp_com.v)
        ├ pl_usrapp - pci_exp_usrapp_pl (pci_exp_usrapp_pl.v)
        └ pcie_axi_trn_bridge_i - pcie_axi_trn_bridge (pcie_axi_trn_bridge.v)
      ├ CLK_GEN_RP - sys_clk_gen (sys_clk_gen.v)
      CLK_GEN_EP - sys_clk_gen_ds (sys_clk_gen_ds.v) (1)
        └ clk_gen - sys_clk_gen (sys_clk_gen.v)
    Unknown (2)
      ├ board.f
      └ xilinx_lib_vcs.f
```

Figure 8 - PCIe IP Example Design Hierarchy (Part-2)



pcie_7x_v1_8_0_example - [/home/deepeshm/h/LFAR_Projects/pcie_vivado/p

```
  Design Sources (1)
    xilinx_pcie_2_1_ep_7x (xilinx_pcie_2_1_ep_7x.
  Constraints (1)
    constrs_1
  Simulation Sources (1)
    sim_1 (7)
```

Figure 9 – ‘Collapse All’ option for Project Hierarchy

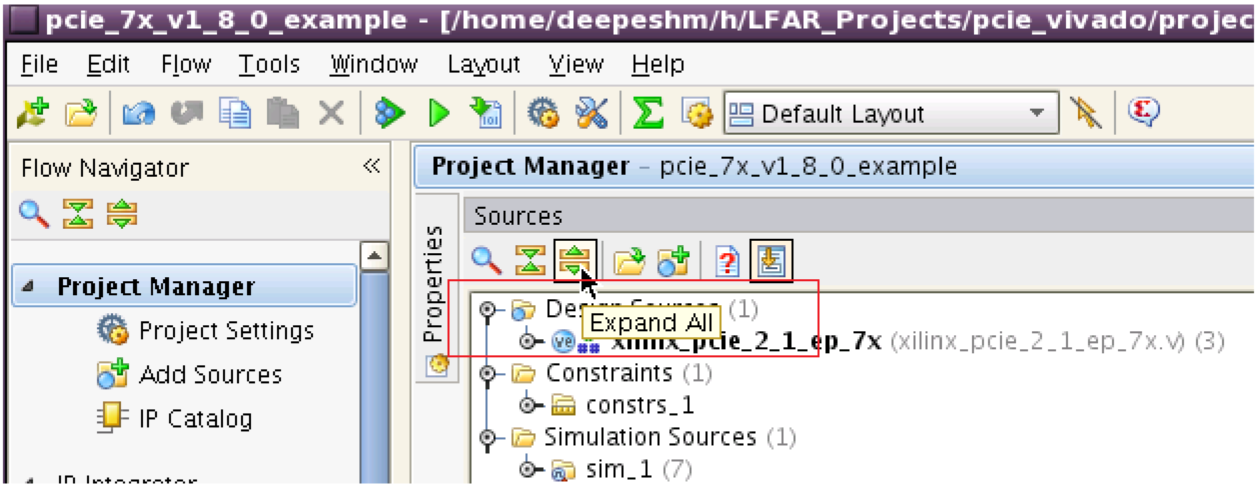
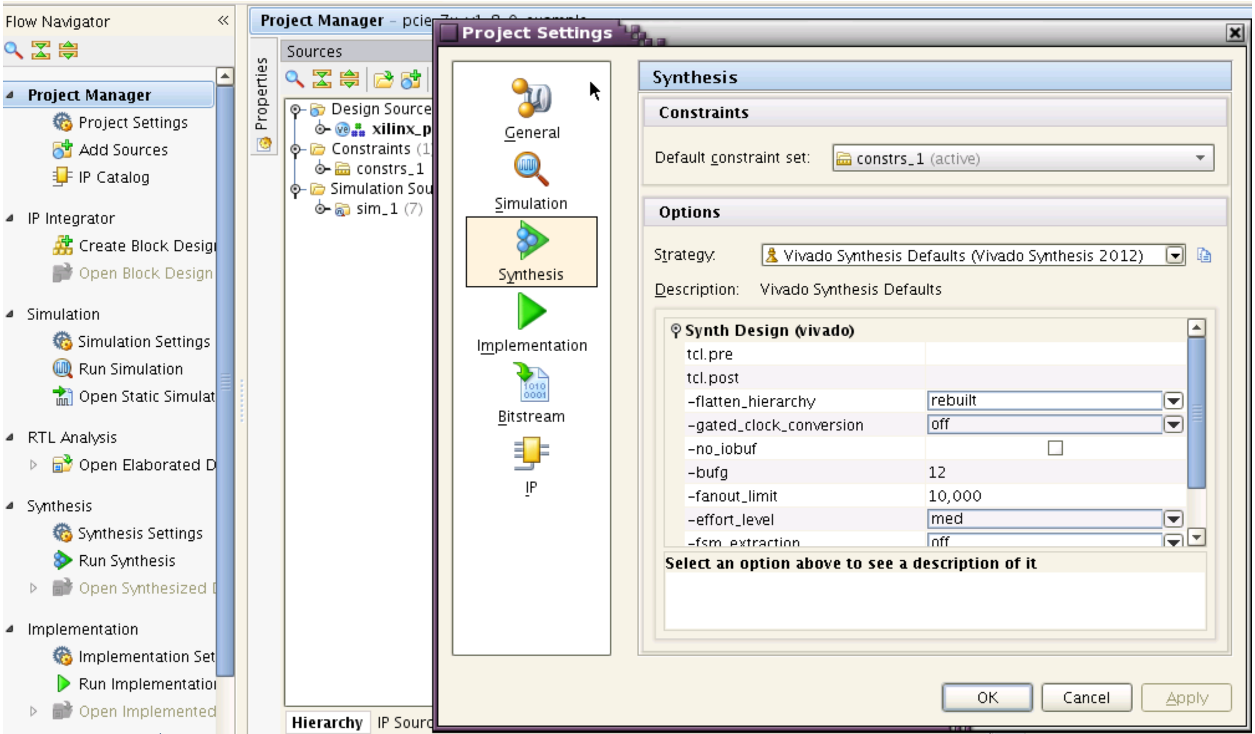

pcie_7x_v1_8_0_example - [/home/deepeshm/h/LFAR_Projects/pcie_vivado/projec
File Edit Flow Tools Window Layout View Help
Default Layout
Flow Navigator
Project Manager
Project Settings
Add Sources
IP Catalog
IP Integrator
Project Manager - pcie_7x_v1_8_0_example
Sources
Properties
Expand All
Design Sources (1)
xilinx_pcie_2_1_ep_7x (xilinx_pcie_2_1_ep_7x.v) (3)
Constraints (1)
constrs_1
Simulation Sources (1)
sim_1 (7)

Figure 10 - 'Expand All' option for Project Hierarchy

PCIe Example Design Synthesis



Synthesis

Constraints

Default constraint set: constrs_1 (active)

Options

Strategy: Vivado Synthesis Defaults (Vivado Synthesis 2012)

Description: Vivado Synthesis Defaults

Synth Design (vivado)

tcl.pre	
tcl.post	
-flatten_hierarchy	rebuilt
-gated_clock_conversion	off
-no_iobuf	□
-bufg	12
-fanout_limit	10,000
-effort_level	med
-fsm_extraction	off

Select an option above to see a description of it

Figure 11 – Vivado Synthesis Settings GUI

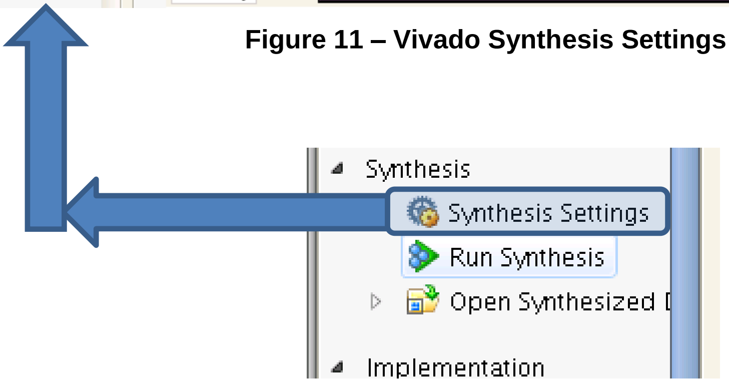
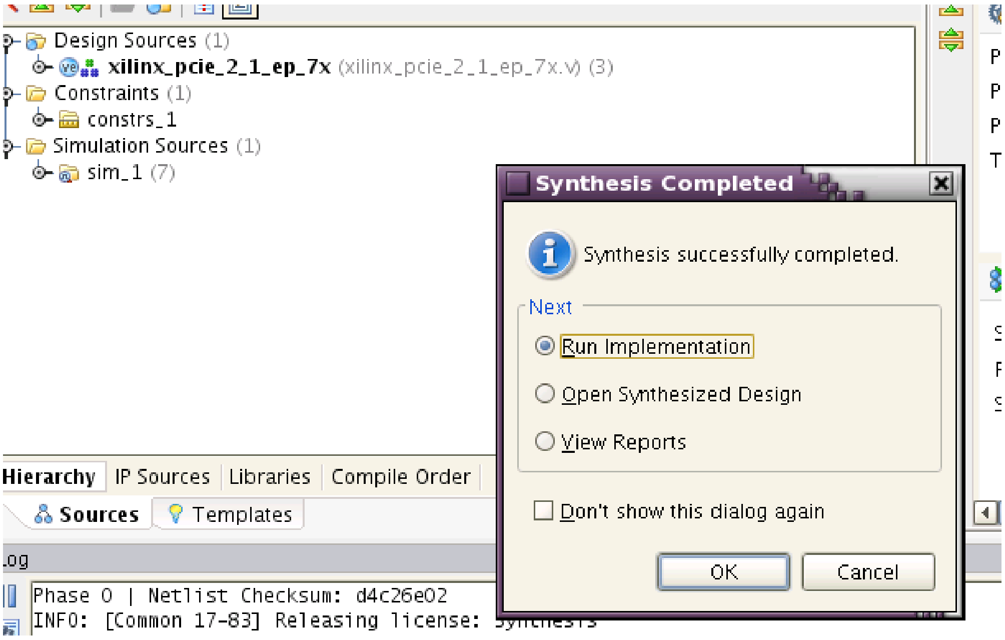


Figure 12 – Run Synthesis



```
Phase 0 | Netlist Checksum: d4c26e02
INFO: [Common 17-83] Releasing license: Synthesis
```

Synthesis Completed

Synthesis successfully completed.

Next

● Run Implementation

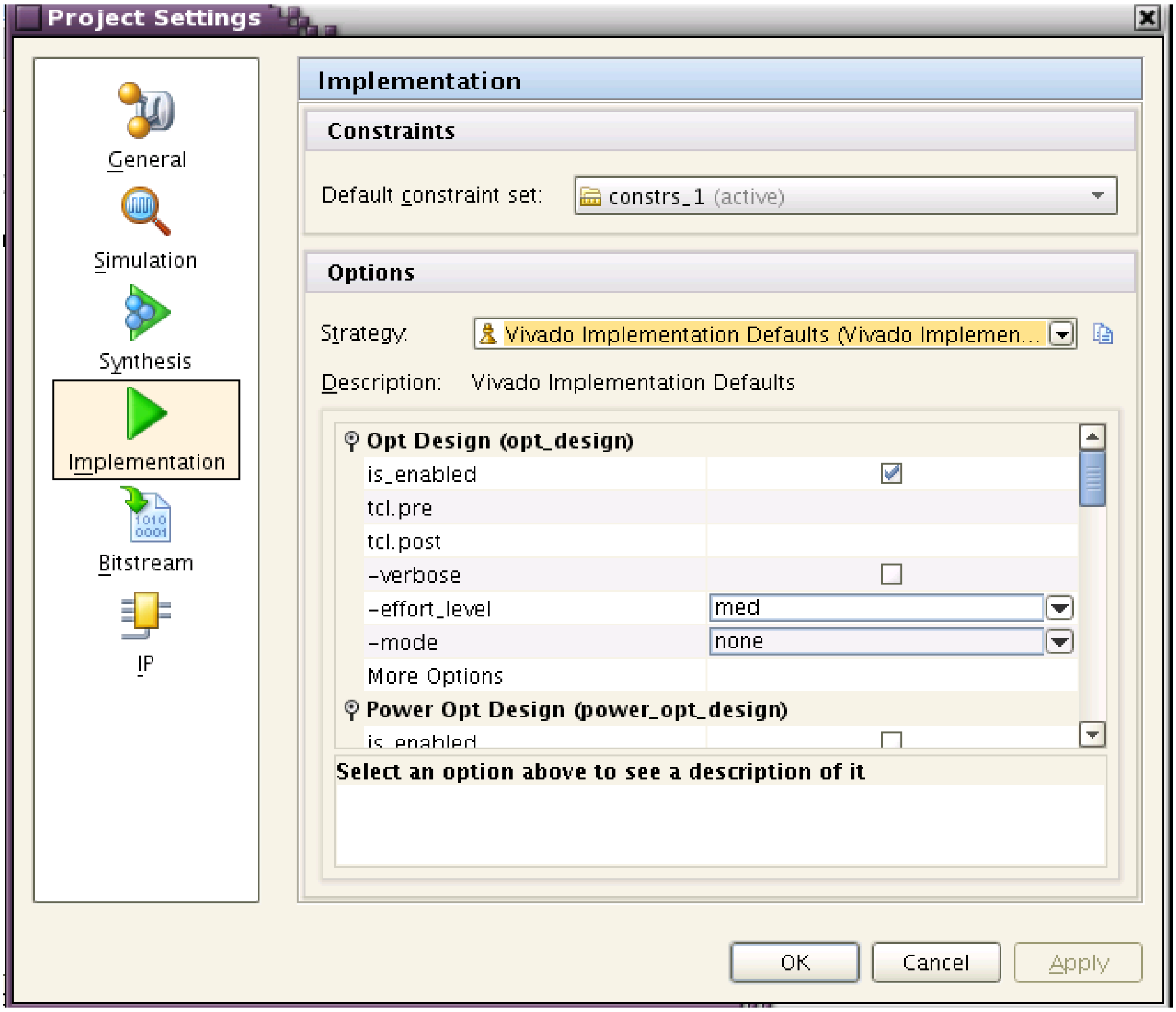
○ Open Synthesized Design

○ View Reports

□ Don't show this dialog again

Figure 13 - After PCIe Example Design Synthesis

PCIe Example Design Implementation



Implementation

Constraints

Default constraint set: constrs_1 (active)

Options

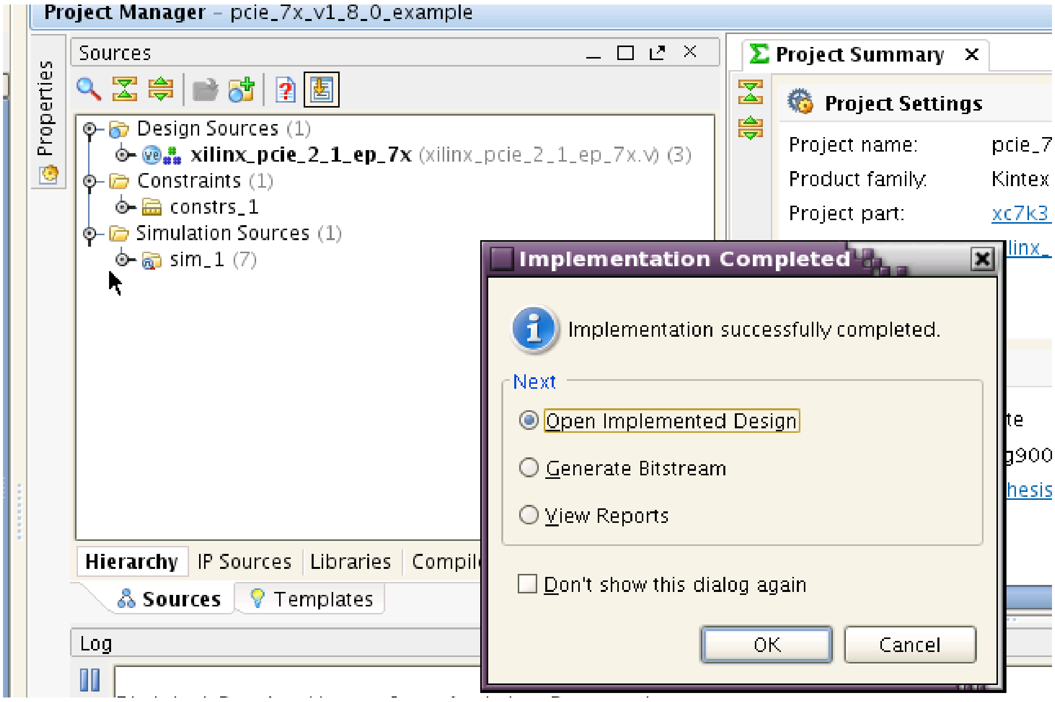
Strategy: Vivado Implementation Defaults (Vivado Implemen...

Description: Vivado Implementation Defaults

Opt Design (opt_design)	
is_enabled	☑
tcl.pre	
tcl.post	
-verbose	□
-effort_level	med
-mode	none
More Options	
Power Opt Design (power_opt_design)	
is_enabled	□

Select an option above to see a description of it

Figure 14 - Vivado Implementation Options GUI



Project name: pcie_7
Product family: Kintex
Project part: xc7k3

Implementation Completed

Implementation successfully completed.

Next

● Open Implemented Design

○ Generate Bitstream

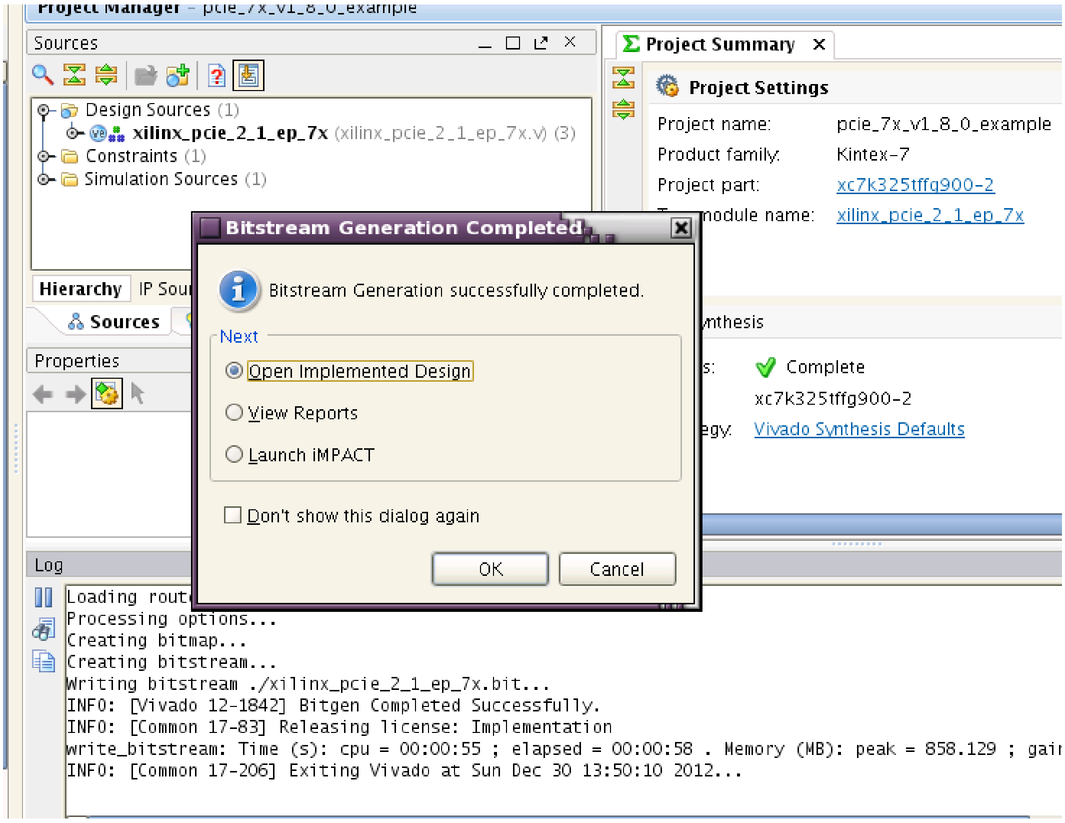
○ View Reports

□ Don't show this dialog again

OK Cancel

Figure 15 - After PCIe Example Design Implementation

PCIe Example Design Bitstream Generation



Project name: pcie_7x_v1_8_0_example
Product family: Kintex-7
Project part: xc7k325tffg900-2
T module name: xilinx_pcie_2_1_ep_7x

s: ✓ Complete
xc7k325tffg900-2
egy: Vivado Synthesis Defaults

Bitstream Generation Completed

Bitstream Generation successfully completed.

Next

● Open Implemented Design

○ View Reports

○ Launch iMPACT

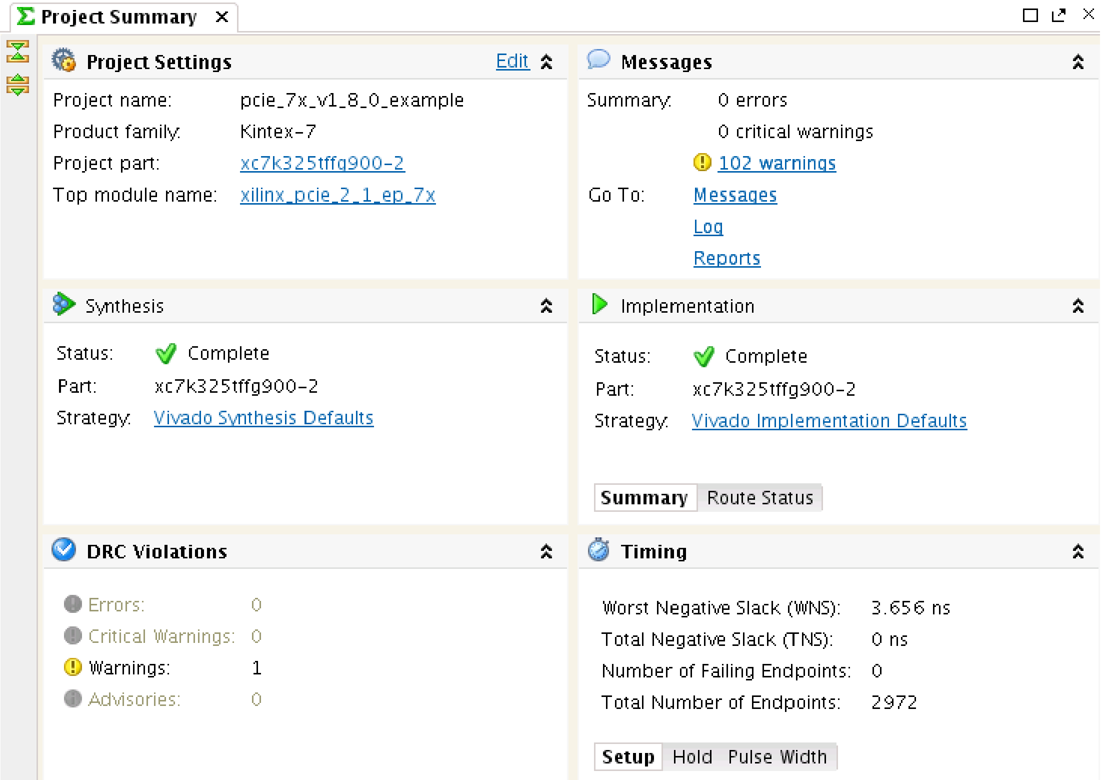
□ Don't show this dialog again

OK Cancel

```
Loading rout
Processing options...
Creating bitmap...
Creating bitstream...
Writing bitstream ./xilinx_pcie_2_1_ep_7x.bit...
INFO: [Vivado 12-1842] Bitgen Completed Successfully.
INFO: [Common 17-83] Releasing license: Implementation
write_bitstream: Time (s): cpu = 00:00:55 ; elapsed = 00:00:58 . Memory (MB): peak = 858.129 ; gai
INFO: [Common 17-206] Exiting Vivado at Sun Dec 30 13:50:10 2012...
```

Figure 16 – After PCIe Example Design Bitstream Generation

PCIe Example Design Implementation Summary and Report



Project Summary

Project Settings Edit

Project name:	pcie_7x_v1_8_0_example
Product family:	Kintex-7
Project part:	xc7k325tffg900-2
Top module name:	xilinx_pcie_2_1_ep_7x

Messages

Summary: 0 errors
0 critical warnings
102 warnings

Go To: Messages
Log
Reports

Synthesis

Status:	✓ Complete
Part:	xc7k325tffg900-2
Strategy:	Vivado Synthesis Defaults

Implementation

Status:	✓ Complete
Part:	xc7k325tffg900-2
Strategy:	Vivado Implementation Defaults

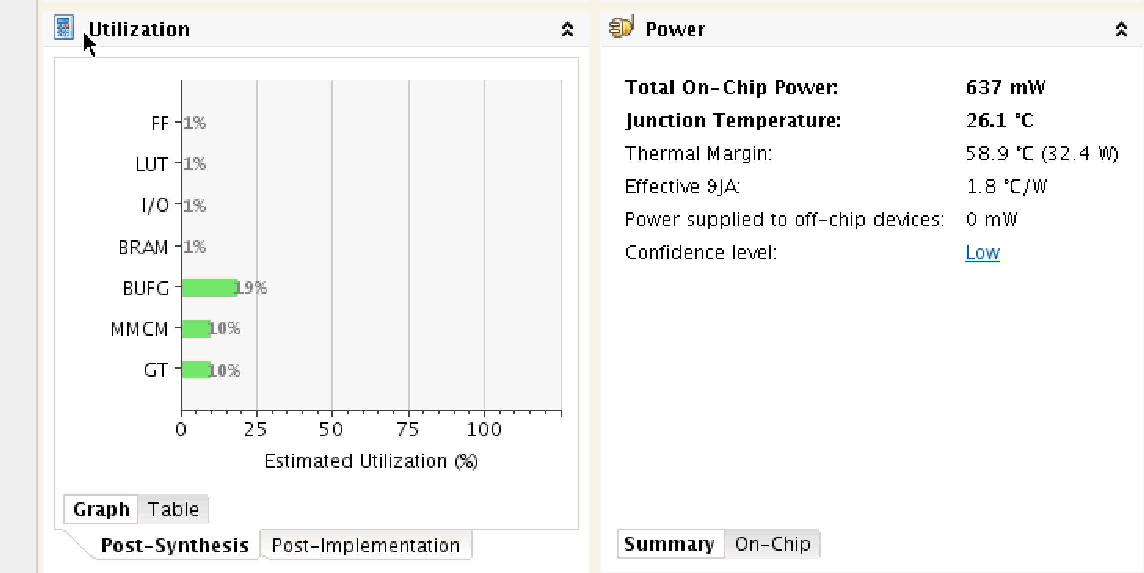
DRC Violations

Errors:	0
Critical Warnings:	0
Warnings:	1
Advisories:	0

Timing

Worst Negative Slack (WNS):	3.656 ns
Total Negative Slack (TNS):	0 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	2972

Figure 17 – PCIe Example Design Project Summary after Bitstream Generation

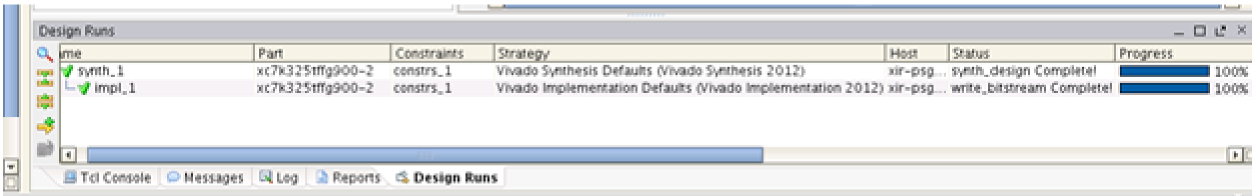


Utilization

Power

Total On-Chip Power:	**637 mW**
Junction Temperature:	**26.1 °C**
Thermal Margin:	58.9 °C (32.4 W)
Effective θJA:	1.8 °C/W
Power supplied to off-chip devices:	0 mW
Confidence level:	Low

Figure 18 – PCIe Example Design Post-Synthesis Resource Utilization



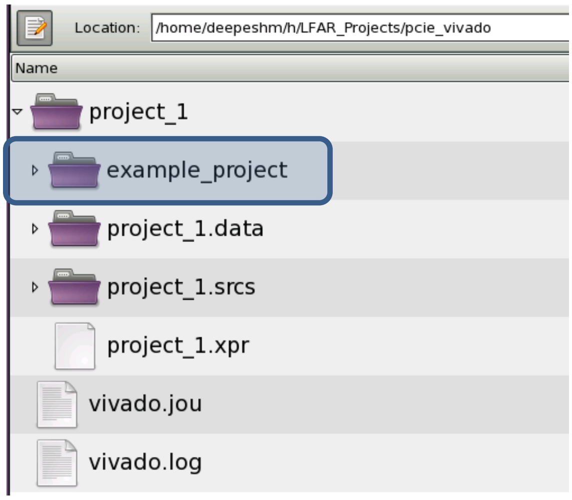
Design Runs

me	Part	Constraints	Strategy	Host	Status	Progress
✓ synth_1	xc7k325tffg900-2	constrs_1	Vivado Synthesis Defaults (Vivado Synthesis 2012)	xir-psg...	synth_design Complete!	100%
✓ impl_1	xc7k325tffg900-2	constrs_1	Vivado Implementation Defaults (Vivado Implementation 2012)	xir-psg...	write_bitstream Complete!	100%

Figure 19 – Post Implementation 'Design Runs' Report

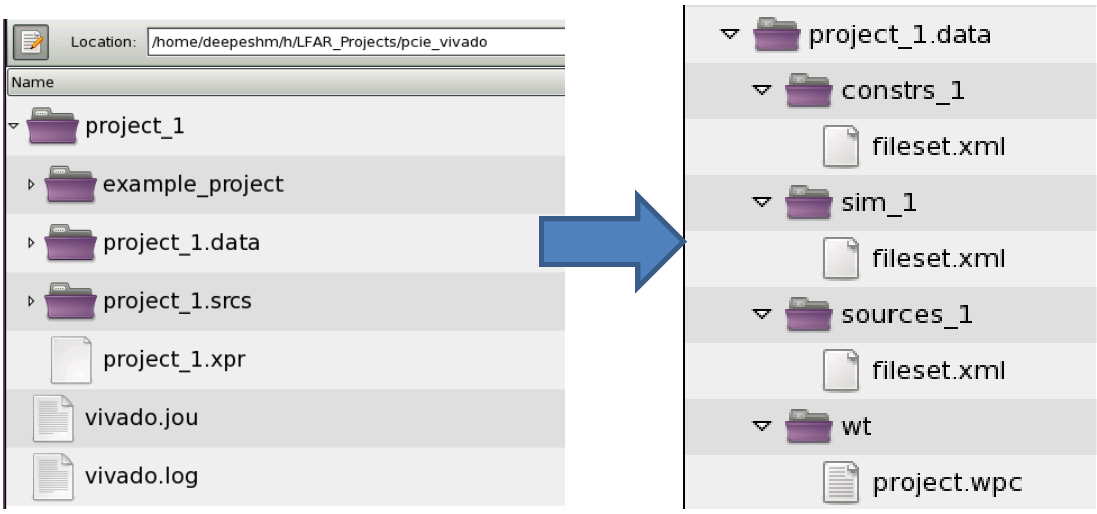
PCIe Example Design Project Directory Structure

Project directory structure in Vivado IP core generation can be confusing. Figure 20 shows the content of the top level project directory after generating the example design files. *example_project* directory shown in Figure 20 is generated only after generating the example design files. Another thing to note is that the content of *project_1.srcs* is different between before and after the example design files generation. This is shown in Figure 22 and Figure 23


Location: /home/deepeshm/h/LFAR_Projects/pcie_vivado

Name
- project_1
  - example_project
  - project_1.data
  - project_1.srcs
  - project_1.xpr
- vivado.jou
- vivado.log

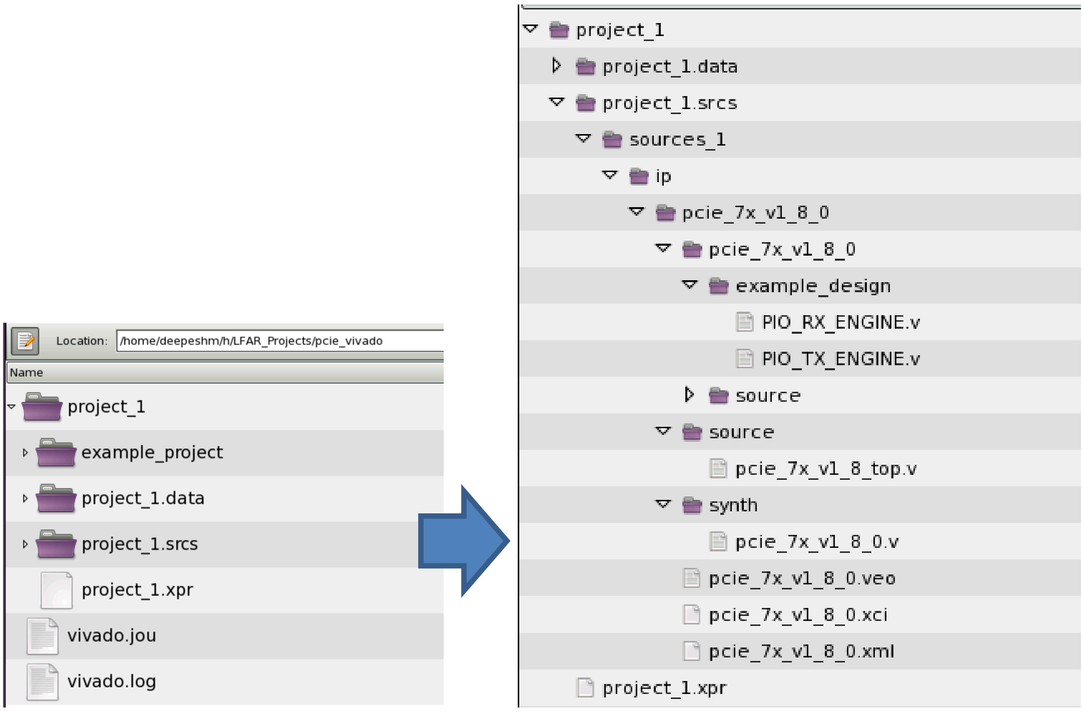
Figure 20 – PCIe Vivado Project Directory Content after Example Design Generation


Location: /home/deepeshm/h/LFAR_Projects/pcie_vivado

Name
- project_1
  - example_project
  - project_1.data
  - project_1.srcs
  - project_1.xpr
- vivado.jou
- vivado.log

- project_1.data
  - constrs_1
    - fileset.xml
  - sim_1
    - fileset.xml
  - sources_1
    - fileset.xml
  - wt
    - project.wpc

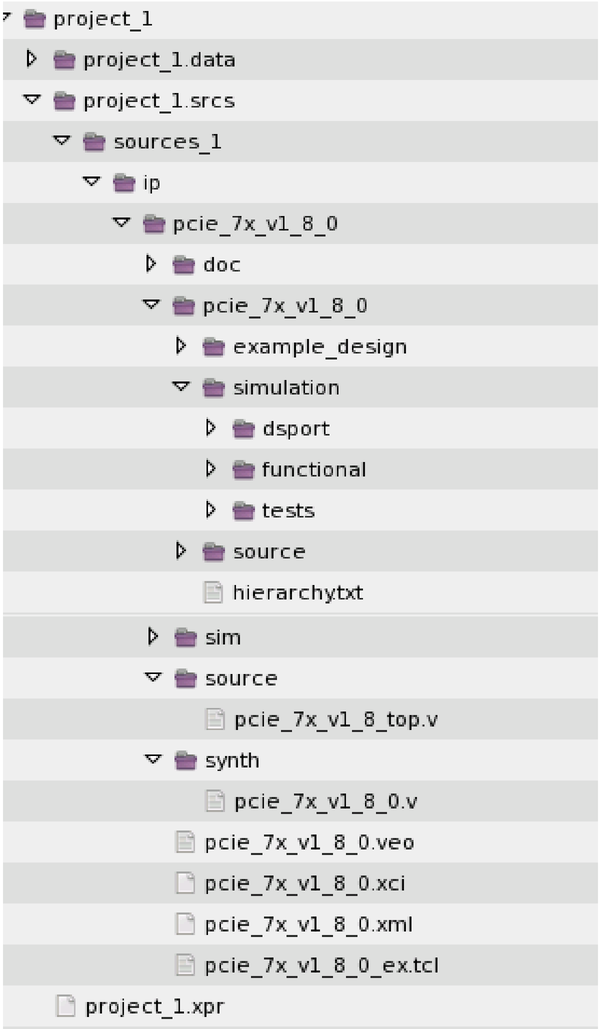
Figure 21 - project_1.data Content



```
Location: /home/deepeshm/h/LFAR_Projects/pcie_vivado
Name
project_1
  example_project
  project_1.data
  project_1.srcs
  project_1.xpr
vivado.jou
vivado.log
```

```
project_1
  project_1.data
  project_1.srcs
    sources_1
      ip
        pcie_7x_v1_8_0
          pcie_7x_v1_8_0
            example_design
              PIO_RX_ENGINE.v
              PIO_TX_ENGINE.v
            source
          source
            pcie_7x_v1_8_top.v
          synth
            pcie_7x_v1_8_0.v
          pcie_7x_v1_8_0.veo
          pcie_7x_v1_8_0.xci
          pcie_7x_v1_8_0.xml
  project_1.xpr
```

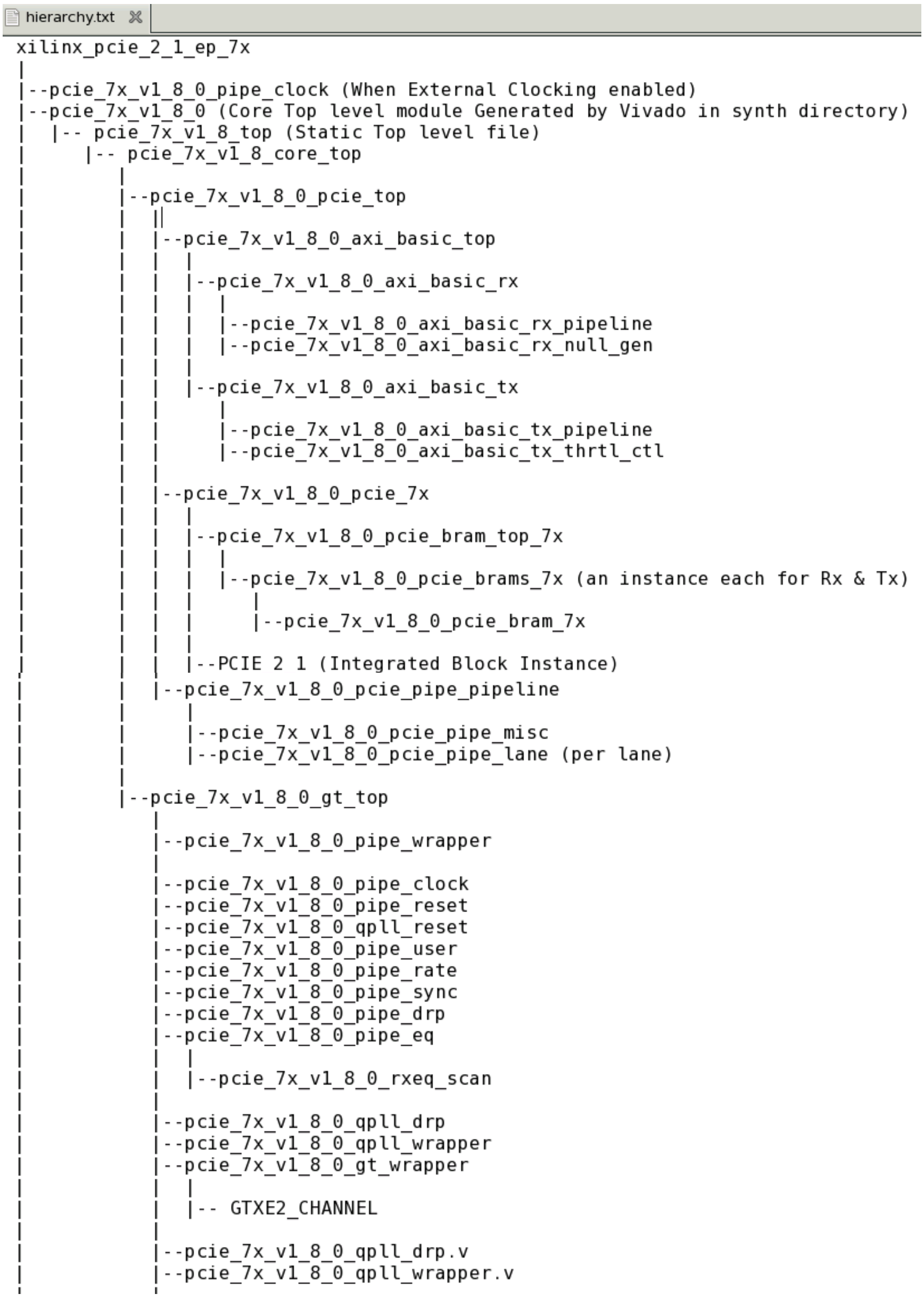
Figure 22 – project_1.srcs Content before PCIe Example Design Generation



```
project_1
  project_1.data
  project_1.srcs
    sources_1
      ip
        pcie_7x_v1_8_0
          doc
          pcie_7x_v1_8_0
            example_design
            simulation
              dsport
              functional
              tests
            source
            hierarchytxt
          sim
          source
            pcie_7x_v1_8_top.v
          synth
            pcie_7x_v1_8_0.v
          pcie_7x_v1_8_0.veo
          pcie_7x_v1_8_0.xci
          pcie_7x_v1_8_0.xml
          pcie_7x_v1_8_0_ex.tcl
  project_1.xpr
```

Figure 23 - project_1.srcs Content after PCIe Example Design Generation

hierarchy.txt is generated with the generation of the example design files. It contains the entire hierarchy of the PCIe example design files. The content of this file is shown in Figure 24 and Figure 25.

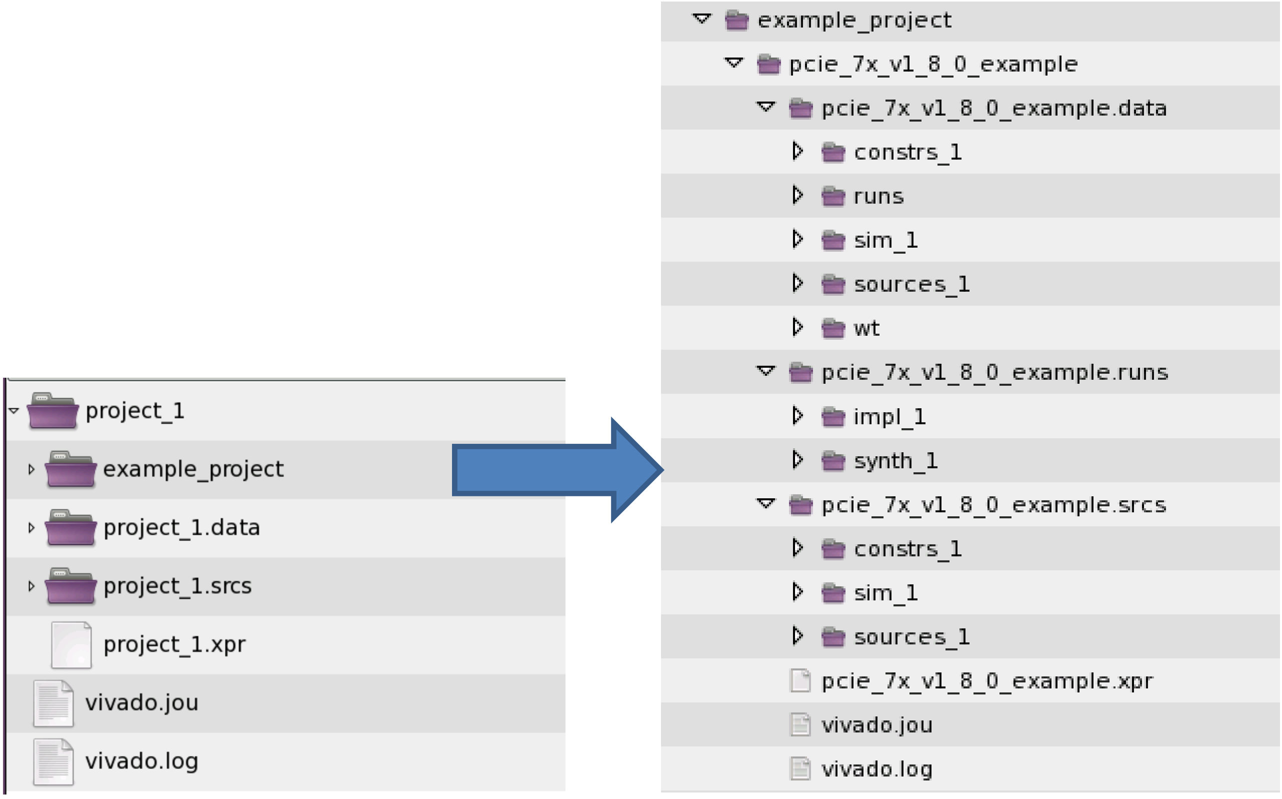


```
xilinx_pcie_2_1_ep_7x
|
|--pcie_7x_v1_8_0_pipe_clock (When External Clocking enabled)
|--pcie_7x_v1_8_0 (Core Top level module Generated by Vivado in synth directory)
|  |-- pcie_7x_v1_8_top (Static Top level file)
|     |-- pcie_7x_v1_8_core_top
|        |
|        |--pcie_7x_v1_8_0_pcie_top
|        |  ||
|        |  |--pcie_7x_v1_8_0_axi_basic_top
|        |  |  |
|        |  |  |--pcie_7x_v1_8_0_axi_basic_rx
|        |  |  |  |
|        |  |  |  |--pcie_7x_v1_8_0_axi_basic_rx_pipeline
|        |  |  |  |--pcie_7x_v1_8_0_axi_basic_rx_null_gen
|        |  |  |
|        |  |  |--pcie_7x_v1_8_0_axi_basic_tx
|        |  |     |
|        |  |     |--pcie_7x_v1_8_0_axi_basic_tx_pipeline
|        |  |     |--pcie_7x_v1_8_0_axi_basic_tx_thrtl_ctl
|        |  |
|        |  |--pcie_7x_v1_8_0_pcie_7x
|        |  |  |
|        |  |  |--pcie_7x_v1_8_0_pcie_bram_top_7x
|        |  |  |  |
|        |  |  |  |--pcie_7x_v1_8_0_pcie_brams_7x (an instance each for Rx & Tx)
|        |  |  |     |
|        |  |  |     |--pcie_7x_v1_8_0_pcie_bram_7x
|        |  |  |
|        |  |  |--PCIE 2 1 (Integrated Block Instance)
|        |  |--pcie_7x_v1_8_0_pcie_pipe_pipeline
|        |     |
|        |     |--pcie_7x_v1_8_0_pcie_pipe_misc
|        |     |--pcie_7x_v1_8_0_pcie_pipe_lane (per lane)
|        |
|        |--pcie_7x_v1_8_0_gt_top
|           |
|           |--pcie_7x_v1_8_0_pipe_wrapper
|           |
|           |--pcie_7x_v1_8_0_pipe_clock
|           |--pcie_7x_v1_8_0_pipe_reset
|           |--pcie_7x_v1_8_0_qpll_reset
|           |--pcie_7x_v1_8_0_pipe_user
|           |--pcie_7x_v1_8_0_pipe_rate
|           |--pcie_7x_v1_8_0_pipe_sync
|           |--pcie_7x_v1_8_0_pipe_drp
|           |--pcie_7x_v1_8_0_pipe_eq
|           |  |
|           |  |--pcie_7x_v1_8_0_rxeq_scan
|           |
|           |--pcie_7x_v1_8_0_qpll_drp
|           |--pcie_7x_v1_8_0_qpll_wrapper
|           |--pcie_7x_v1_8_0_gt_wrapper
|           |  |
|           |  |-- GTXE2_CHANNEL
|           |
|           |--pcie_7x_v1_8_0_qpll_drp.v
|           |--pcie_7x_v1_8_0_qpll_wrapper.v
```

Figure 24 – PCIe Example Design Files Hierarchy (Part-1)

```
|             |
|             |-- GTXE2_COMMON
|
|--pcie_app_7x (PIO design, in example_design directory)
     |
     |--PIO
          |
          |--PIO_EP
          |    |
          |    |--PIO_EP_MEM_ACCESS
          |    |    |
          |    |    |--EP_MEM
          |    |         |
          |    |         |--RAMB36
          |    |
          |    |--PIO_RX_ENGINE
          |    |--PIO_TX_ENGINE
          |
          |--PIO_TO_CTRL
```

Figure 25 - PCIe Example Design File Hierarchy (Part-2)



```
project_1
    example_project
    project_1.data
    project_1.srcs
    project_1.xpr
vivado.jou
vivado.log
```

```
example_project
    pcie_7x_v1_8_0_example
        pcie_7x_v1_8_0_example.data
            constrs_1
            runs
            sim_1
            sources_1
            wt
        pcie_7x_v1_8_0_example.runs
            impl_1
            synth_1
        pcie_7x_v1_8_0_example.srcs
            constrs_1
            sim_1
            sources_1
        pcie_7x_v1_8_0_example.xpr
        vivado.jou
        vivado.log
```

Figure 26 – 'example_project' content after PCIe Example Design Implementation

PCIe Example Design Vivado Simulation

Simulation of PCIe Example Design in Vivado can be done with Vivado Simulator and Modelsim. In this section, steps for simulating the PCIe example design are shown for Vivado Simulator.

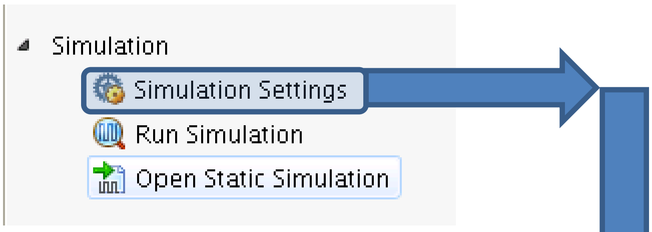
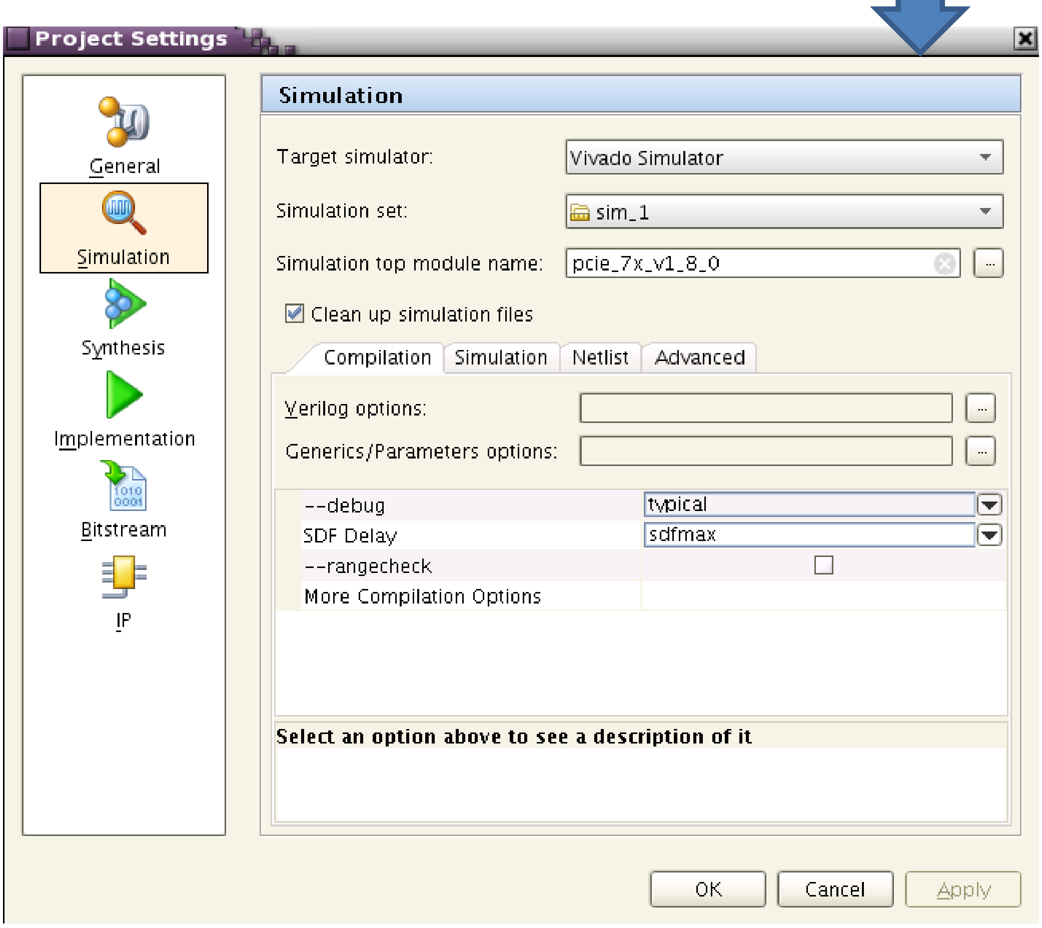


Figure 27 – Vivado Simulation Panel



Simulation

Target simulator: Vivado Simulator

Simulation set: sim_1

Simulation top module name: pcie_7x_v1_8_0

☑ Clean up simulation files

Verilog options:

Generics/Parameters options:

--debug	typical
SDF Delay	sdfmax
--rangecheck	□
More Compilation Options	

Select an option above to see a description of it

Figure 28 – Vivado Simulation Settings

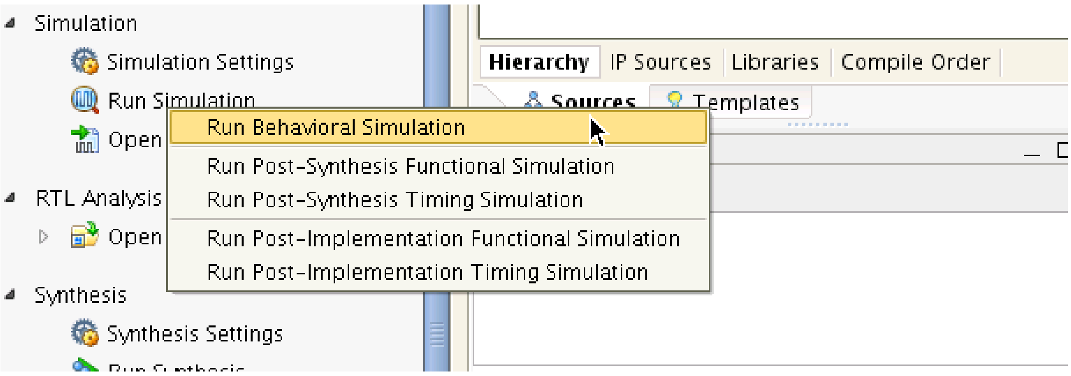
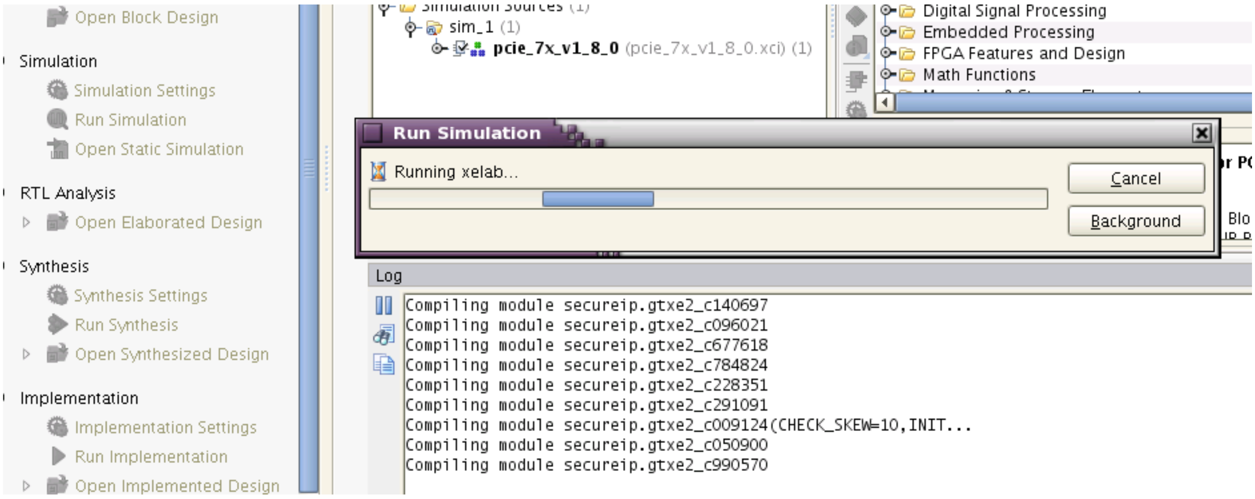

Simulation
Simulation Settings
Run Simulation
Open
RTL Analysis
Open
Synthesis
Synthesis Settings
Run Synthesis
Hierarchy
IP Sources
Libraries
Compile Order
Sources
Templates
Run Behavioral Simulation
Run Post-Synthesis Functional Simulation
Run Post-Synthesis Timing Simulation
Run Post-Implementation Functional Simulation
Run Post-Implementation Timing Simulation

Figure 29 – PCIe Example Design Behavioral Simulation in Vivado

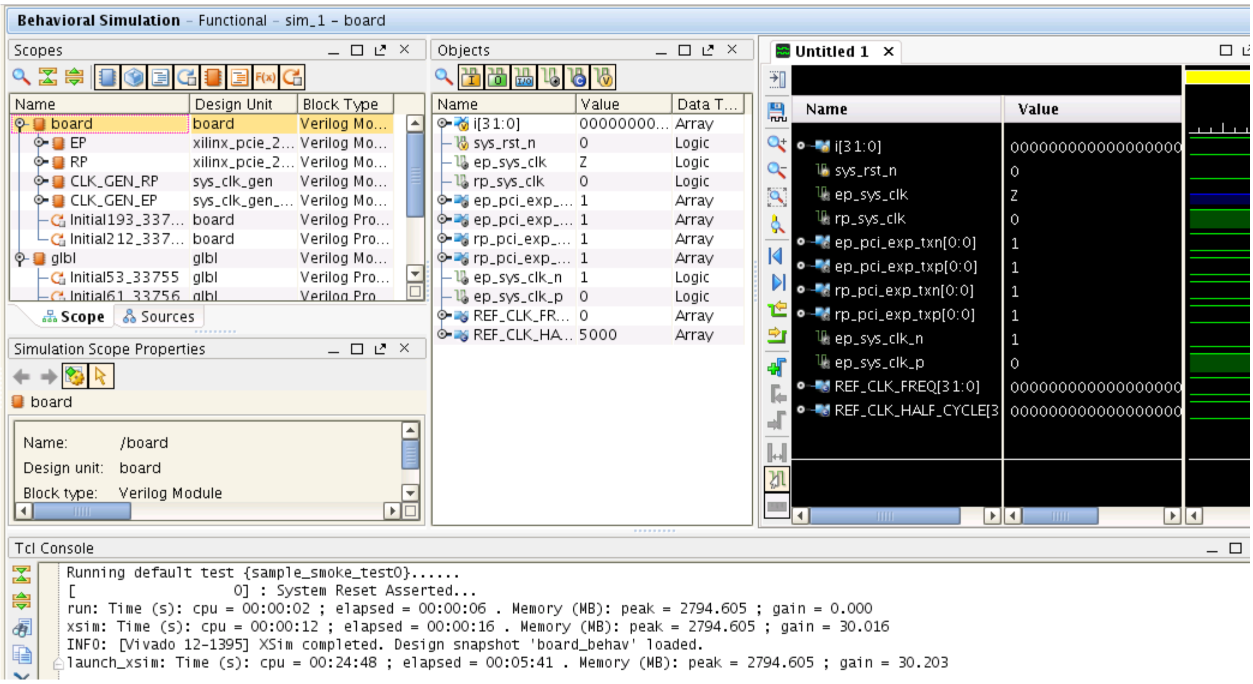
In Figure 29, it shows all ‘simulation’ options are enabled. If the design has not been synthesized yet, only ‘ Run Behavioral Simulation’ will be enabled.



Running xelab...

```
Compiling module secureip.gtxe2_c140697
Compiling module secureip.gtxe2_c096021
Compiling module secureip.gtxe2_c677618
Compiling module secureip.gtxe2_c784824
Compiling module secureip.gtxe2_c228351
Compiling module secureip.gtxe2_c291091
Compiling module secureip.gtxe2_c009124(CHECK_SKEW=10,INIT...
Compiling module secureip.gtxe2_c050900
Compiling module secureip.gtxe2_c990570
```

Figure 30 – PCIe Example Design Simulation in Vivado Simulator


Behavioral Simulation - Functional - sim_1 - board
Scopes
Objects
Untitled 1
Scope
Sources
Simulation Scope Properties
Tcl Console

Name	Design Unit	Block Type
board	board	Verilog Mo…
EP	xilinx_pcie_2…	Verilog Mo…
RP	xilinx_pcie_2…	Verilog Mo…
CLK_GEN_RP	sys_clk_gen	Verilog Mo…
CLK_GEN_EP	sys_clk_gen_…	Verilog Mo…
Initial193_337…	board	Verilog Pro…
Initial212_337…	board	Verilog Pro…
glbl	glbl	Verilog Mo…
Initial53_33755	glbl	Verilog Pro…
Initial61_33756	glbl	Verilog Pro

board

Name: /board
Design unit: board
Block type: Verilog Module

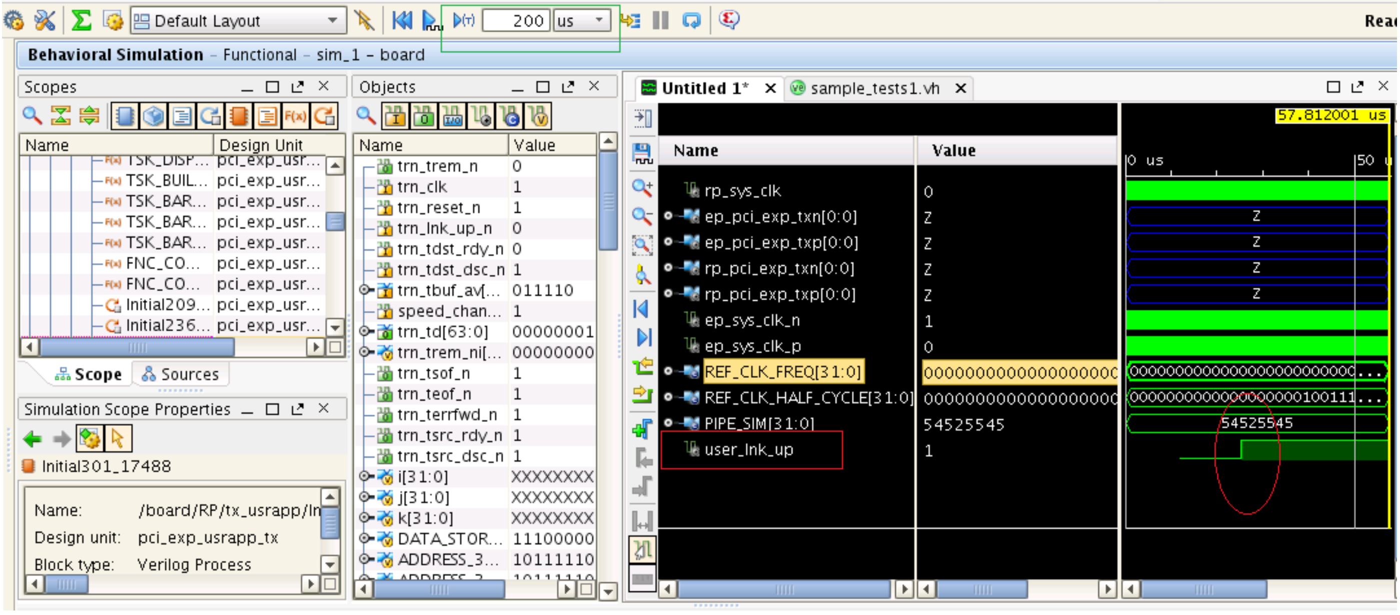
Name	Value	Data T…
i[31:0]	00000000…	Array
sys_rst_n	0	Logic
ep_sys_clk	Z	Logic
rp_sys_clk	0	Logic
ep_pci_exp_…	1	Array
ep_pci_exp_…	1	Array
rp_pci_exp_…	1	Array
rp_pci_exp_…	1	Array
ep_sys_clk_n	1	Logic
ep_sys_clk_p	0	Logic
REF_CLK_FR…	0	Array
REF_CLK_HA…	5000	Array

Name	Value
i[31:0]	000000000000000000
sys_rst_n	0
ep_sys_clk	Z
rp_sys_clk	0
ep_pci_exp_txn[0:0]	1
ep_pci_exp_txp[0:0]	1
rp_pci_exp_txn[0:0]	1
rp_pci_exp_txp[0:0]	1
ep_sys_clk_n	1
ep_sys_clk_p	0
REF_CLK_FREQ[31:0]	000000000000000000
REF_CLK_HALF_CYCLE[3	000000000000000000

```
Running default test {sample_smoke_test0}......
[                    0] : System Reset Asserted...
run: Time (s): cpu = 00:00:02 ; elapsed = 00:00:06 . Memory (MB): peak = 2794.605 ; gain = 0.000
xsim: Time (s): cpu = 00:00:12 ; elapsed = 00:00:16 . Memory (MB): peak = 2794.605 ; gain = 30.016
INFO: [Vivado 12-1395] XSim completed. Design snapshot 'board_behav' loaded.
launch_xsim: Time (s): cpu = 00:24:48 ; elapsed = 00:05:41 . Memory (MB): peak = 2794.605 ; gain = 30.203
```

Figure 31 – Vivado Example Design Project GUI after running Behavioral Simulation

After running the simulation, you could select the signals from the 'objects' window shown in Figure 32 and drag it to the waveform viewer. Figure 32 shows *user_lnk_up* signal in the waveform viewer. This signal indicates that the PCIe link between the Endpoint and the Root Port has come up and the enumeration from root port to the endpoint can be started.



Name	Design Unit
TSK_DISP...	pci_exp_usr...
TSK_BUIL...	pci_exp_usr...
TSK_BAR...	pci_exp_usr...
TSK_BAR...	pci_exp_usr...
TSK_BAR...	pci_exp_usr...
FNC_CO...	pci_exp_usr...
FNC_CO...	pci_exp_usr...
Initial209...	pci_exp_usr...
Initial236...	pci_exp_usr...

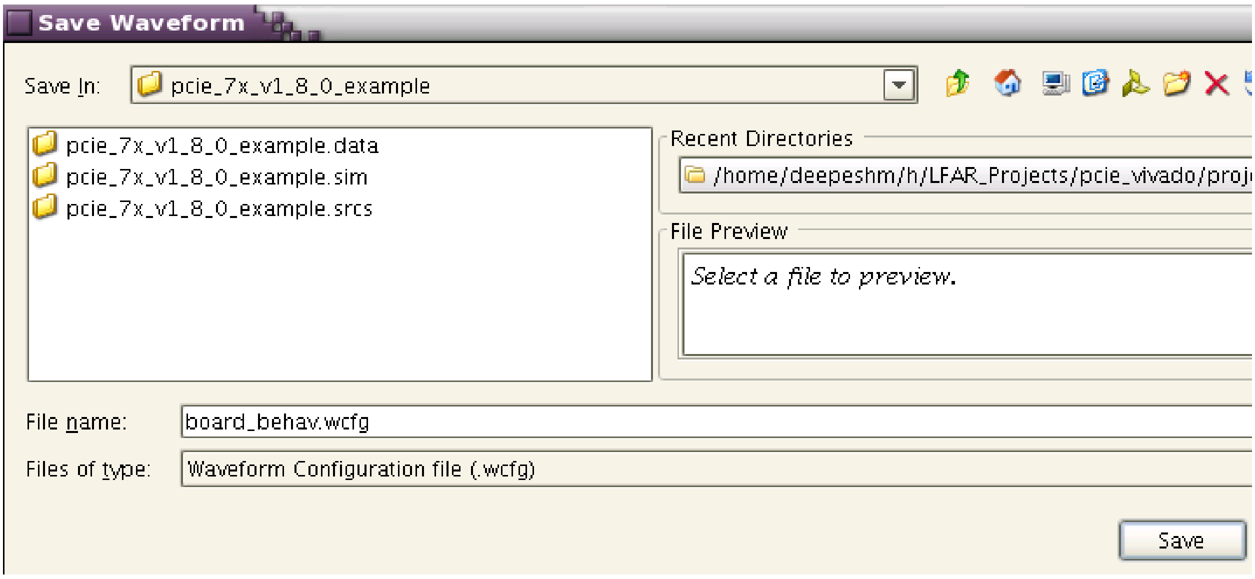
Name: /board/RP/tx_usrapp/In
Design unit: pci_exp_usrapp_tx
Block type: Verilog Process

Name	Value
trn_trem_n	0
trn_clk	1
trn_reset_n	1
trn_lnk_up_n	0
trn_tdst_rdy_n	0
trn_tdst_dsc_n	1
trn_tbuf_av[...	011110
speed_chan...	1
trn_td[63:0]	00000001
trn_trem_ni[...	00000000
trn_tsof_n	1
trn_teof_n	1
trn_terrfwd_n	1
trn_tsrc_rdy_n	1
trn_tsrc_dsc_n	1
i[31:0]	XXXXXXXX
j[31:0]	XXXXXXXX
k[31:0]	XXXXXXXX
DATA_STOR...	11100000
ADDRESS_3...	10111110

Name	Value
rp_sys_clk	0
ep_pci_exp_txn[0:0]	Z
ep_pci_exp_txp[0:0]	Z
rp_pci_exp_txn[0:0]	Z
rp_pci_exp_txp[0:0]	Z
ep_sys_clk_n	1
ep_sys_clk_p	0
REF_CLK_FREQ[31:0]	0000000000000000000
REF_CLK_HALF_CYCLE[31:0]	0000000000000000000
PIPE_SIM[31:0]	54525545
user_lnk_up	1

Figure 32 – PCIe 'user_lnk_up' Assertion

If you do not save the signals that you selected for monitoring in the waveform viewer, all this will be lost if you re-run the simulation. In order that the same set of selected signals appear on the waveform viewer after re-running the simulation, save your waveform file as shown in Figure 33 and also select this waveform in the 'view wave' option as shown in Figure 34.



Save In: pcie_7x_v1_8_0_example

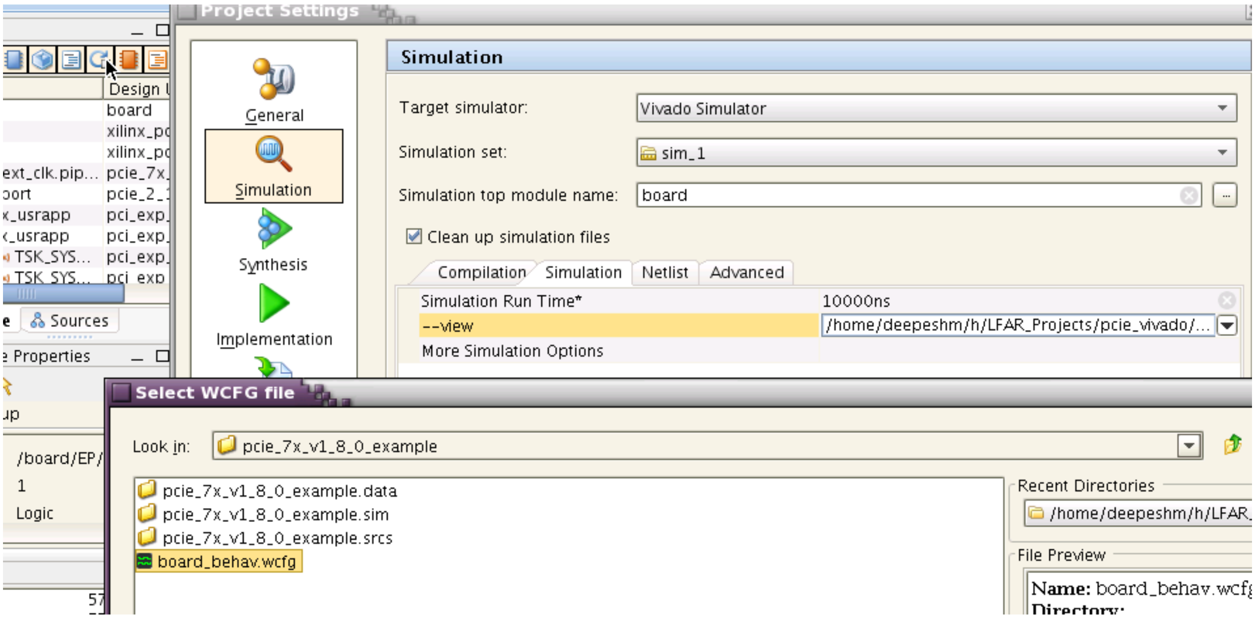
pcie_7x_v1_8_0_example.data
pcie_7x_v1_8_0_example.sim
pcie_7x_v1_8_0_example.srcs

/home/deepeshm/h/LFAR_Projects/pcie_vivado/proj

File name: board_behav.wcfg

Files of type: Waveform Configuration file (.wcfg)

Figure 33 – Saving Vivado Simulation Waveform



Project Settings

Simulation

Target simulator: Vivado Simulator

Simulation set: sim_1

Simulation top module name: board

☑ Clean up simulation files

Simulation Run Time*	10000ns
--view	/home/deepeshm/h/LFAR_Projects/pcie_vivado/...
More Simulation Options	

Select WCFG file

Look in: pcie_7x_v1_8_0_example

- pcie_7x_v1_8_0_example.data
- pcie_7x_v1_8_0_example.sim
- pcie_7x_v1_8_0_example.srcs
- board_behav.wcfg

Recent Directories: /home/deepeshm/h/LFAR_

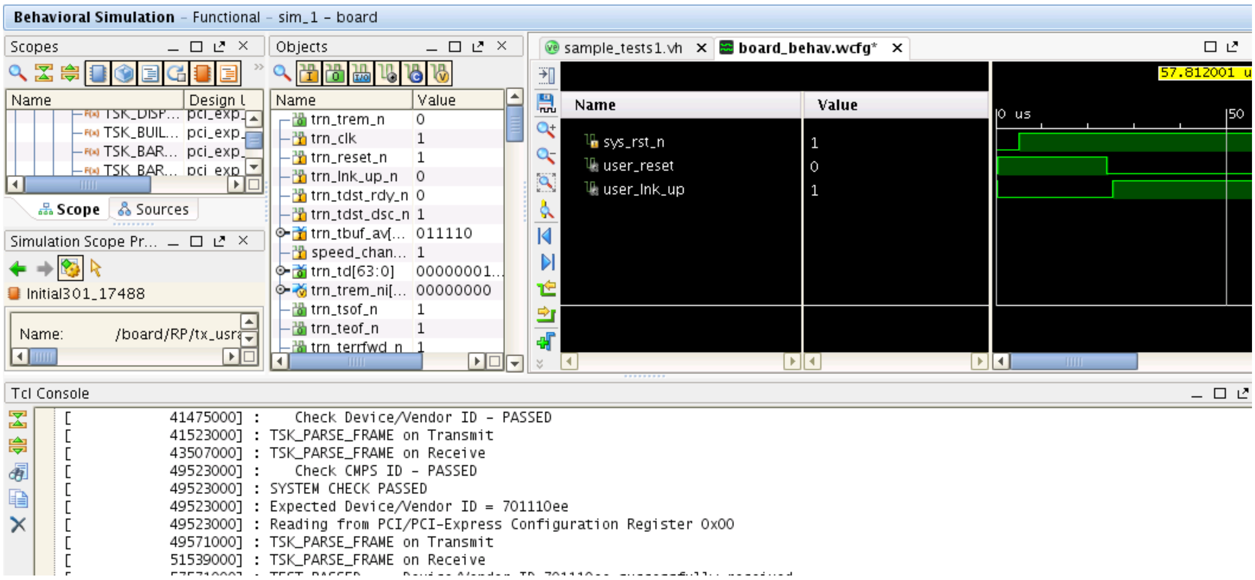
File Preview

Name: board_behav.wcfg

Directory:

Figure 34 - Open already Saved Vivado Simulation Waveform

Figure 35 shows the PCIe example design simulation in progress. In the working simulation, the *user_lnk_up* should be asserted and you should see the output on the console as shown in Figure 35.



Behavioral Simulation - Functional - sim_1 - board

Simulation Scope Properties: Initial301_17488

Name: /board/RP/tx_usra

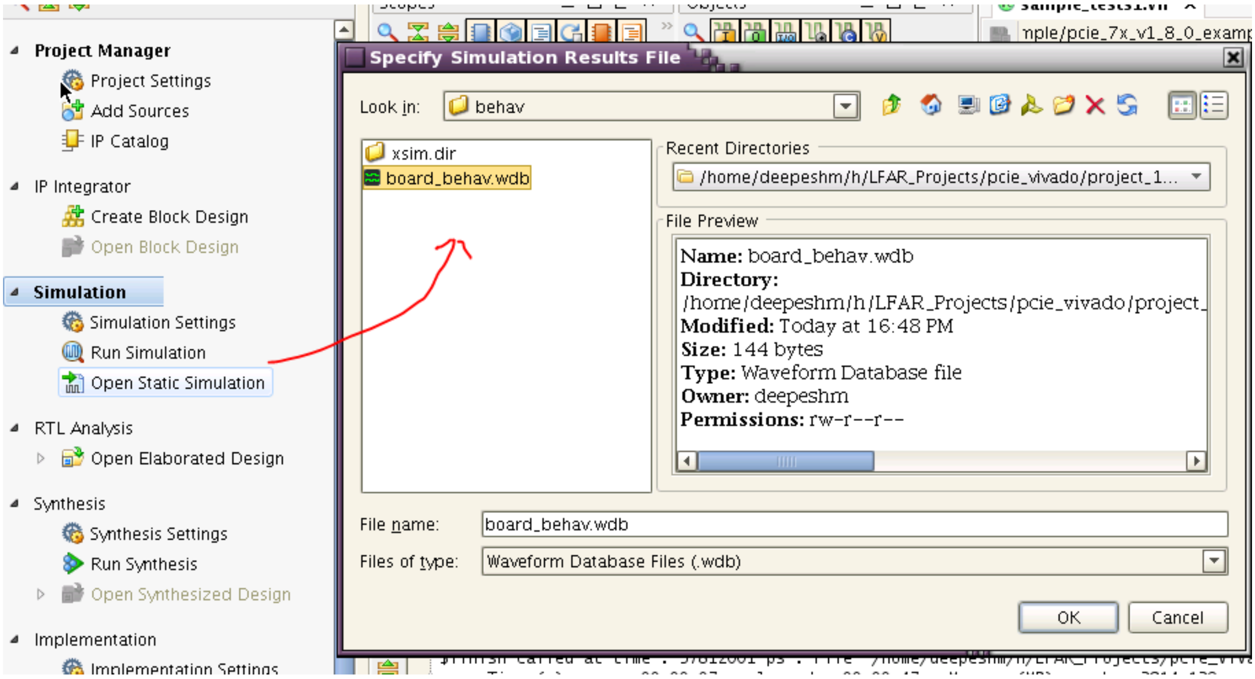
Name	Value
trn_trem_n	0
trn_clk	1
trn_reset_n	1
trn_lnk_up_n	0
trn_tdst_rdy_n	0
trn_tdst_dsc_n	1
trn_tbuf_av[...	011110
speed_chan...	1
trn_td[63:0]	00000001...
trn_trem_ni[...	00000000
trn_tsof_n	1
trn_teof_n	1
trn_terrfwd_n	1

Name	Value
sys_rst_n	1
user_reset	0
user_lnk_up	1

```
[            41475000] :     Check Device/Vendor ID - PASSED
[            41523000] : TSK_PARSE_FRAME on Transmit
[            43507000] : TSK_PARSE_FRAME on Receive
[            49523000] :     Check CMPS ID - PASSED
[            49523000] : SYSTEM CHECK PASSED
[            49523000] : Expected Device/Vendor ID = 701110ee
[            49523000] : Reading from PCI/PCI-Express Configuration Register 0x00
[            49571000] : TSK_PARSE_FRAME on Transmit
[            51539000] : TSK_PARSE_FRAME on Receive
[            57571000] : TEST PASSED --- Device/Vendor ID 701110ee successfully received
```

Figure 35 –PCIe Example Design Simulation in Progress

You could also run the already ran simulation by opening *.wdb file as shown in Figure 36.



Look in: behav

xsim.dir
board_behav.wdb

Recent Directories: /home/deepeshm/h/LFAR_Projects/pcie_vivado/project_1...

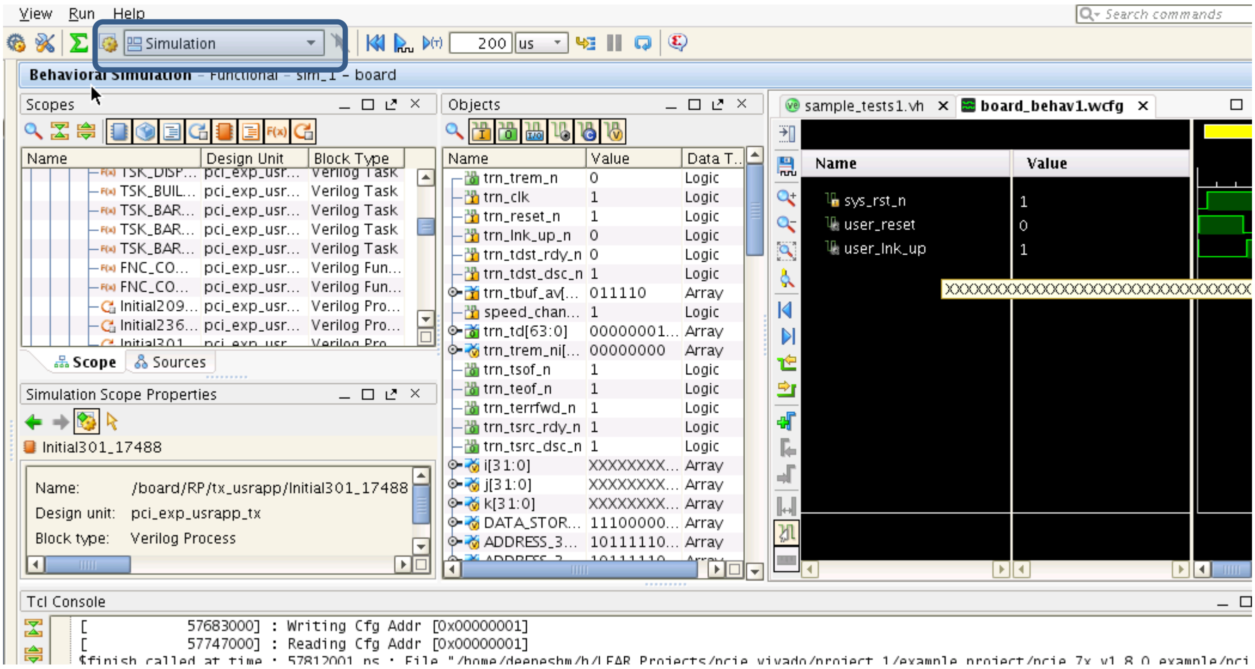
Name: board_behav.wdb
Directory: /home/deepeshm/h/LFAR_Projects/pcie_vivado/project_
Modified: Today at 16:48 PM
Size: 144 bytes
Type: Waveform Database file
Owner: deepeshm
Permissions: rw-r--r--

File name: board_behav.wdb

Files of type: Waveform Database Files (.wdb)

Figure 36 – Open Already Completed Simulation

Vivado has a number of windows. The Vivado GUI allows customizing windows layout by providing a certain layouts specific for Simulation, Floorplanning etc. Figure 37 shows the 'Simulation Layout'



Name	Design Unit	Block Type
TSK_DISP...	pci_exp_usr...	Verilog Task
TSK_BUIL...	pci_exp_usr...	Verilog Task
TSK_BAR...	pci_exp_usr...	Verilog Task
TSK_BAR...	pci_exp_usr...	Verilog Task
TSK_BAR...	pci_exp_usr...	Verilog Task
FNC_CO...	pci_exp_usr...	Verilog Fun...
FNC_CO...	pci_exp_usr...	Verilog Fun...
Initial209...	pci_exp_usr...	Verilog Pro...
Initial236...	pci_exp_usr...	Verilog Pro...
Initial301...	pci_exp_usr...	Verilog Pro...

Initial301_17488

Name: /board/RP/tx_usrapp/Initial301_17488
Design unit: pci_exp_usrapp_tx
Block type: Verilog Process

Name	Value	Data T...
trn_trem_n	0	Logic
trn_clk	1	Logic
trn_reset_n	1	Logic
trn_lnk_up_n	0	Logic
trn_tdst_rdy_n	0	Logic
trn_tdst_dsc_n	1	Logic
trn_tbuf_av[...	011110	Array
speed_chan...	1	Logic
trn_td[63:0]	00000001...	Array
trn_trem_ni[...	00000000	Array
trn_tsof_n	1	Logic
trn_teof_n	1	Logic
trn_terrfwd_n	1	Logic
trn_tsrc_rdy_n	1	Logic
trn_tsrc_dsc_n	1	Logic
i[31:0]	XXXXXXXX...	Array
j[31:0]	XXXXXXXX...	Array
k[31:0]	XXXXXXXX...	Array
DATA_STOR...	11100000...	Array
ADDRESS_3...	10111110...	Array

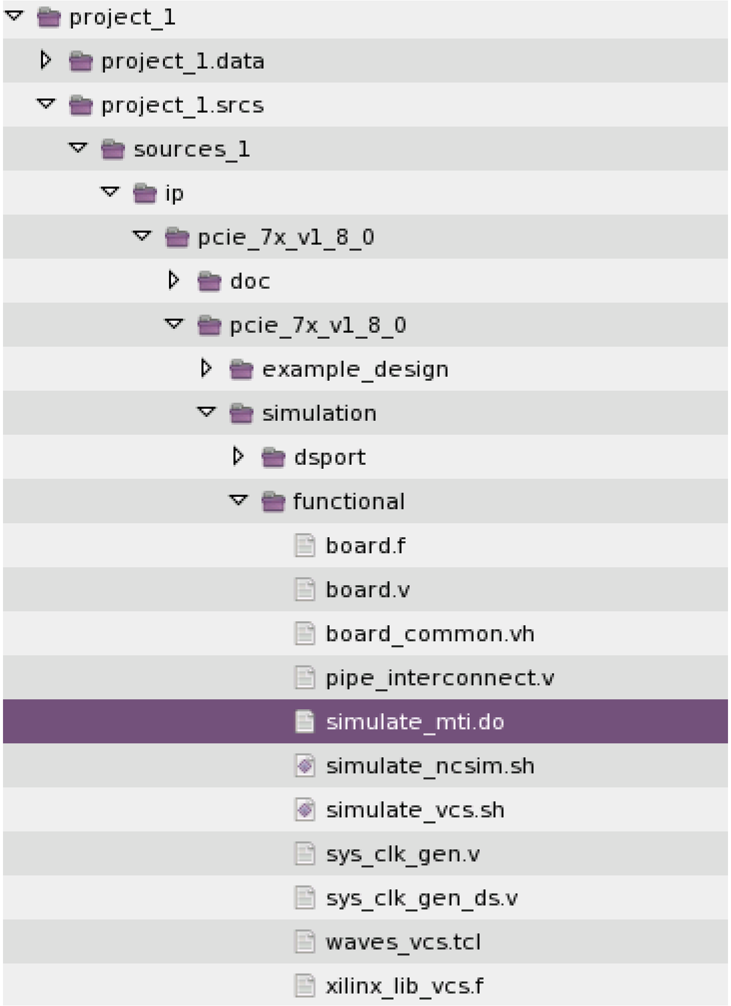
Name	Value
sys_rst_n	1
user_reset	0
user_lnk_up	1

```
[            57683000] : Writing Cfg Addr [0x00000001]
[            57747000] : Reading Cfg Addr [0x00000001]
$finish called at time : 57812001 ns : File "/home/deepeshm/h/LFAR_Projects/pcie_vivado/project_1/example_project/pcie_7x_v1_8_0_example/pci
```

Figure 37 - Vivado Simulation Layout

Simulation in Modelsim

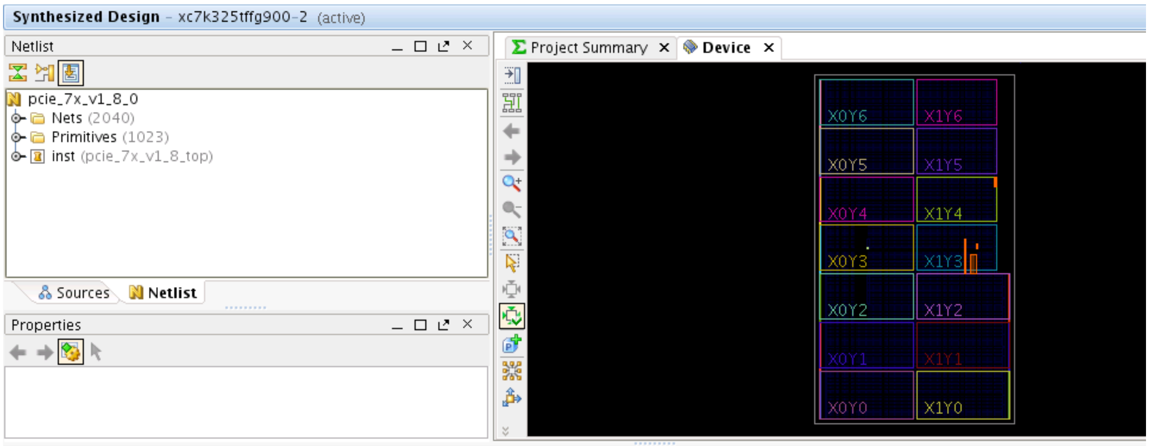
When generating the PCIe Example Design as illustrated in the previous section, it comes with an entire simulation setup along with a script to simulate the example design in Modelsim. The location of that script is shown in Figure 38.



```
project_1
  project_1.data
  project_1.srcs
    sources_1
      ip
        pcie_7x_v1_8_0
          doc
          pcie_7x_v1_8_0
            example_design
            simulation
              dsport
              functional
                board.f
                board.v
                board_common.vh
                pipe_interconnect.v
                simulate_mti.do
                simulate_ncsim.sh
                simulate_vcs.sh
                sys_clk_gen.v
                sys_clk_gen_ds.v
                waves_vcs.tcl
                xilinx_lib_vcs.f
```

Figure 38 – PCIe Example Design Modelsim Simulation Script

Debugging with Chipscope



Synthesized Design - xc7k325tffg900-2 (active)

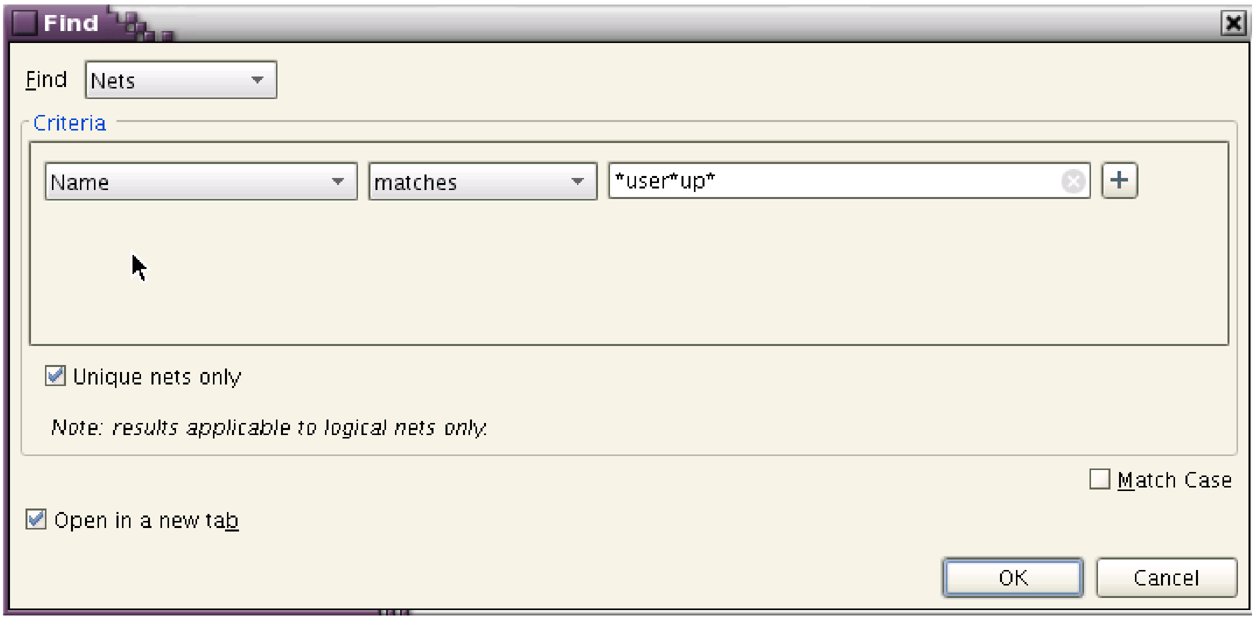
Netlist

```
pcie_7x_v1_8_0
  Nets (2040)
  Primitives (1023)
  inst (pcie_7x_v1_8_top)
```

Figure 39 – PCIe Example Design Vivado Project GUI after opening the Synthesized Design

The details on how to debug a design using chipscope in Vivado is provided in UG936[1]. This section illustrates how to grab signals for debugging in PCIe example design. For more information, please refer to UG936.

Vivado allows selecting signals for debugging, same as in Chipscope inserter. There is an additional feature where you could search for specific nets, using wild cards, in the whole design. This is shown in Figure 40. To start grabbing signals for chipscope, you should first open the synthesized design as shown in Figure 39.



Find: Nets

Criteria

Name | matches | *user*up*

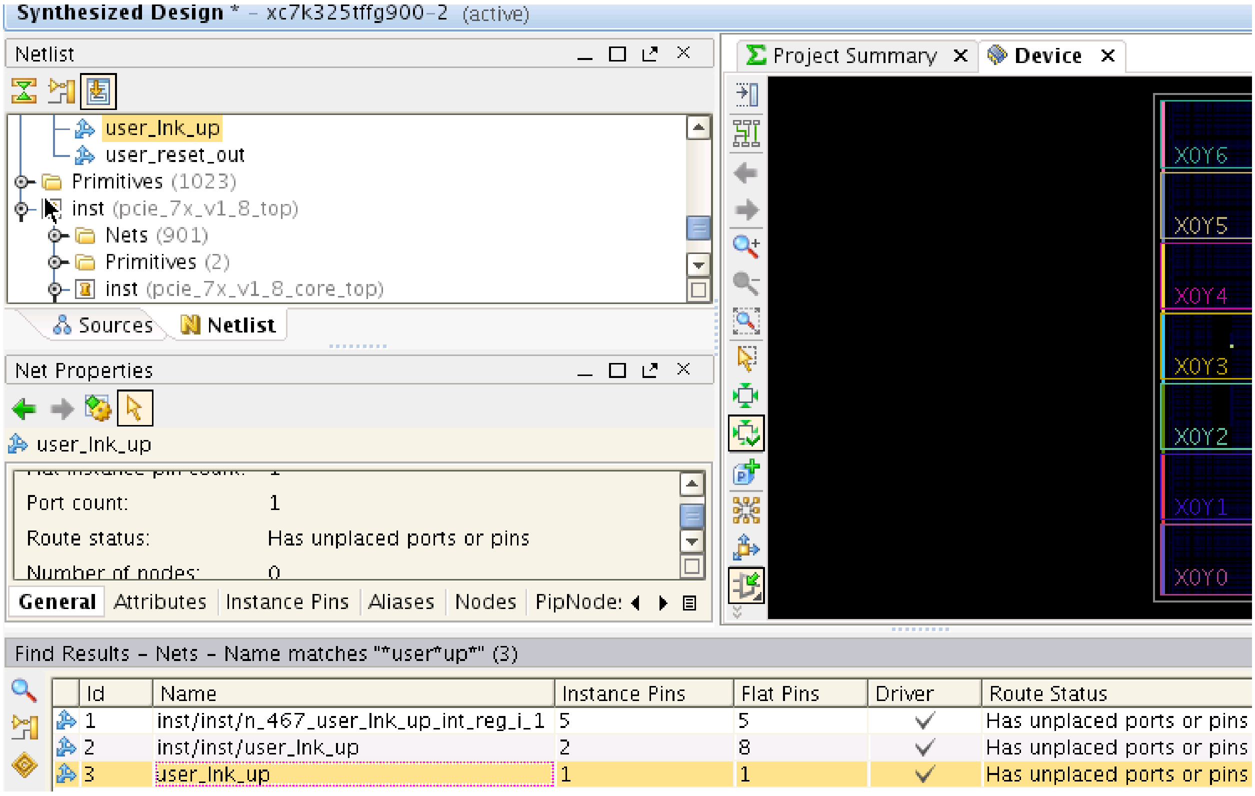
☑ Unique nets only

Note: results applicable to logical nets only.

□ Match Case

☑ Open in a new tab

Figure 40 – Search 'nets' for Probing in Chiscope


Synthesized Design * - xc7k325tffg900-2 (active)

user_lnk_up

Port count: 1

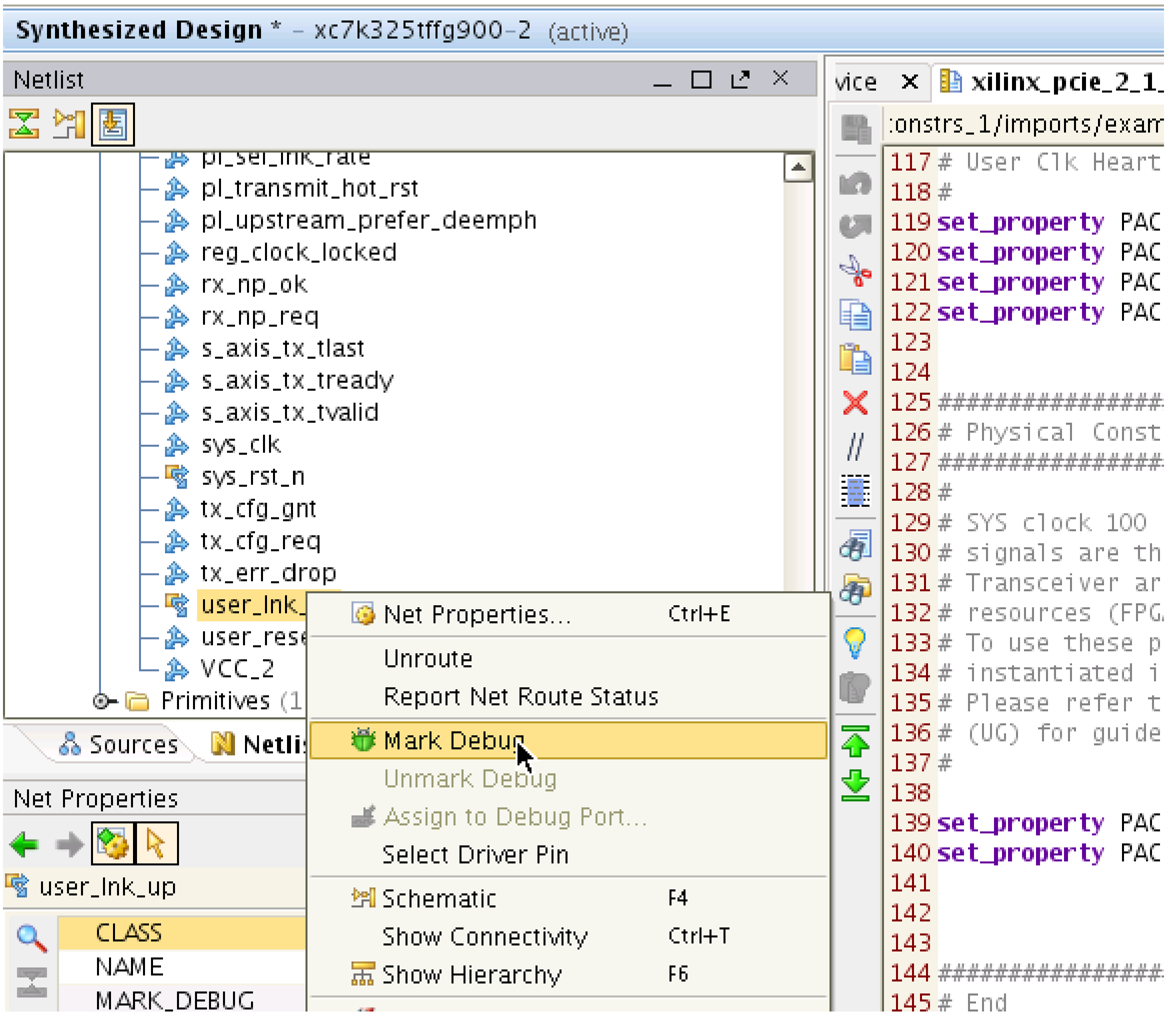
Route status: Has unplaced ports or pins

Number of nodes: 0

Find Results - Nets - Name matches "*user*up*" (3)

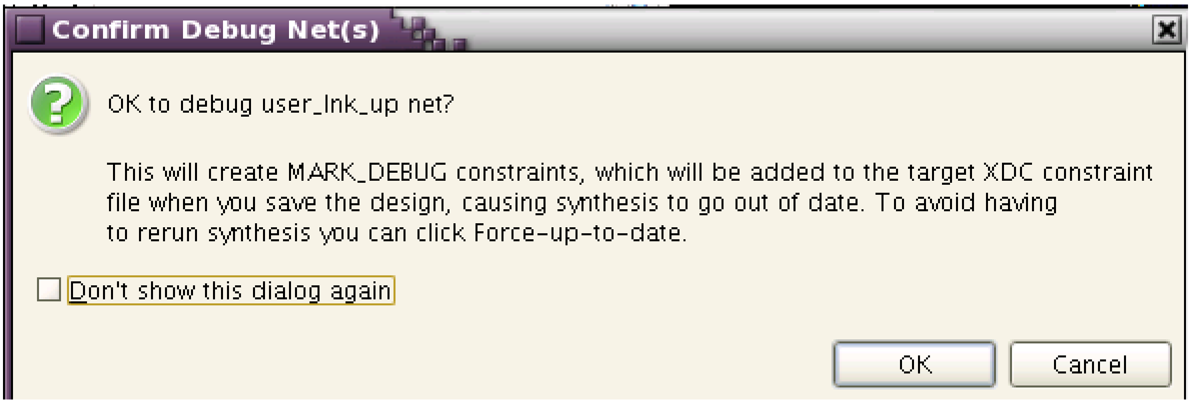
Id	Name	Instance Pins	Flat Pins	Driver	Route Status
1	inst/inst/n_467_user_lnk_up_int_reg_i_1	5	5	✓	Has unplaced ports or pins
2	inst/inst/user_lnk_up	2	8	✓	Has unplaced ports or pins
3	user_lnk_up	1	1	✓	Has unplaced ports or pins

Figure 41 – PCIe Example Design user_lnk_up Signal



```
# User Clk Heart
#
set_property PAC
set_property PAC
set_property PAC
set_property PAC


################
# Physical Const
################
#
# SYS clock 100
# signals are th
# Transceiver ar
# resources (FPG
# To use these p
# instantiated i
# Please refer t
# (UG) for guide
#

set_property PAC
set_property PAC



################
# End
```

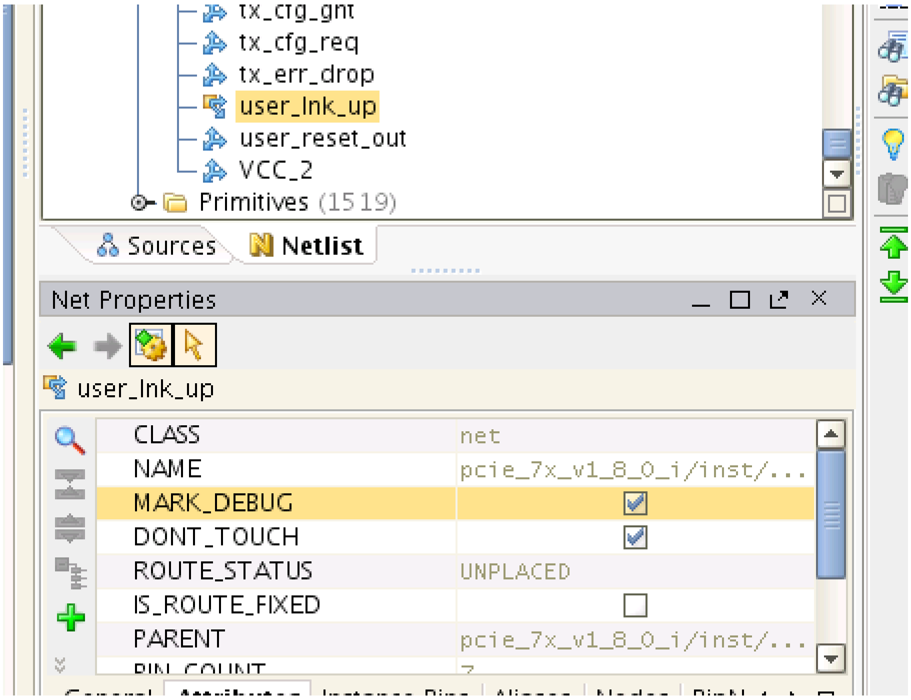
Figure 42 – 'Mark Debug' for Probing user_lnk_up in Chipscope



OK to debug user_lnk_up net?

This will create MARK_DEBUG constraints, which will be added to the target XDC constraint file when you save the design, causing synthesis to go out of date. To avoid having to rerun synthesis you can click Force-up-to-date.

☐ Don't show this dialog again

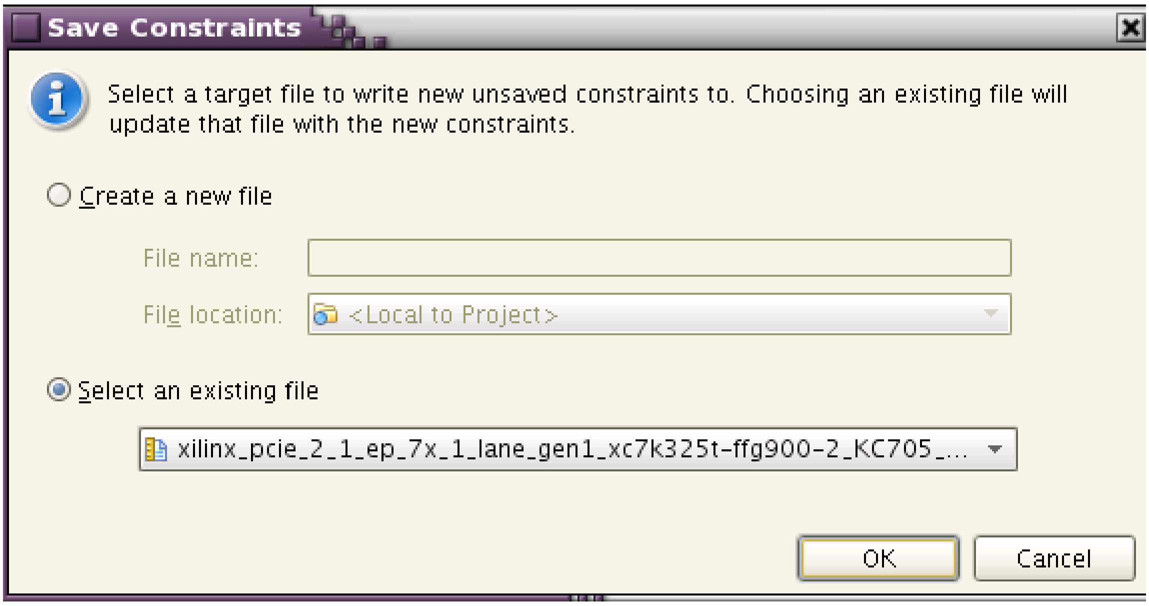


tx_cfg_gnt
tx_cfg_req
tx_err_drop
user_lnk_up
user_reset_out
VCC_2
Primitives (1519)

user_lnk_up

CLASS	net
NAME	pcie_7x_v1_8_0_i/inst/...
MARK_DEBUG	☑
DONT_TOUCH	☑
ROUTE_STATUS	UNPLACED
IS_ROUTE_FIXED	□
PARENT	pcie_7x_v1_8_0_i/inst/...

Figure 43 – user_lnk_up Net Properties after enabling 'MARK_DEBUG'



Save Constraints

Select a target file to write new unsaved constraints to. Choosing an existing file will update that file with the new constraints.

○ Create a new file

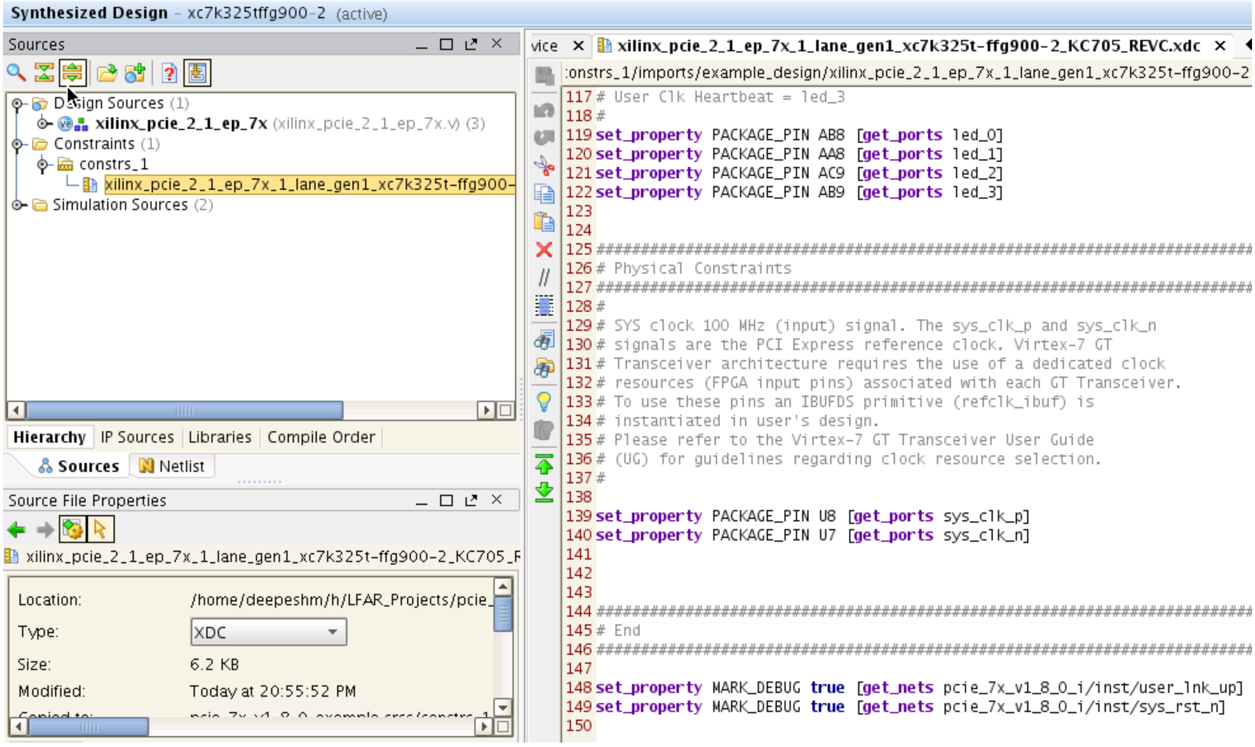
File name:

File location: <Local to Project>

● Select an existing file

xilinx_pcie_2_1_ep_7x_1_lane_gen1_xc7k325t-ffg900-2_KC705_...

Figure 44 – Saving 'Mark Debug' Constraints to the existing XDC file.


Synthesized Design - xc7k325tffg900-2 (active)
Sources
Design Sources (1)
xilinx_pcie_2_1_ep_7x (xilinx_pcie_2_1_ep_7x.v) (3)
Constraints (1)
constrs_1
xilinx_pcie_2_1_ep_7x_1_lane_gen1_xc7k325t-ffg900-
Simulation Sources (2)
Hierarchy
IP Sources
Libraries
Compile Order
Sources
Netlist
Source File Properties
xilinx_pcie_2_1_ep_7x_1_lane_gen1_xc7k325t-ffg900-2_KC705_F
vice
xilinx_pcie_2_1_ep_7x_1_lane_gen1_xc7k325t-ffg900-2_KC705_REVC.xdc
:onstrs_1/imports/example_design/xilinx_pcie_2_1_ep_7x_1_lane_gen1_xc7k325t-ffg900-2

Location: /home/deepeshm/h/LFAR_Projects/pcie_
Type: XDC
Size: 6.2 KB
Modified: Today at 20:55:52 PM

```
# User Clk Heartbeat = led_3
#
set_property PACKAGE_PIN AB8 [get_ports led_0]
set_property PACKAGE_PIN AA8 [get_ports led_1]
set_property PACKAGE_PIN AC9 [get_ports led_2]
set_property PACKAGE_PIN AB9 [get_ports led_3]


##########################################################################
# Physical Constraints
##########################################################################
#
# SYS clock 100 MHz (input) signal. The sys_clk_p and sys_clk_n
# signals are the PCI Express reference clock. Virtex-7 GT
# Transceiver architecture requires the use of a dedicated clock
# resources (FPGA input pins) associated with each GT Transceiver.
# To use these pins an IBUFDS primitive (refclk_ibuf) is
# instantiated in user's design.
# Please refer to the Virtex-7 GT Transceiver User Guide
# (UG) for guidelines regarding clock resource selection.
#

set_property PACKAGE_PIN U8 [get_ports sys_clk_p]
set_property PACKAGE_PIN U7 [get_ports sys_clk_n]



##########################################################################
# End
##########################################################################

set_property MARK_DEBUG true [get_nets pcie_7x_v1_8_0_i/inst/user_lnk_up]
set_property MARK_DEBUG true [get_nets pcie_7x_v1_8_0_i/inst/sys_rst_n]

```

Figure 45 – MARK_DEBUG Constraint in PCIe Example Design XDC File

Generating Debug Cores (Set up Debug)

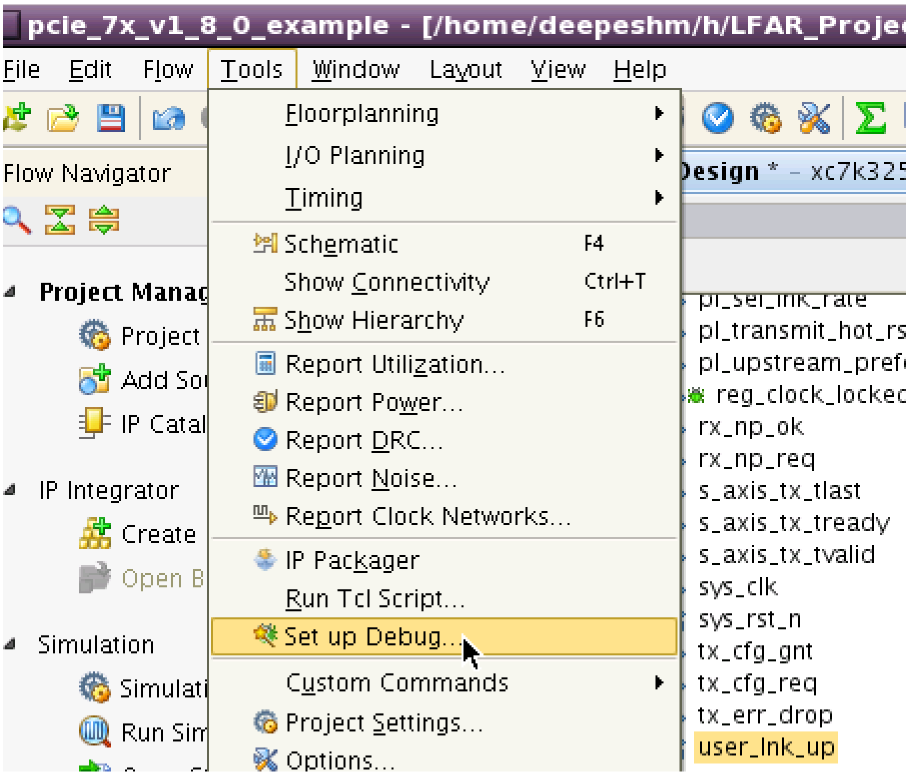
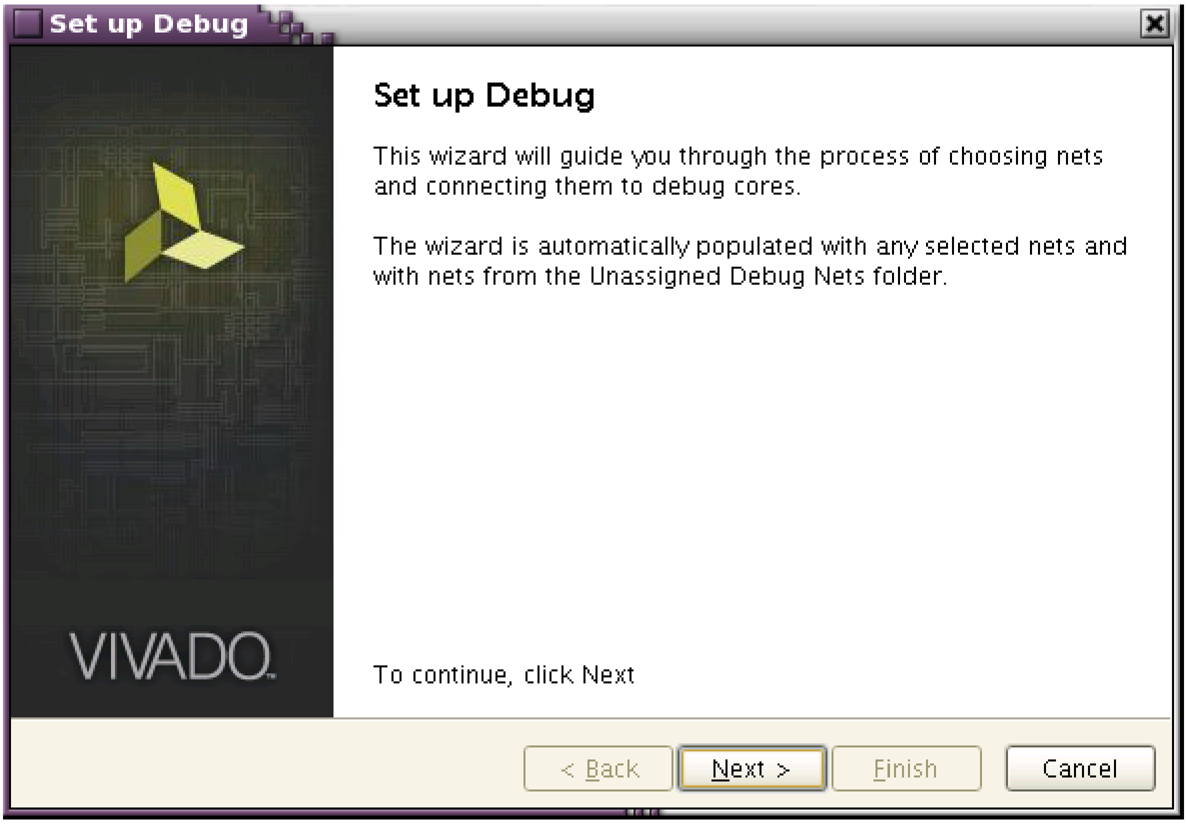


Figure 46 – Generating Debug Cores



Set up Debug

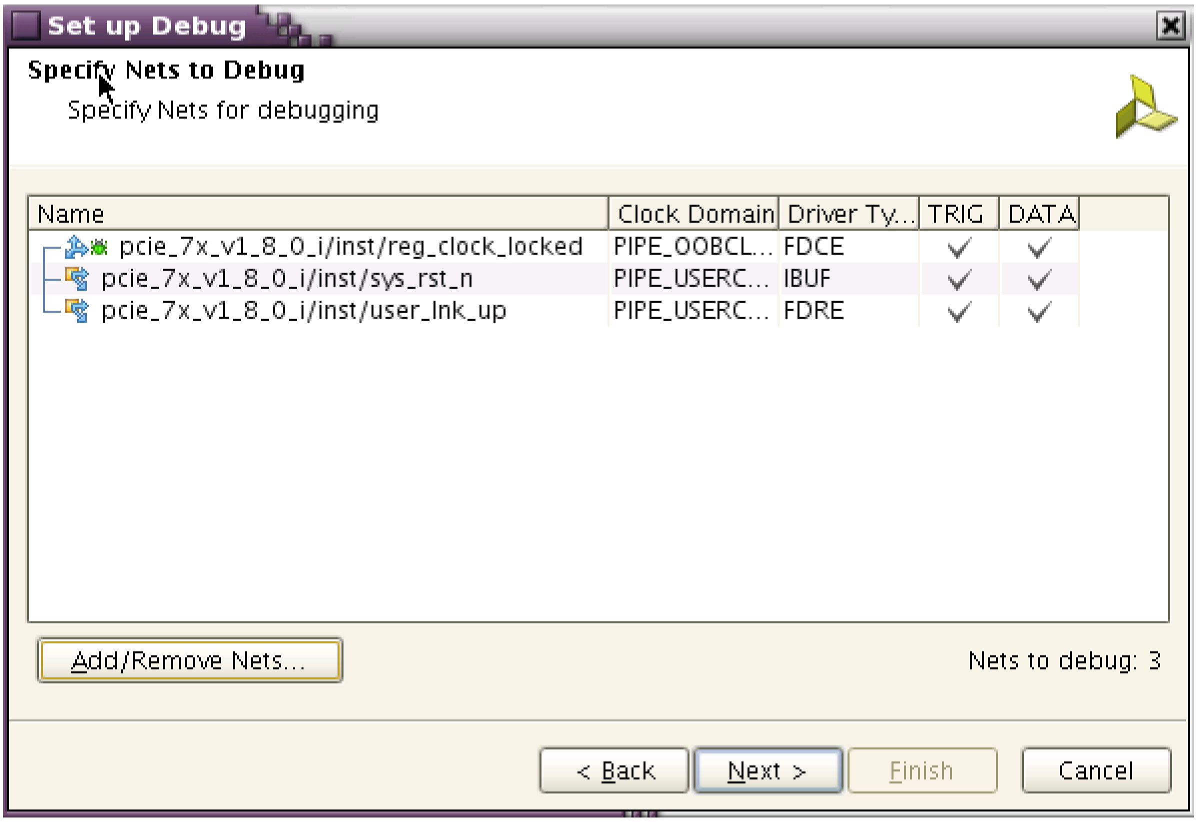
Set up Debug

This wizard will guide you through the process of choosing nets and connecting them to debug cores.

The wizard is automatically populated with any selected nets and with nets from the Unassigned Debug Nets folder.

To continue, click Next

Figure 47 – Setup Debug GUI



Set up Debug

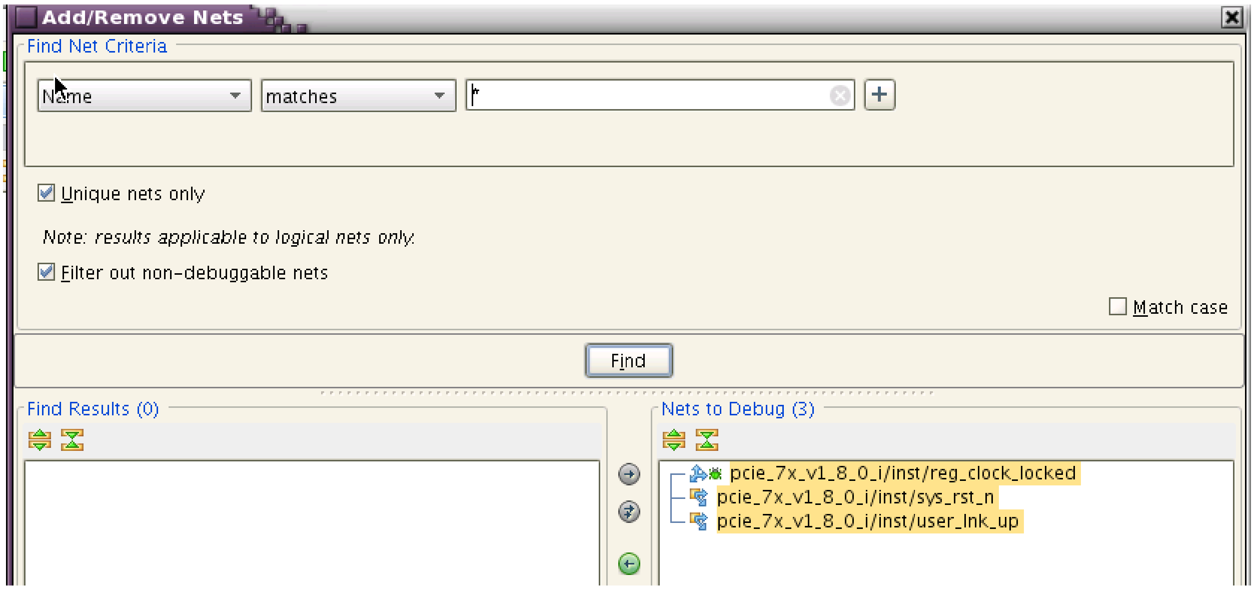
Specify Nets to Debug

Specify Nets for debugging

Name	Clock Domain	Driver Ty...	TRIG	DATA
pcie_7x_v1_8_0_i/inst/reg_clock_locked	PIPE_OOBCL...	FDCE	✓	✓
pcie_7x_v1_8_0_i/inst/sys_rst_n	PIPE_USERC...	IBUF	✓	✓
pcie_7x_v1_8_0_i/inst/user_lnk_up	PIPE_USERC...	FDRE	✓	✓

Nets to debug: 3

Figure 48 – Selected Nets for Probing in Chipscope



Add/Remove Nets

Find Net Criteria

Name matches *

☑ Unique nets only

Note: results applicable to logical nets only.

☑ Filter out non-debuggable nets

□ Match case

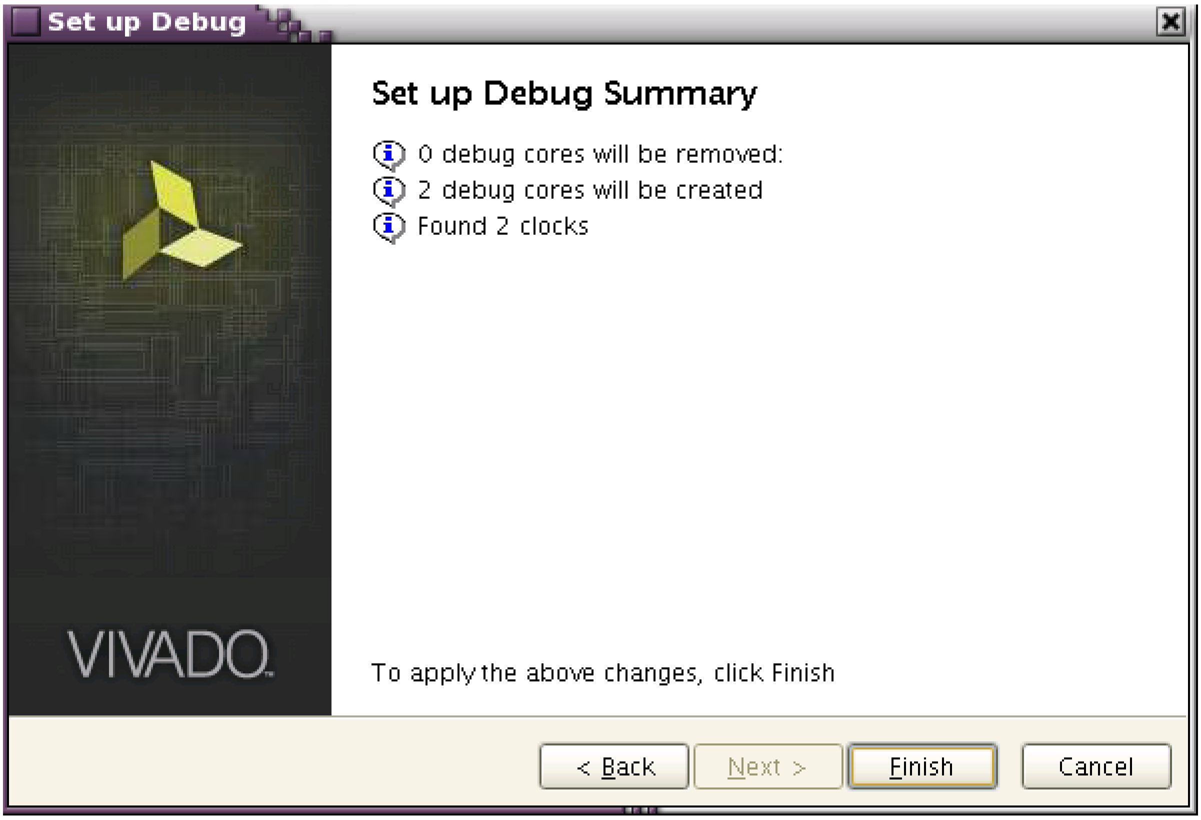
Find

Find Results (0)

Nets to Debug (3)

- pcie_7x_v1_8_0_i/inst/reg_clock_locked
- pcie_7x_v1_8_0_i/inst/sys_rst_n
- pcie_7x_v1_8_0_i/inst/user_lnk_up

Figure 49 – Add/Remove nets in Setup Debug



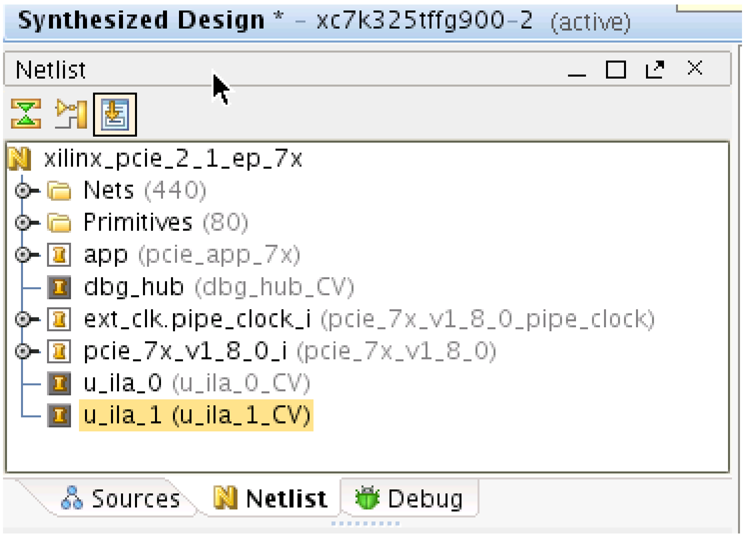
Set up Debug

Set up Debug Summary

- 0 debug cores will be removed:
- 2 debug cores will be created
- Found 2 clocks

To apply the above changes, click Finish

Figure 50 - Set up Debug Summary

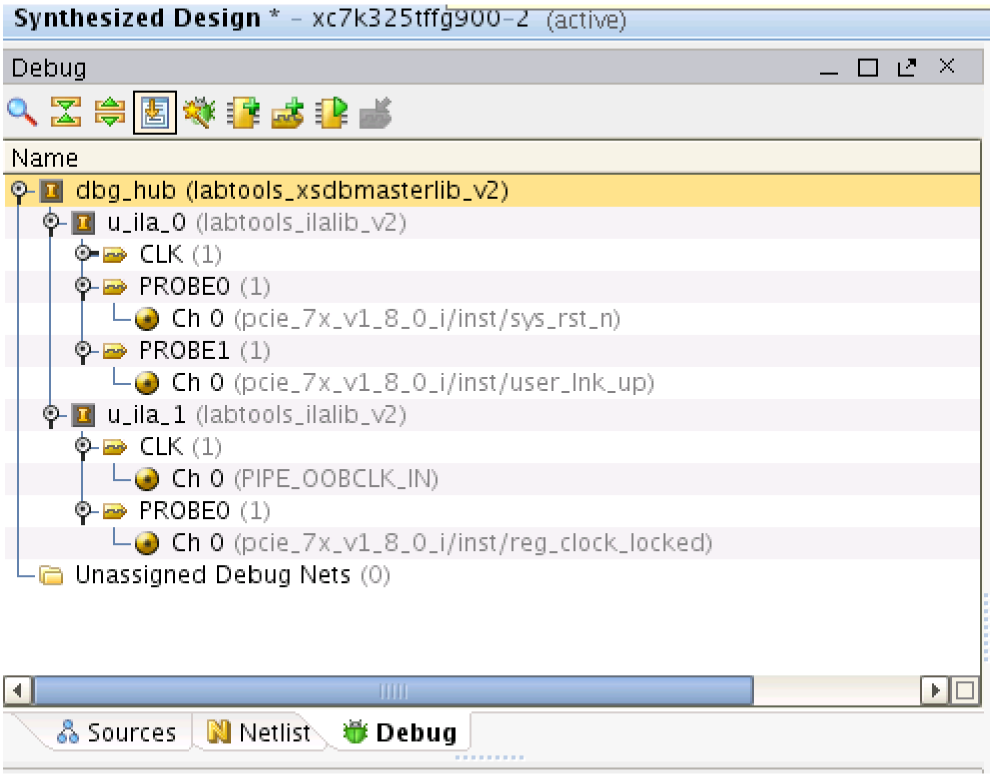


Synthesized Design * – xc7k325tffg900-2 (active)

Netlist

- xilinx_pcie_2_1_ep_7x
  - Nets (440)
  - Primitives (80)
  - app (pcie_app_7x)
  - dbg_hub (dbg_hub_CV)
  - ext_clk.pipe_clock_i (pcie_7x_v1_8_0_pipe_clock)
  - pcie_7x_v1_8_0_i (pcie_7x_v1_8_0)
  - u_ila_0 (u_ila_0_CV)
  - u_ila_1 (u_ila_1_CV)

Figure 51 – Chipscope Debug Cores in Netlist Window



Synthesized Design * – xc7k325tffg900-2 (active)

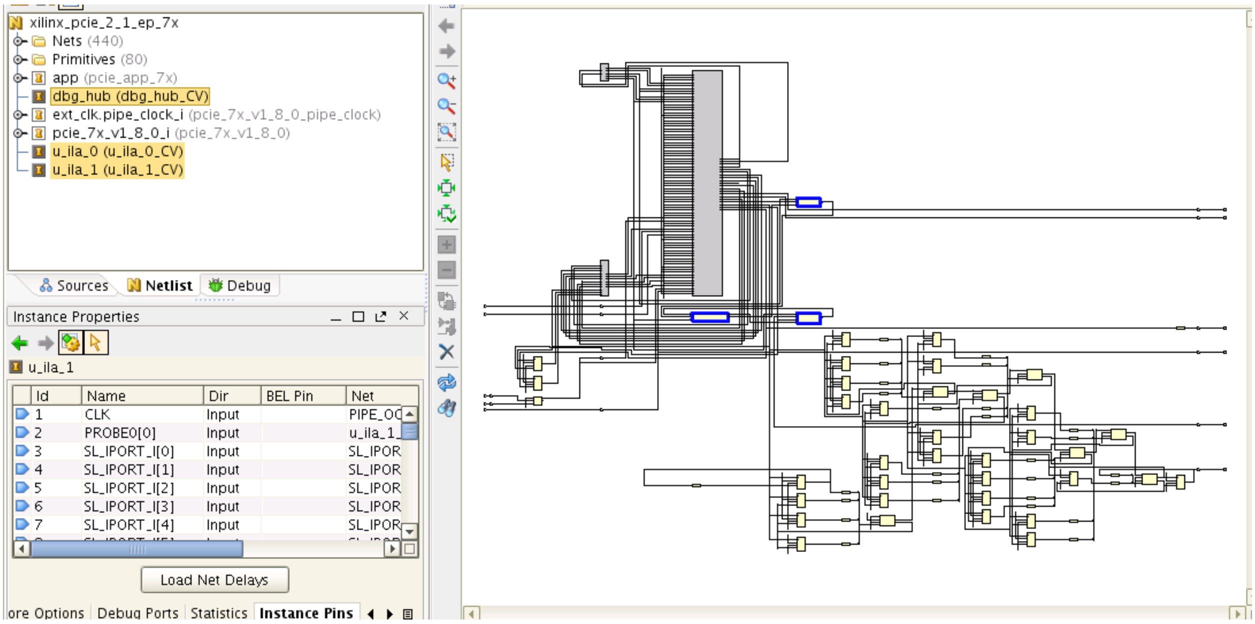
Debug

Name

- dbg_hub (labtools_xsdbmasterlib_v2)
  - u_ila_0 (labtools_ilalib_v2)
    - CLK (1)
    - PROBE0 (1)
      - Ch 0 (pcie_7x_v1_8_0_i/inst/sys_rst_n)
    - PROBE1 (1)
      - Ch 0 (pcie_7x_v1_8_0_i/inst/user_lnk_up)
  - u_ila_1 (labtools_ilalib_v2)
    - CLK (1)
      - Ch 0 (PIPE_OOBCLK_IN)
    - PROBE0 (1)
      - Ch 0 (pcie_7x_v1_8_0_i/inst/reg_clock_locked)
- Unassigned Debug Nets (0)

Figure 52 – PCIe Example Design Selected Debug Signals in 'Debug' Window

Debug Cores Schematic



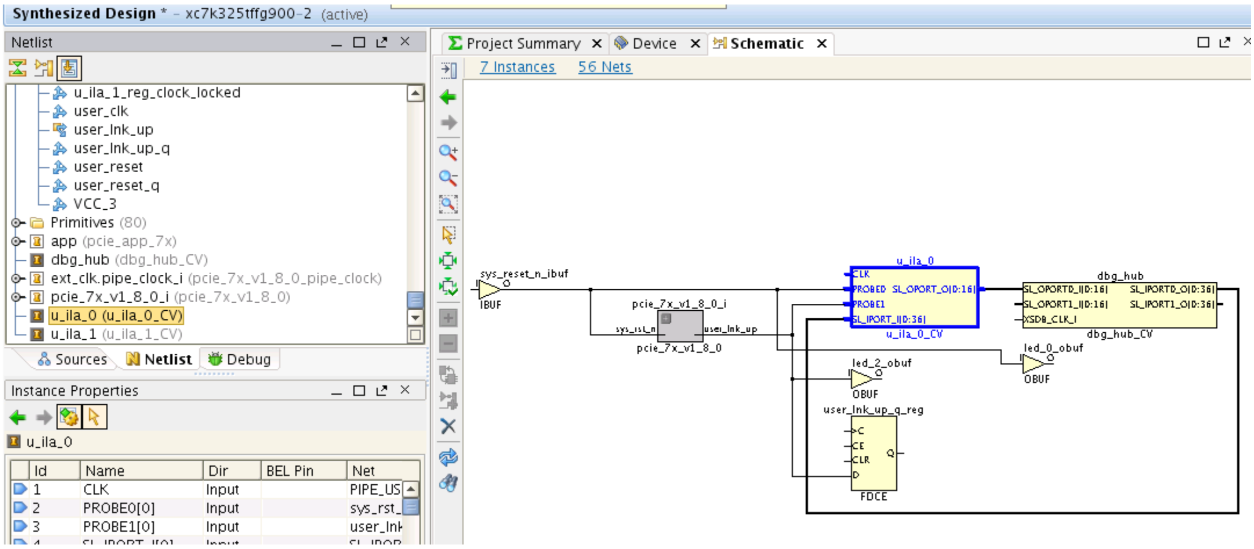
xilinx_pcie_2_1_ep_7x
- Nets (440)
- Primitives (80)
- app (pcie_app_7x)
- dbg_hub (dbg_hub_CV)
- ext_clk.pipe_clock_i (pcie_7x_v1_8_0_pipe_clock)
- pcie_7x_v1_8_0_i (pcie_7x_v1_8_0)
- u_ila_0 (u_ila_0_CV)
- u_ila_1 (u_ila_1_CV)

Instance Properties

u_ila_1

Id	Name	Dir	BEL Pin	Net
1	CLK	Input		PIPE_OC
2	PROBE0[0]	Input		u_ila_1_
3	SL_IPORT_I[0]	Input		SL_IPOR
4	SL_IPORT_I[1]	Input		SL_IPOR
5	SL_IPORT_I[2]	Input		SL_IPOR
6	SL_IPORT_I[3]	Input		SL_IPOR
7	SL_IPORT_I[4]	Input		SL_IPOR

Figure 53 - PCIe Example Design Schematic with Debug Cores



Synthesized Design * - xc7k325tffg900-2 (active)

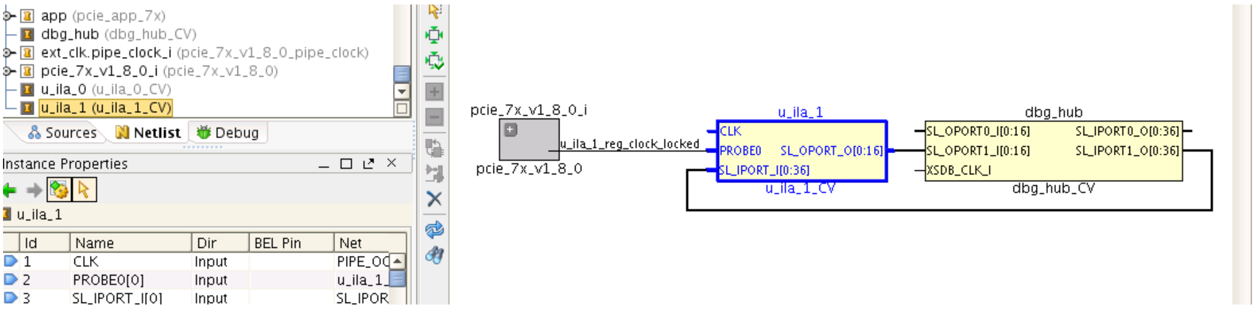
Netlist
- u_ila_1_reg_clock_locked
- user_clk
- user_lnk_up
- user_lnk_up_q
- user_reset
- user_reset_q
- VCC_3
- Primitives (80)
- app (pcie_app_7x)
- dbg_hub (dbg_hub_CV)
- ext_clk.pipe_clock_i (pcie_7x_v1_8_0_pipe_clock)
- pcie_7x_v1_8_0_i (pcie_7x_v1_8_0)
- u_ila_0 (u_ila_0_CV)
- u_ila_1 (u_ila_1_CV)

Instance Properties

u_ila_0

Id	Name	Dir	BEL Pin	Net
1	CLK	Input		PIPE_US
2	PROBE0[0]	Input		sys_rst_
3	PROBE1[0]	Input		user_lnk

Figure 54 – ILA_0 Core



- app (pcie_app_7x)
- dbg_hub (dbg_hub_CV)
- ext_clk.pipe_clock_i (pcie_7x_v1_8_0_pipe_clock)
- pcie_7x_v1_8_0_i (pcie_7x_v1_8_0)
- u_ila_0 (u_ila_0_CV)
- u_ila_1 (u_ila_1_CV)

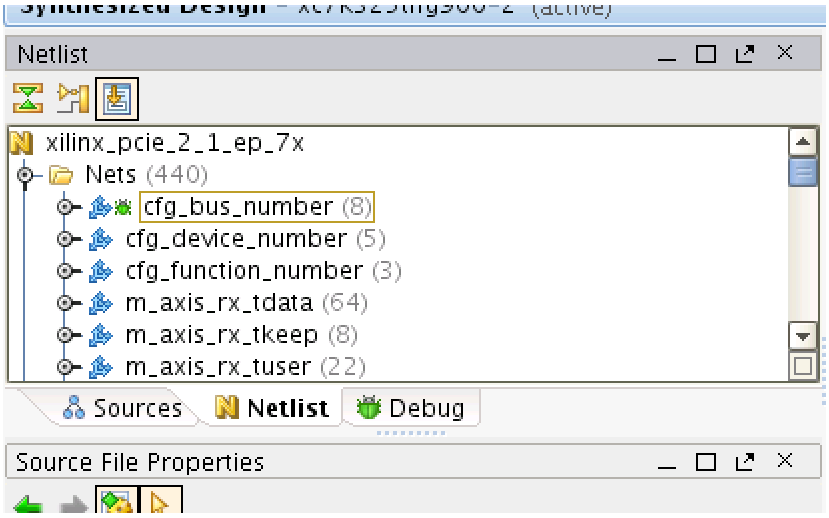
Instance Properties

u_ila_1

Id	Name	Dir	BEL Pin	Net
1	CLK	Input		PIPE_OC
2	PROBE0[0]	Input		u_ila_1_
3	SL_IPORT_I[0]	Input		SL_IPOR

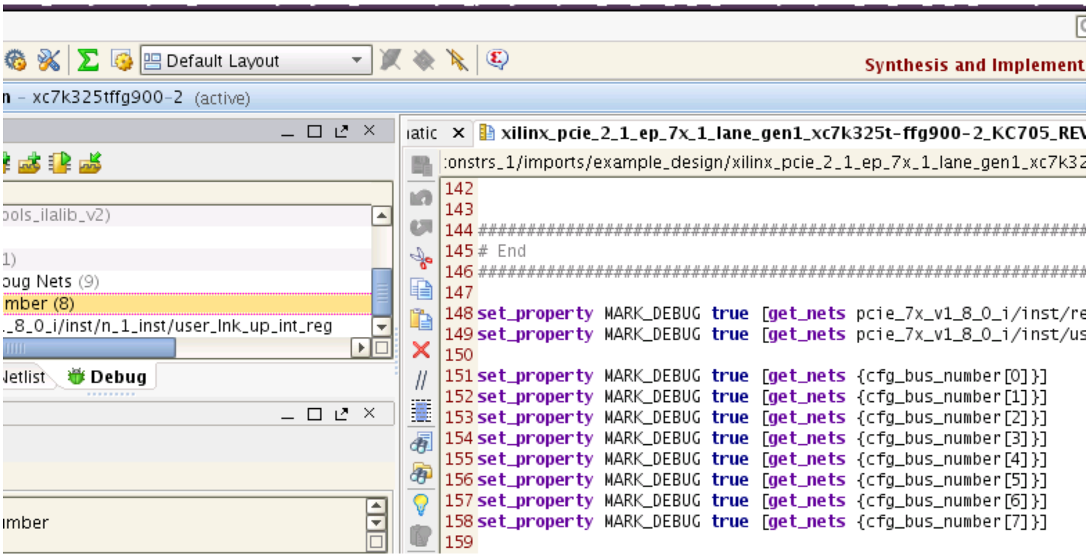
Figure 55 – ILA_1 Core

Adding More Nets for Chipscope Debugging



```
xilinx_pcie_2_1_ep_7x
  Nets (440)
    cfg_bus_number (8)
    cfg_device_number (5)
    cfg_function_number (3)
    m_axis_rx_tdata (64)
    m_axis_rx_tkeep (8)
    m_axis_rx_tuser (22)
```

Figure 56 – Add cfg_bus_number for probing in Chipscope

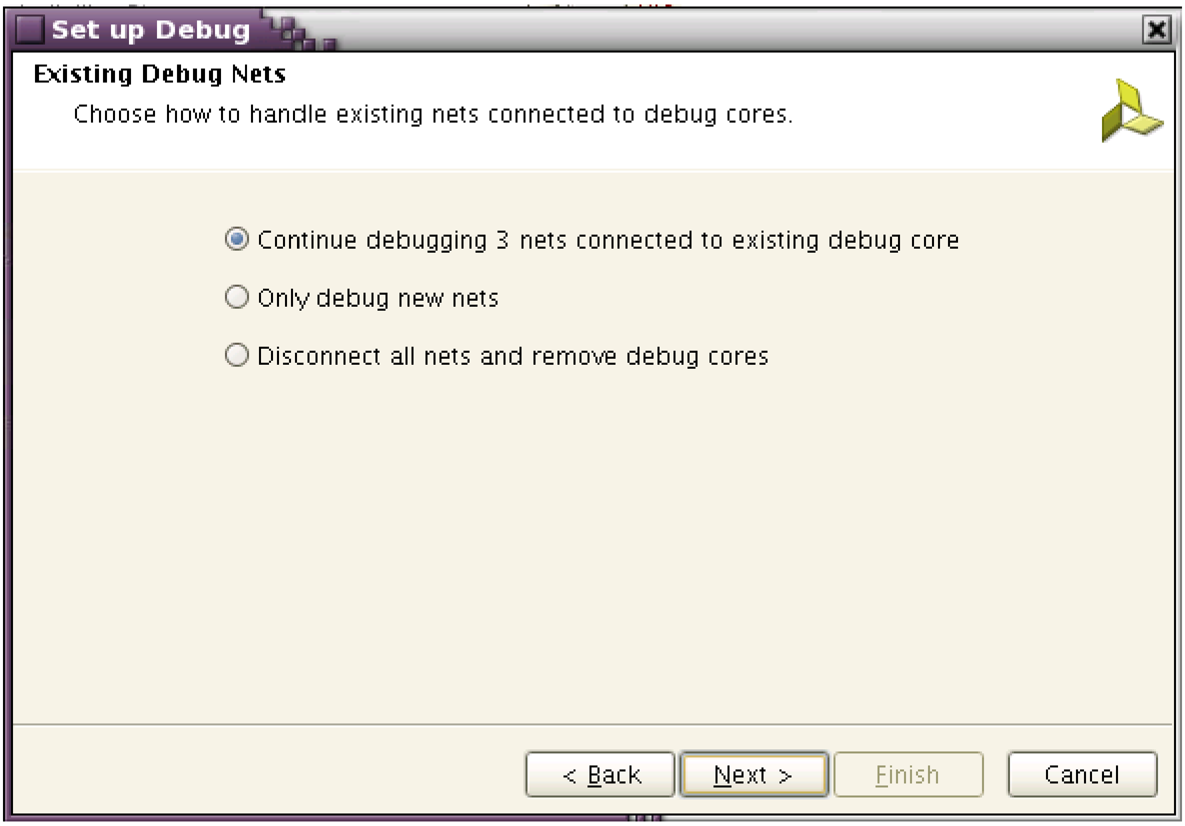


Default Layout
Synthesis and Implement
n - xc7k325tffg900-2 (active)
ools_ilalib_v2)
1)
oug Nets (9)
mber (8)
_8_0_i/inst/n_1_inst/user_lnk_up_int_reg
Netlist
Debug
umber
iatic
xilinx_pcie_2_1_ep_7x_1_lane_gen1_xc7k325t-ffg900-2_KC705_REV

:onstrs_1/imports/example_design/xilinx_pcie_2_1_ep_7x_1_lane_gen1_xc7k32

```


##############################################################################
# End
##############################################################################

set_property MARK_DEBUG true [get_nets pcie_7x_v1_8_0_i/inst/re
set_property MARK_DEBUG true [get_nets pcie_7x_v1_8_0_i/inst/us

set_property MARK_DEBUG true [get_nets {cfg_bus_number[0]}]
set_property MARK_DEBUG true [get_nets {cfg_bus_number[1]}]
set_property MARK_DEBUG true [get_nets {cfg_bus_number[2]}]
set_property MARK_DEBUG true [get_nets {cfg_bus_number[3]}]
set_property MARK_DEBUG true [get_nets {cfg_bus_number[4]}]
set_property MARK_DEBUG true [get_nets {cfg_bus_number[5]}]
set_property MARK_DEBUG true [get_nets {cfg_bus_number[6]}]
set_property MARK_DEBUG true [get_nets {cfg_bus_number[7]}]

```

Figure 57 – MARK_DEBUG constraints in the XDC file for cfg_bus_number


Set up Debug
Existing Debug Nets
Choose how to handle existing nets connected to debug cores.

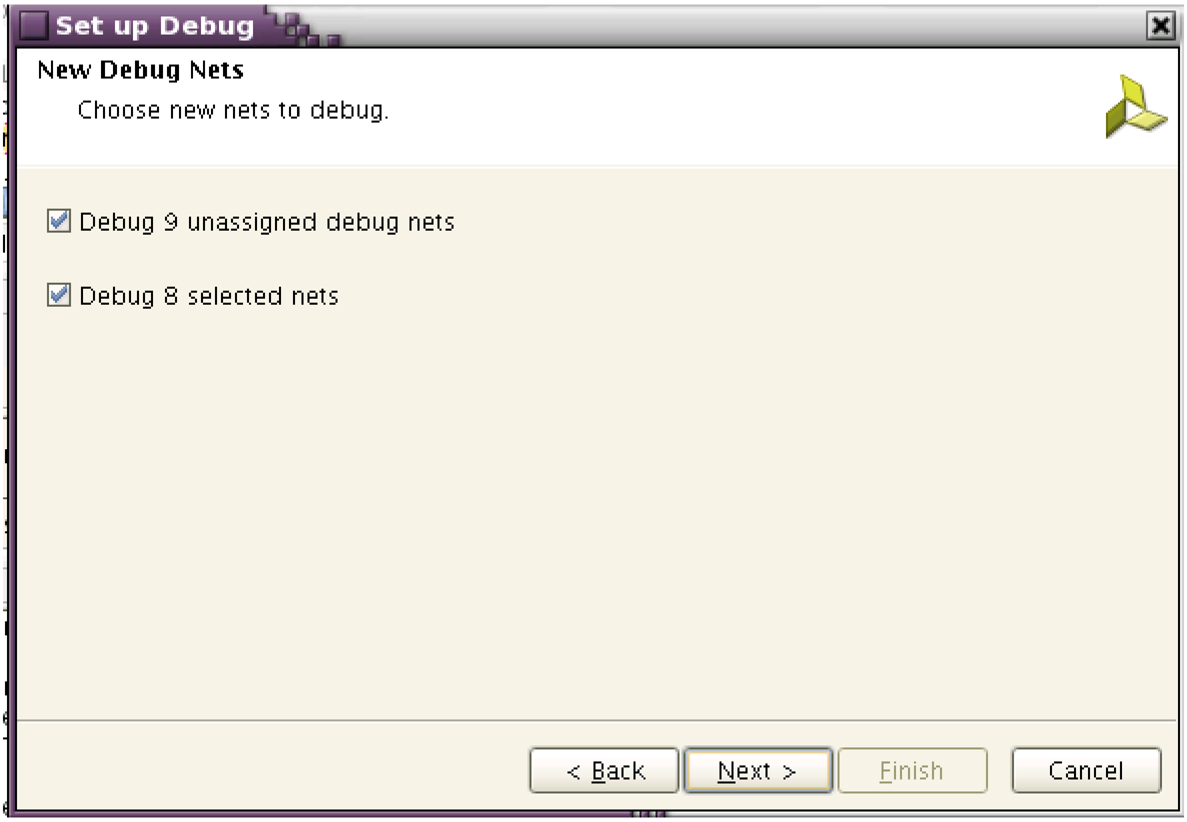
● Continue debugging 3 nets connected to existing debug core

○ Only debug new nets

○ Disconnect all nets and remove debug cores

< Back
Next >
Finish
Cancel

Figure 58 – Setup Debug Options for the added signals



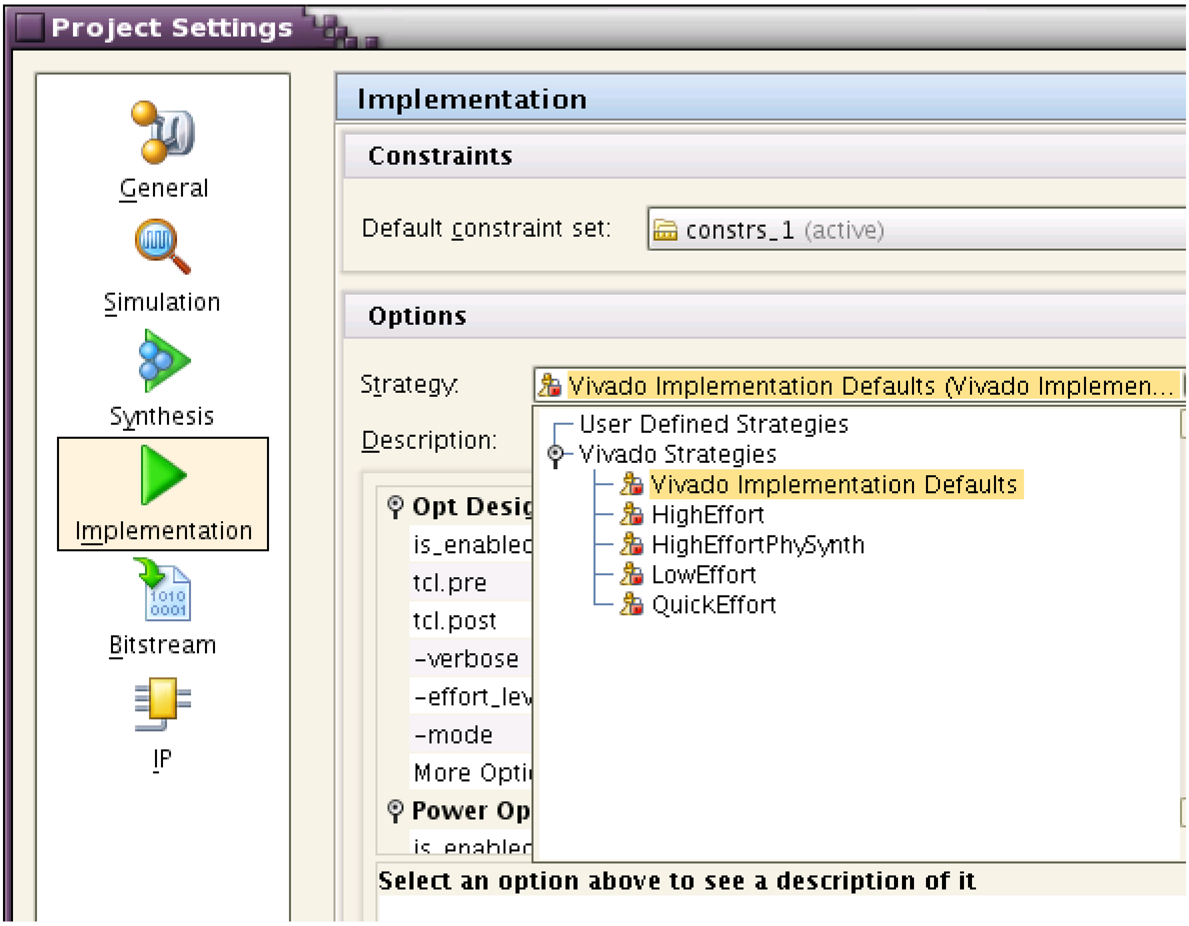
☑ Debug 9 unassigned debug nets

☑ Debug 8 selected nets

Figure 59 - Setup Debug Options for New Nets

Vivado Design Implementation Strategies

Vivado provides different implementation strategies as shown in Figure 60. A user could try by playing with these implementation strategies if the timing is not met. If the timing is still not met after trying out all the implementation strategies shown, the user might need to implement the design by altering different implementation options.



Implementation

Constraints

Default constraint set: constrs_1 (active)

Options

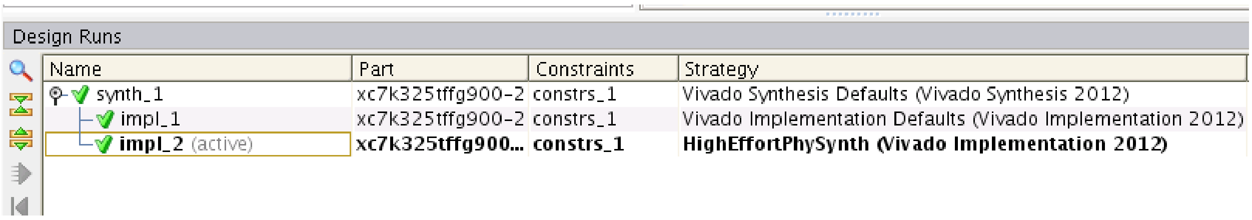
Strategy: Vivado Implementation Defaults (Vivado Implemen...

Description:

Select an option above to see a description of it

Figure 60 – Vivado Implementation Strategies

The 'Design Runs' window shows the result for different implementation strategies as shown in Figure 61.

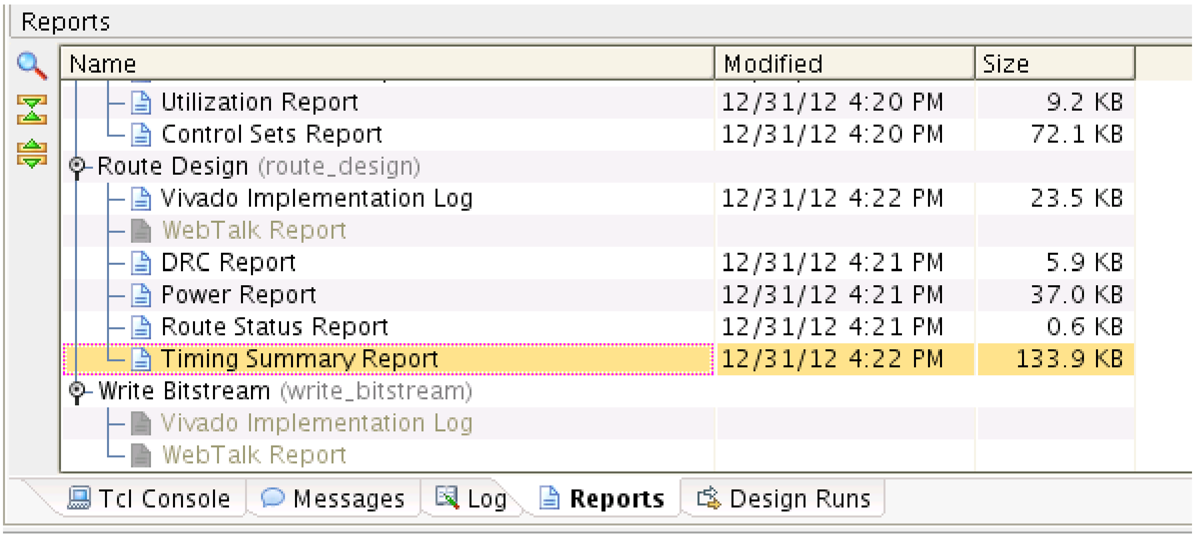

Design Runs

Name	Part	Constraints	Strategy
synth_1	xc7k325tffg900-2	constrs_1	Vivado Synthesis Defaults (Vivado Synthesis 2012)
impl_1	xc7k325tffg900-2	constrs_1	Vivado Implementation Defaults (Vivado Implementation 2012)
impl_2 (active)	**xc7k325tffg900...**	**constrs_1**	**HighEffortPhySynth (Vivado Implementation 2012)**

Figure 61 – PCIe Example Design Implementation with different Strategies

PCIe Example Design with Debug Cores - Timing Analysis

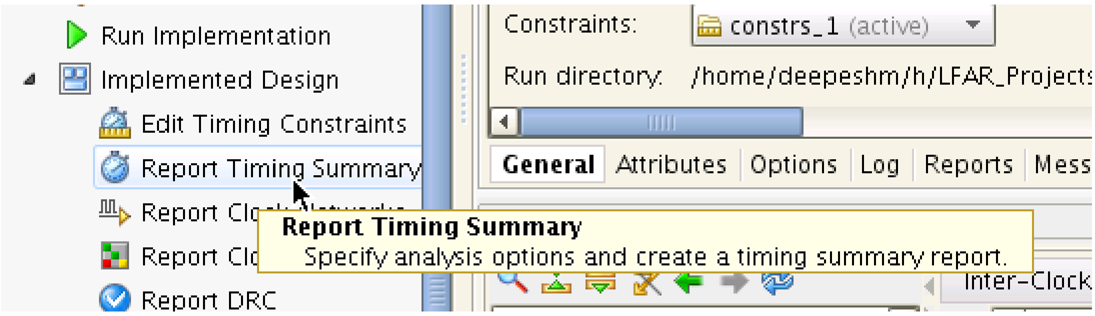
This section illustrates techniques and tools for timing analysis in Vivado for the PCIe example design with the debug cores. In this specific test example, there is a hold time violation in one of the paths. The screenshots provided show how to dig in detail information on that particular path.



Reports

Name	Modified	Size
Utilization Report	12/31/12 4:20 PM	9.2 KB
Control Sets Report	12/31/12 4:20 PM	72.1 KB
Route Design (route_design)		
Vivado Implementation Log	12/31/12 4:22 PM	23.5 KB
WebTalk Report		
DRC Report	12/31/12 4:21 PM	5.9 KB
Power Report	12/31/12 4:21 PM	37.0 KB
Route Status Report	12/31/12 4:21 PM	0.6 KB
Timing Summary Report	12/31/12 4:22 PM	133.9 KB
Write Bitstream (write_bitstream)		
Vivado Implementation Log		
WebTalk Report		

Figure 62 - Reports Tab

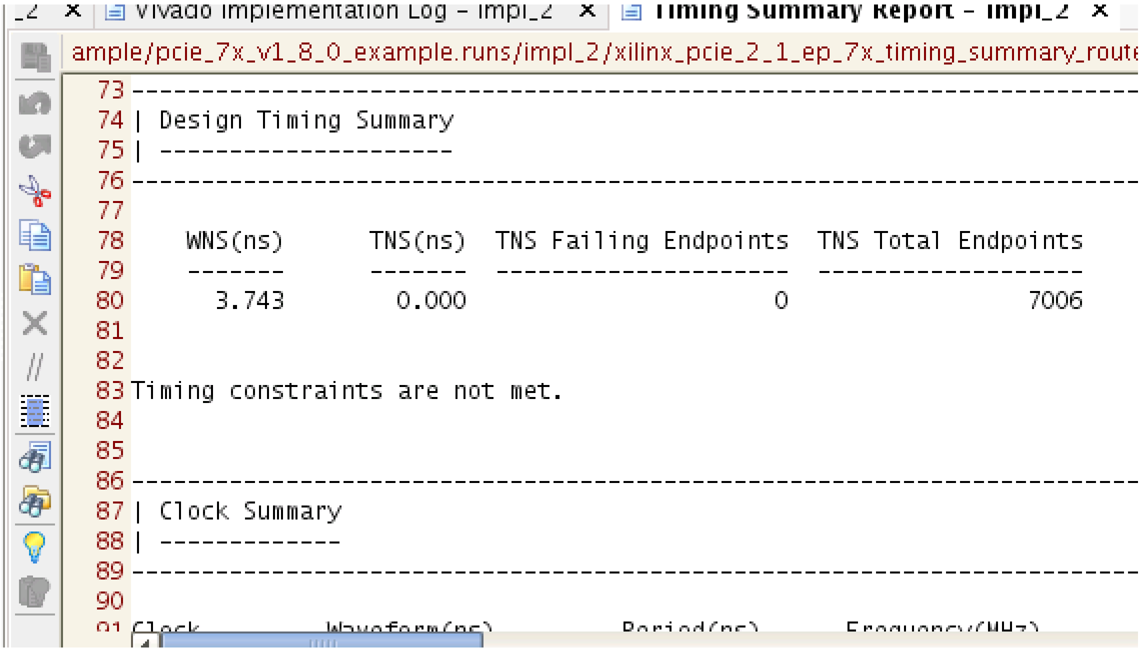


Constraints: constrs_1 (active)

Run directory: /home/deepeshm/h/LFAR_Projects

Report Timing Summary
Specify analysis options and create a timing summary report.

Figure 63 - Invoking Timing Summary Report after Implementation

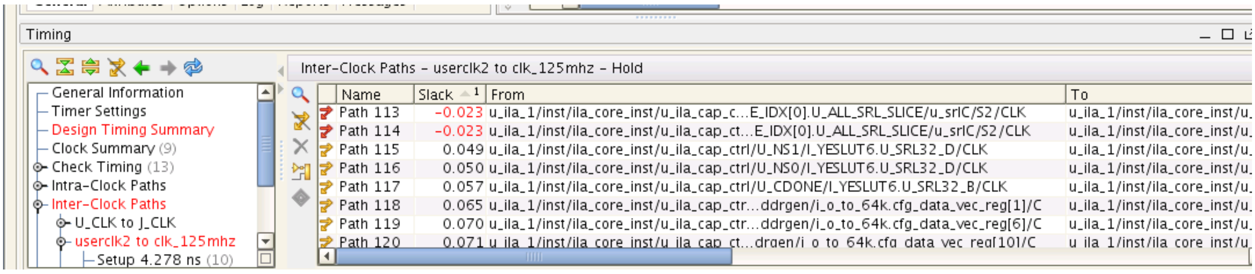


Vivado Implementation Log - impl_2
Timing Summary Report - impl_2

ample/pcie_7x_v1_8_0_example.runs/impl_2/xilinx_pcie_2_1_ep_7x_timing_summary_route

```
------------------------------------------------------------------------------
| Design Timing Summary
| ---------------------
------------------------------------------------------------------------------

    WNS(ns)      TNS(ns)  TNS Failing Endpoints  TNS Total Endpoints
    -------      -------  ---------------------  -------------------
      3.743        0.000                      0                 7006


Timing constraints are not met.


------------------------------------------------------------------------------
| Clock Summary
| -------------
------------------------------------------------------------------------------

Clock              Waveform(ns)          Period(ns)        Frequency(MHz)
```

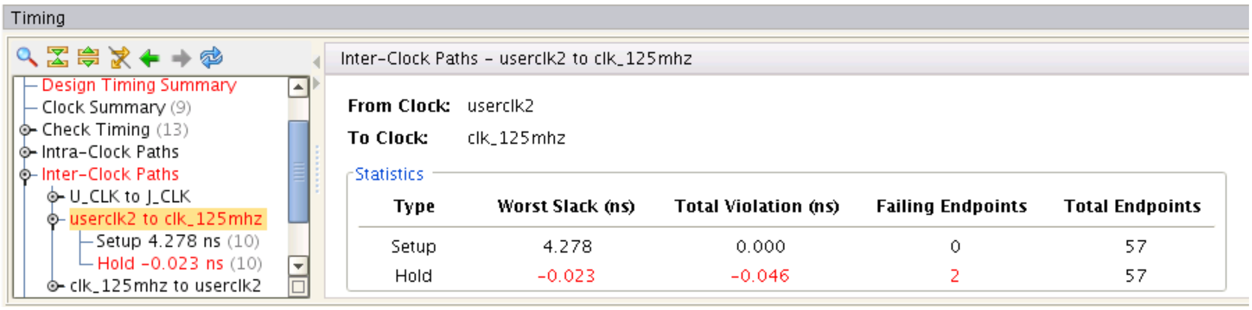
Figure 64 – Timing Summary Report



Inter-Clock Paths – userclk2 to clk_125mhz – Hold

Name	Slack	From	To
Path 113	-0.023	u_ila_1/inst/ila_core_inst/u_ila_cap_c...E_IDX[0].U_ALL_SRL_SLICE/u_srlC/S2/CLK	u_ila_1/inst/ila_core_inst/u_
Path 114	-0.023	u_ila_1/inst/ila_core_inst/u_ila_cap_ct...E_IDX[0].U_ALL_SRL_SLICE/u_srlC/S2/CLK	u_ila_1/inst/ila_core_inst/u_
Path 115	0.049	u_ila_1/inst/ila_core_inst/u_ila_cap_ctrl/U_NS1/I_YESLUT6.U_SRL32_D/CLK	u_ila_1/inst/ila_core_inst/u_
Path 116	0.050	u_ila_1/inst/ila_core_inst/u_ila_cap_ctrl/U_NS0/I_YESLUT6.U_SRL32_D/CLK	u_ila_1/inst/ila_core_inst/u_
Path 117	0.057	u_ila_1/inst/ila_core_inst/u_ila_cap_ctrl/U_CDONE/I_YESLUT6.U_SRL32_B/CLK	u_ila_1/inst/ila_core_inst/u_
Path 118	0.065	u_ila_1/inst/ila_core_inst/u_ila_cap_ctr...ddrgen/i_o_to_64k.cfg_data_vec_reg[1]/C	u_ila_1/inst/ila_core_inst/u_
Path 119	0.070	u_ila_1/inst/ila_core_inst/u_ila_cap_ctr...ddrgen/i_o_to_64k.cfg_data_vec_reg[6]/C	u_ila_1/inst/ila_core_inst/u_
Path 120	0.071	u_ila_1/inst/ila_core_inst/u_ila_cap_ct...drgen/i_o_to_64k.cfg_data_vec_reg[10]/C	u_ila_1/inst/ila_core_inst/u_

Figure 65 - Timing Error Example



Inter-Clock Paths – userclk2 to clk_125mhz

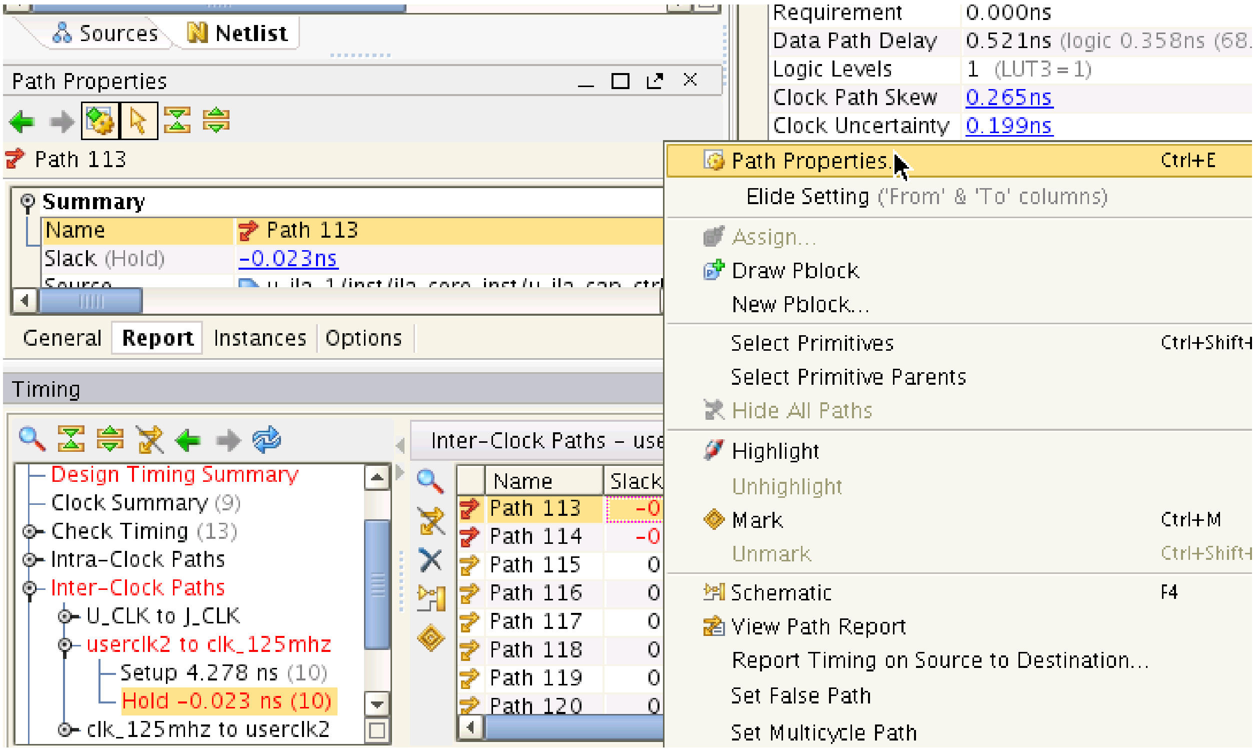
From Clock: userclk2

To Clock: clk_125mhz

Statistics

Type	Worst Slack (ns)	Total Violation (ns)	Failing Endpoints	Total Endpoints
Setup	4.278	0.000	0	57
Hold	-0.023	-0.046	2	57

Figure 66 – Timing Error Quick Summary

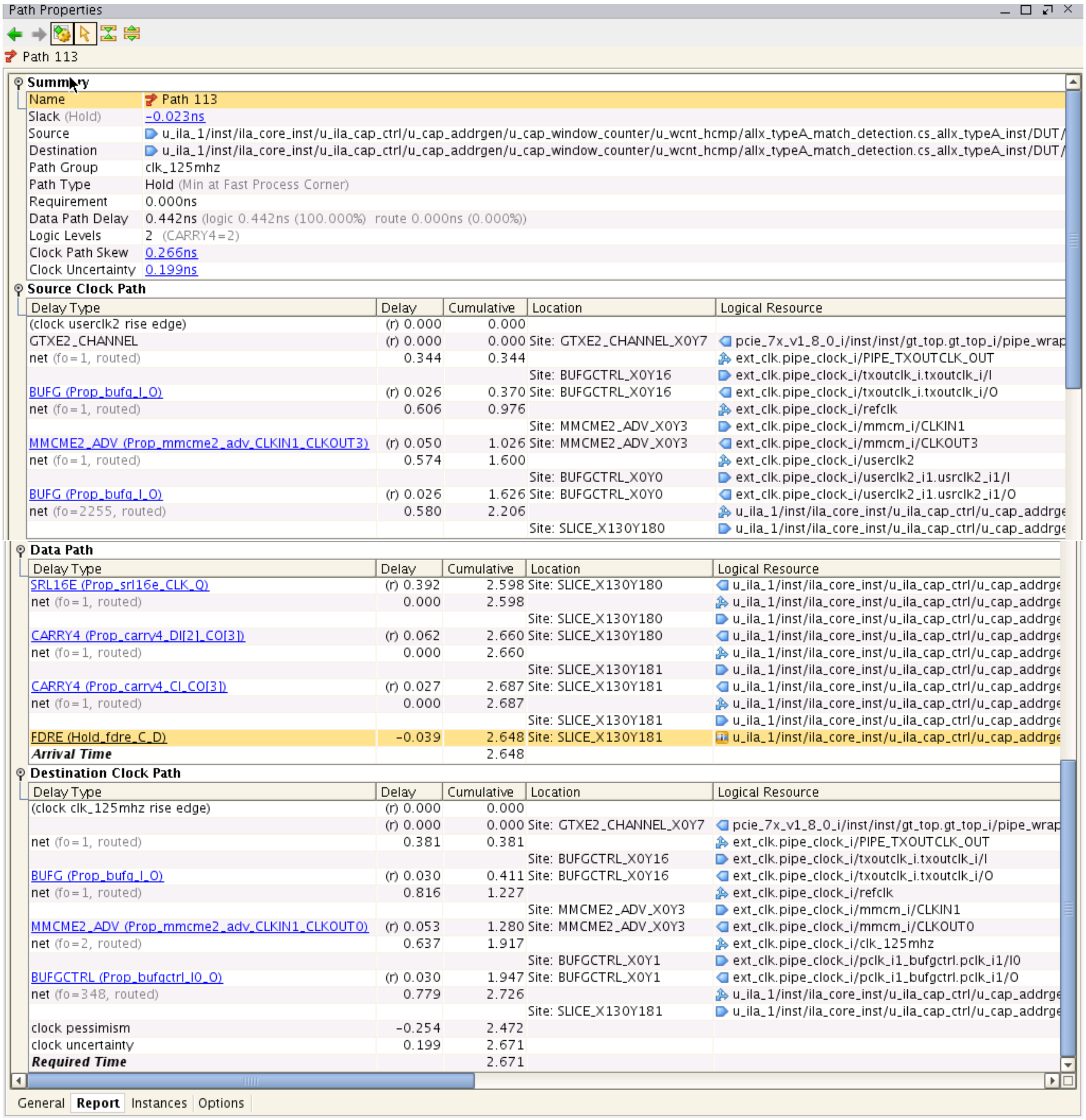


Name	Path 113
Slack (Hold)	-0.023ns
Source	u_ila_1/inst/ila_core_inst/u_ila_cap_ctrl

Requirement	0.000ns
Data Path Delay	0.521ns (logic 0.358ns (68.
Logic Levels	1 (LUT3=1)
Clock Path Skew	0.265ns
Clock Uncertainty	0.199ns

Name	Slack
Path 113	-0
Path 114	-0
Path 115	0
Path 116	0
Path 117	0
Path 118	0
Path 119	0
Path 120	0

Figure 67 – Path Properties for the Failing Path



Path 113

Summary

Name	Path 113
Slack (Hold)	-0.023ns
Source	u_ila_1/inst/ila_core_inst/u_ila_cap_ctrl/u_cap_addrgen/u_cap_window_counter/u_wcnt_hcmp/allx_typeA_match_detection.cs_allx_typeA_inst/DUT/
Destination	u_ila_1/inst/ila_core_inst/u_ila_cap_ctrl/u_cap_addrgen/u_cap_window_counter/u_wcnt_hcmp/allx_typeA_match_detection.cs_allx_typeA_inst/DUT/
Path Group	clk_125mhz
Path Type	Hold (Min at Fast Process Corner)
Requirement	0.000ns
Data Path Delay	0.442ns (logic 0.442ns (100.000%) route 0.000ns (0.000%))
Logic Levels	2 (CARRY4=2)
Clock Path Skew	0.266ns
Clock Uncertainty	0.199ns

Source Clock Path

Delay Type	Delay	Cumulative	Location	Logical Resource
(clock userclk2 rise edge)	(r) 0.000	0.000		
GTXE2_CHANNEL	(r) 0.000	0.000	Site: GTXE2_CHANNEL_X0Y7	pcie_7x_v1_8_0_i/inst/inst/gt_top.gt_top_i/pipe_wrap
net (fo=1, routed)	0.344	0.344		ext_clk.pipe_clock_i/PIPE_TXOUTCLK_OUT
			Site: BUFGCTRL_X0Y16	ext_clk.pipe_clock_i/txoutclk_i.txoutclk_i/I
BUFG (Prop_bufg_I_O)	(r) 0.026	0.370	Site: BUFGCTRL_X0Y16	ext_clk.pipe_clock_i/txoutclk_i.txoutclk_i/O
net (fo=1, routed)	0.606	0.976		ext_clk.pipe_clock_i/refclk
			Site: MMCME2_ADV_X0Y3	ext_clk.pipe_clock_i/mmcm_i/CLKIN1
MMCME2_ADV (Prop_mmcme2_adv_CLKIN1_CLKOUT3)	(r) 0.050	1.026	Site: MMCME2_ADV_X0Y3	ext_clk.pipe_clock_i/mmcm_i/CLKOUT3
net (fo=1, routed)	0.574	1.600		ext_clk.pipe_clock_i/userclk2
			Site: BUFGCTRL_X0Y0	ext_clk.pipe_clock_i/userclk2_i1.usrclk2_i1/I
BUFG (Prop_bufg_I_O)	(r) 0.026	1.626	Site: BUFGCTRL_X0Y0	ext_clk.pipe_clock_i/userclk2_i1.usrclk2_i1/O
net (fo=2255, routed)	0.580	2.206		u_ila_1/inst/ila_core_inst/u_ila_cap_ctrl/u_cap_addrge
			Site: SLICE_X130Y180	u_ila_1/inst/ila_core_inst/u_ila_cap_ctrl/u_cap_addrge

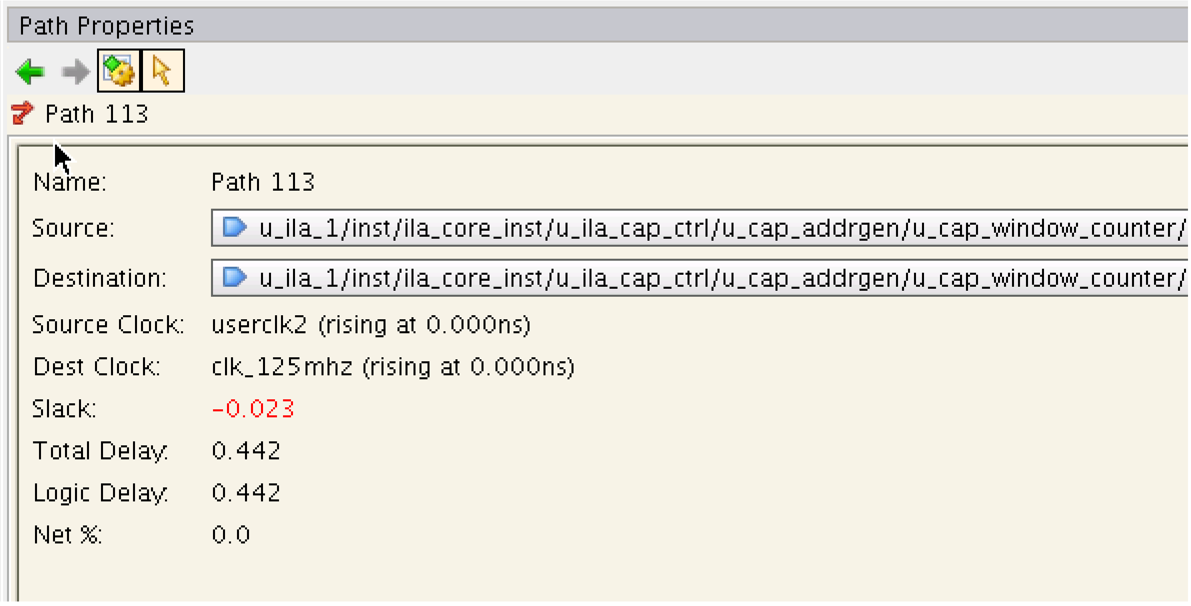
Data Path

Delay Type	Delay	Cumulative	Location	Logical Resource
SRL16E (Prop_srl16e_CLK_Q)	(r) 0.392	2.598	Site: SLICE_X130Y180	u_ila_1/inst/ila_core_inst/u_ila_cap_ctrl/u_cap_addrge
net (fo=1, routed)	0.000	2.598		u_ila_1/inst/ila_core_inst/u_ila_cap_ctrl/u_cap_addrge
			Site: SLICE_X130Y180	u_ila_1/inst/ila_core_inst/u_ila_cap_ctrl/u_cap_addrge
CARRY4 (Prop_carry4_DI[2]_CO[3])	(r) 0.062	2.660	Site: SLICE_X130Y180	u_ila_1/inst/ila_core_inst/u_ila_cap_ctrl/u_cap_addrge
net (fo=1, routed)	0.000	2.660		u_ila_1/inst/ila_core_inst/u_ila_cap_ctrl/u_cap_addrge
			Site: SLICE_X130Y181	u_ila_1/inst/ila_core_inst/u_ila_cap_ctrl/u_cap_addrge
CARRY4 (Prop_carry4_CI_CO[3])	(r) 0.027	2.687	Site: SLICE_X130Y181	u_ila_1/inst/ila_core_inst/u_ila_cap_ctrl/u_cap_addrge
net (fo=1, routed)	0.000	2.687		u_ila_1/inst/ila_core_inst/u_ila_cap_ctrl/u_cap_addrge
			Site: SLICE_X130Y181	u_ila_1/inst/ila_core_inst/u_ila_cap_ctrl/u_cap_addrge
FDRE (Hold_fdre_C_D)	-0.039	2.648	Site: SLICE_X130Y181	u_ila_1/inst/ila_core_inst/u_ila_cap_ctrl/u_cap_addrge
Arrival Time		2.648		

Destination Clock Path

Delay Type	Delay	Cumulative	Location	Logical Resource
(clock clk_125mhz rise edge)	(r) 0.000	0.000		
	(r) 0.000	0.000	Site: GTXE2_CHANNEL_X0Y7	pcie_7x_v1_8_0_i/inst/inst/gt_top.gt_top_i/pipe_wrap
net (fo=1, routed)	0.381	0.381		ext_clk.pipe_clock_i/PIPE_TXOUTCLK_OUT
			Site: BUFGCTRL_X0Y16	ext_clk.pipe_clock_i/txoutclk_i.txoutclk_i/I
BUFG (Prop_bufg_I_O)	(r) 0.030	0.411	Site: BUFGCTRL_X0Y16	ext_clk.pipe_clock_i/txoutclk_i.txoutclk_i/O
net (fo=1, routed)	0.816	1.227		ext_clk.pipe_clock_i/refclk
			Site: MMCME2_ADV_X0Y3	ext_clk.pipe_clock_i/mmcm_i/CLKIN1
MMCME2_ADV (Prop_mmcme2_adv_CLKIN1_CLKOUT0)	(r) 0.053	1.280	Site: MMCME2_ADV_X0Y3	ext_clk.pipe_clock_i/mmcm_i/CLKOUT0
net (fo=2, routed)	0.637	1.917		ext_clk.pipe_clock_i/clk_125mhz
			Site: BUFGCTRL_X0Y1	ext_clk.pipe_clock_i/pclk_i1_bufgctrl.pclk_i1/I0
BUFGCTRL (Prop_bufgctrl_I0_O)	(r) 0.030	1.947	Site: BUFGCTRL_X0Y1	ext_clk.pipe_clock_i/pclk_i1_bufgctrl.pclk_i1/O
net (fo=348, routed)	0.779	2.726		u_ila_1/inst/ila_core_inst/u_ila_cap_ctrl/u_cap_addrge
			Site: SLICE_X130Y181	u_ila_1/inst/ila_core_inst/u_ila_cap_ctrl/u_cap_addrge
clock pessimism	-0.254	2.472		
clock uncertainty	0.199	2.671		
Required Time		2.671		

Figure 68 – Detailed Timing Report for the Failing Path



Name: Path 113

Source: u_ila_1/inst/ila_core_inst/u_ila_cap_ctrl/u_cap_addrgen/u_cap_window_counter/

Destination: u_ila_1/inst/ila_core_inst/u_ila_cap_ctrl/u_cap_addrgen/u_cap_window_counter/

Source Clock: userclk2 (rising at 0.000ns)

Dest Clock: clk_125mhz (rising at 0.000ns)

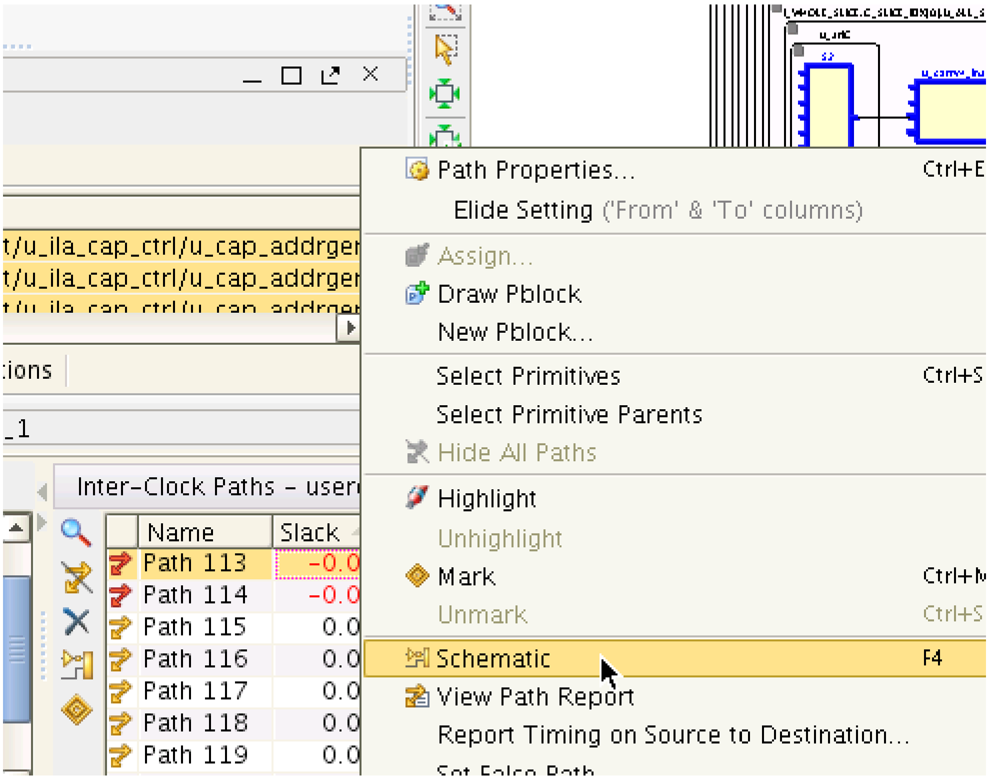
Slack: -0.023

Total Delay: 0.442

Logic Delay: 0.442

Net %: 0.0

Figure 69 - Timing Summary for the Failing Path



Name	Slack
Path 113	-0.0
Path 114	-0.0
Path 115	0.0
Path 116	0.0
Path 117	0.0
Path 118	0.0
Path 119	0.0

Figure 70 - Schematic Generation for the Failing Path

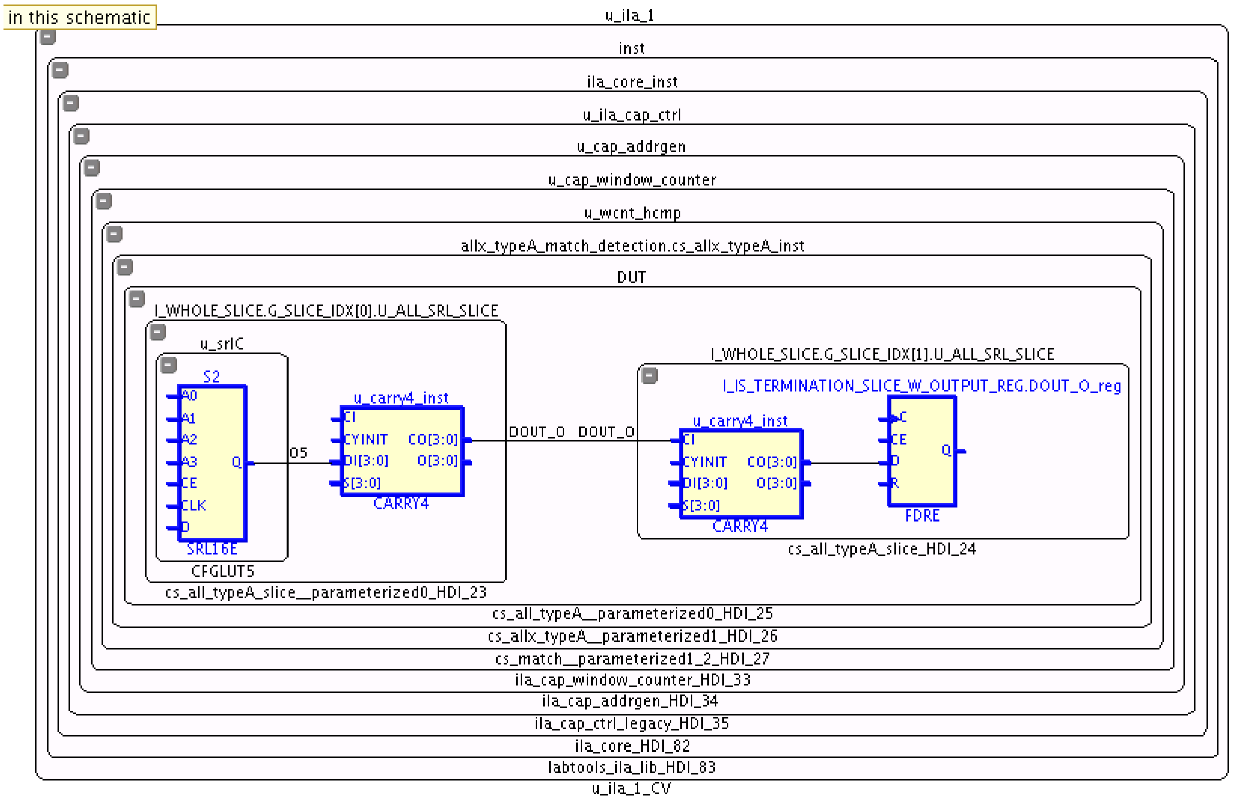
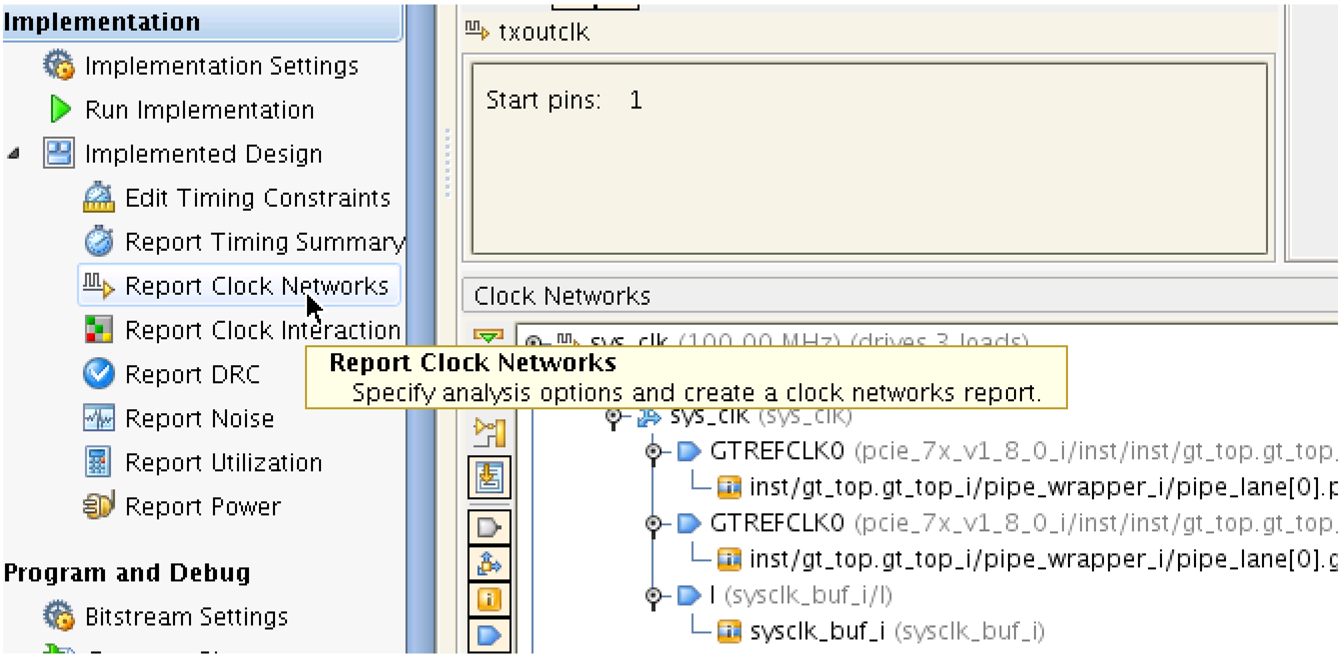

in this schematic
u_ila_1
inst
ila_core_inst
u_ila_cap_ctrl
u_cap_addrgen
u_cap_window_counter
u_wcnt_hcmp
allx_typeA_match_detection.cs_allx_typeA_inst
DUT
I_WHOLE_SLICE.G_SLICE_IDX[0].U_ALL_SRL_SLICE
u_srlC
S2
A0
A1
A2
A3
CE
CLK
D
Q
SRL16E
CFGLUT5
O5
u_carry4_inst
CI
CYINIT
DI[3:0]
S[3:0]
CO[3:0]
O[3:0]
CARRY4
DOUT_O
DOUT_O
I_WHOLE_SLICE.G_SLICE_IDX[1].U_ALL_SRL_SLICE
I_IS_TERMINATION_SLICE_W_OUTPUT_REG.DOUT_O_reg
C
CE
D
R
Q
FDRE
cs_all_typeA_slice_HDL_24
cs_all_typeA_slice__parameterized0_HDL_23
cs_all_typeA__parameterized0_HDL_25
cs_allx_typeA__parameterized1_HDL_26
cs_match__parameterized1_2_HDL_27
ila_cap_window_counter_HDL_33
ila_cap_addrgen_HDL_34
ila_cap_ctrl_legacy_HDL_35
ila_core_HDL_82
labtools_ila_lib_HDL_83
u_ila_1_CV

Figure 71 - Failing Path Schematic

PCI Example Design Clock Network Analysis

This section provides features in Vivado that could be used for PCIe example design clock network analysis. The screenshots provided show the clock networks in the design, list of clock nets and the clocking resources usage such as BUFG, BUFR etc.



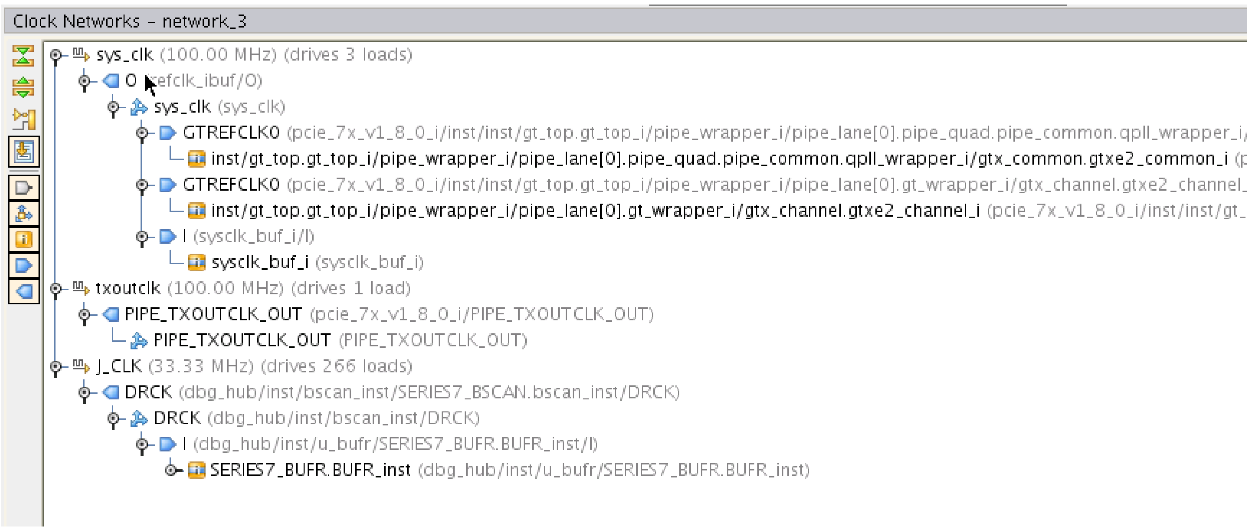
Start pins: 1

sys_clk (100.00 MHz) (drives 3 loads)

Report Clock Networks
Specify analysis options and create a clock networks report.

sys_clk (sys_clk)
GTREFCLK0 (pcie_7x_v1_8_0_i/inst/inst/gt_top.gt_top.
inst/gt_top.gt_top_i/pipe_wrapper_i/pipe_lane[0].p
GTREFCLK0 (pcie_7x_v1_8_0_i/inst/inst/gt_top.gt_top.
inst/gt_top.gt_top_i/pipe_wrapper_i/pipe_lane[0].g
I (sysclk_buf_i/I)
sysclk_buf_i (sysclk_buf_i)

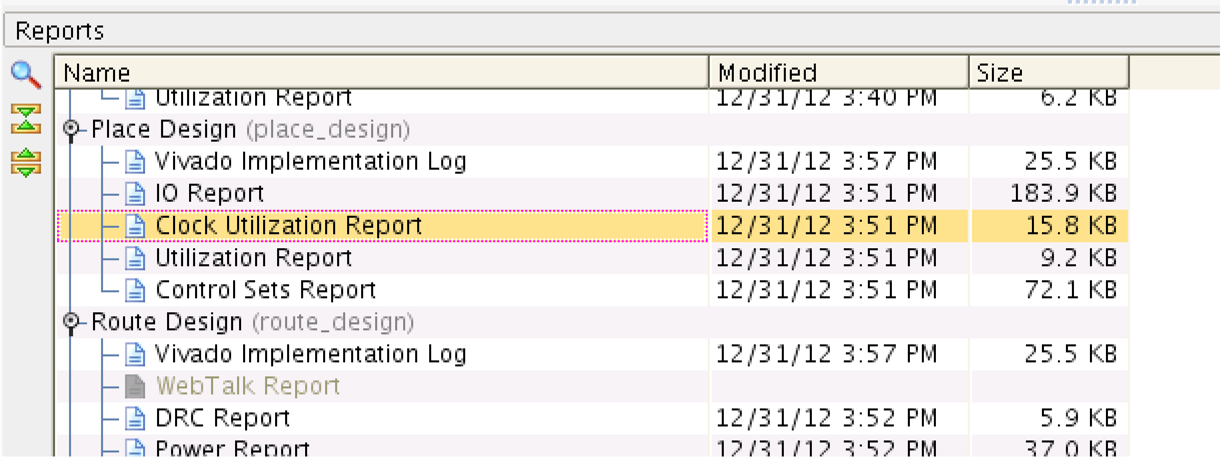
Figure 72 – Creating Clock Networks Report



Clock Networks – network_3

```
sys_clk (100.00 MHz) (drives 3 loads)
  O refclk_ibuf/O)
    sys_clk (sys_clk)
      GTREFCLK0 (pcie_7x_v1_8_0_i/inst/inst/gt_top.gt_top_i/pipe_wrapper_i/pipe_lane[0].pipe_quad.pipe_common.qpll_wrapper_i/
        inst/gt_top.gt_top_i/pipe_wrapper_i/pipe_lane[0].pipe_quad.pipe_common.qpll_wrapper_i/gtx_common.gtxe2_common_i (p
      GTREFCLK0 (pcie_7x_v1_8_0_i/inst/inst/gt_top.gt_top_i/pipe_wrapper_i/pipe_lane[0].gt_wrapper_i/gtx_channel.gtxe2_channel_
        inst/gt_top.gt_top_i/pipe_wrapper_i/pipe_lane[0].gt_wrapper_i/gtx_channel.gtxe2_channel_i (pcie_7x_v1_8_0_i/inst/inst/gt_
      I (sysclk_buf_i/I)
        sysclk_buf_i (sysclk_buf_i)
txoutclk (100.00 MHz) (drives 1 load)
  PIPE_TXOUTCLK_OUT (pcie_7x_v1_8_0_i/PIPE_TXOUTCLK_OUT)
    PIPE_TXOUTCLK_OUT (PIPE_TXOUTCLK_OUT)
J_CLK (33.33 MHz) (drives 266 loads)
  DRCK (dbg_hub/inst/bscan_inst/SERIES7_BSCAN.bscan_inst/DRCK)
    DRCK (dbg_hub/inst/bscan_inst/DRCK)
      I (dbg_hub/inst/u_bufr/SERIES7_BUFR.BUFR_inst/I)
        SERIES7_BUFR.BUFR_inst (dbg_hub/inst/u_bufr/SERIES7_BUFR.BUFR_inst)
```

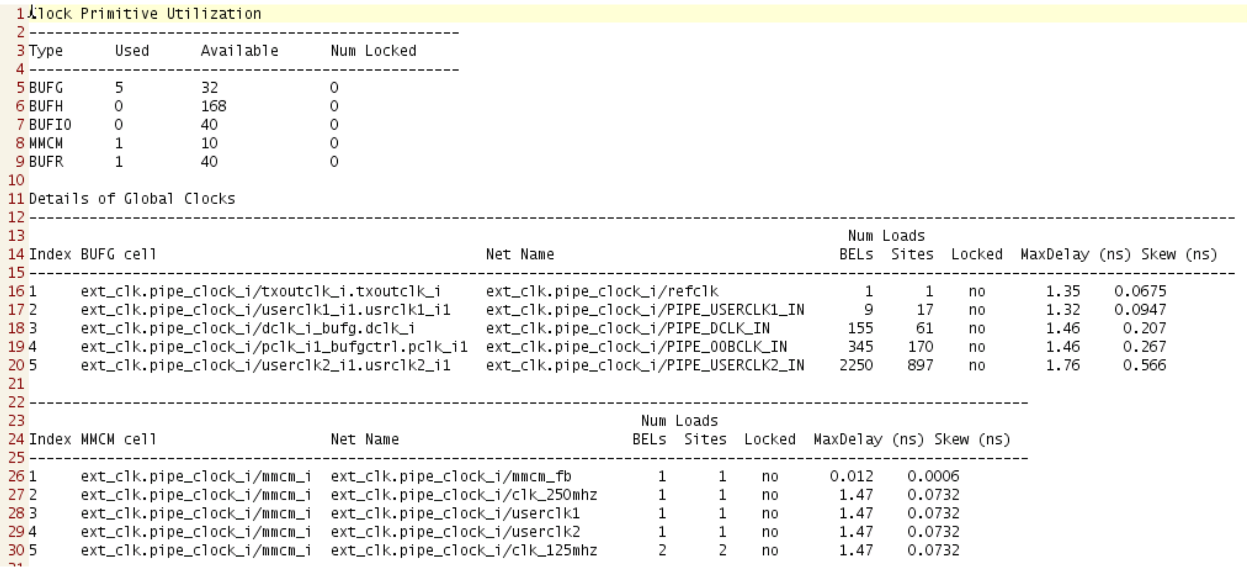
Figure 73 – Clock Networks in PCIe Example Design



Reports

Name	Modified	Size
Utilization Report	12/31/12 3:40 PM	6.2 KB
Place Design (place_design)		
Vivado Implementation Log	12/31/12 3:57 PM	25.5 KB
IO Report	12/31/12 3:51 PM	183.9 KB
Clock Utilization Report	12/31/12 3:51 PM	15.8 KB
Utilization Report	12/31/12 3:51 PM	9.2 KB
Control Sets Report	12/31/12 3:51 PM	72.1 KB
Route Design (route_design)		
Vivado Implementation Log	12/31/12 3:57 PM	25.5 KB
WebTalk Report		
DRC Report	12/31/12 3:52 PM	5.9 KB
Power Report	12/31/12 3:52 PM	37.0 KB

Figure 74 –Generate Clock PCIe Example Design Clock Utilization Report



```
Clock Primitive Utilization
--------------------------------------------------
Type      Used      Available      Num Locked
--------------------------------------------------
BUFG      5         32             0
BUFH      0         168            0
BUFIO     0         40             0
MMCM      1         10             0
BUFR      1         40             0

Details of Global Clocks
------------------------------------------------------------------------------------------------------------------------------
                                                                                         Num Loads
Index BUFG cell                                   Net Name                              BELs  Sites  Locked  MaxDelay (ns) Skew (ns)
------------------------------------------------------------------------------------------------------------------------------
1     ext_clk.pipe_clock_i/txoutclk_i.txoutclk_i    ext_clk.pipe_clock_i/refclk               1      1    no       1.35    0.0675
2     ext_clk.pipe_clock_i/userclk1_i1.usrclk1_i1   ext_clk.pipe_clock_i/PIPE_USERCLK1_IN     9     17    no       1.32    0.0947
3     ext_clk.pipe_clock_i/dclk_i_bufg.dclk_i       ext_clk.pipe_clock_i/PIPE_DCLK_IN       155     61    no       1.46     0.207
4     ext_clk.pipe_clock_i/pclk_i1_bufgctrl.pclk_i1 ext_clk.pipe_clock_i/PIPE_OOBCLK_IN     345    170    no       1.46     0.267
5     ext_clk.pipe_clock_i/userclk2_i1.usrclk2_i1   ext_clk.pipe_clock_i/PIPE_USERCLK2_IN  2250    897    no       1.76     0.566

------------------------------------------------------------------------------------------------------------
                                                                   Num Loads
Index MMCM cell                  Net Name                          BELs  Sites  Locked  MaxDelay (ns) Skew (ns)
------------------------------------------------------------------------------------------------------------
1     ext_clk.pipe_clock_i/mmcm_i  ext_clk.pipe_clock_i/mmcm_fb        1      1    no      0.012    0.0006
2     ext_clk.pipe_clock_i/mmcm_i  ext_clk.pipe_clock_i/clk_250mhz     1      1    no       1.47    0.0732
3     ext_clk.pipe_clock_i/mmcm_i  ext_clk.pipe_clock_i/userclk1       1      1    no       1.47    0.0732
4     ext_clk.pipe_clock_i/mmcm_i  ext_clk.pipe_clock_i/userclk2       1      1    no       1.47    0.0732
5     ext_clk.pipe_clock_i/mmcm_i  ext_clk.pipe_clock_i/clk_125mhz     2      2    no       1.47    0.0732
```

Figure 75 - PCIe Example Design Clock Resource Usage and Clock Nets

References

[1]. UG936, Vivado Design Suite Tutorial, Programming and Debugging
[2]. PG054, 7 Series Integrated PCI Express Block core
[3]. UG939, Vivado Design Suite Tutorial, Designing with IP
[4]. UG893, Vivado Design Suite User Guide, Using the Vivado IDE
[5]. UG900, Vivado Design Suite User Guide, Logic Simulation