How FPGAs Have Evolved to Address Compute Acceleration and Interconnects

Ken Chang

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Xilinx at OFC Booth #1811

Agenda

- Why FPGA, Adaptable Compute?
- FPGA to Adaptable Compute Evolution
- FPGA Transceiver Evolution
- Summary

Compute and Bandwidth Needs Across All Industries

CLOUD

NETWORK

EDGE

AI ADOPTION ACROSS MARKETS

EXPONENTIAL DATA BANDWIDTH GROWTH

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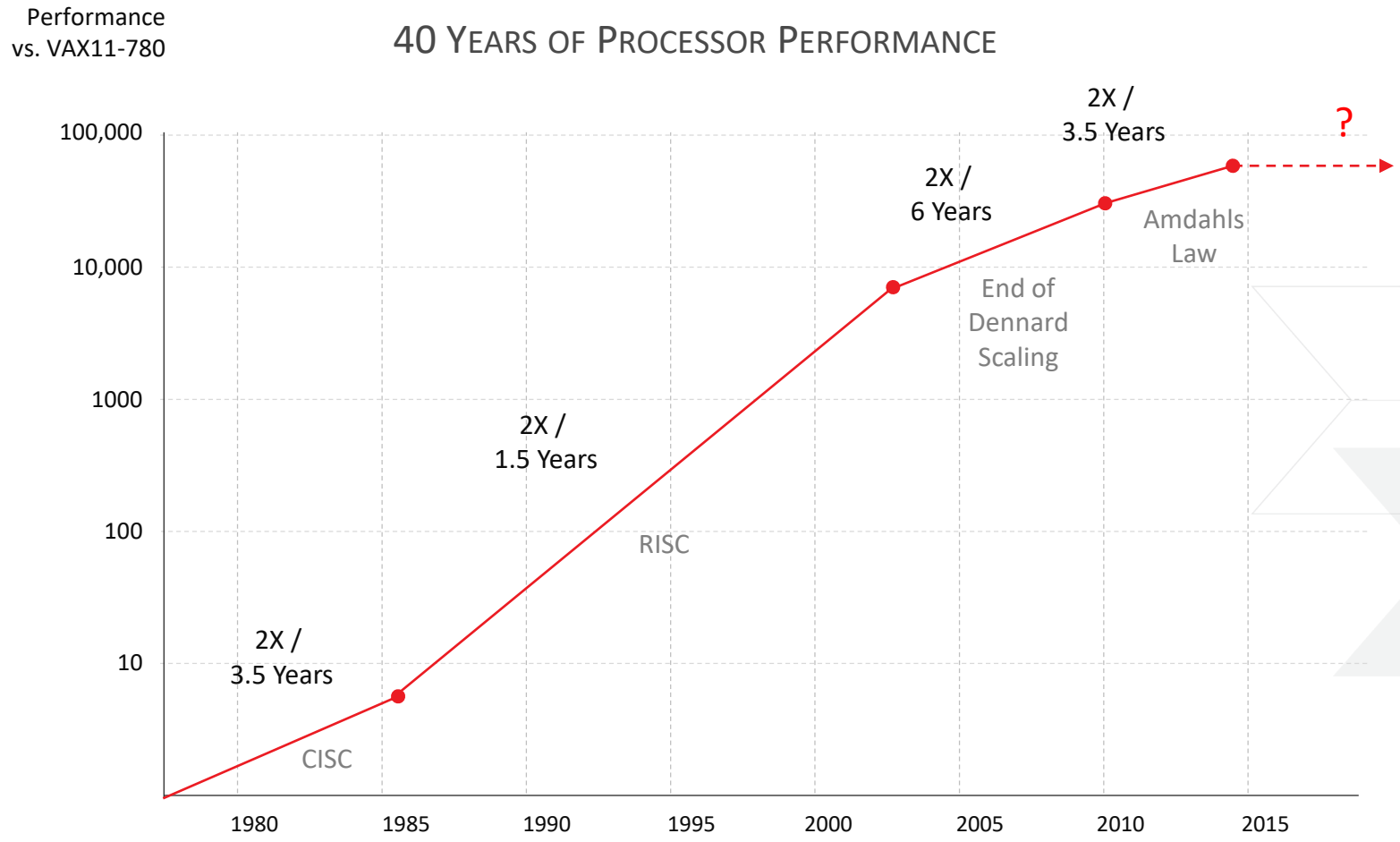
The Slowdown of Moore's Law and Technology Scaling

Processing Architectures are Not Scaling



Source: John Hennessy and David Patterson, Computer Architecture: A Quantitative Approach, 6/e 2018

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FPGA Evolution: From FPGA to SoC to ACAP

First FPGA Introduced

1985

First Virtex FPGA

1998

Virtex-2 Pro

2001

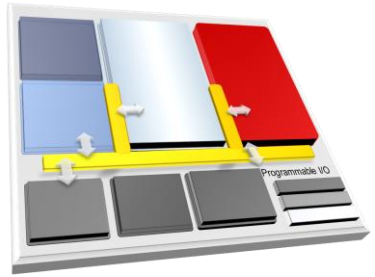
First 3D FPGA & HW/SW Programmable SoC

2011

First MPSoC & RFSoC

2016

ACAP



2019

Moore's Law Era | **SoC Era**

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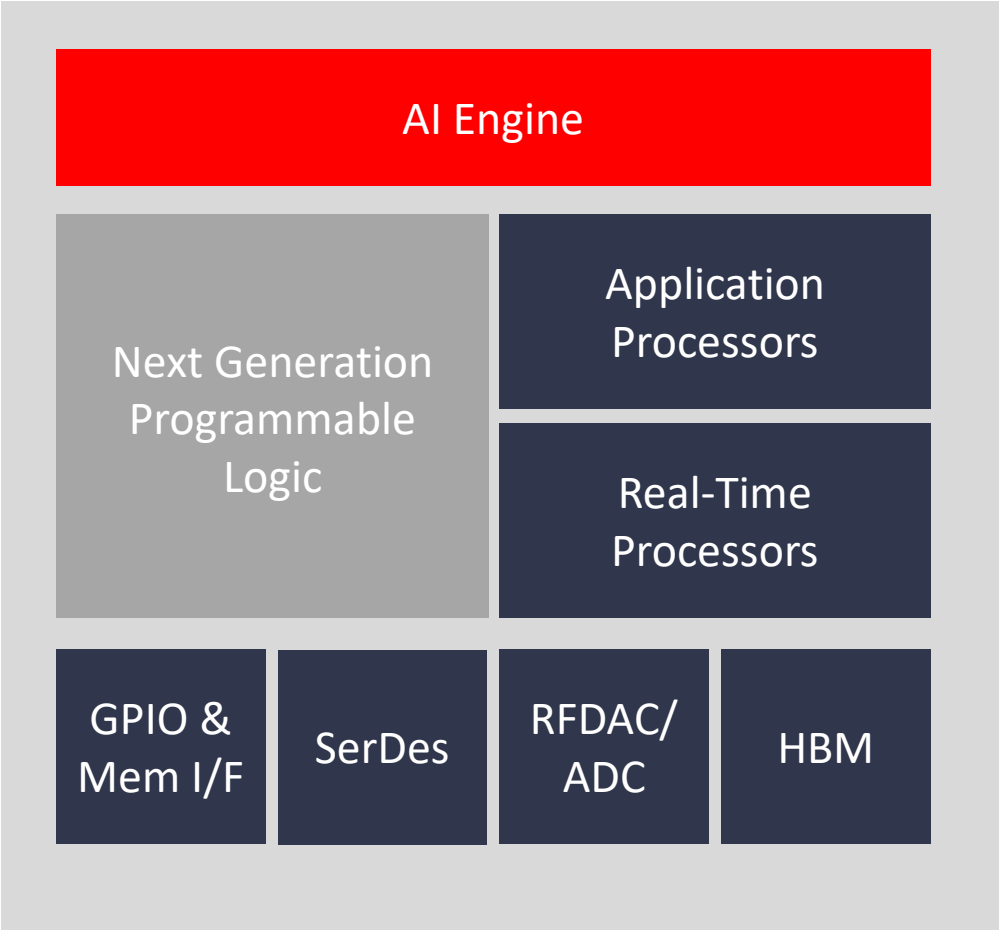
Adaptive Compute Acceleration Platform



- Based on 7nm FinFET
- Platform Solution for Compute / Storage / Network Acceleration
- IP Subsystems and a Network-on-Chip
- Programmable AI Engine

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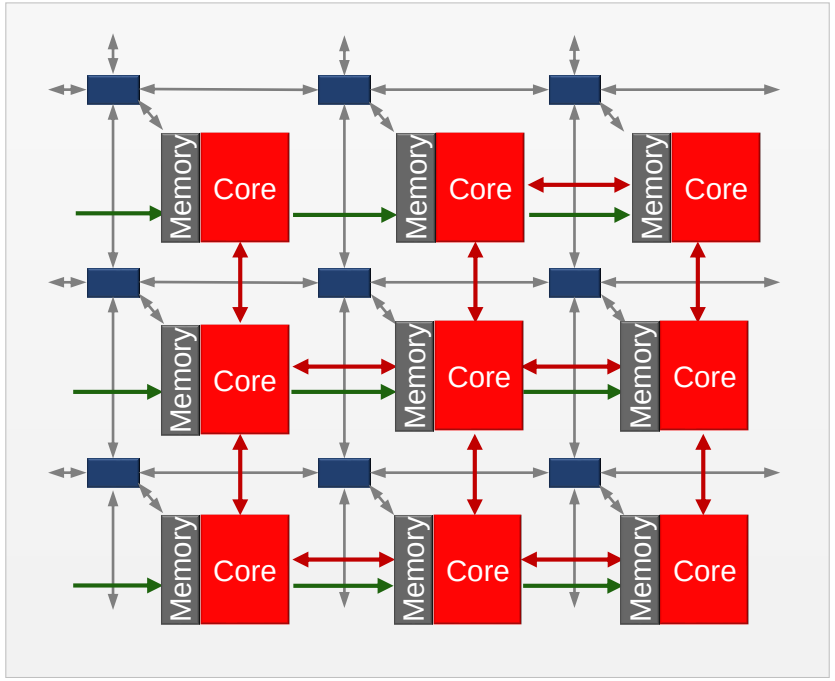
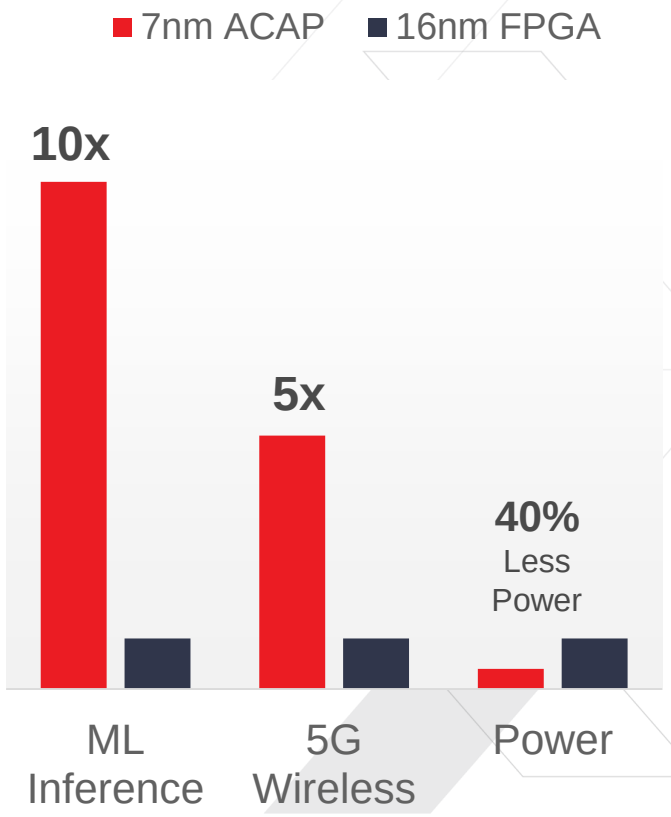
AI Engine

- Target Applications
  - ML Inference for Cloud DC
  - 5G wireless: Radio, Baseband
  - ADAS/AD Embedded Vision
- Each Tile:
  - ISA-based Vector Processor *(SW programmable, C++, e.g.)*
  - Local Memory
  - Adaptable, Non-blocking Interconnect

Array Architecture





Source: Juanjo Noguera, “HW/SW Programmable Engine: Increased Compute Density Architecture for Project Everest”, Hot Chips 2018

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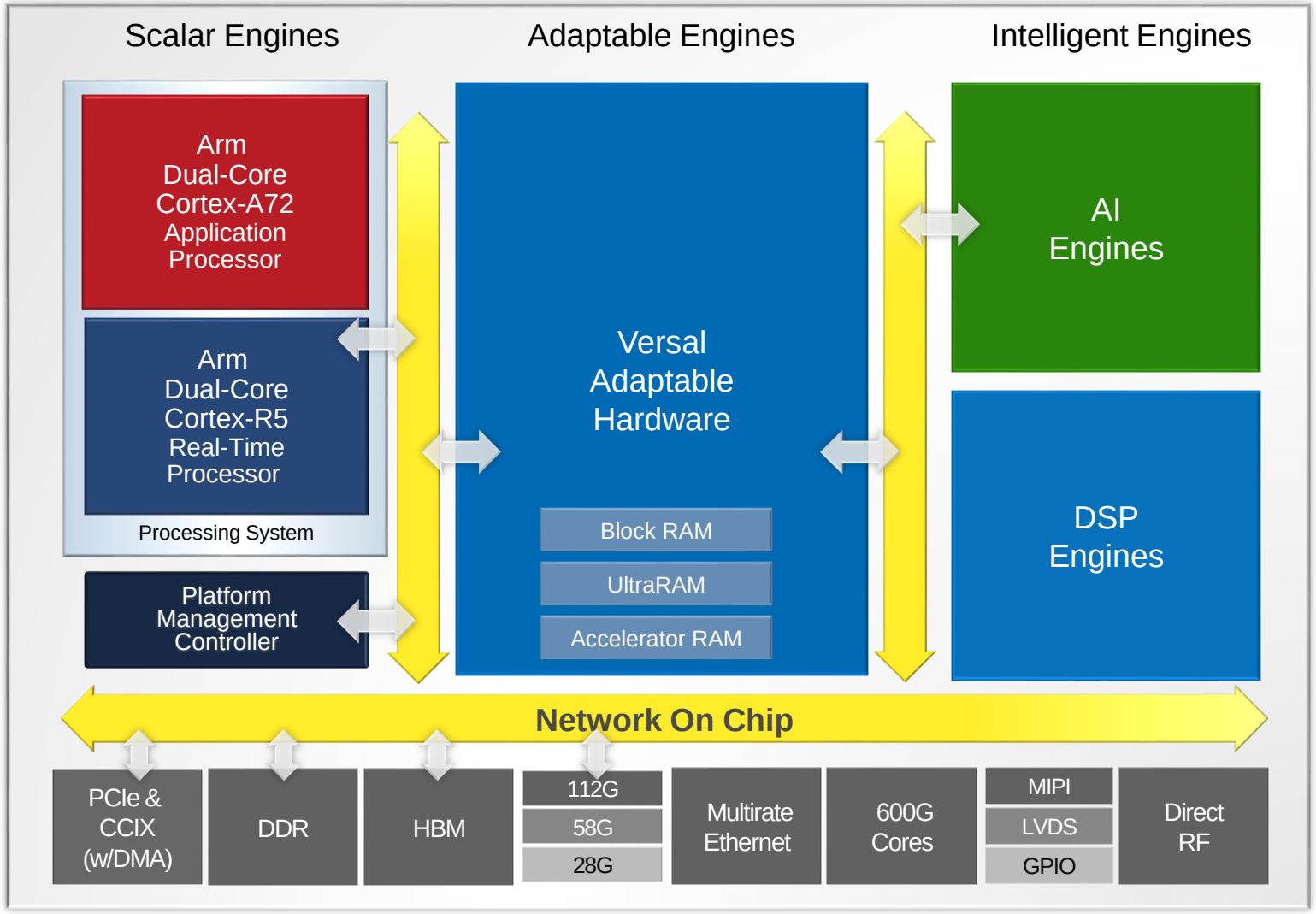
Industry's First ACAP: Versal Architecture Overview

7nm FinFET



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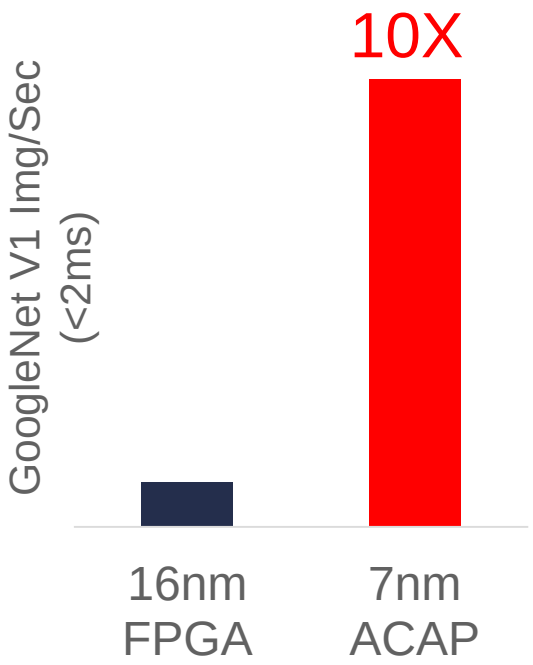
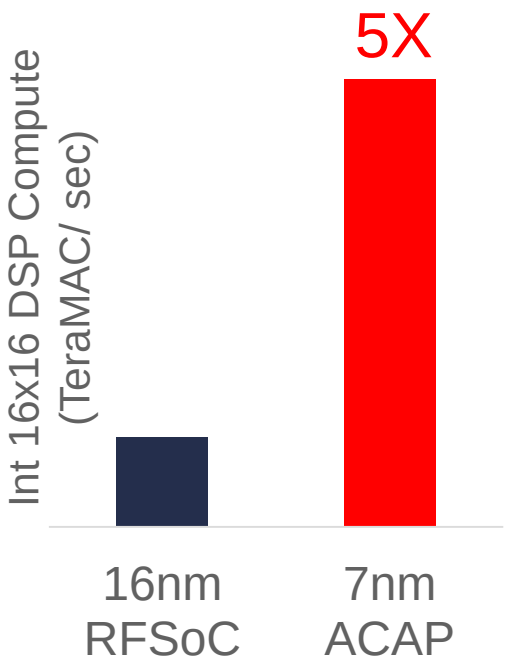
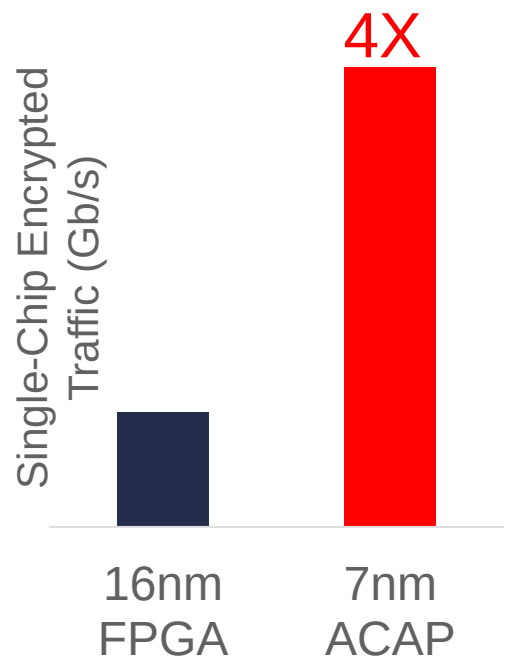
ACAP Meets Compute Demands for Cloud, Network, and Edge

CLOUD

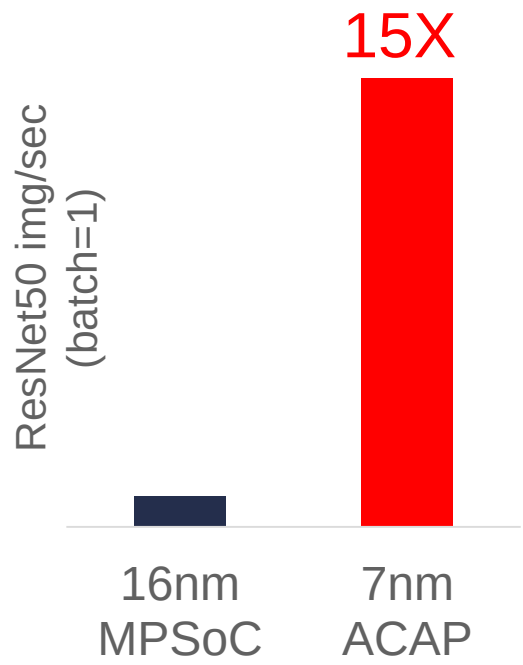


NETWORK





EDGE



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FPGA Transceiver Evolution

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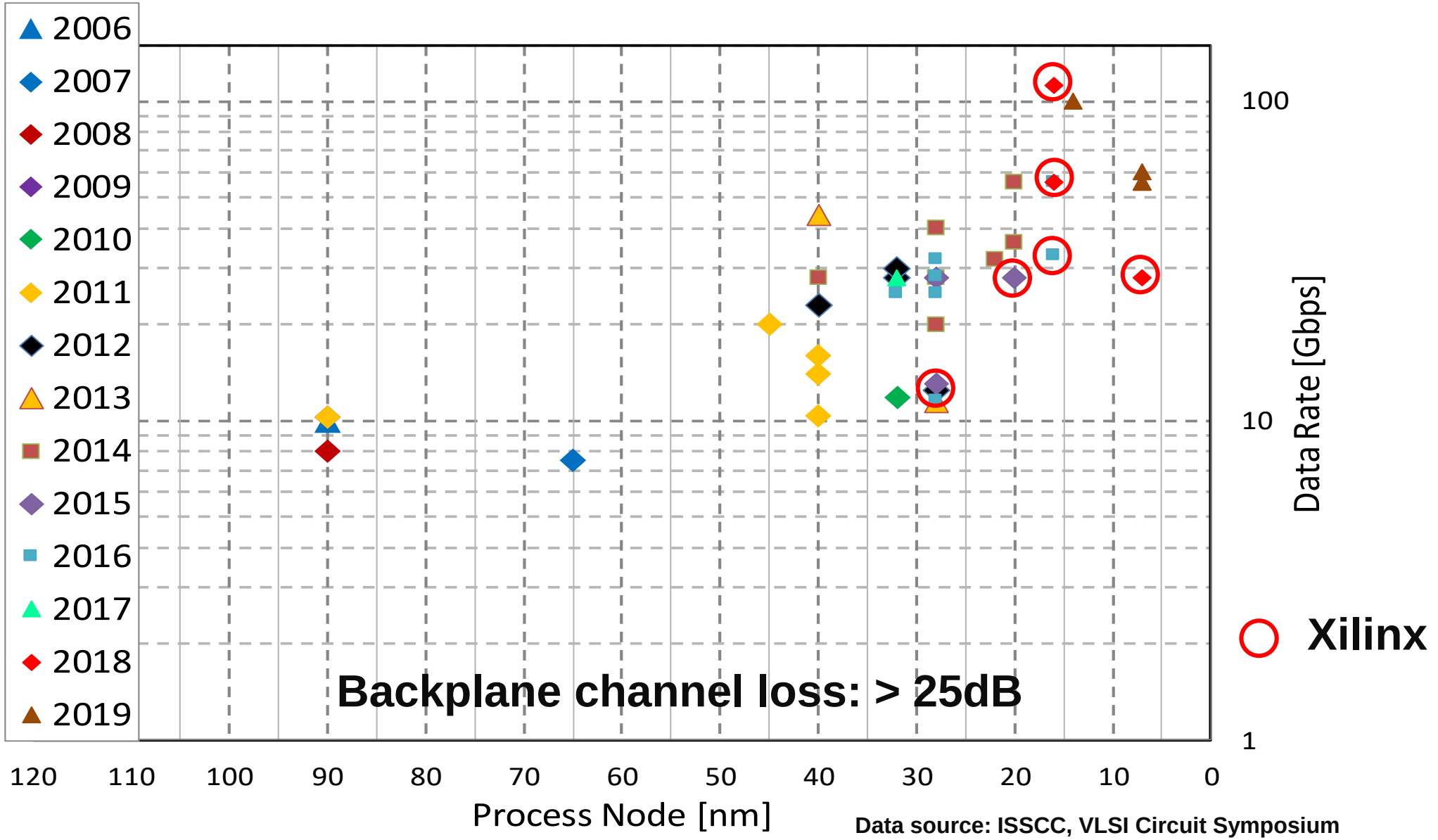
Backplane Transceiver Trend from Industry



Data source: ISSCC, VLSI Circuit Symposium

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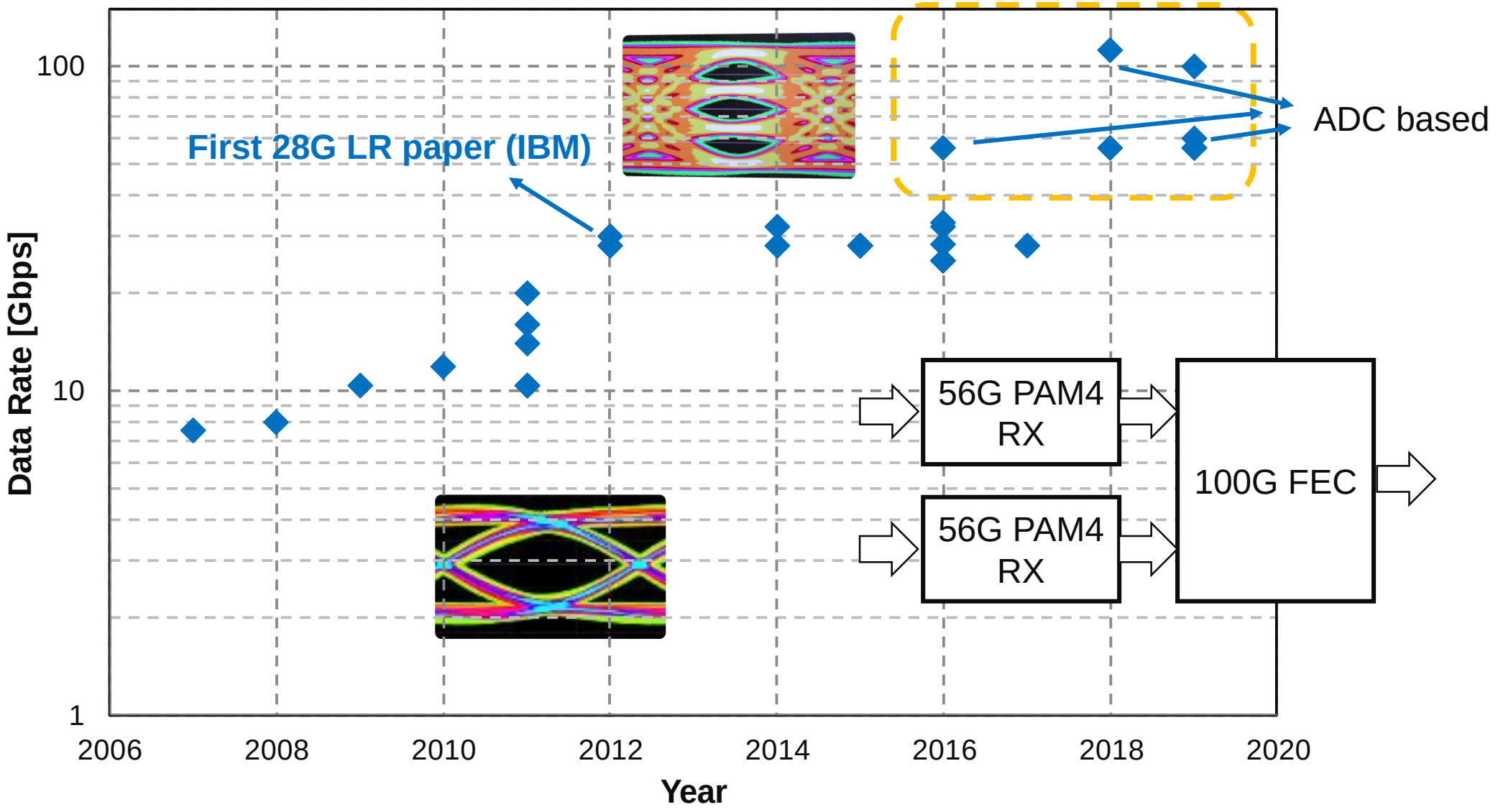
Backplane Transceiver Trend: Date Rate vs Year



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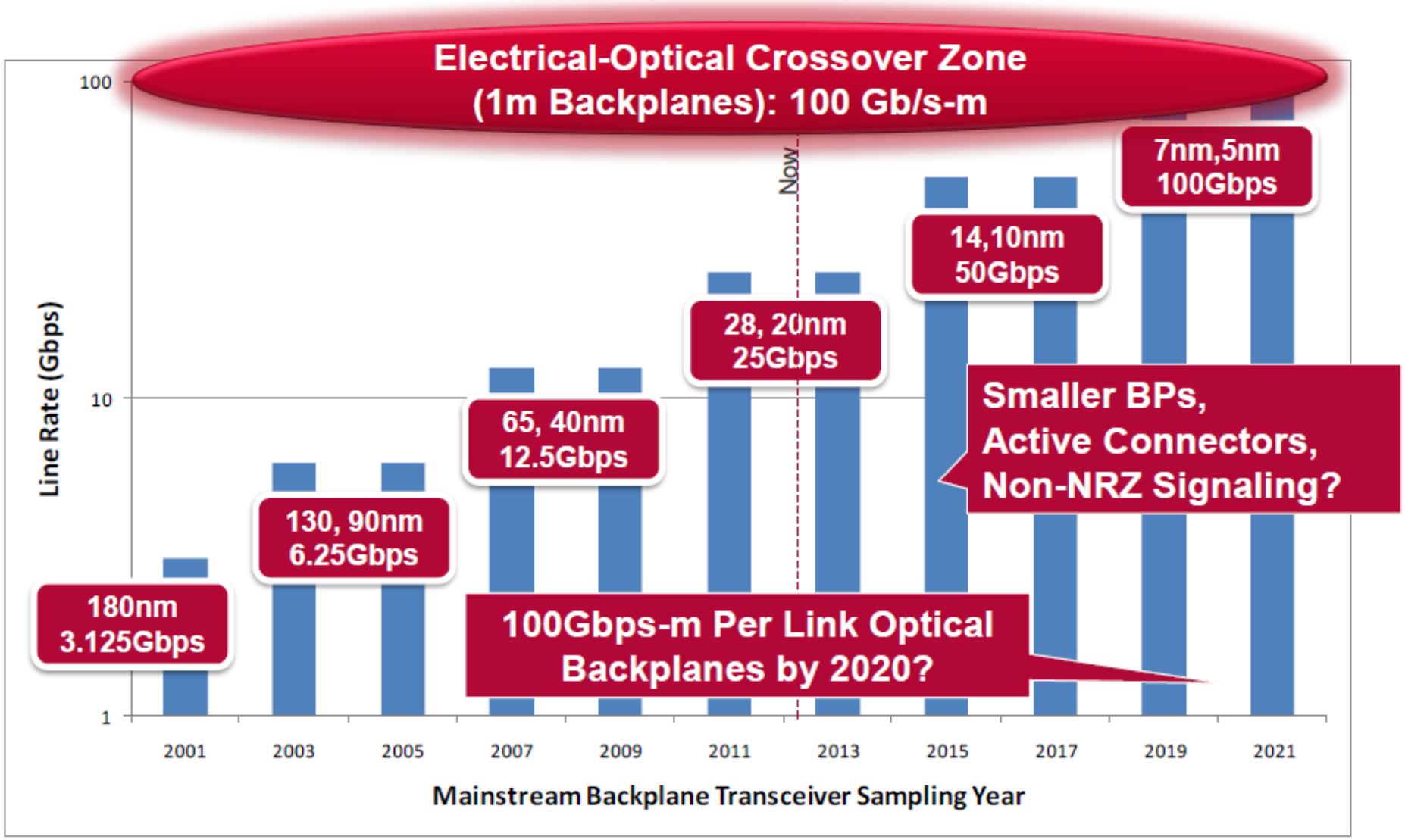
Backplane Roadmap (From 2012)



> Courtesy of E. Wu, "FPGA Optical Connectivity," OFC Workshop 2012

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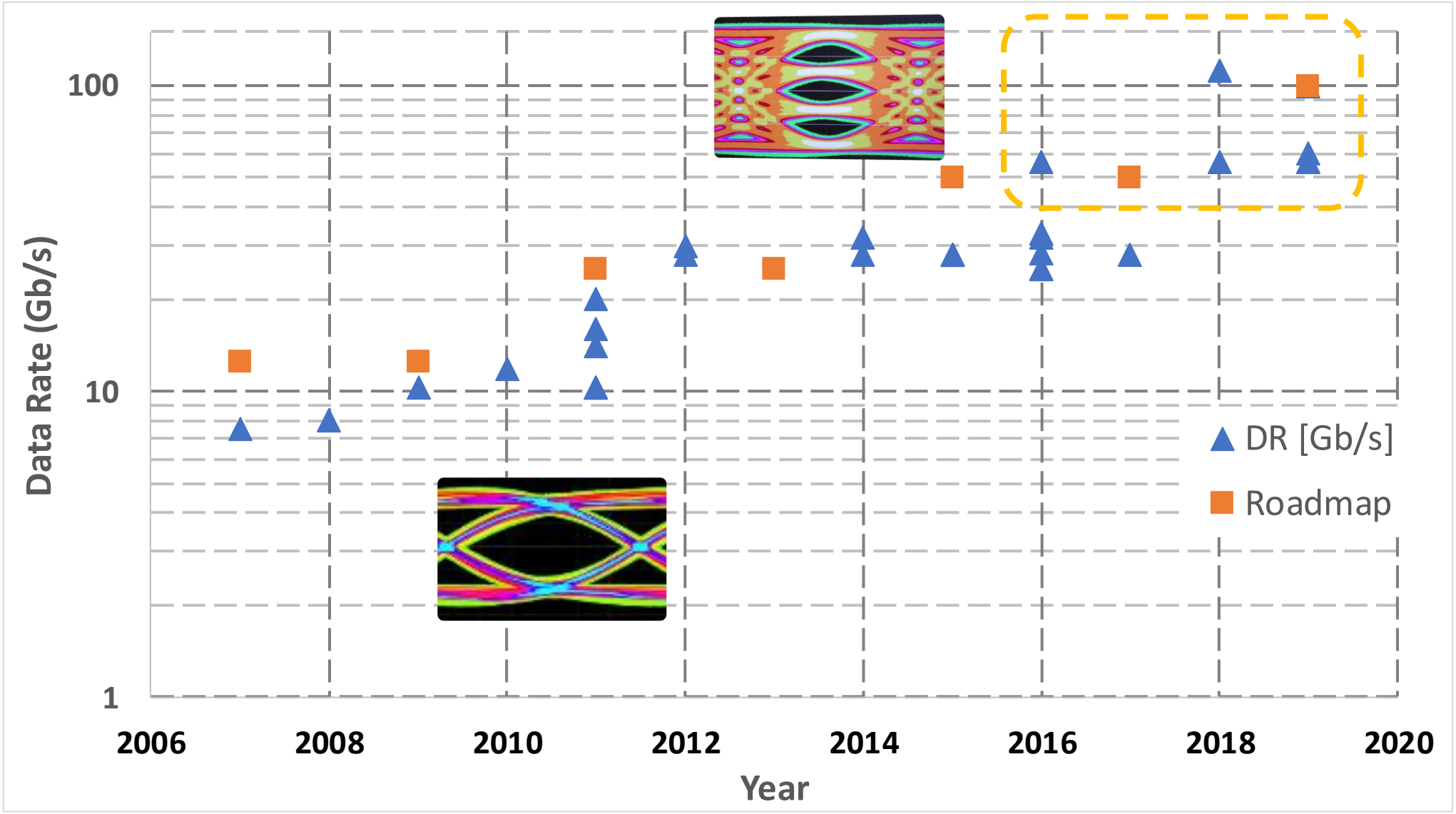
Backplane Transceiver Trend: Date Rate vs Year



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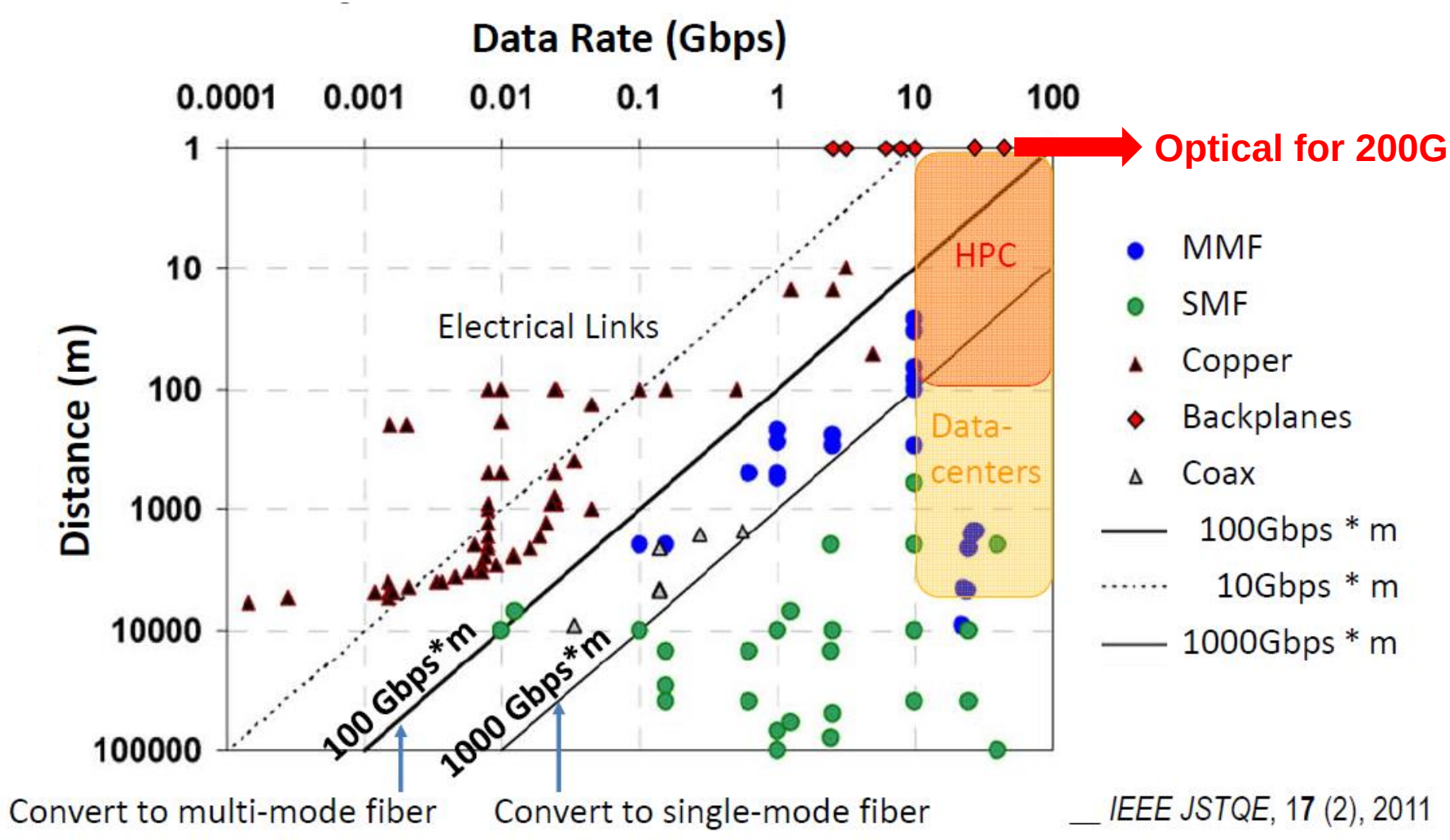
Electrical vs Optical

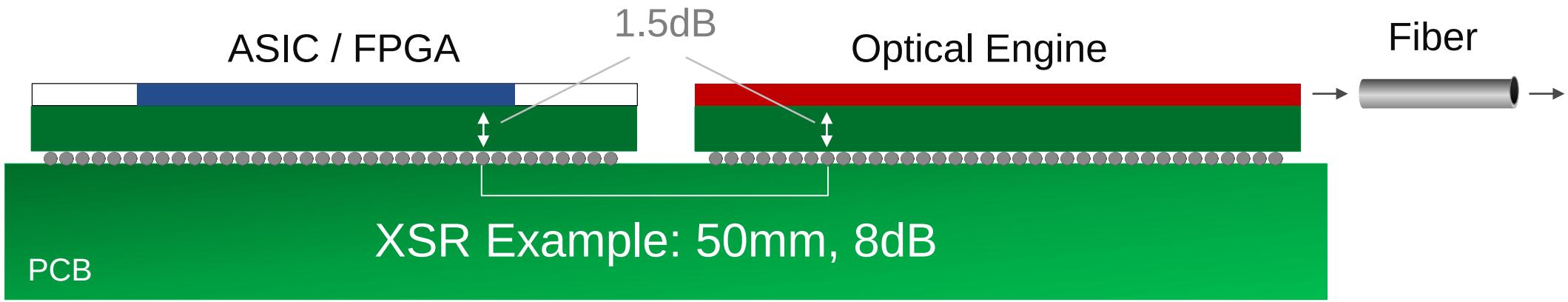


Ashok Krishnamoorthy, "Optical interconnects in computing and switching systems: the anatomy of a 20Tbps switch card", ISSCC 2018

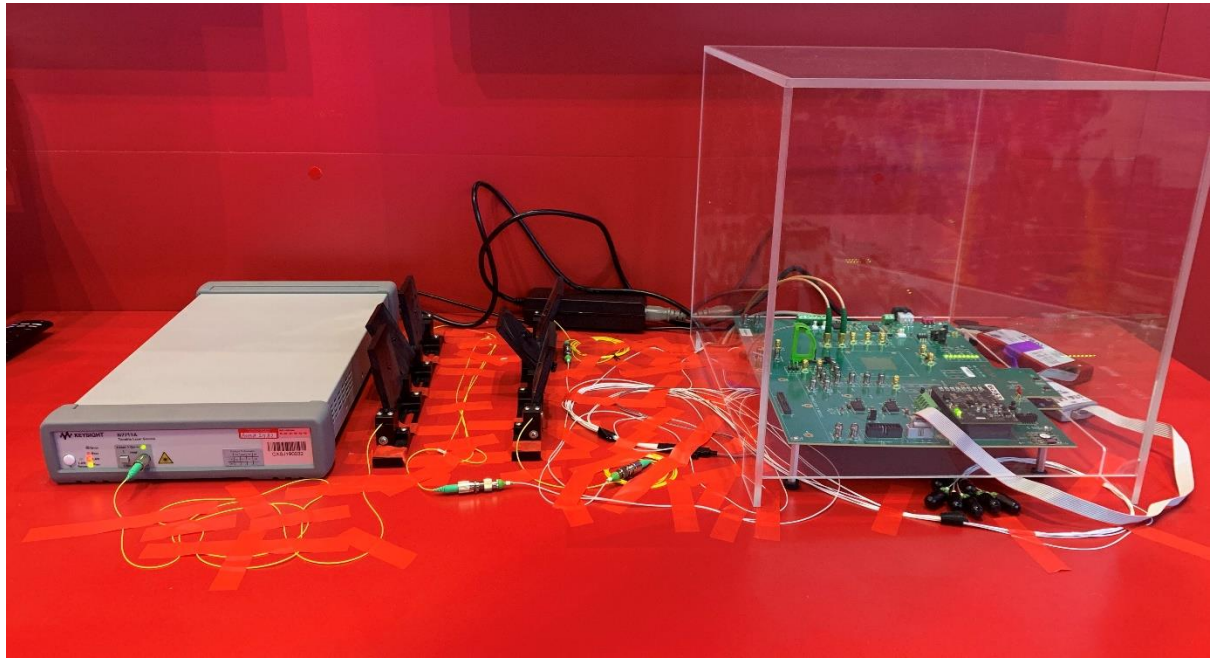
On-Board Optics Solution

- Capable of error free (BER < 10^{-12}) for compute application
- Electrical portion (16nm FinFET) based on CEI-56G-NRZ ➔ Published in ISSCC 2018
- Optical portion based on EAM silicon photonics with Driver/TIA in 16nm FinFET ➔ Submitted to VLSI 2019

Total Power per Channel	mW	pJ/bit
	126	2.25



Optical …



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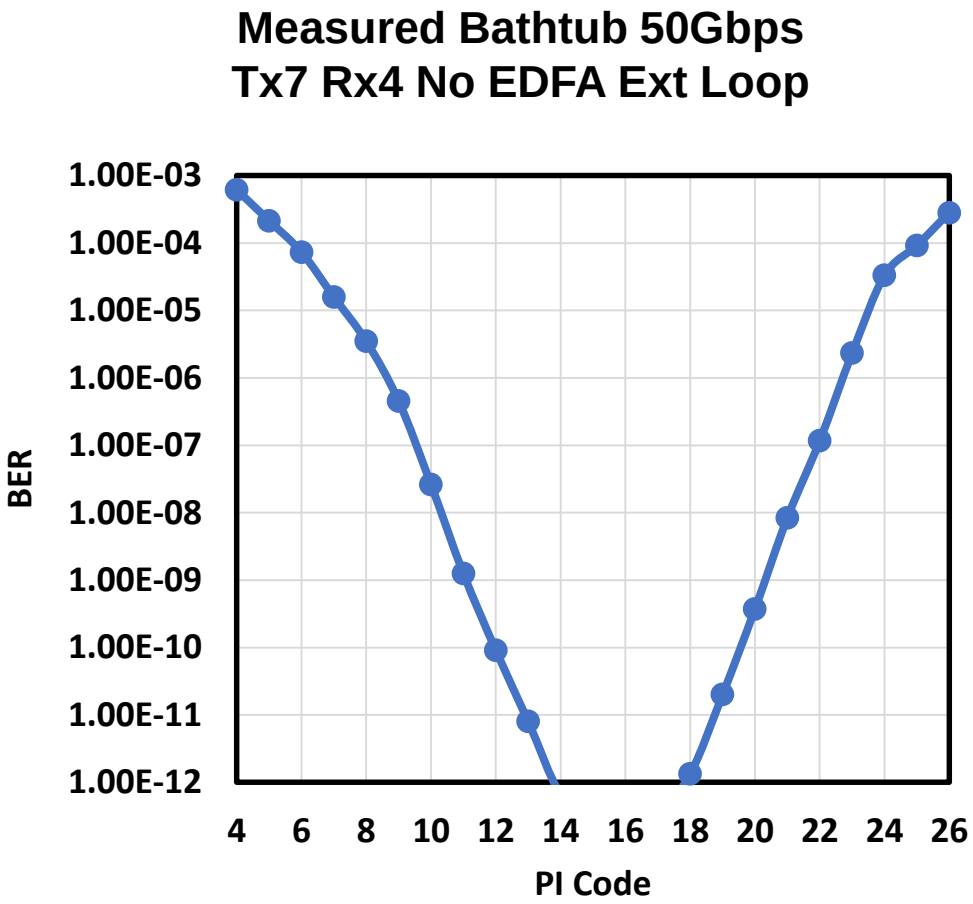

Error free at 50Gb/s!

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Transceiver Evolution: the “On Package” Stage

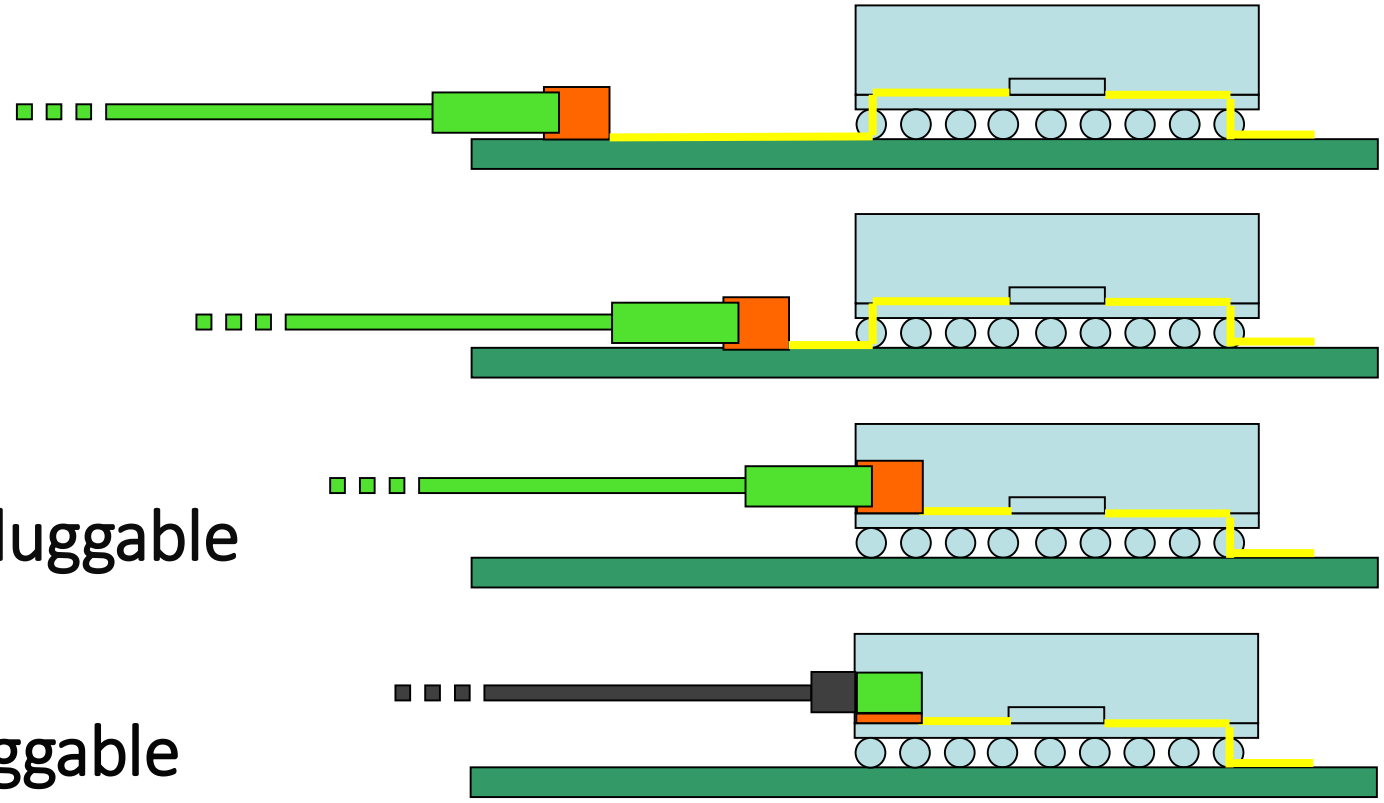
Slide courtesy of samtec

> Front Panel Pluggable

> Mid-Board Optics

> On Package, Electrically Pluggable

> On Package, Optically Pluggable



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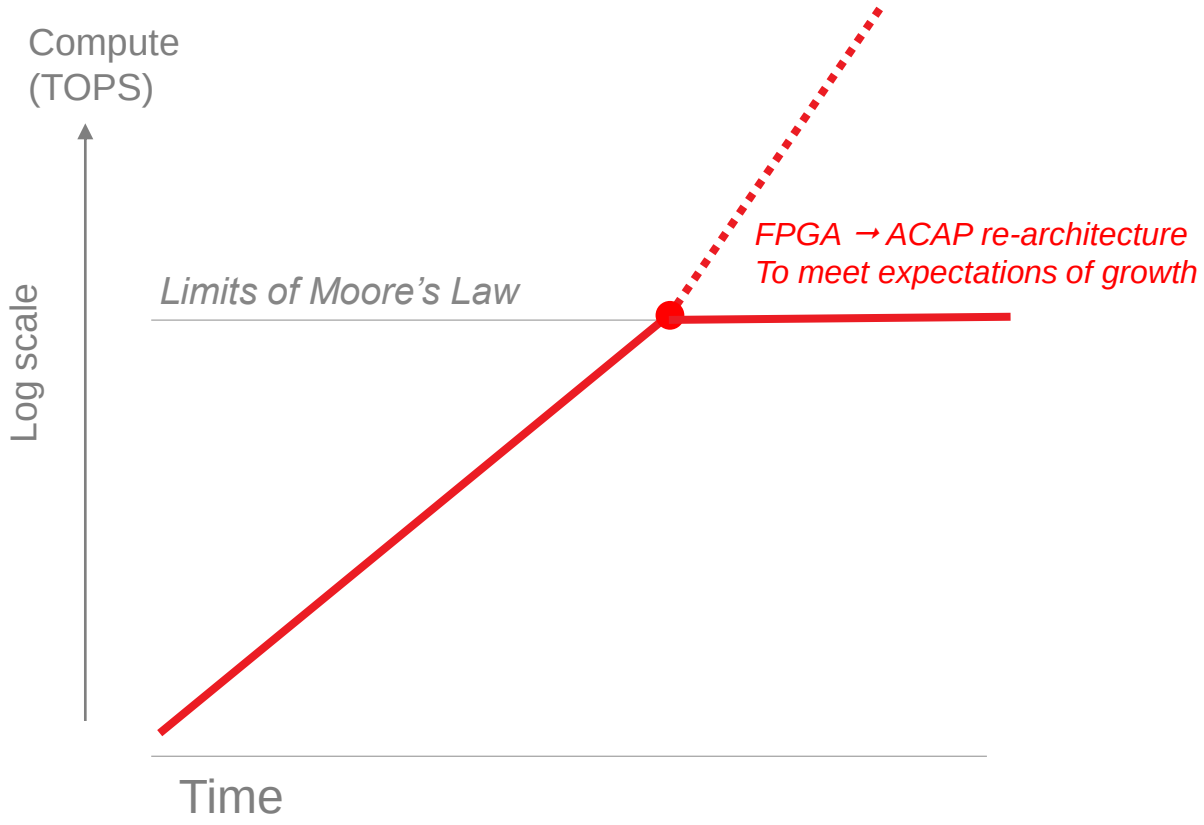
Summary

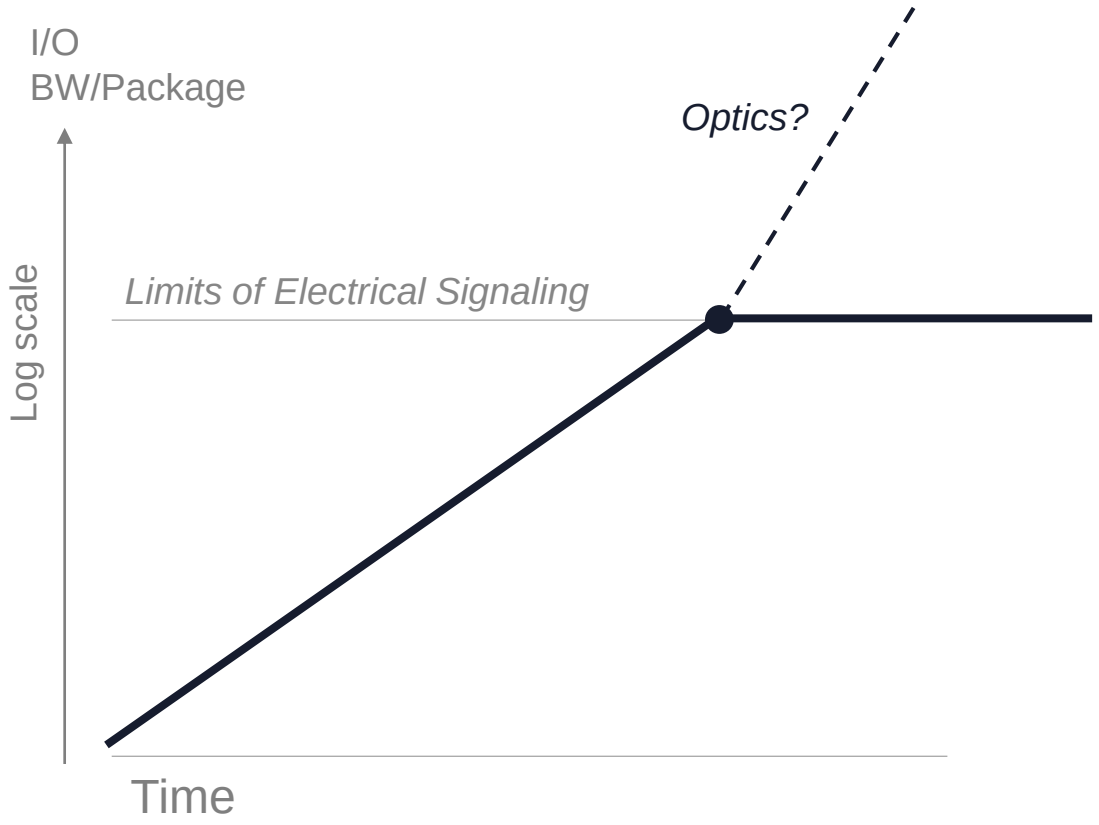
Evolution of Compute Bandwidth

Surpassed Moore's Law with New Architecture



Evolution of Serial I/O Bandwidth

Surpass Electrical Limits with New Architecture?



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Acknowledgments

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  - Anthony Torza, Ehab Mohsen, Kees Vissers, Vamsi Boppana, Gaurav Singh, Yohan Frans, Geoff Zhang, Ephrem Wu, Liam Madden

Adaptable.
Intelligent.

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