(Preliminary Agenda) 2018 Functional Safety Working Group (FSWG)

Hotel Mercure Munchen Sued Messe, Karl-Marx-Ring 87, 81735, Munich, Germany

Day 1 June 5, 2018		
Topic	**Presenter**	**Time**
Check In 7:15 / Continental Breakfast		7:15 - 8:00 AM
Welcome/Intro: Xilinx Functional Safety Solutions	**Xilinx**	8:00 - 8:30 AM
Keynote	**TBD**	8:30 - 9:30 AM
Xilinx Functional Safety Solutions State of the Union	**Xilinx**	9:30 - 10:30 AM
Break		10:30 - 11:00 AM
Zynq UltraScale+ Overview	**Xilinx**	11:00 - 12:00 PM
Lunch		12:00 - 1:00 PM
Zynq UltraScale+ Common Cause Mitigation	**Xilinx**	1:00 - 2:00 PM
Zynq UltraScale+ Security Capabilities for Safety applications	**Xilinx**	2:00 - 3:00 PM
Break		3:00 - 3:30 PM
Zynq UltraScale+ Isolation Capabilities & Implementation	**Xilinx**	3:30 - 4:30 PM
Day One Wrap Up	**Xilinx**	4:30 - 4:45 PM
June 5, 2018 : Day 1 Social		
Join us for light appetizers and cocktails		4:45 - 7:30 PM

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Day 2 June 6, 2018		
Topic	**Presenter**	**Time**
Re-Check In 7:30 / Continental Breakfast		7:30 - 8:00 AM
Quality and Reliability	**Xilinx**	8:00 - 9:00 AM
Single Event Upset & Soft Error Mitigation IP	**Xilinx**	9:00 - 10:00 AM
Break		10:00 - 10:30 AM
Isolation Design Flow & Partial Reconfiguration	**Xilinx**	10:30 - 11:30 AM
Xilinx Intellectual Property Solutions for Functional Safety	**Xilinx**	11:30 - 12:15 PM
Lunch		12:15 - 1:15 PM
Functional Safety in FPGAs/Programmable Logic	**Xilinx**	1:15 - 2:15 PM
Zynq Safety Design Example	**Xilinx**	2:15 - 3:15 PM
Break		3:15 - 3:45 PM
Zynq-7000 Safety Design Example - Metrics Calculation	**Xilinx**	3:45 - 4:45 PM
FSWG Adjournment and Call to Action	**Xilinx**	4:45 - 5:00 PM

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