Automotive Applications for Machine Learning

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March 2019

XILINX.

Outline

- **Xilinx in Automotive**
- **ML in Automotive Applications**
  - Internal Camera
  - Forward Camera
  - Central Modules
- **DFX (Dynamic Function Exchange) Concept**

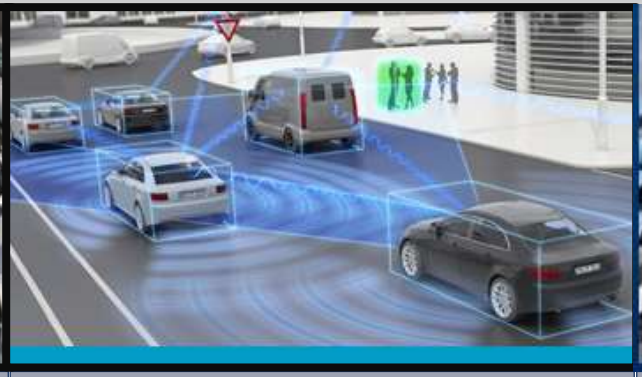
Xilinx in Automotive

Xilinx Automotive Solutions and Products

Automotive Solutions

Automated / Autonomous Driving (AD)

Next decade of growth as the market drives adoption of conditional automated driving features up through full autonomous vehicles. Includes key new technologies such as Deep Learning paired with traditional Discriminatory Object Detection.



Advanced Driver Assistance Systems (ADAS)

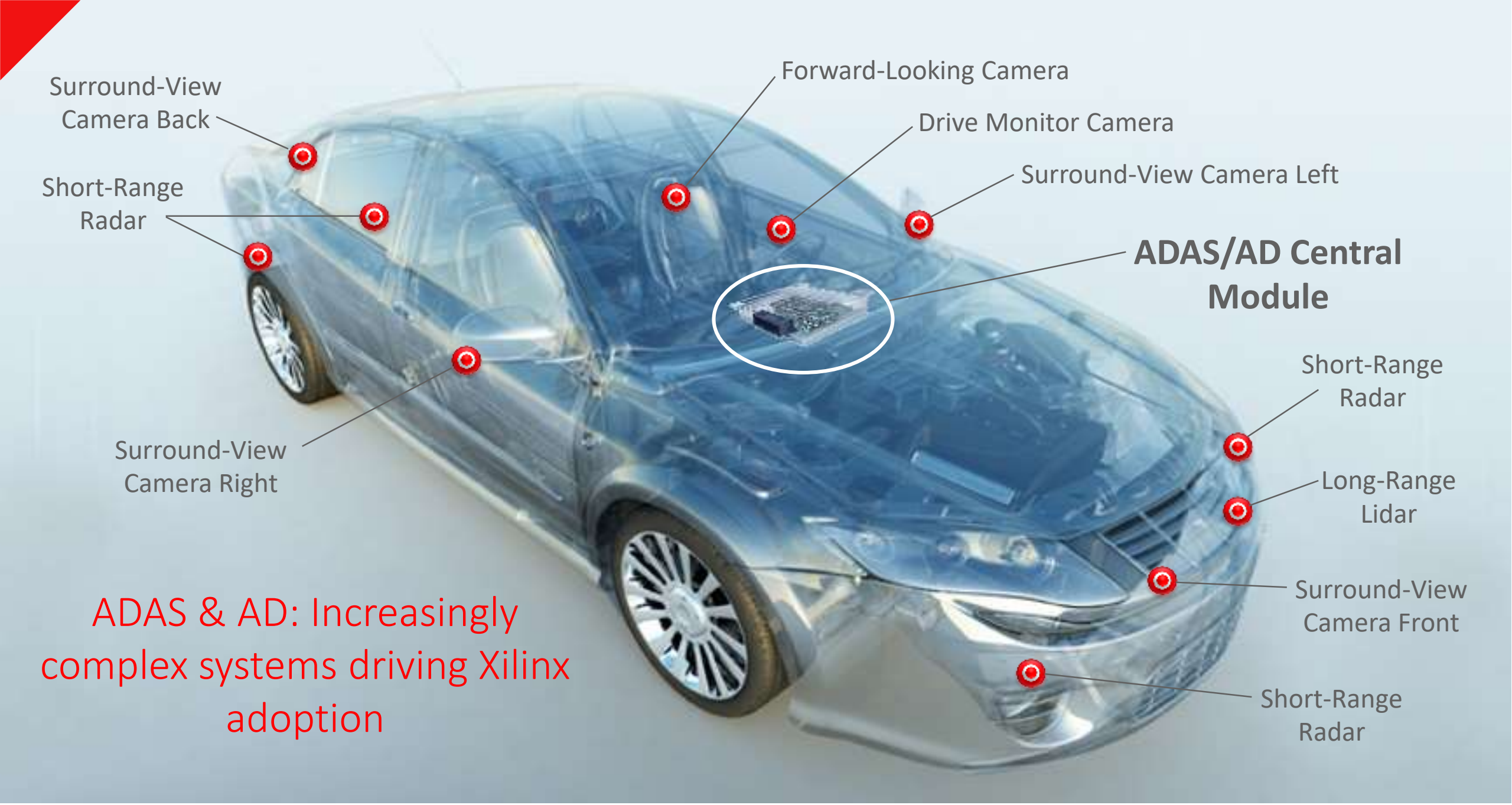
Currently driven by regional NCAP initiatives pushing collision avoidance, pedestrian, bicycle/motorcycle, vehicle, sign detection and tracking features.

In Cabin Driver Information

IVI and DI are converging with sharing of information and larger. HMI trends like Heads-Up Displays (HUD), Augmented Reality, eMirror - and Gesture Recognition are changing the way Drivers and Passengers interact with the vehicle. Secure Vehicle to Infrastructure/Vehicle (V2X) networks required.

Electrification

Electrification will provide new opportunities in Motor Control, charging systems, etc. Xilinx can leverage existing industrial motor control heritage to address these applications



ADAS & AD: Increasingly complex systems driving Xilinx adoption

ADAS and AD Focus Applications

ADAS Applications

Front Camera

LiDAR

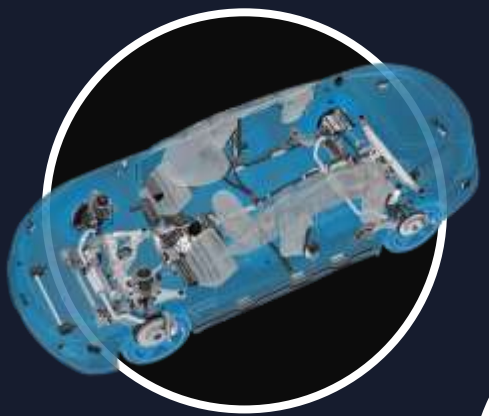
Full Display Mirror

Surround View Camera

RADAR

Driver Monitoring System

AD Central Module Functions



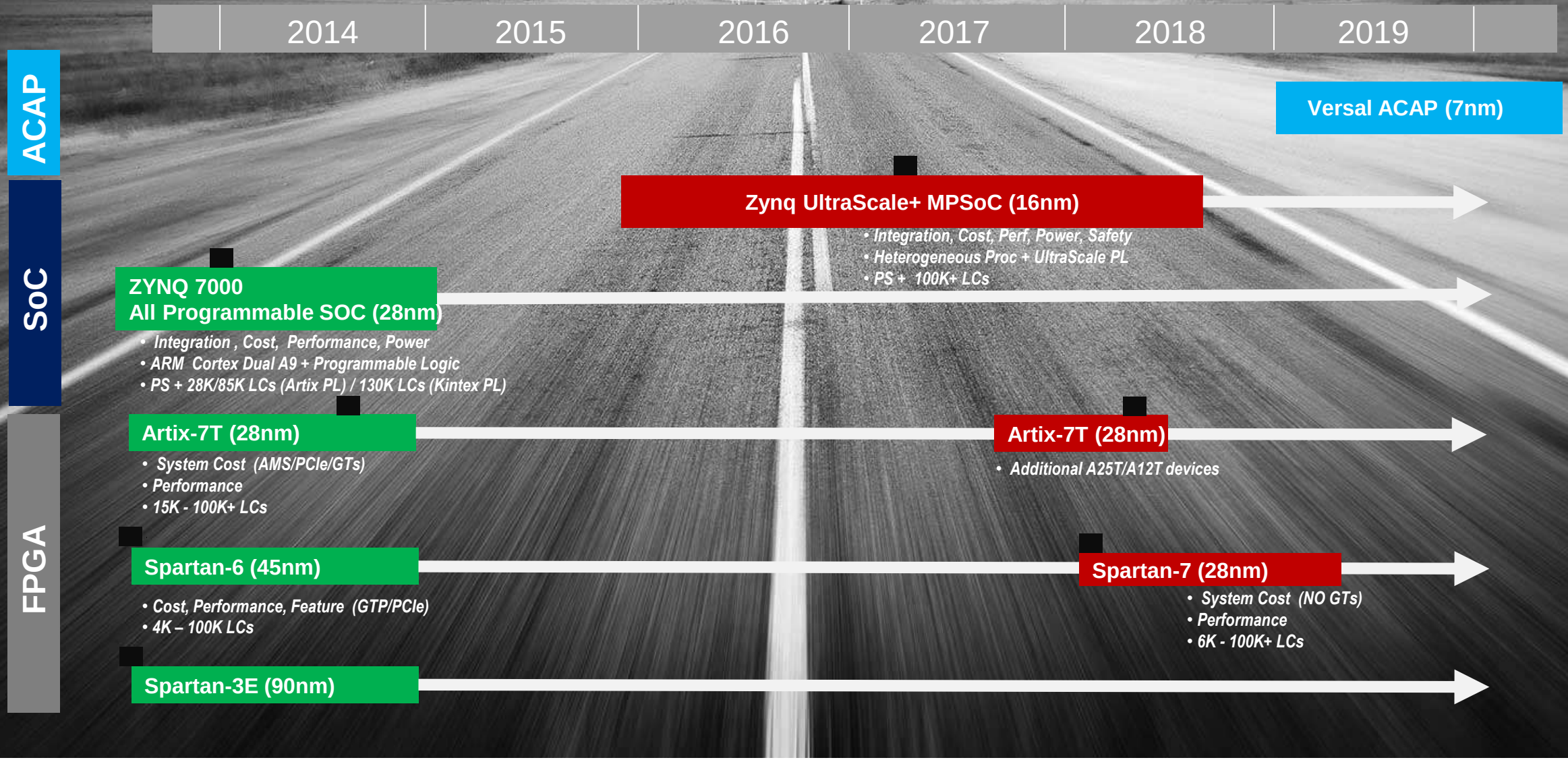
Data Aggregation & Pre-processing

Sensor Fusion

Compute Acceleration

Xilinx Automotive Devices

Xilinx Automotive (XA) Silicon Roadmap



■ 1st XA Prod

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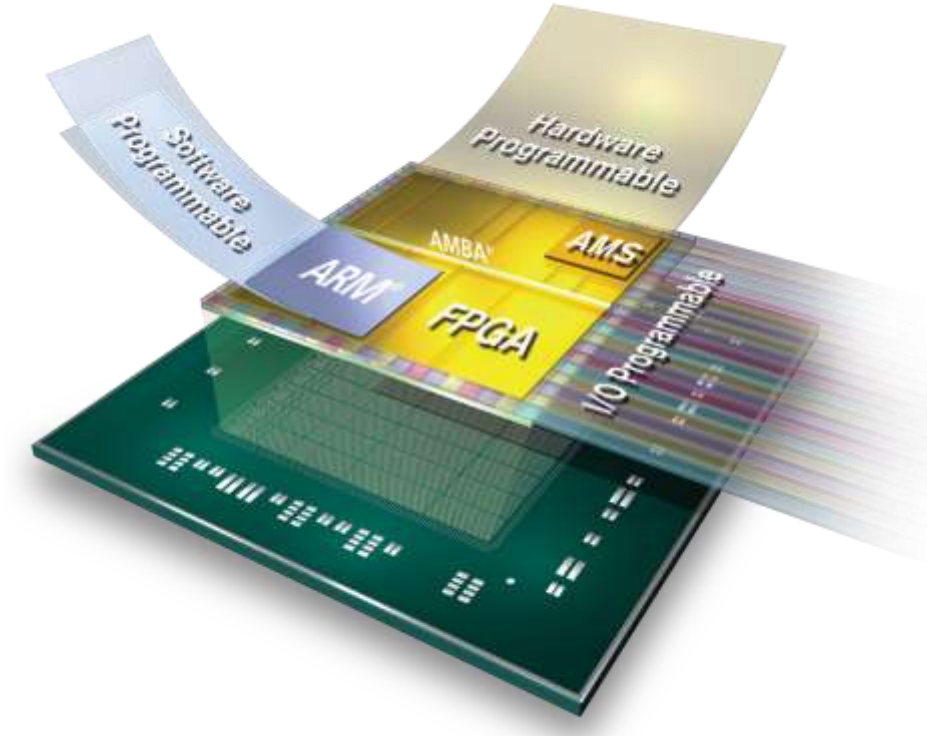
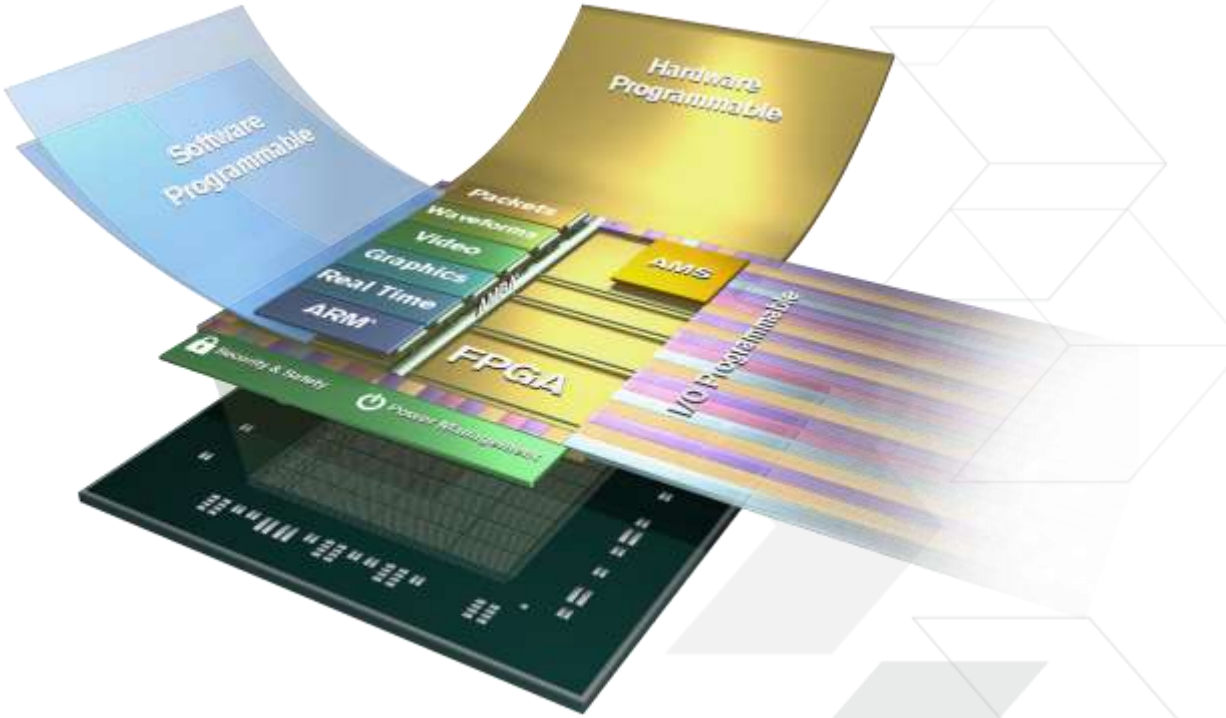
Xilinx All Programmable SoC and MPSoC
A Game Changing Technology in Automotive



ZYNQ | 28nm



ZYNQ UltraSCALE+ | 16FF+

SoC: System on Chip
MPSoC: Multi-Processor System on Chip

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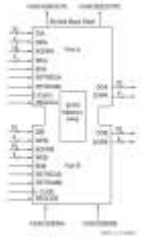
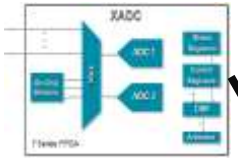
Field Programmable Gate Array Based SoC's

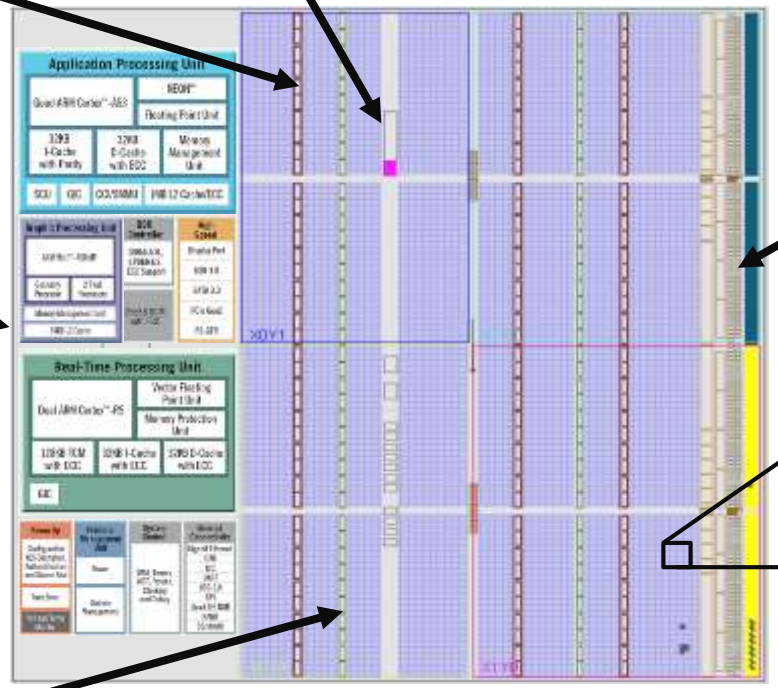
Block RAMs

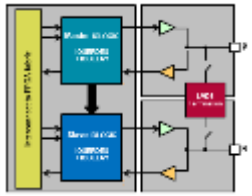




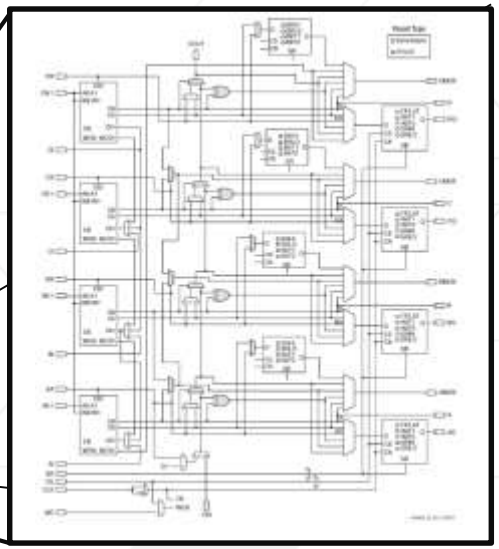
SysMon / ADCs

Processing System

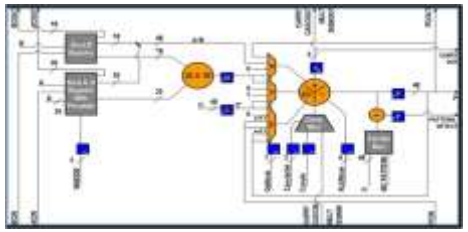




I/O Blocks



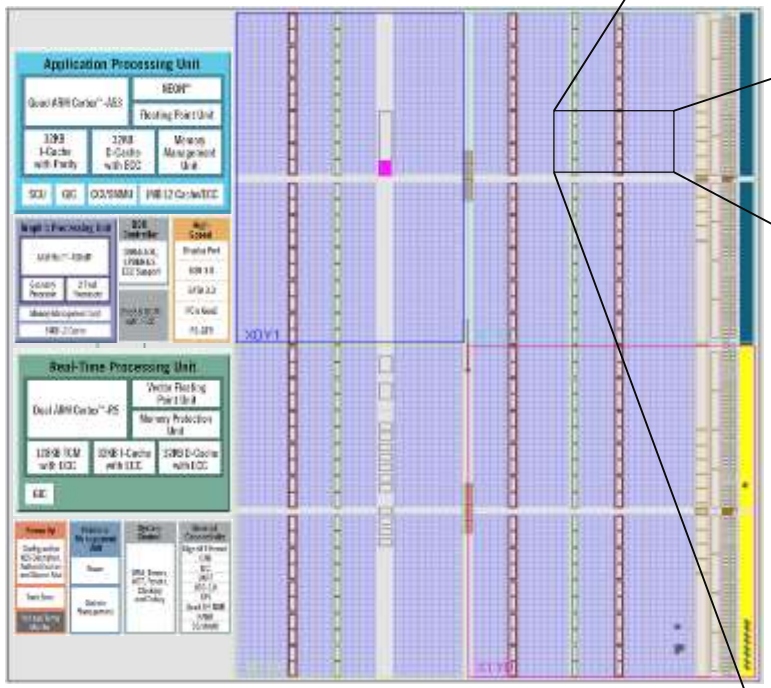
Configurable Logic Blocks

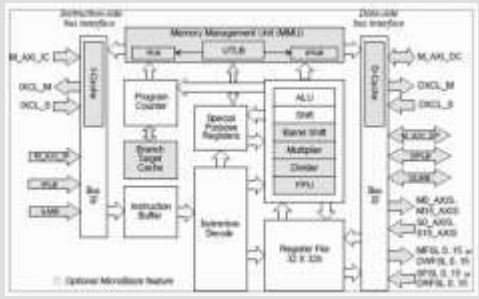


DSP Slices

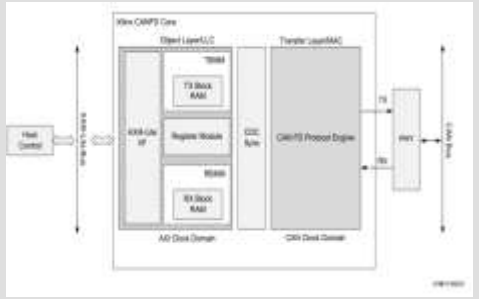
Field Programmable Gate Array Based SoC's

FPGA Fabric = Programmable Logic

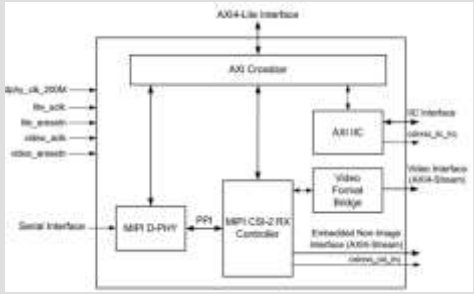




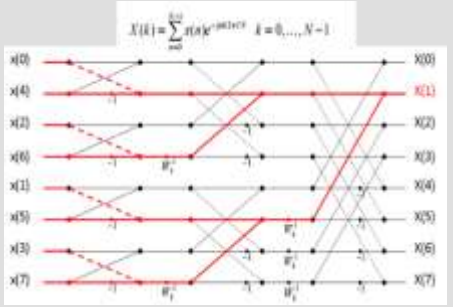
- **Common Processor Peripherals** (e.g. CAN / CAN-FD)



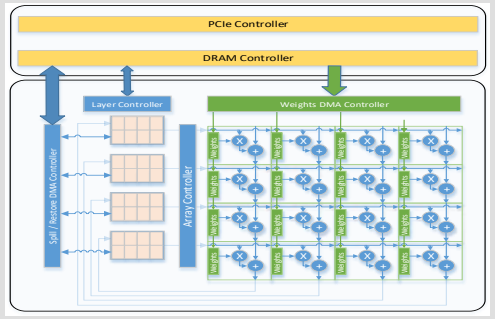
- **MicroBlaze 32-bit Soft Processor**



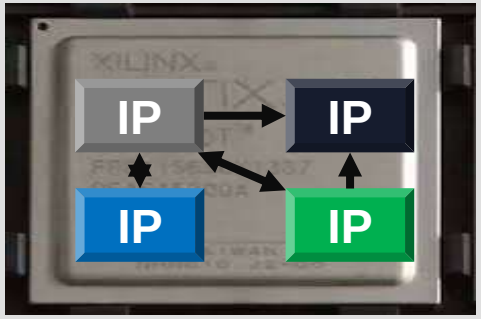
- **Application Focused Connectivity** (e.g. MIPI CSI-2 Controller and D-PHY)



- **Highly Parallelized and Customized DSP Acceleration** (e.g. FFT)



- **Inference DNN Processing Engines**



- **Unique, Differentiating User-Defined Functions or Pipelines of Functions**

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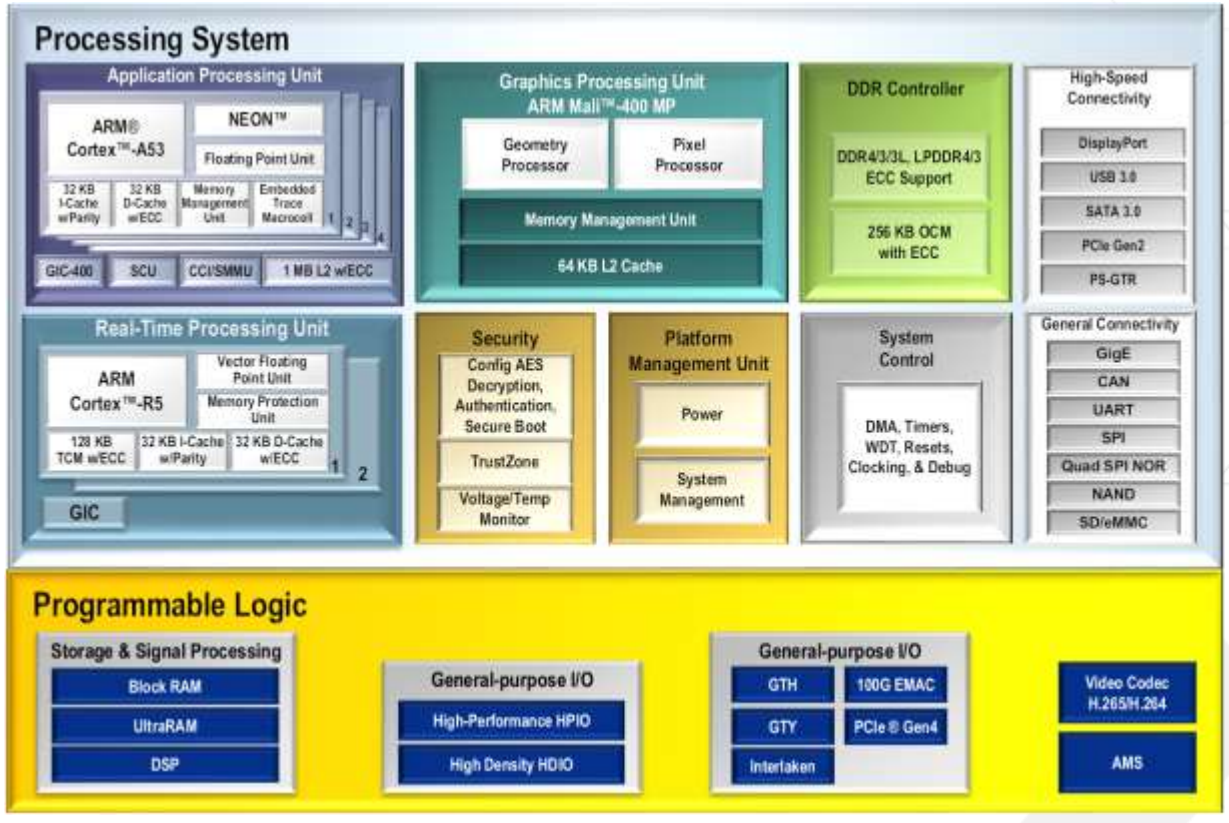
Zynq® UltraScale+™ MPSoC

Heterogeneous Multi-Processing at the Heart of the System

Device Domains

- Full Power Domain (FPD)
- Low Power Domain (LPD)
- Programmable Logic (PL)



- **PS Processing Units**
  - Applications Processor Unit (APU) = A53 Complex
  - Real-Time Processing Unit (RPU) = R5 Complex
  - Graphic Processing Unit (GPU) = Mali-400MP Complex
  - Configuration Security Unit (CSU): Configuration & Security
  - Platform Management Unit (PMU): Power & Safety

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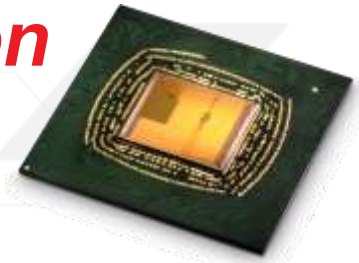
XA Zynq UltraScale+ MPSoC – *Smarter Control & Vision*

Scalable platform offers easy migration between devices



	XA Zynq® UltraScale+™ MPSoC Devices	Smarter Control & Vision			
		ZU2EG	ZU3EG	ZU4EV	ZU5EV
Processing System	Application Processor Core	**Quad** ARM® Cortex™-A53 MPCore™ up to 1.2 GHz L1 Cache 32 KB I (w/ Parity) / D (w/ ECC), L2 Cache 1 MB (w/ ECC), on-chip Memory 256 KB (w/ ECC)			
	Real-Time Processor Core	**Dual** ARM® Cortex™-R5 MPCore™ up to 500 MHz L1 Cache 32 KB I (w/ Parity) / D (w/ ECC), L2 Cache 1 MB (w/ ECC), Tightly Coupled Memory 128 KB (w/ ECC)			
	GPU	Mali™-400, 600 MHz, 64 KB L2 Cache (w/ ECC)			
	External Memory Support	DDR3, DDR3L, LPDDR3, DDR4, LPDDR4, 2x QSPI, NAND (DDR Controller w/ ECC in all modes)			
	Peripherals	2x USB 2.0/3.0 (OTG), SATA 3.0, DisplayPort, 4x Tri-mode Gigabit Ethernet, PCIe® Gen2x4, 2x SD/SDIO, 2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO			
Programmable Logic	System Logic Cells (K)	103	154	192	256
	Block RAM (Mb)	5.3	7.6	4.5	5.1
	UltraRAM (Mb)	-	-	14	18
	DSP Slices	240	360	728	1056
	PCI Express® Gen 4	-	-	2	2
	Video Codec Unit	-	-	1	1
Package	**Footprint**	**Dimensions**	**PS I/O, 3.3V HD I/O , 1.8V HP I/Os, PS-GTR 6 Gb/s, GTH 12.5Gb/s, GTY 33 Gb/s**		
	SBVA484	19 mm @ 0.8	170, 24, 52 4,0,0	170, 24, 52 4,0,0	
	SFVA625	21 mm @ 0.8	170,24,156 4,0,0	170,24,156 4,0,0	
	SFVC784	23 mm @ 0.8	214,96,156 4,0,0	214,96,156 4,0,0	214,96,156 4,4,0	214,96,156 4,4,0

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Partitioning Functionality in a Xilinx Automotive Device

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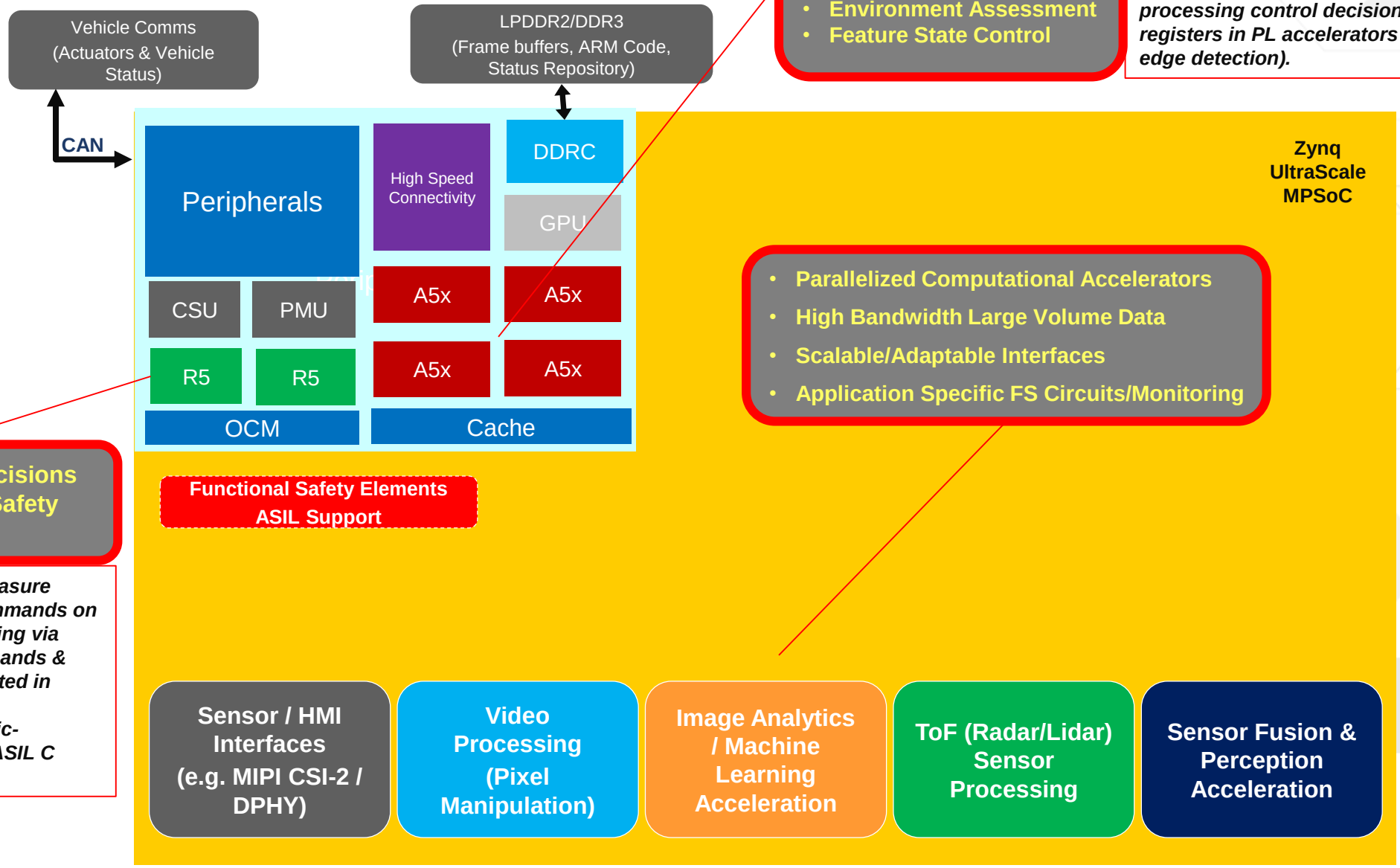
ZU+ Based Automotive Applications General Partitioning Guidelines

- Feature Application SW
- Algo Config &Control
- Object Tracking
- Environment Assessment
- Feature State Control

A53's perform sensor processing and environmental characterization tasks in conjunction with HW accelerators. HW Accelerator results (e.g motion vectors) written to cache/OCM memory via ACP port. A5x's also implement processing control decisions by setting parametric registers in PL accelerators (e.g. thresholds for edge detection).



- Parallelized Computational Accelerators
- High Bandwidth Large Volume Data
- Scalable/Adaptable Interfaces
- Application Specific FS Circuits/Monitoring

- System Control Decisions
- Diagnostics /FuncSafety
- Vehicle Comms

Safety critical countermeasure decisions & actuator commands on lockstep R5's. Data sharing via OCM. CAN output commands & key decision points initiated in lockstep R5's with cross-monitoring and diagnostic-protected voting in PL. (ASIL C certified safety island)

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Xilinx Automotive Applications Leveraging AI/ML Processing

- Interior Cabin Sensing
- Forward Camera
- Central ADAS/AD Modules

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Innovating In-Cabin AI Sensing

DAIMLER

Jun. 26, 2018

- **Strategic Collaboration Announcement: Daimler Selects Xilinx for AI-based Auto Applications**
  - "Xilinx is providing technology that will enable us to deliver **very low latency and power-efficient solutions for vehicles that must operate in thermally constrained environments**. We have been very impressed by Xilinx's heritage and selected the company as a trusted partner for our future products."
    - Georges Massing, Director, Daimler AG
  - The system will be powered by a Xilinx automotive platform consisting of system-on-a-chip (SoC) devices and AI acceleration software. Mercedes-Benz will productize Xilinx's AI processor technology, **enabling the most efficient execution of their neural networks.**

Mercedes-Benz

Jan. 11, 2019

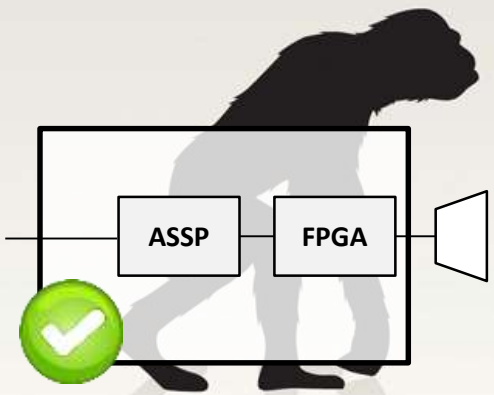
- **MBUX Interior Assistant in Mercedes Benz GLE & CLA**
  - **Interior Assist**: AI-based gesture input system, powered by Zynq® UltraScale+™ MPSoC
  - "Recognizes the occupants' natural movements so the vehicle can predict driver and passenger needs"
  - The interior assist on GLE and CLA both using Zynq® UltraScale+™ MPSoC, using a single camera

Ralph Wittig on stage at CES

Automotive Forward Camera Evolution

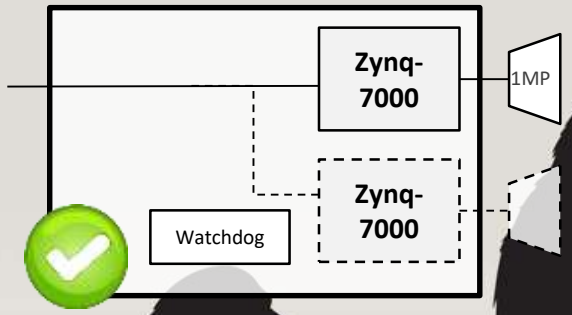
Xilinx Deployed in Production Systems for first 3 Generations and targets NCAP2022 with Next Generation of Devices

- GEN1: Spartan 6
  - Camera: VGA/WVGA
  - Warning Only, e.g. Lane Departure Warning
  - Xilinx Value
    - Imager Interfacing
    - Image Conditioning and Feature Extraction



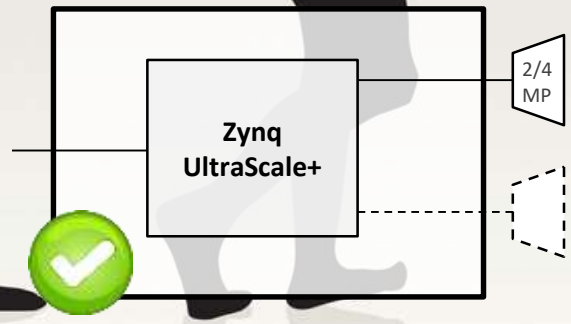
GEN2: Zynq 7000

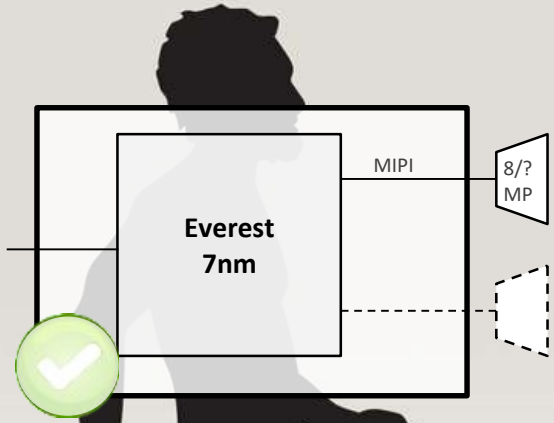
- Camera: Up to 2 Mpixel
- Lane Departure Warning, Speed Alert, Collision Mitigation
- Xilinx Value
  - Optimal HW/SW Partitioning
  - Scalability
  - Differentiation



GEN 3: Zynq MPSoC

- Camera: Up to 4 Mpixel
- Broader Protection (e.g. Pedestrian/Cyclist Protection)
- Vehicle Convenience Control (e.g. Traffic Jam Assist)
- Xilinx Value
  - Heterogeneous processors
  - Tightly coupled Application SW and custom HW accelerators
  - Safety Island for FuSa functions





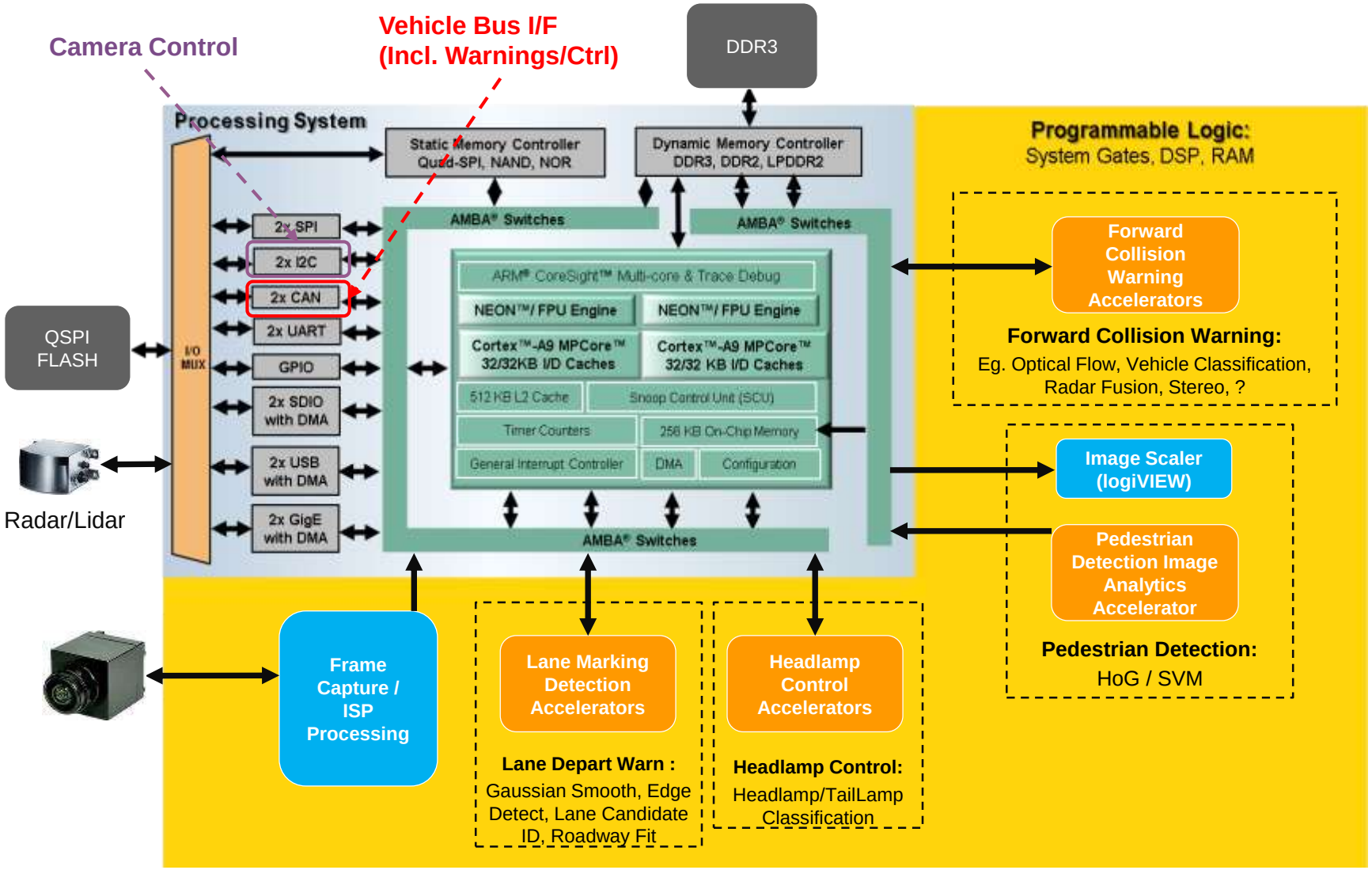
2008 2010 2012 2014 2016 2018 2020 2022

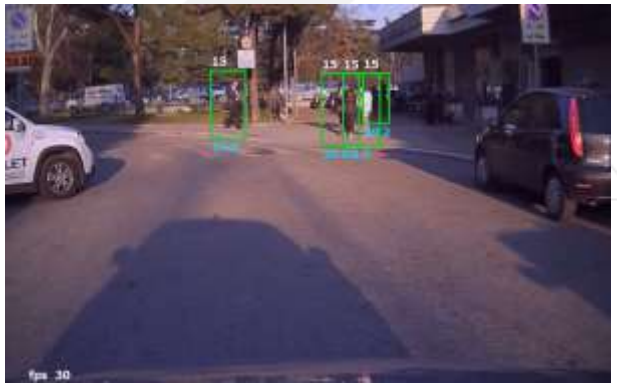
Future: ACAP

- Camera: Up to 8 Mpixel
- System Features:
- Level 2/3 Automation
- Urban and Highway Scenarios
- Xilinx Value
  - Higher Data Bandwidth Channels
  - High Performance / Low Power CNN Processing for environment Cognition
  - Advancing FuSa

Zynq 7000 Forward Looking Camera

LDW + FCW / AEB – CV-based





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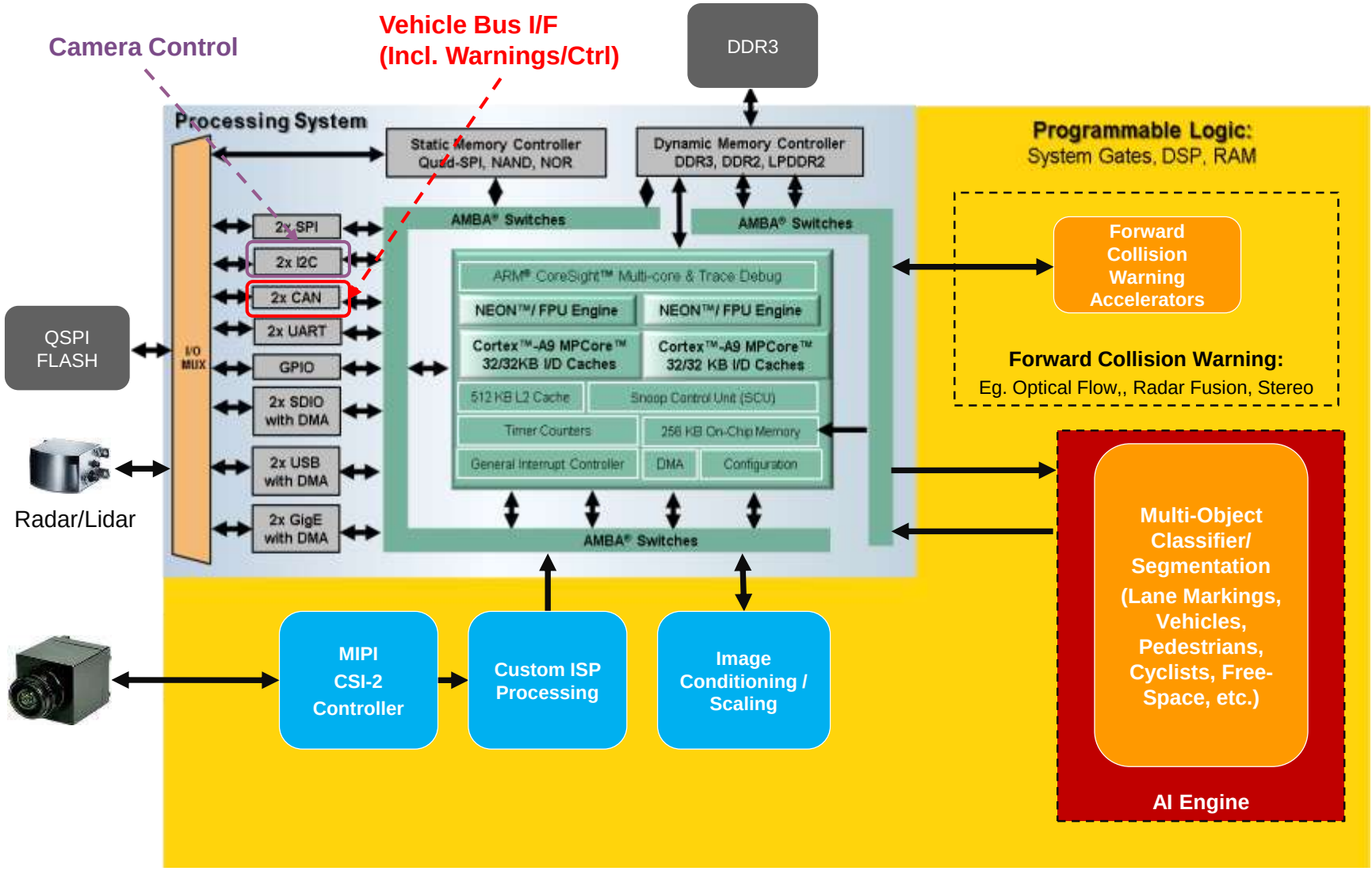
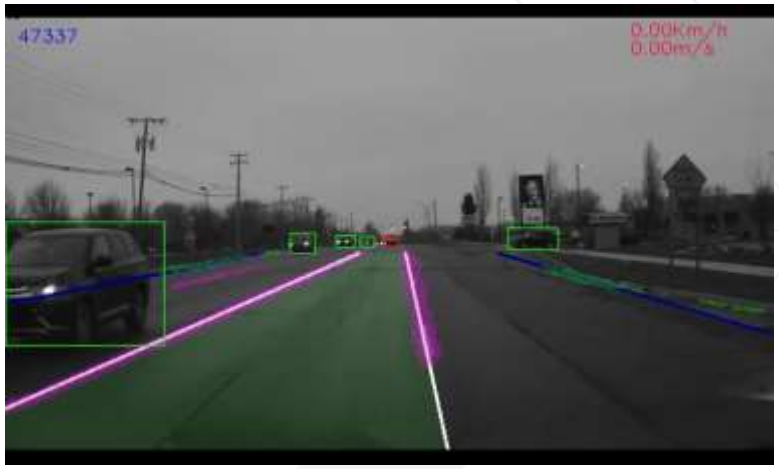
Zynq 7000 Forward Looking Camera

LDW + FCW / AEB – AI-based





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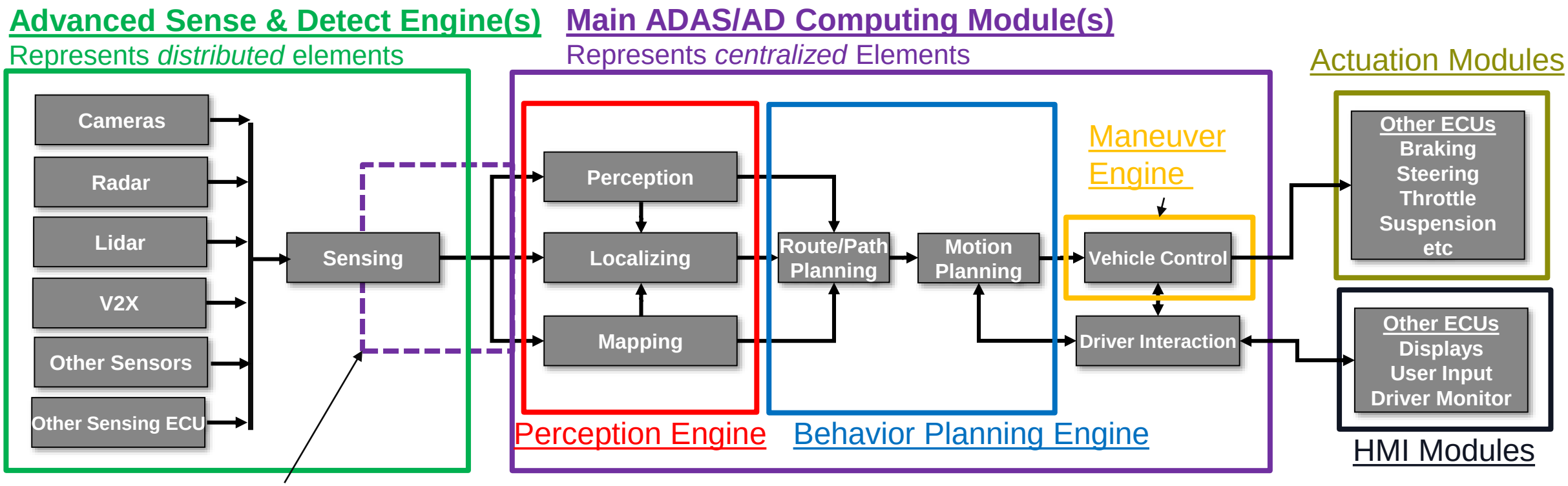
Automated Driving System Functional Diagram



Some Sense & Detect Processing may be done in Main ADAS/AD Compute Module

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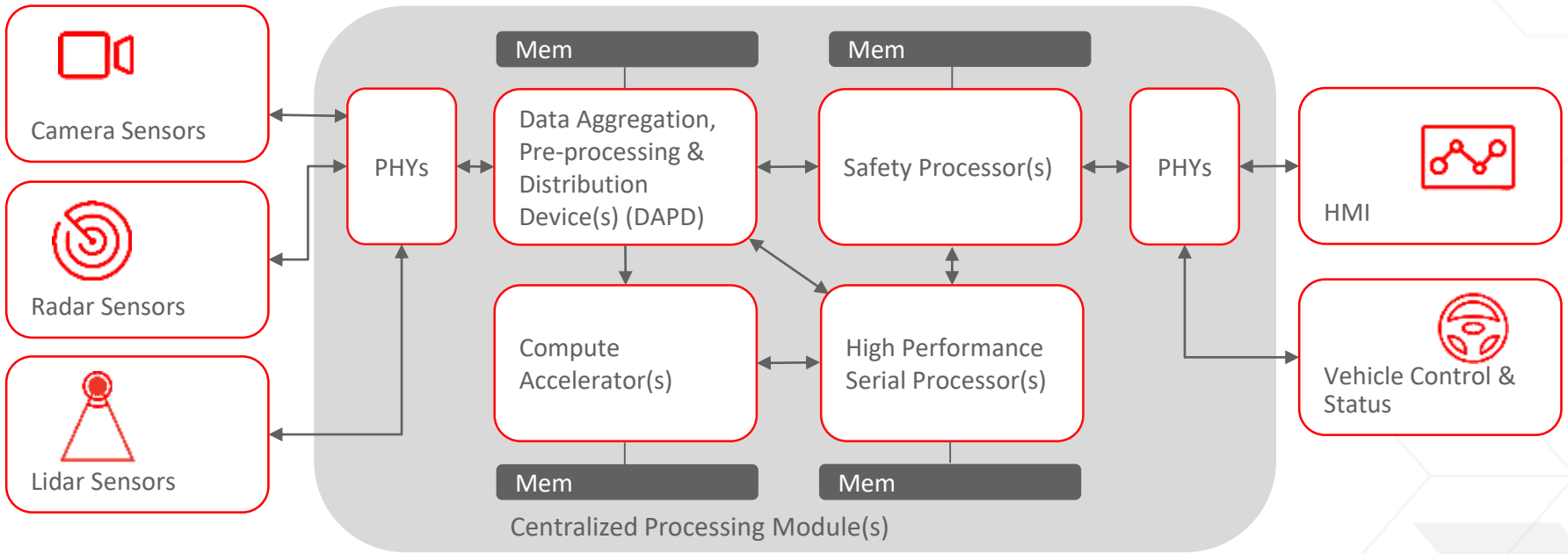
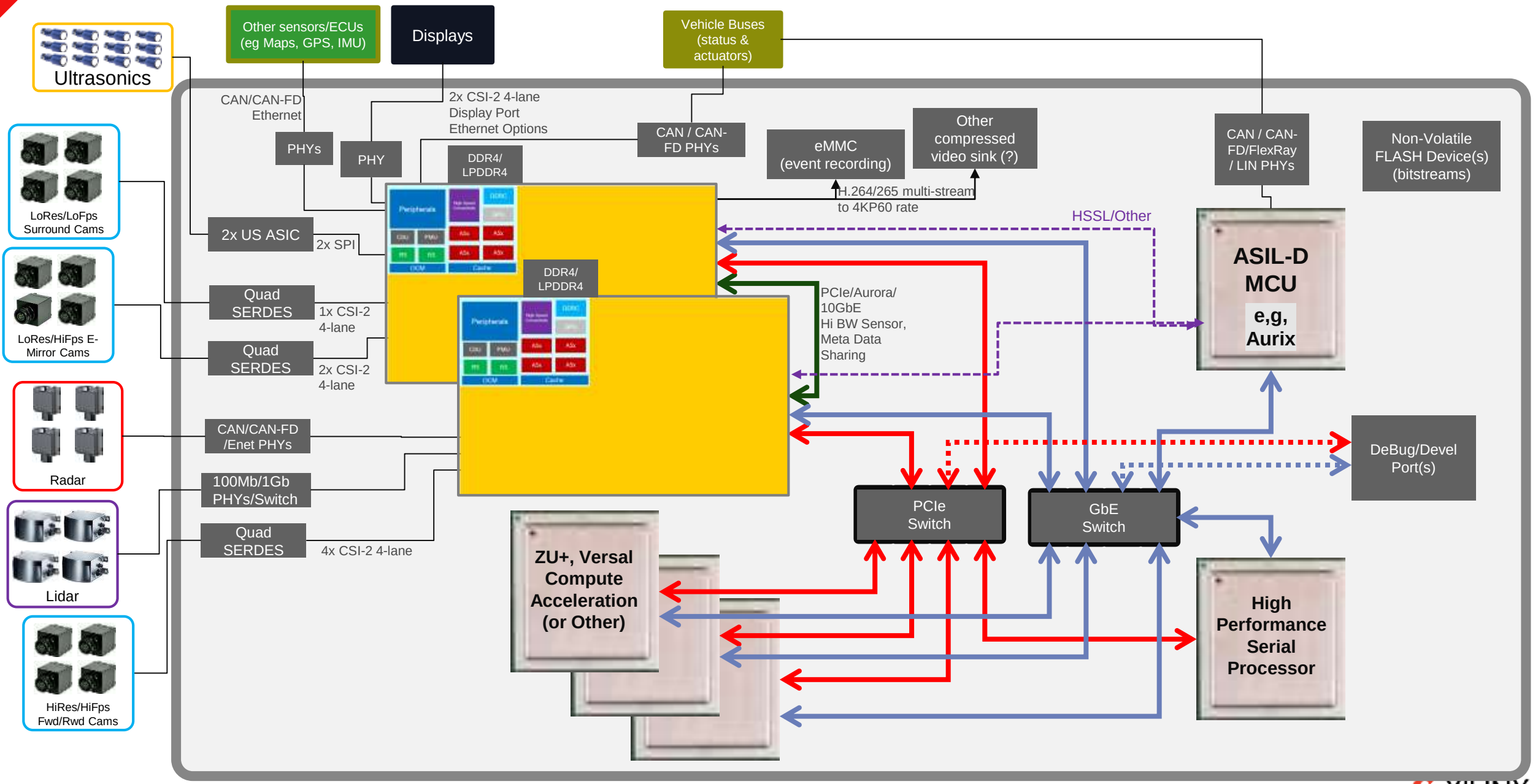
AD Central Module Processing Element Architecture



- **A centralized AD processing module is commonly comprised of a *heterogeneous set* of processing element types:**
  - Data Aggregator, Pre-Processor and Distributor
  - High Performance Compute Processor(s)
  - Computational Accelerators
  - Safety Processor(s)

AD ECU Architecture



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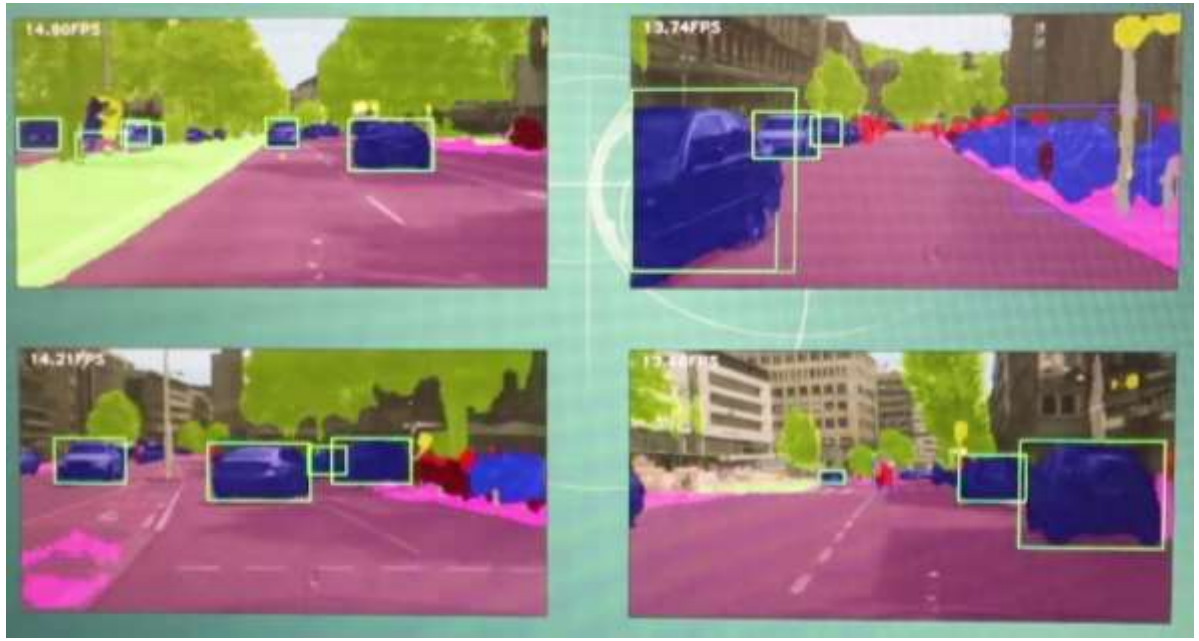
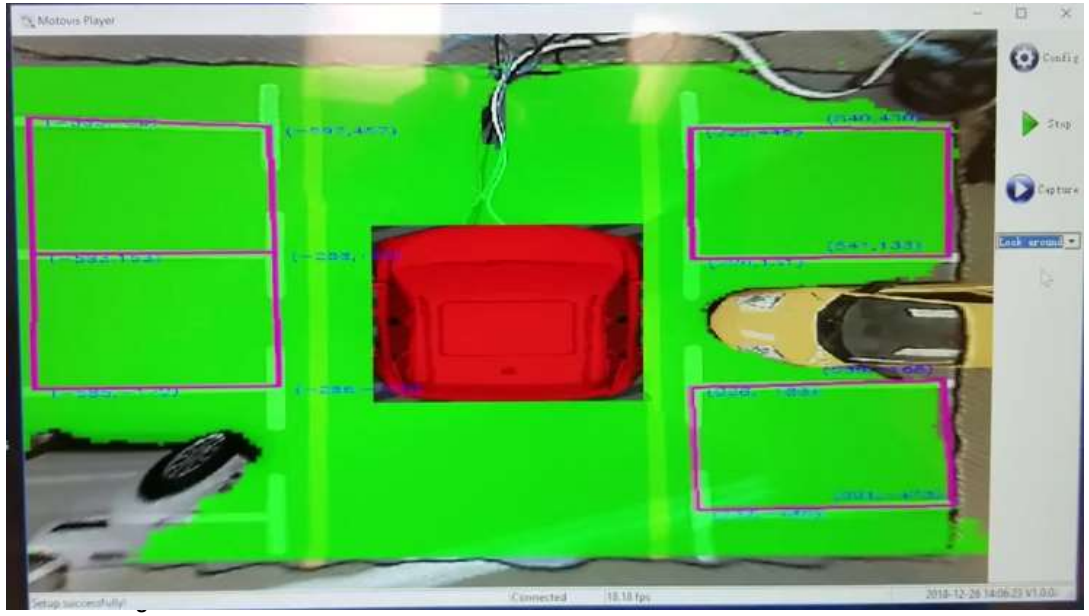
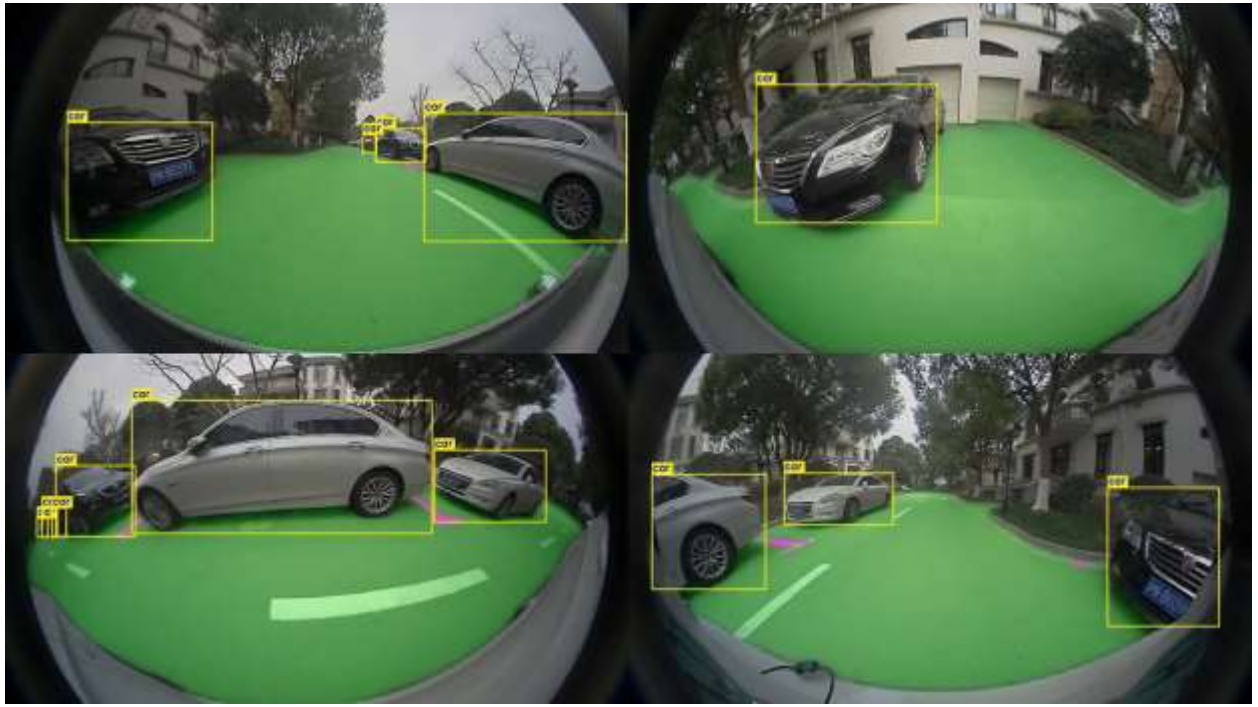
Multi-camera Central Module AI Processing in XA







Summary

- AI / ML being broadly adopted into a variety of Automotive Applications
- Xilinx Automotive devices offer unique advantages in ML inference (e.g. DAPD integration, power, HW programmability for next generation innovations, etc.)
- Dynamic Function Exchange is a unique capability which efficiently enables bundles of mutually exclusive features in a minimized piece of silicon area
- Xilinx Automotive team is eager to discuss your application with you.