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Getting Started with Versal

Software Application Engineer
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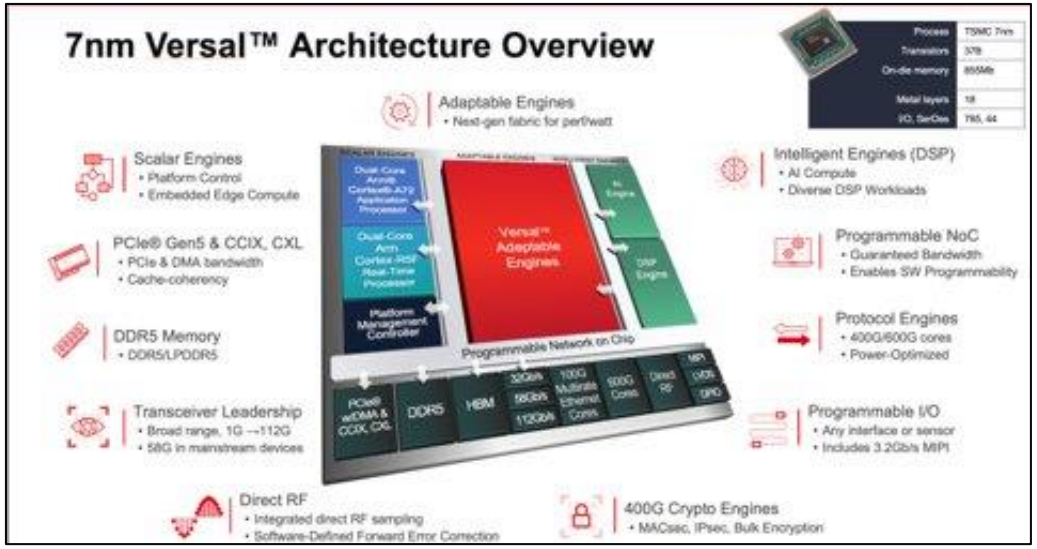
Outline

- ACAP architecture and methodology
- Versal design flows overview
  - Traditional hardware design
  - Platforms
    - Fixed
    - Extensible
- Versal specific IP
- Simulation and Debug Flows
- Programming

Versal Adaptive Compute Acceleration Platform (ACAP) Overview

- Revolutionary architecture designed to be completely SW programmable:
  - Shared DDR through NoC (no PS DDR)
  - PL Configuration through PMC
  - Debug through PMC
  - System Monitor through PMC
  - SEU through PMC (no more SEM IP)
  - CFI, AXI, NPI interfaces vs. CFI only
  - DRP (GT/MMCM ports) replaced with APB (PS<>AXI)
  - PCIe / CPM / GT-based IP sharing methodology (in new quad)
  - AXI interface for all Hard IP and Soft IP
  - SW-driven AIE processor (vs. HW design w/ DSP block)



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System Design Methodology – Vivado Flow

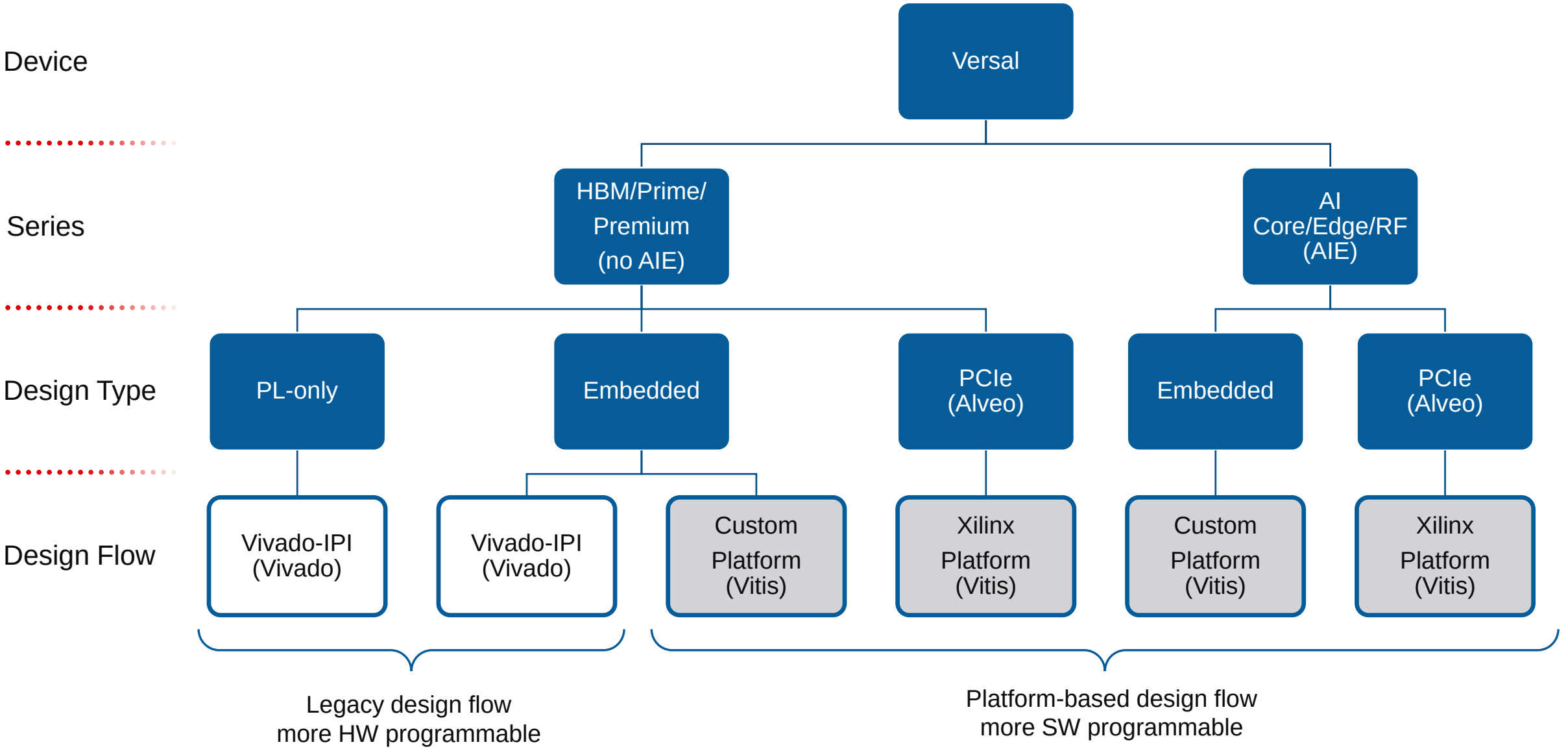
Paper Algorithm	Traffic Analysis	Data Flow Modelling (IPI)	Data Flow Simulation	Power Estimation & Analysis	System Simulation	Synthesis & Implementation
Develop a paper mapping of algorithm/ application to Versal	• Capture traffic flow for NoC • Static analysis • System C simulation	• **Connect:** traffic generators, memories, performance monitors • **Configure:** traffic generators, NoC connectivity, QoS requirements • **Elaborate**: Design and export netlist	• System Verilog simulation • Gather and analyze statistics from performance monitors	Leverage XPE with output from IP Integrator for accurate power analysis	• Full system simulation; replacing traffic generators • Co-simulate with PS VIP and PL blocks	• Take completed design through back-end tools • Timing Closure • PDI Generation

Leverage These Steps

Design Flows

Versal Design Flow

- PMC is required design component for all the flows
- PLM (PMC software) provided by Xilinx



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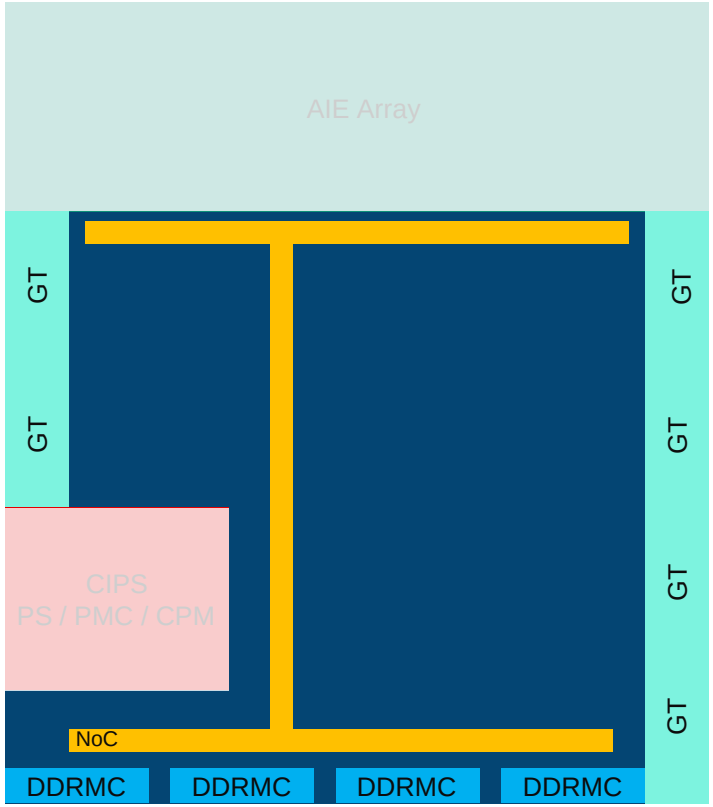
Versal Design Flows (Vivado only)

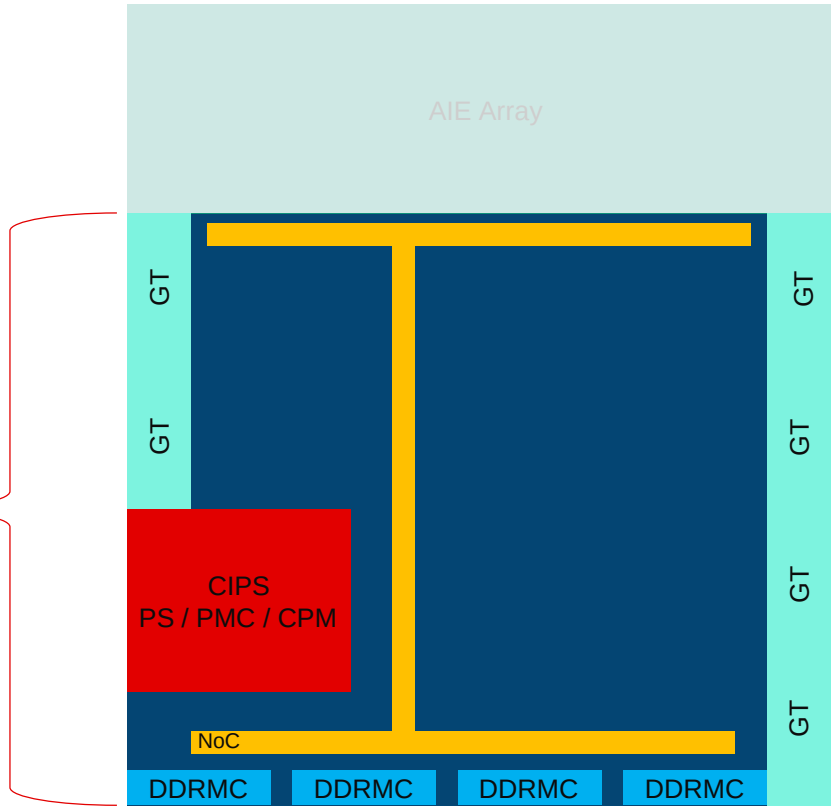
- Hardware Design Flow
  - Design uses fabric (+ NoC, DDR, GT, PCIe)
  - Tools:
    - Vivado to create the PDI directly
  - CIPS must be included in the design
  - IPI will play a larger part in your design process



Versal Design Flows (Vivado to Vitis)

- Traditional Embedded
  - Fabric + PS
  - Tools:
    - Vivado to create a fixed platform (XSA)
    - Vitis to program the PS

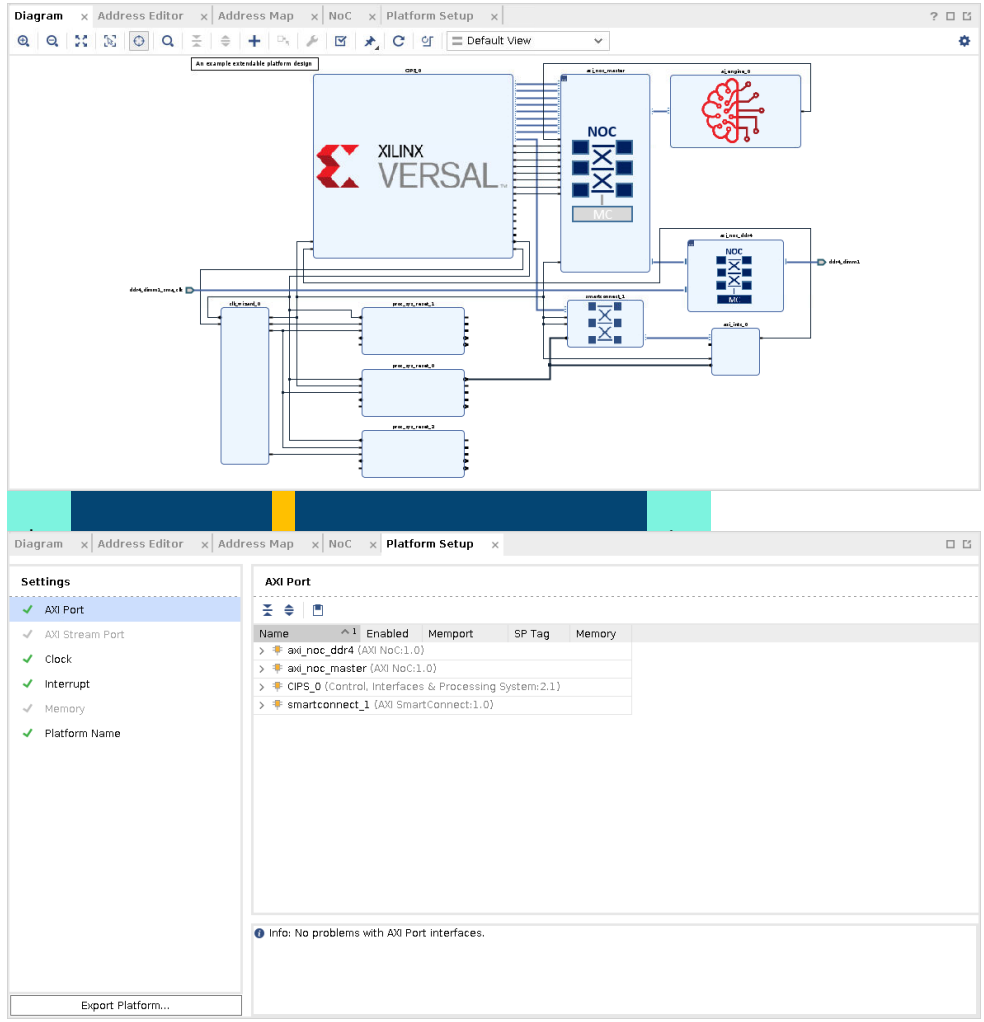
write_hw_platform -fixed



Versal Design Flows (Vivado and Vitis)

- Acceleration
  - Fabric + PS + AIE
  - Tools:
    - Vivado to build extensible platform
    - Vitis to program, PS, AIE, PL accelerators

write_hw_platform



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Vitis adds PL/AIE kernels and PS software

VIVADO HLx Editions

Extensible Platform (XSA)

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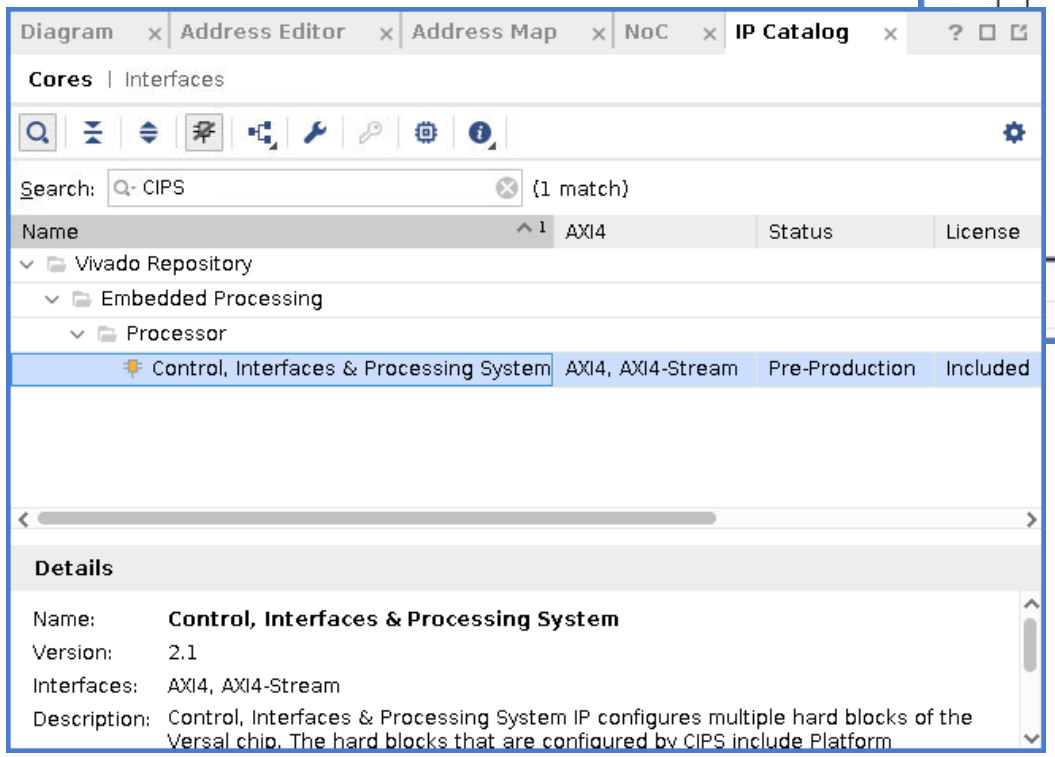
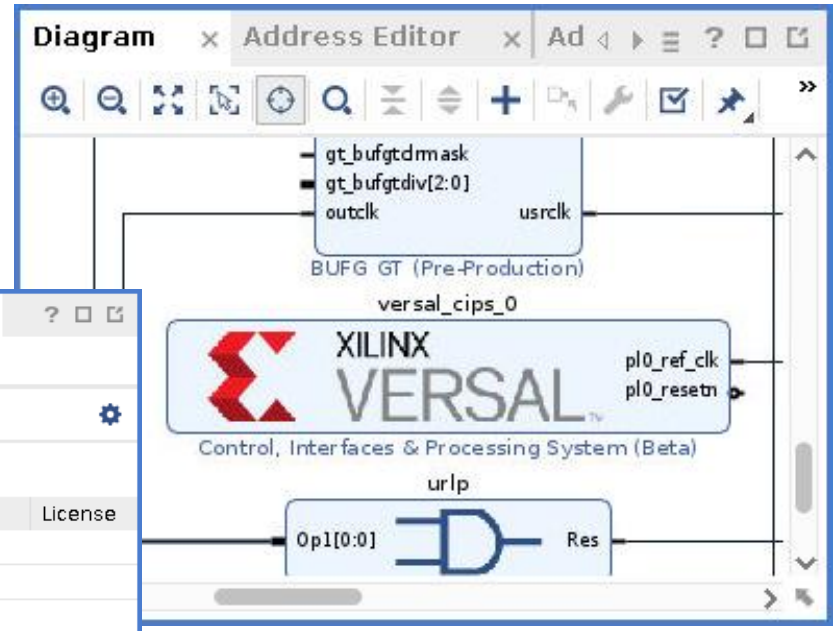
Versal Specific IP

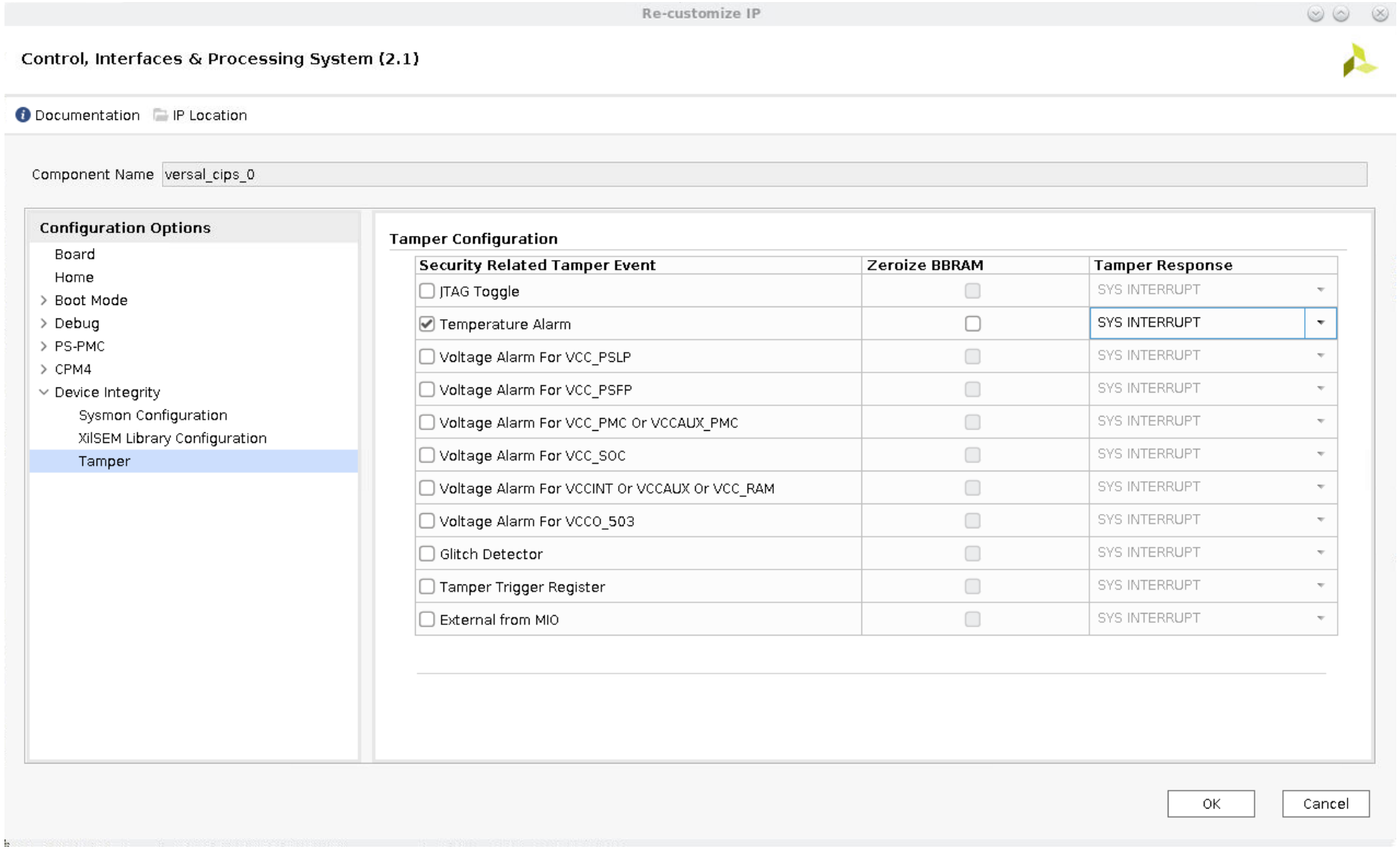
Versal IP- CIPS

- CIPS- Control, Interfaces, and Processing System
- One IP contains covers many functions
  - PS
  - PMC
  - Debug
  - NoC
  - CPM
  - System monitors
  - SEM
  - Tamper



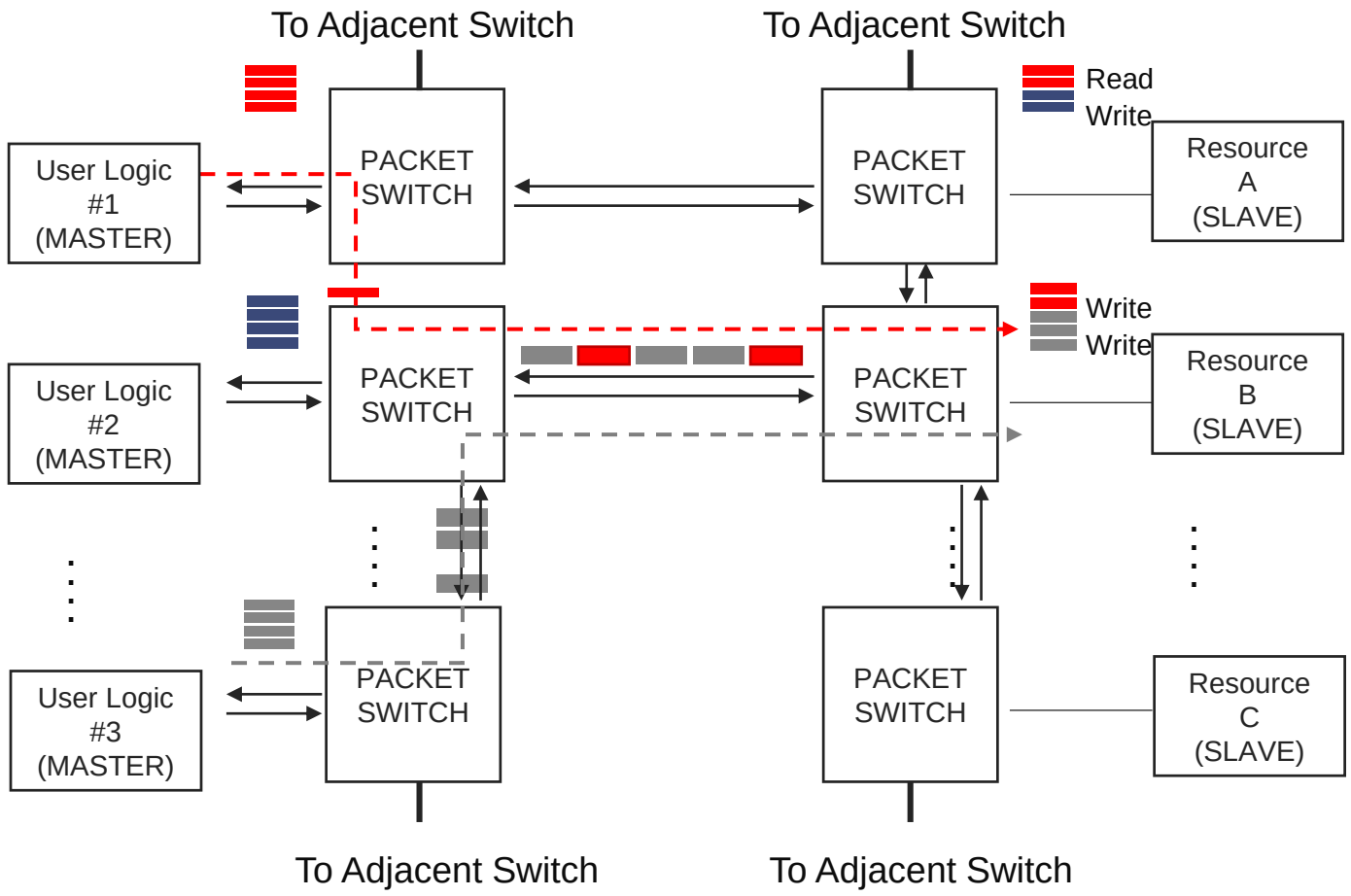


Versal IP- CIPS Configuration



Versal IP – NoC (Network on Chip)

- Shared connectivity to move packetized data around the SoC
- Facilitates communication between
  - Processing system
  - DDR
  - AI Engines
  - Programmable logic
  - Any other hardened components



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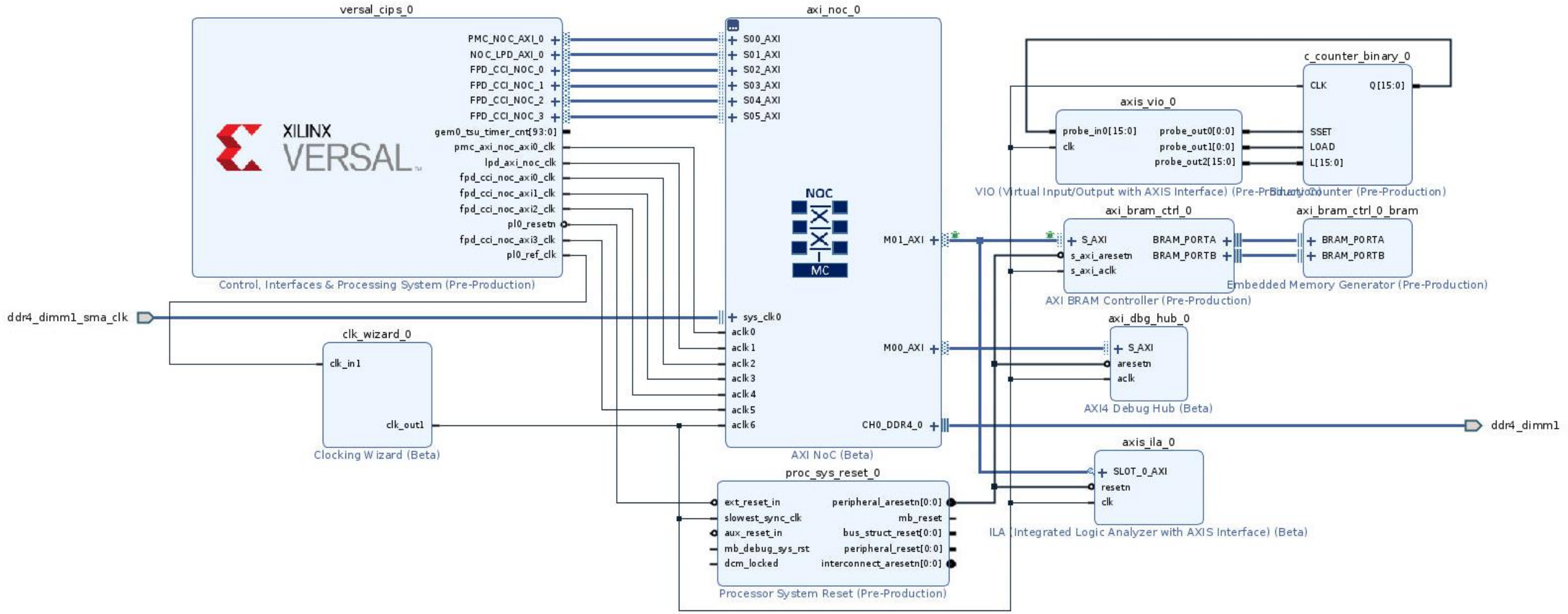
Versal IP – Using the NoC (Network on Chip)



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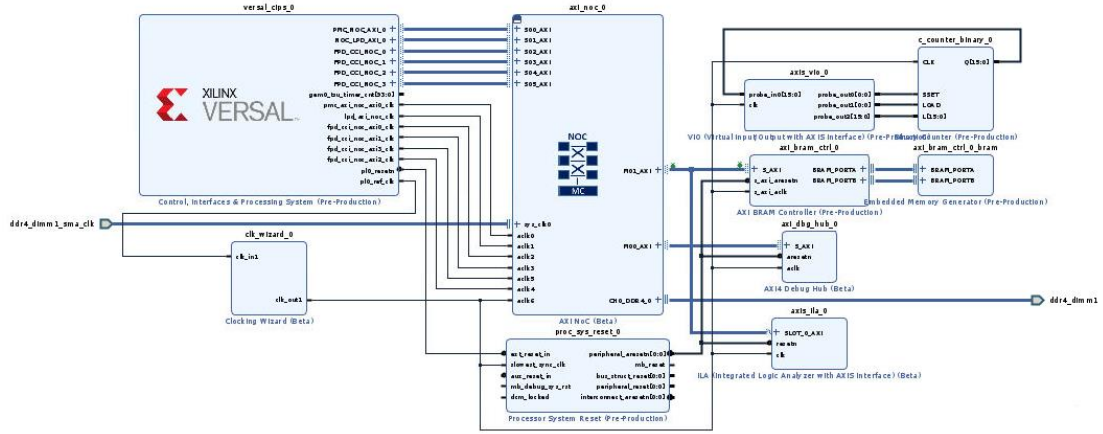
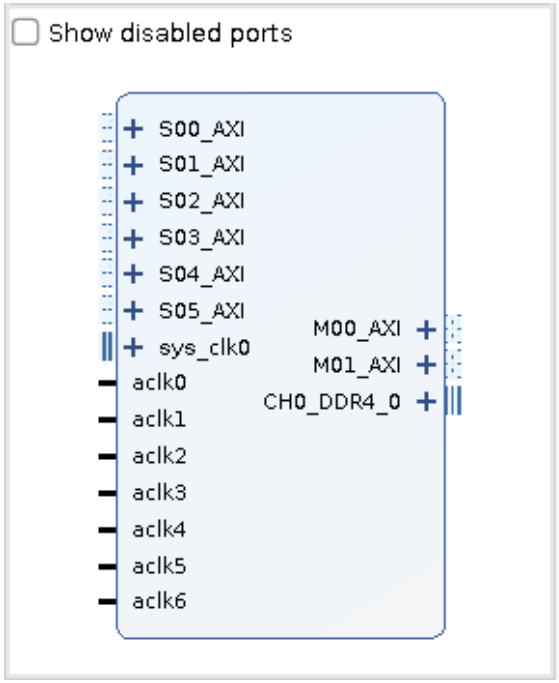
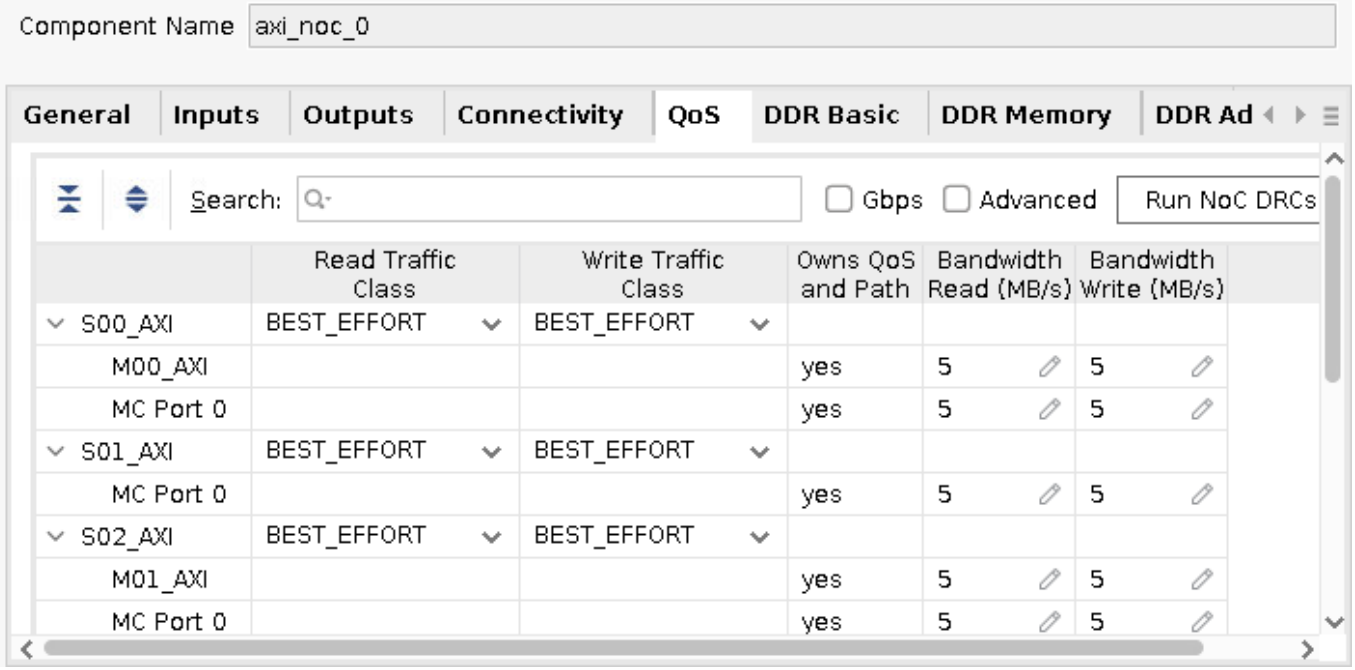
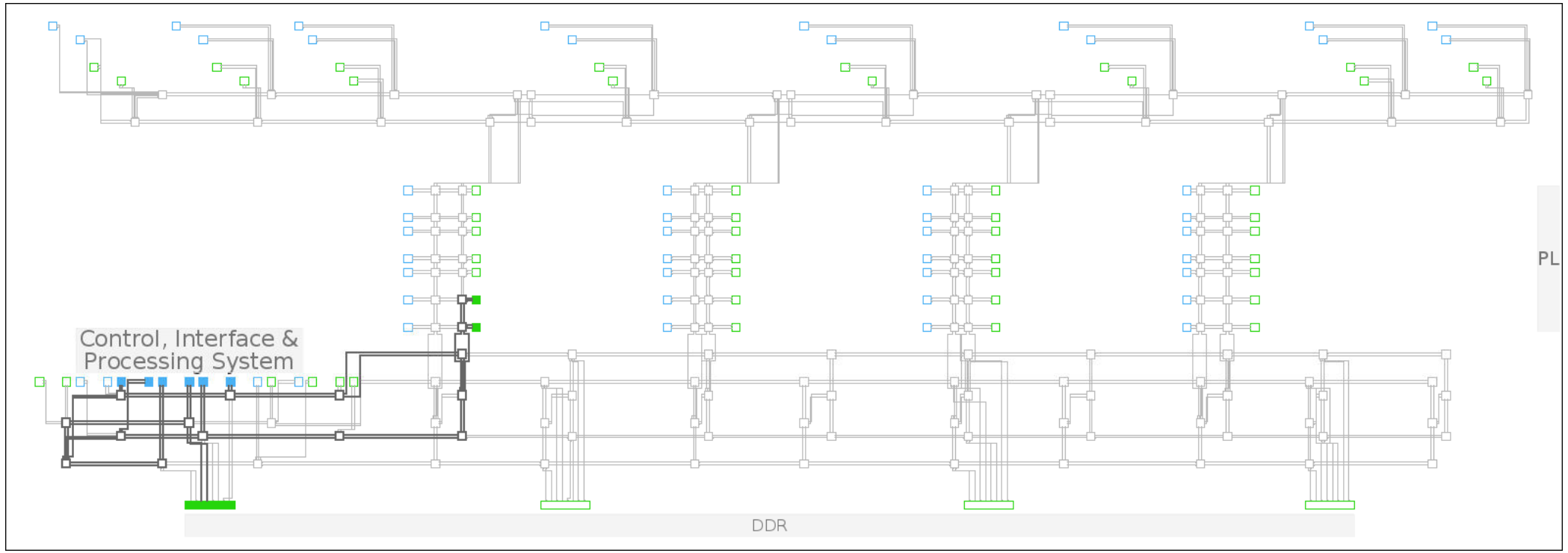






Versal IP – NoC (Network on Chip)

- The NoC physically spans the SoC
  - Blue NMUs (NoC master units)
  - Green NSUs (NoC slave units)
  - White NPS (NoC packet switch)



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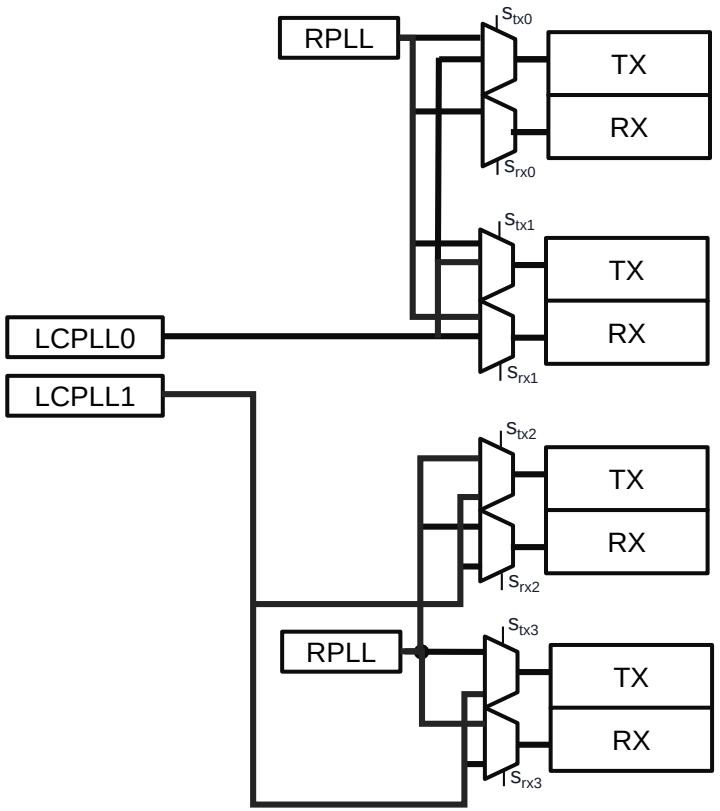
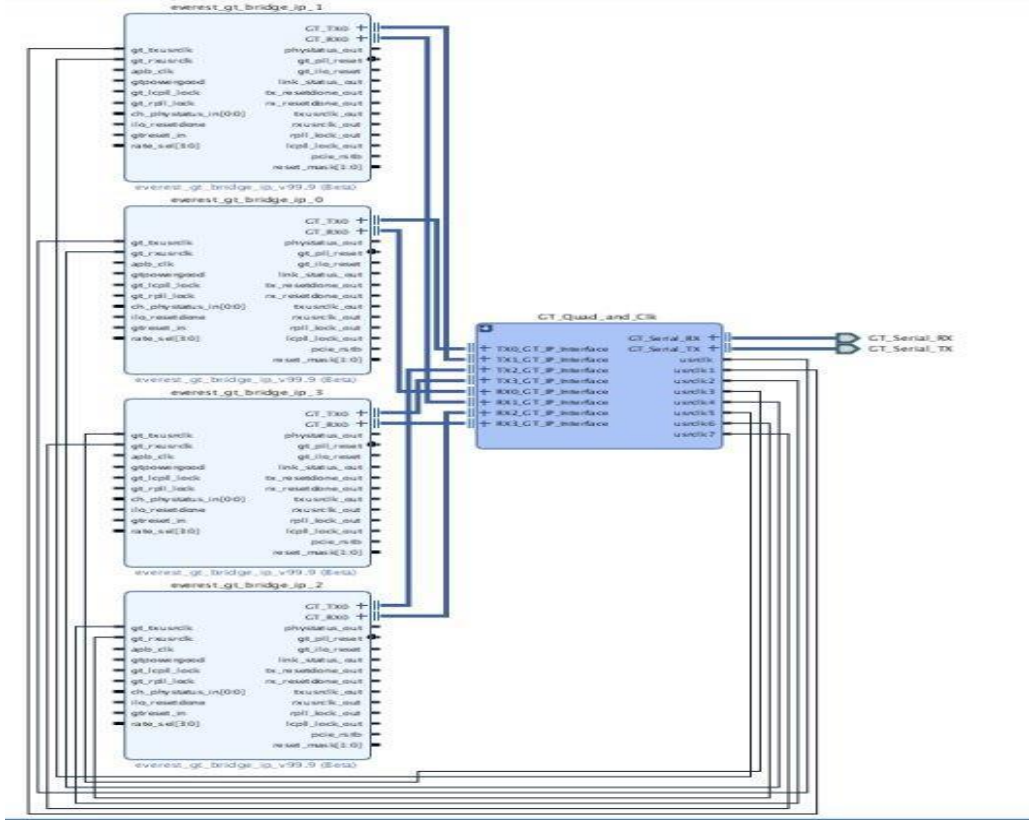
GT Wizard Features

- GTs inherit values from the parent IPs
  - Makes it easier to split up the GT Quad
  - Configure the GT through the parent without ever having to open the Wizard
  - Parent IP is packaged without the GT
- Flow is primarily IPI based
  - RTL flow is possible but multi-IP flow not integrated into wizard
  - Allows more intelligent sharing of PLL resources, validation of use cases at run time
- Pin Planning now part of Vivado, not IP generation
  - New GT tab similar to the Memory flow
  - Only full Quad pin planning allowed, no lane swapping allowed



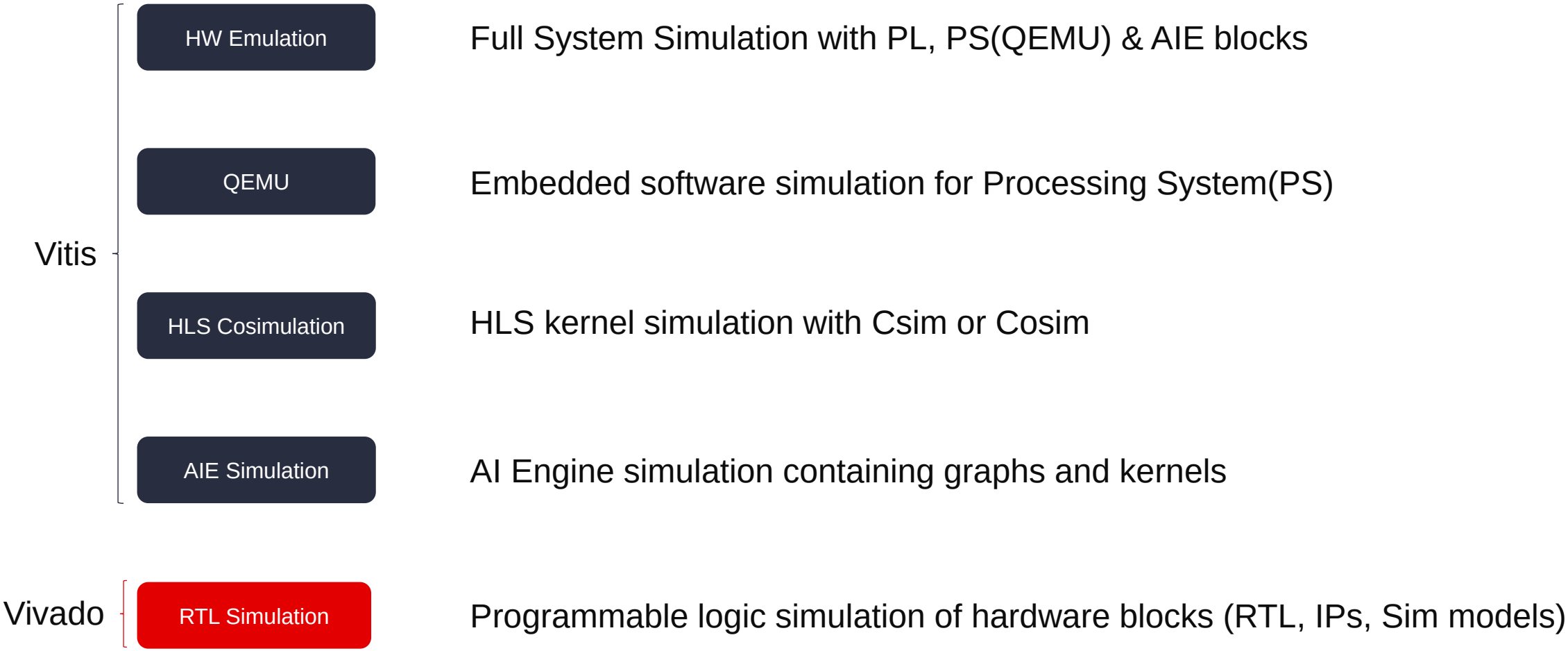
GT Wizard Features

- Resource sharing is now a lot easier
  - Split up the Quad as you see fit
  - Let the tools give you a best fit
- Simplify rate changes
  - GT wizard can generate multiple ELF configuration files through GT Quad customization options
  - DRP-like functionality is natively incorporated into the Quad (APB AXI bus)
- Bridge IP
  - For third party solutions
  - Acts as an interface between GT Quad and custom logic



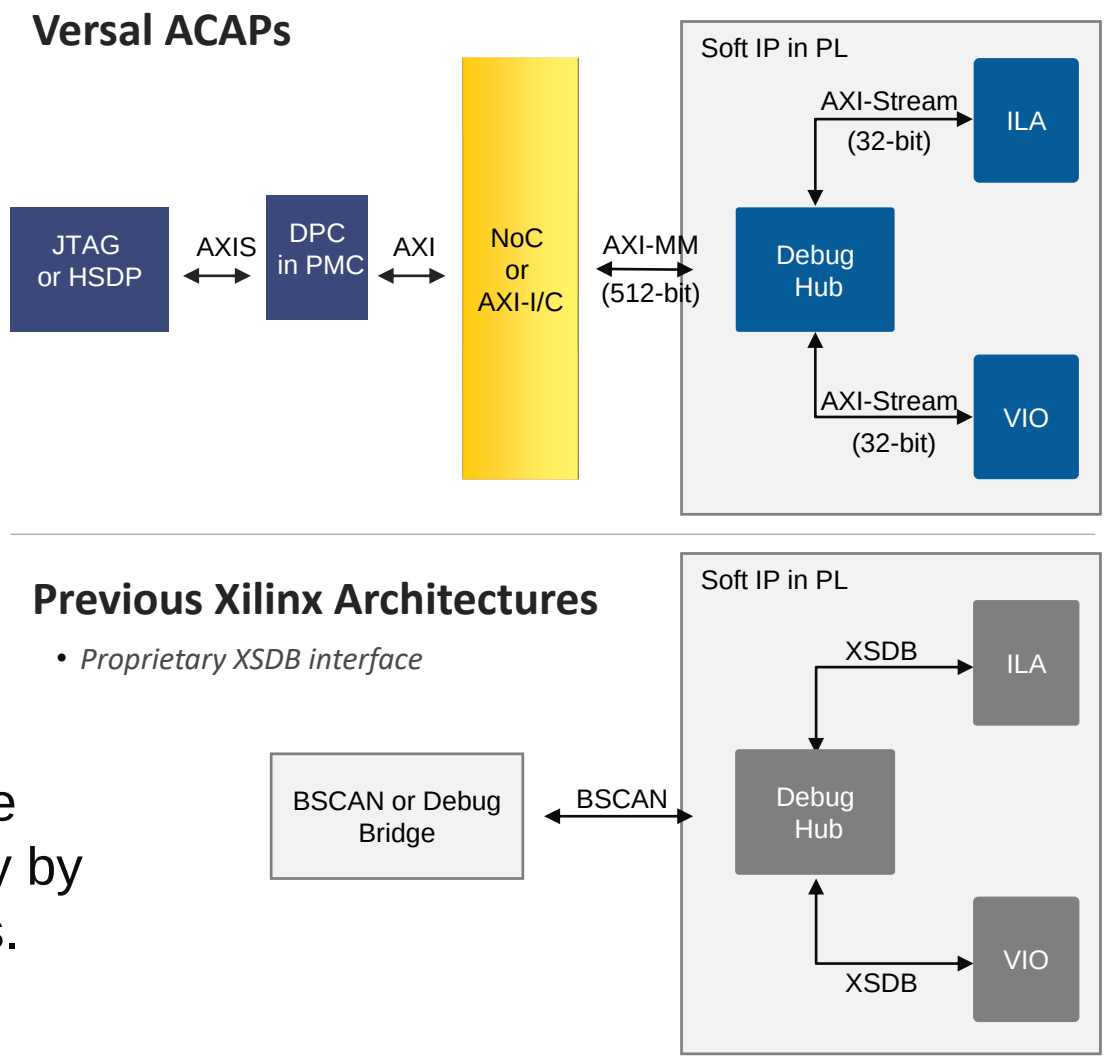
Simulation and Debug

Simulation



Versal IP - HW Debug

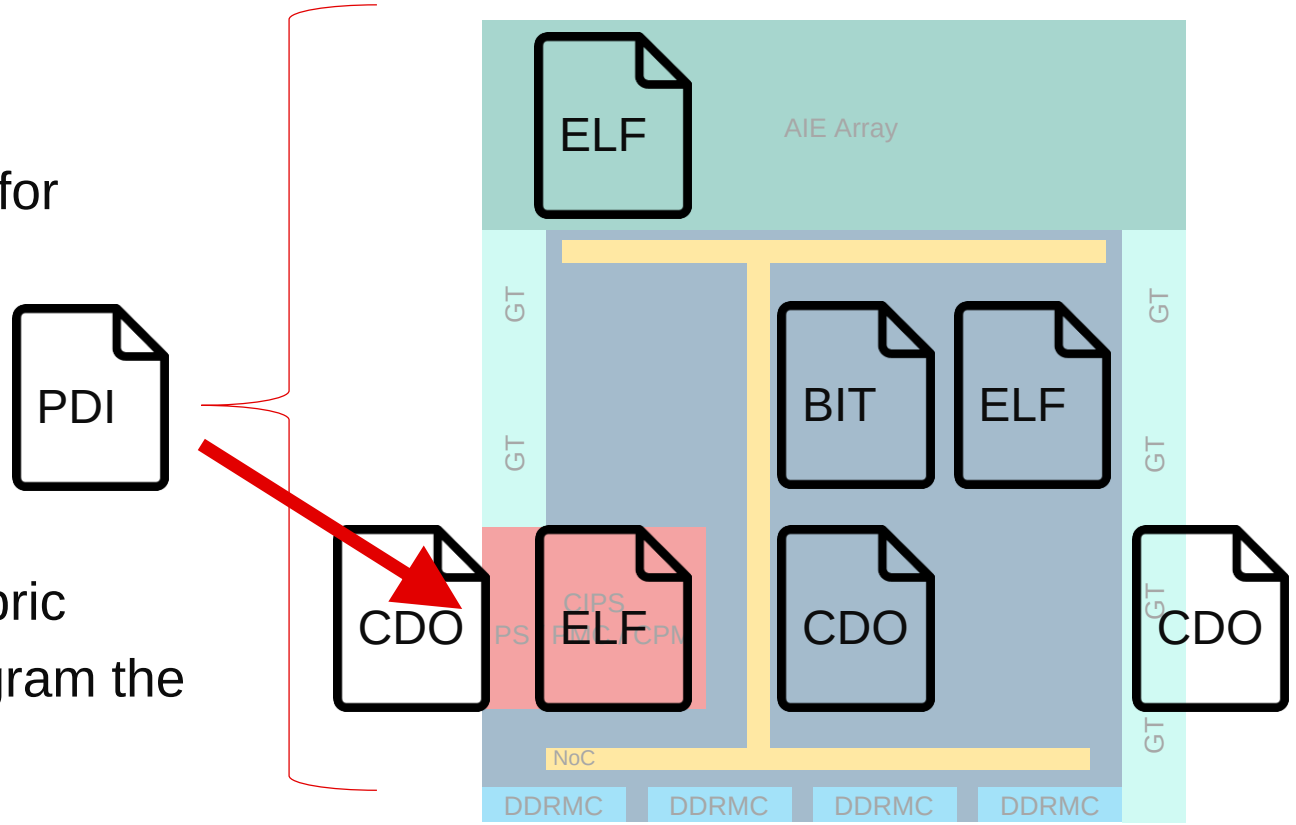
- Versal Debug Cores Use AXI-Streaming Infrastructure
- Familiar Debug IP
  - Integrated Logic Analyzer (AXIS-ILA)
  - Virtual Input/Output (AXIS-VIO)
  - Memory Calibration Debug Interface
- New Debug IP
  - PCI Express Link Debug
  - Hardened Integrated Bit Error Ratio Test (IBERT)
- HSDP (hardened part of XPIPE)– performance benefits – loading the linux kernel into memory by JTAG is slow (12.8Gb Smart link plus 10Gb vs. JTAG 100Mb)



Device Programming

Programmable Device Image Demystified

- A PDI is essentially the Versal equivalent of a “bitstream”
- PDI contents
  - CDO files – Configuration register writes for hardened IP
  - BIT file – Fabric CFrame data
  - ELF files – AIE/PS/uB software
- PMC uses
  - Cframe interface (CFI) to program the fabric
  - NoC programming interface (NPI) to program the NoC interconnect
  - AXI interface to load the AIE



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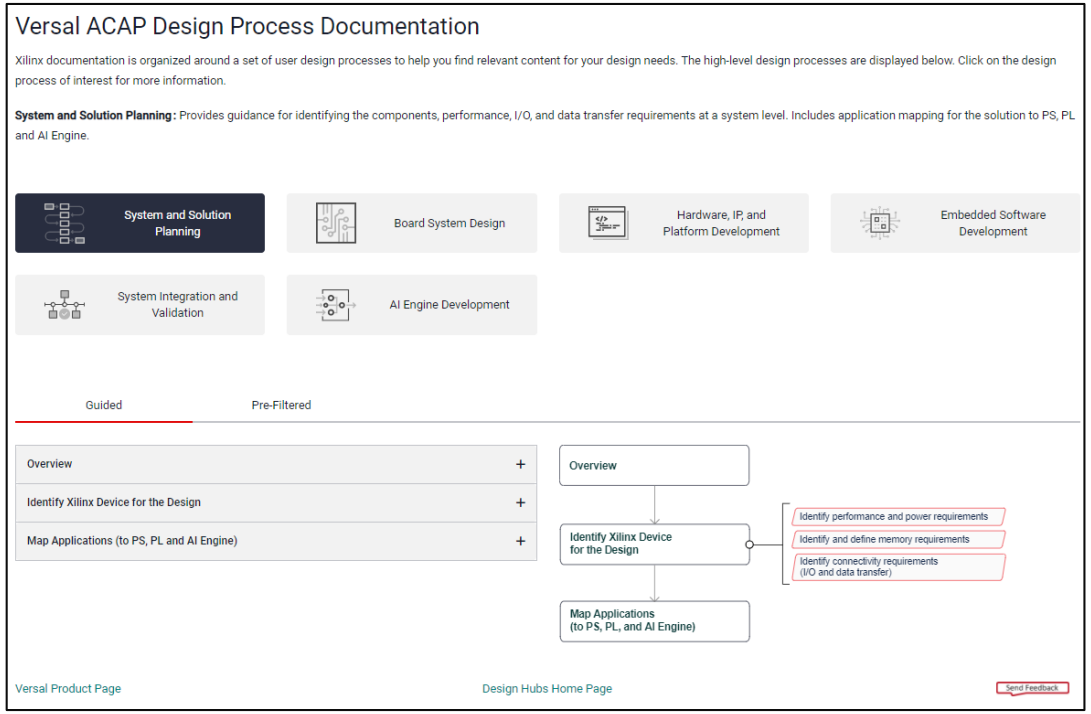
Conclusion / Resources

- Three recommended design entry flows used for Versal
- New Versal Hard IP
- Simulation and debug
- PDI
- Resources
  - AM011 – Versal Technical Reference Manual
  - UG1273 – Versal ACAP Design Guide
  - PG352 – CIPS IP
  - PG313 – NoC IP
  - PG331 – Transceiver Wizard
  - Versal online documentation



https://www.xilinx.com/support/documentation-navigation/design-process/system-and-solution-planning.html