XILINX

Model Composer and System Generator

Xilinx Add-on for MATLAB® & Simulink®

George Wang
Sr. Product Marketing Manager
Xilinx SW & AI

Agenda

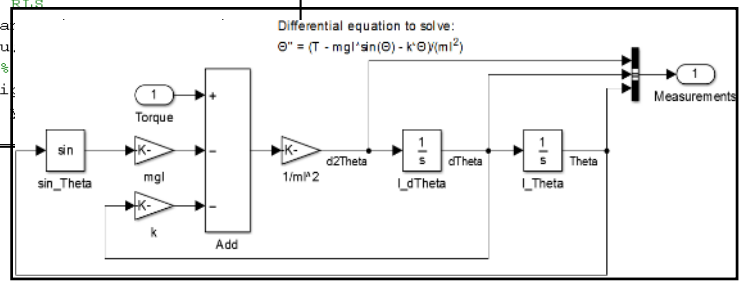
- Introduction
- Add-on for MATLAB & Simulink Capabilities
  - Modeling a heterogenous device with AI Engines
  - Design visualization
  - Verification, test bench creation and execution
- Summary

Xilinx Add-on for MATLAB & Simulink connects algorithms and system designs with FPGA, SoC and ACAP hardware

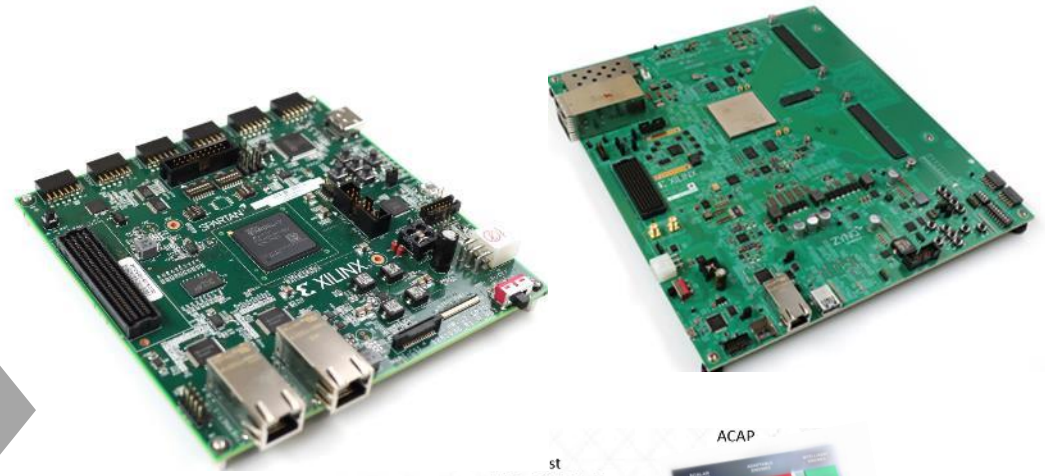
Xilinx Add-on for MATLAB & Simulink


```
for n = 1:length(rxsig)
    u = rxsig(n);  % received sample
    y = conj(weights) * u;
    if n<=length(train)
        d = train(n);
    else
        d = detect(real(y)) + 1j*detect(im
    end
    % Single-tap RLS
    Delta = 1/(la
    G = Delta * u
    e = d - y;  %
    weights = wei
    symbols(n) =
end
```

MATLAB



Simulink

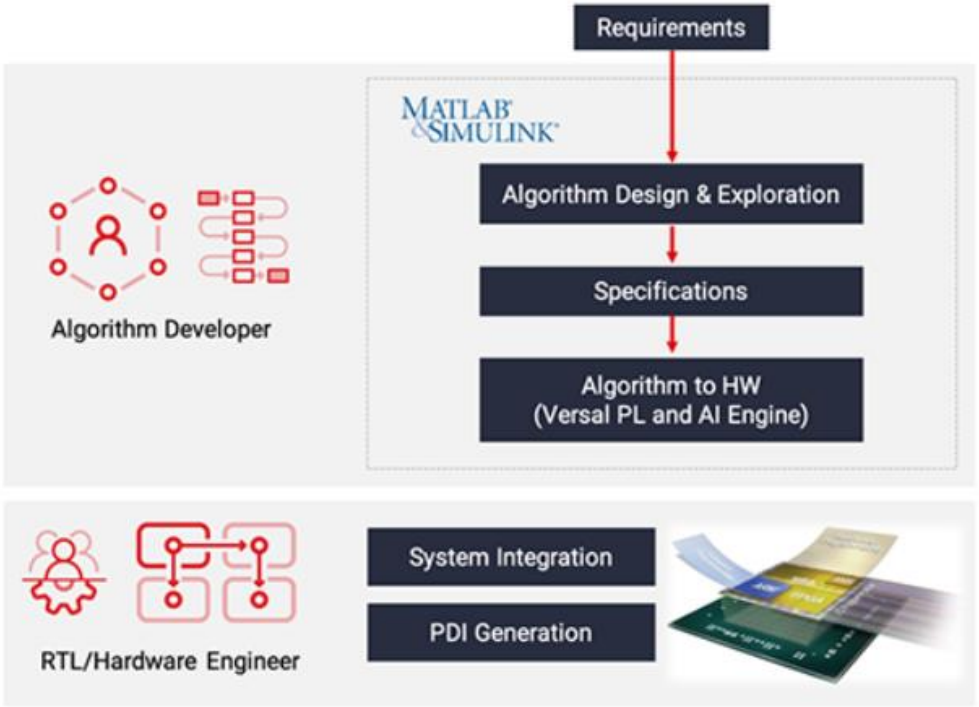


MathWorks

XILINX

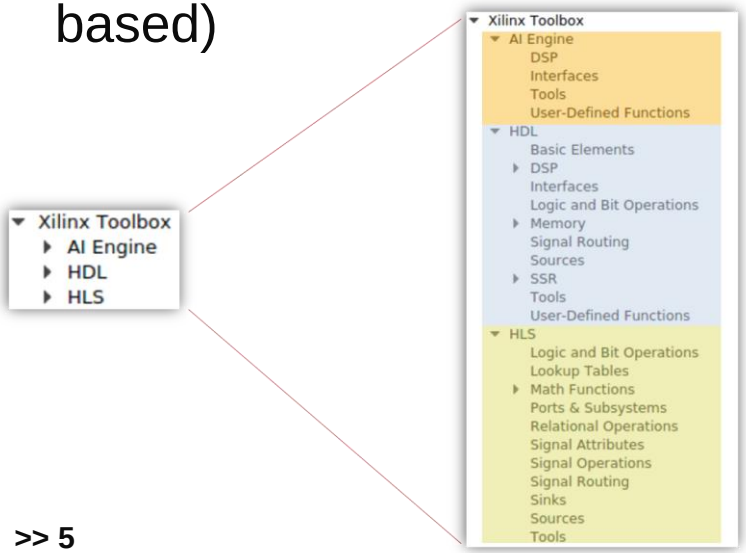
Using the Add-on for MATLAB & Simulink Design Framework, Users can

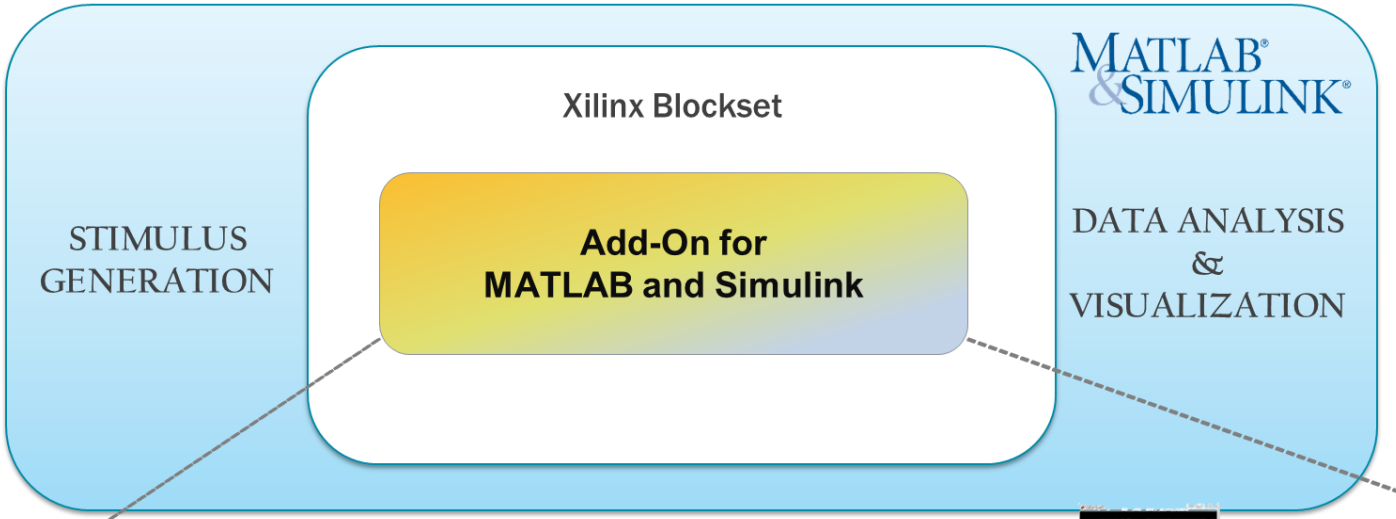
- Link designs directly to requirements
- Refine algorithms via multidomain simulation
- Collaborate better across disciplines
- Automatically generate embedded code and documentation, eliminate hand coding
- Manage changing requirements better
- Improve quality through early verification
- Finish R&D and reach production faster

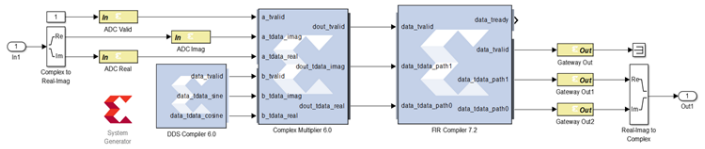


Unified Xilinx Tool for Model-Based Design: 2020.2
Add-On for MATLAB & Simulink

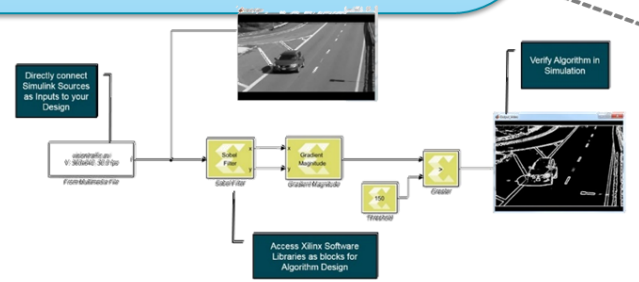
- First Release: **2020.2**
- A single tool for
  - System Generator for DSP (HDL based)
  - Model Composer (HLS based)
  - Model Composer (AI Engine based)





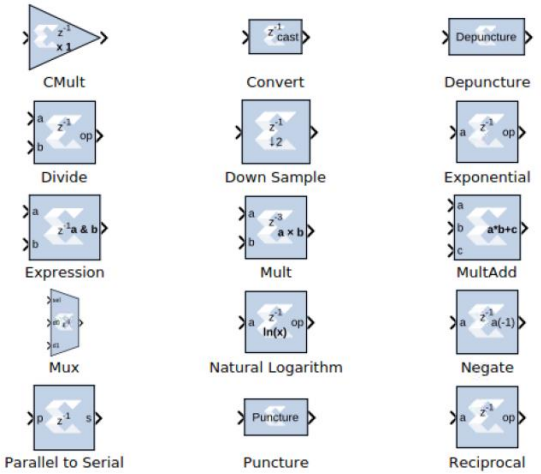


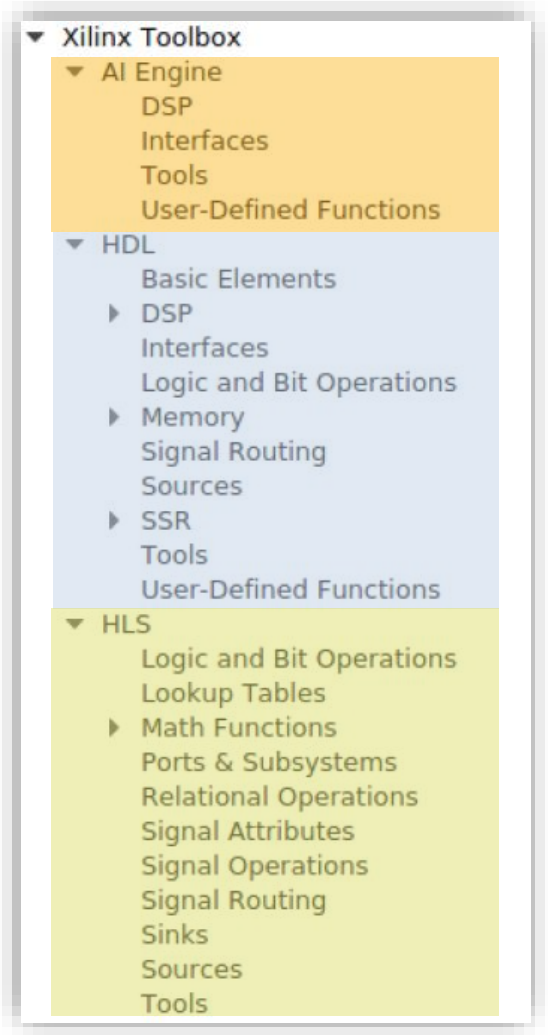
RTL-level design within Simulink

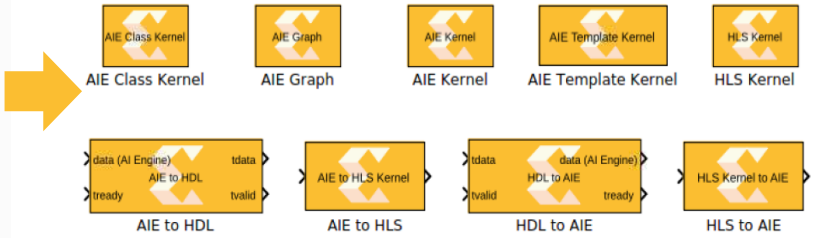


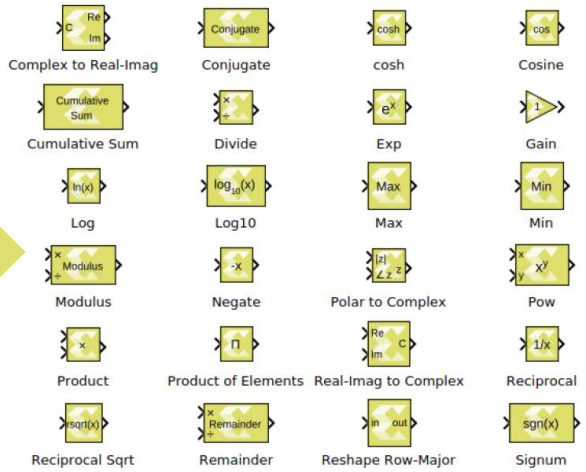
HLS Design in Simulink

Single Design, 2 Domains (PL & AI Engine), 3 Ways









XILINX.

Add-on for MATLAB® and Simulink®

- Versal AI Engine design
  - Automatically generates the SDF (static data flow) graph
  - Simple HDL co-simulation support
  - Native support for DSPLIB components
  - MC simulation mode is bit accurate (Simulation-SW, orders of magnitudes) **100x** faster than (Simulation-AIE, bit & cycle accurate)
- Provides a library of performance-optimized blocks for design and implementation of algorithms on Xilinx devices totaling 210 HDL, HLS, and AI Engine blocks

Customer Stories
BAE Systems Achieves 80% Reduction in Software-Defined Radio Development Time

Challenge

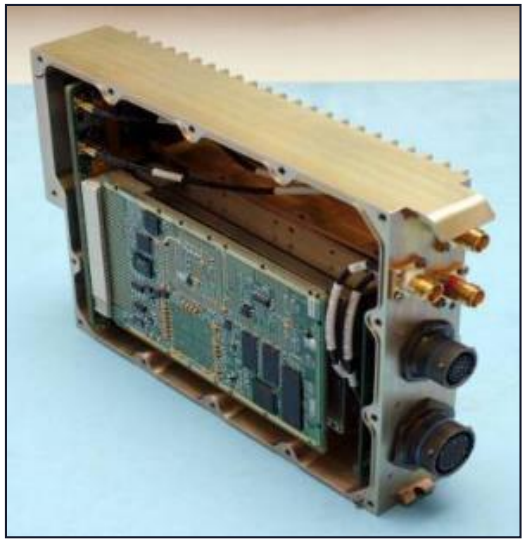
To develop a military standard SDR waveform for satellite communications

Solution

Use Simulink and Xilinx System Generator to rapidly design, debug, and automatically generate code for an
SDR signal processing chain

Results

- Project development time reduced 80%
- Problems found and eliminated faster
- Clocking and interface simplified



Custom board used in the traditional design workflow.

"It took 645 hours for an engineer with years of VHDL coding experience to hand code a fully functional SDR waveform using our traditional design flow. A second engineer with limited experience completed the same project using Simulink and Xilinx System Generator in fewer than 46 hours."

Dr. David Haessig, BAE Systems

Link to Technical Article

Customer Stories
RF Pixels Verifies Millimeter Wave RF Electronics on a Zynq RFSoC Based Digital Baseband

Challenge

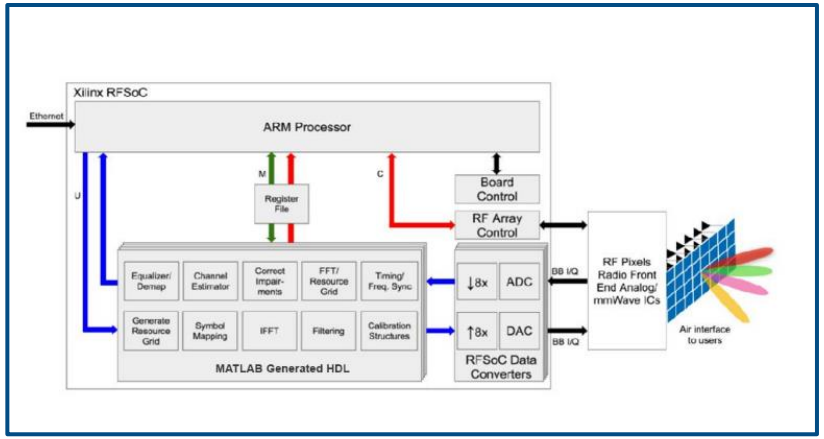
Test and demonstrate radio front-end designs that incorporate specialized RF electronics hardware and millimeter wave spectrum technology

Solution

Use MATLAB and Simulink to implement a digital baseband and deploy it to a Zynq RFSoC board for over-the-air testing

Results

- Engineering effort reduced by one year or more
- Digital baseband implementation completed by a single engineer
- Design iterations reduced from weeks to days



Digital baseband implemented in HDL, used to verify the RF Pixels radio front end.

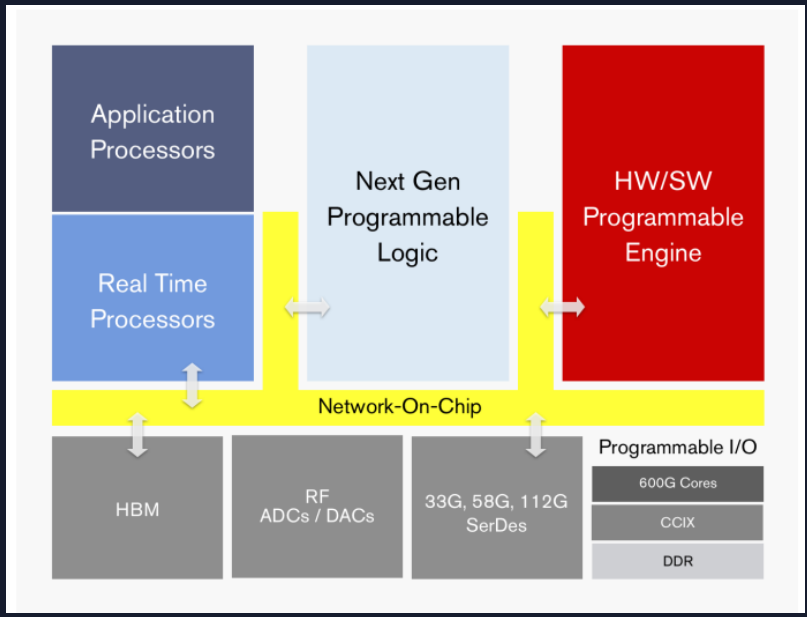
"By adapting the LTE golden reference model from Wireless HDL Toolbox and deploying it to a Zynq UltraScale+ RFSoC board using HDL Coder, we saved at least a year of engineering effort—and this approach enabled me to complete the implementation myself, without having to hire an additional digital engineer."

- Matthew Weiner, RF Pixels

Link to technical article

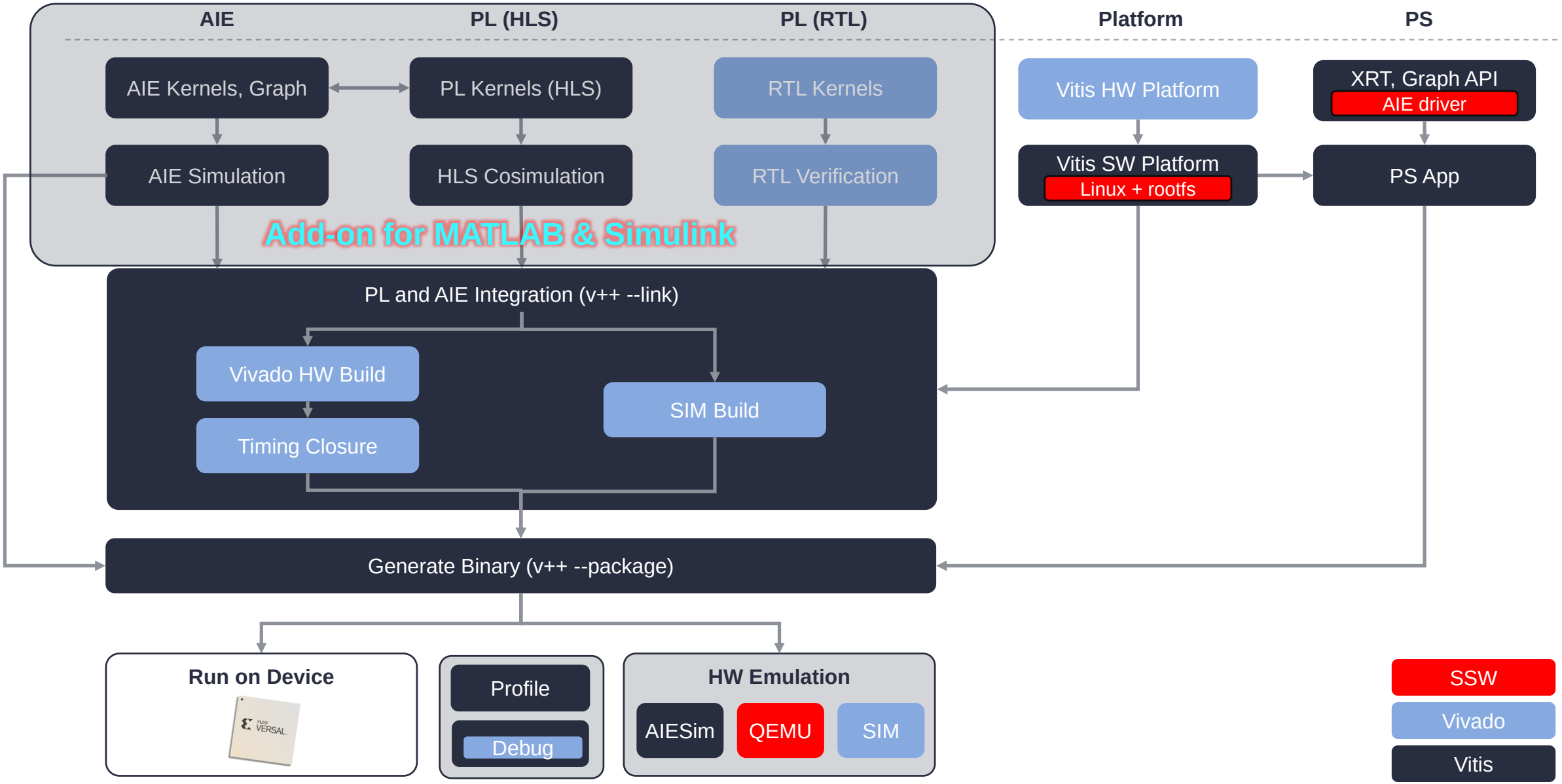
XILINX.

Modeling Heterogenous Device: Putting an AI Engine Design Together

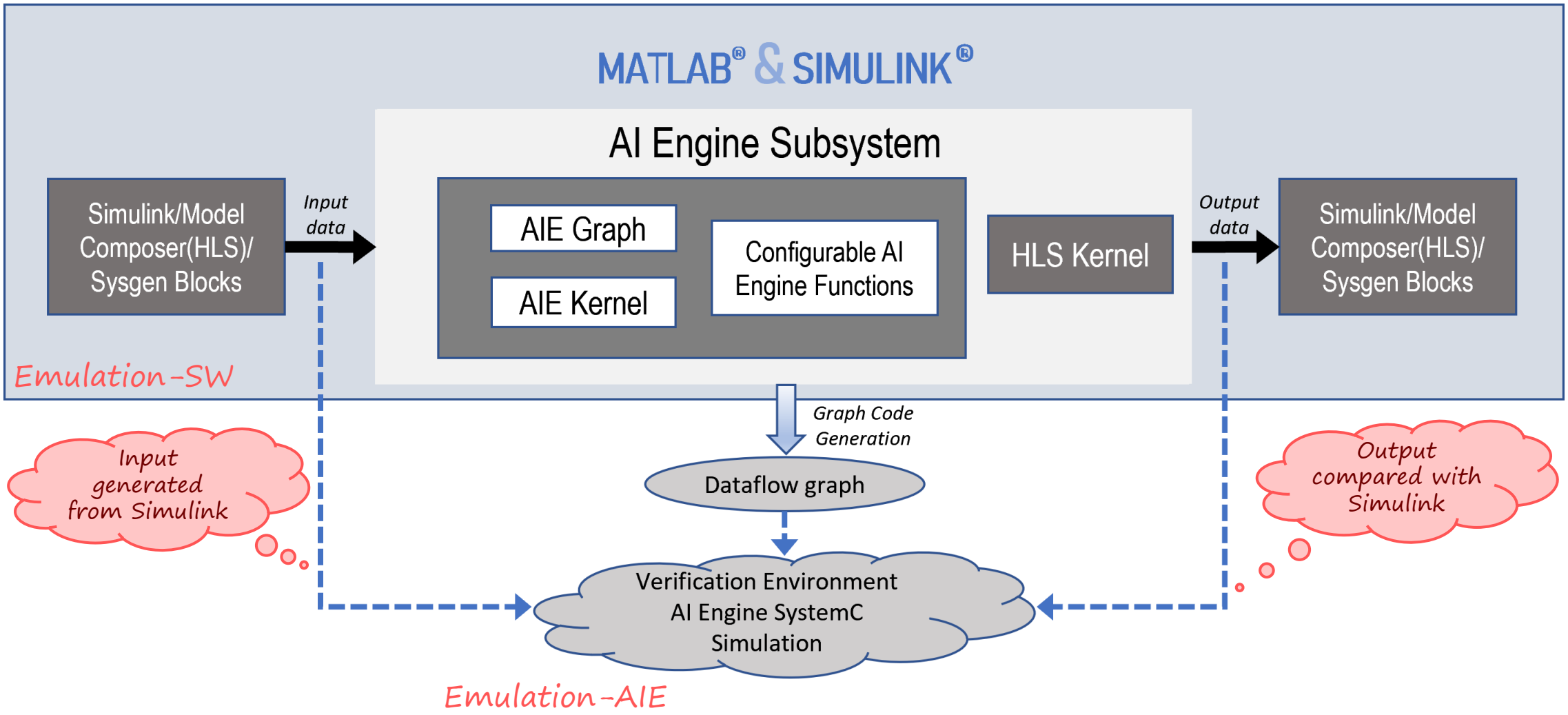


XILINX.

Vitis 2020.2 Flow for Versal AI Engine



AI Engine Domain Design



XILINX.

Demo: Importing AI Engine Kernels

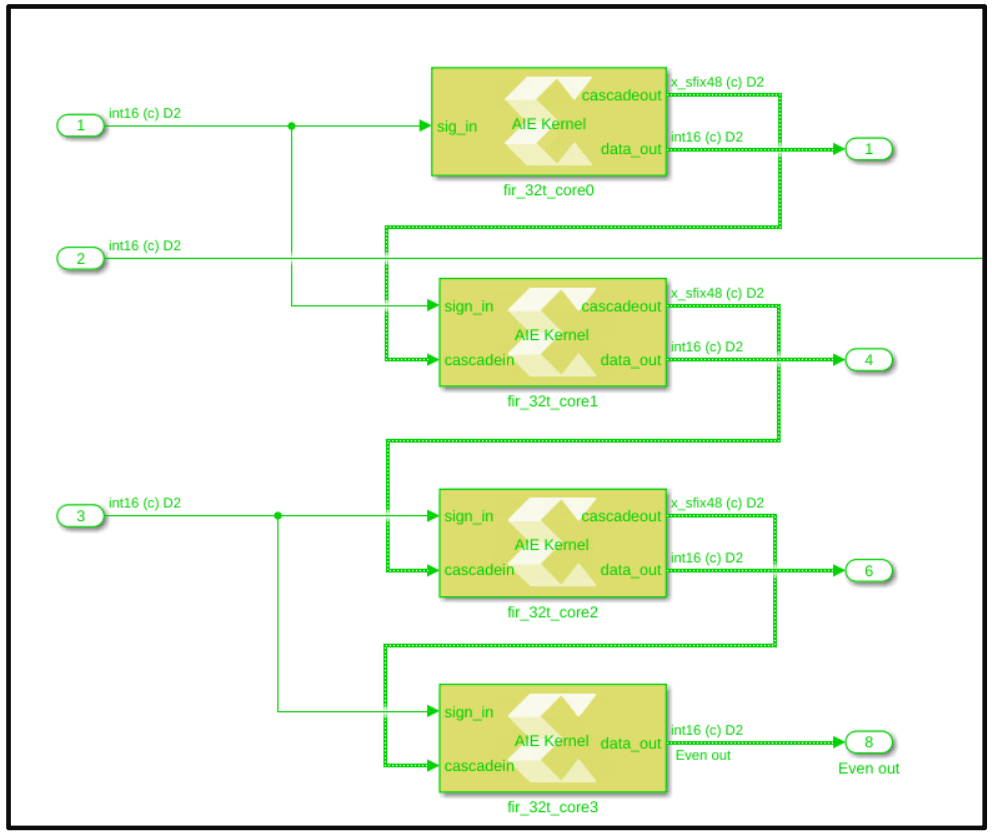
XILINX.

Visualization

Visualization (connectivity)

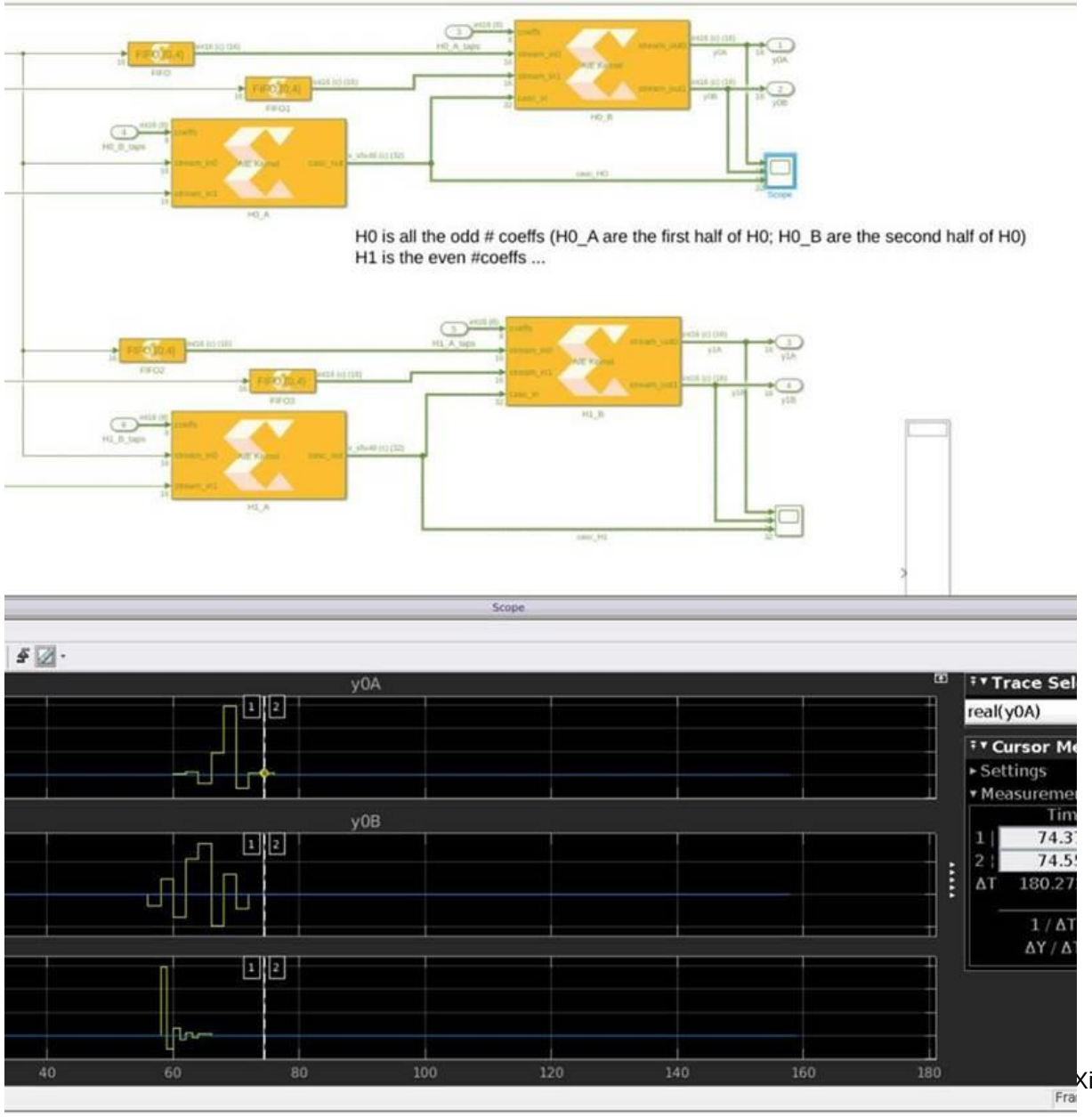
graph.h

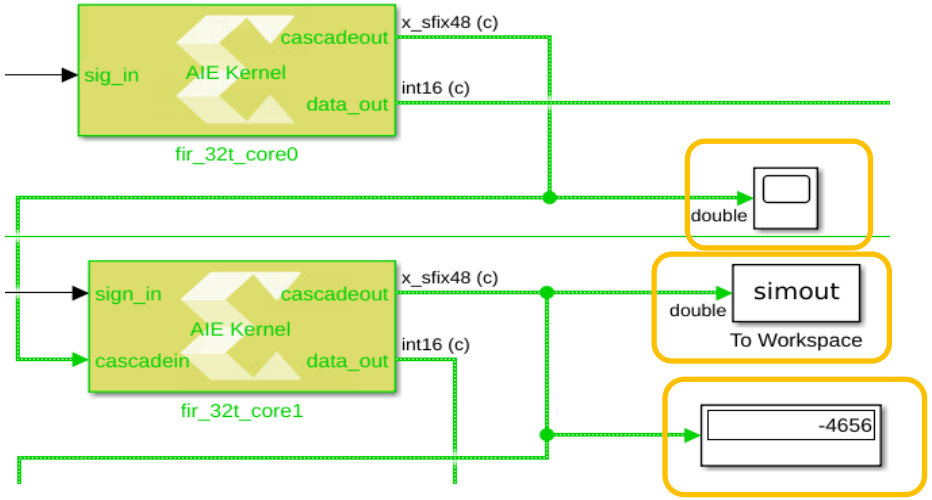
```
adf::connect< adf::stream > net4 (In2, fir_32t_core2_0.in[0]);
adf::connect< adf::stream > net5 (In2, fir_32t_core3_0.in[0]);
adf::connect< adf::stream > net6 (In2, fir_32t_core4_0.in[0]);
adf::connect< adf::stream > net7 (In2, fir_32t_core5_0.in[0]);
adf::connect< adf::cascade > net8 (fir_32t_core0_0.out[0], fir_32t_cc
adf::connect< adf::stream > net9 (fir_32t_core0_0.out[1], Out1);
adf::connect< adf::cascade > net10 (fir_32t_core4_0.out[0], fir_32t_c
adf::connect< adf::stream > net11 (fir_32t_core4_0.out[1], Out2);
adf::connect< adf::cascade > net12 (fir_32t_core1_0.out[0], fir_32t_c
adf::connect< adf::stream > net13 (fir_32t_core1_0.out[1], Out4);
adf::connect< adf::cascade > net14 (fir_32t_core5_0.out[0], fir_32t_c
adf::connect< adf::stream > net15 (fir_32t_core5_0.out[1], Out5);
adf::connect< adf::cascade > net16 (fir_32t_core2_0.out[0], fir_32t_c
```

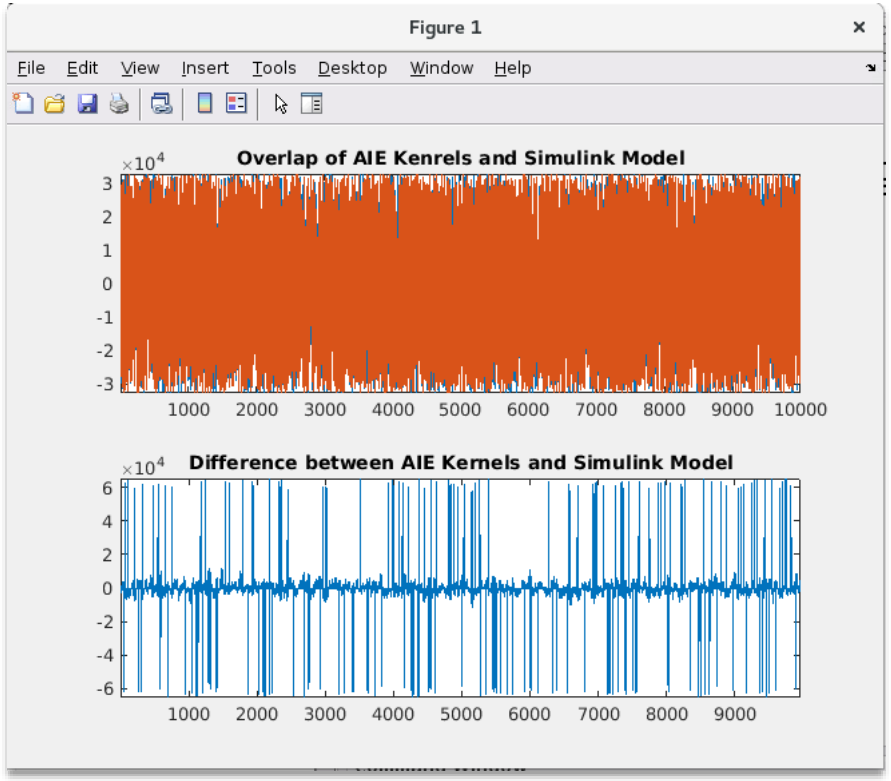


XILINX.

Visualization (Data)



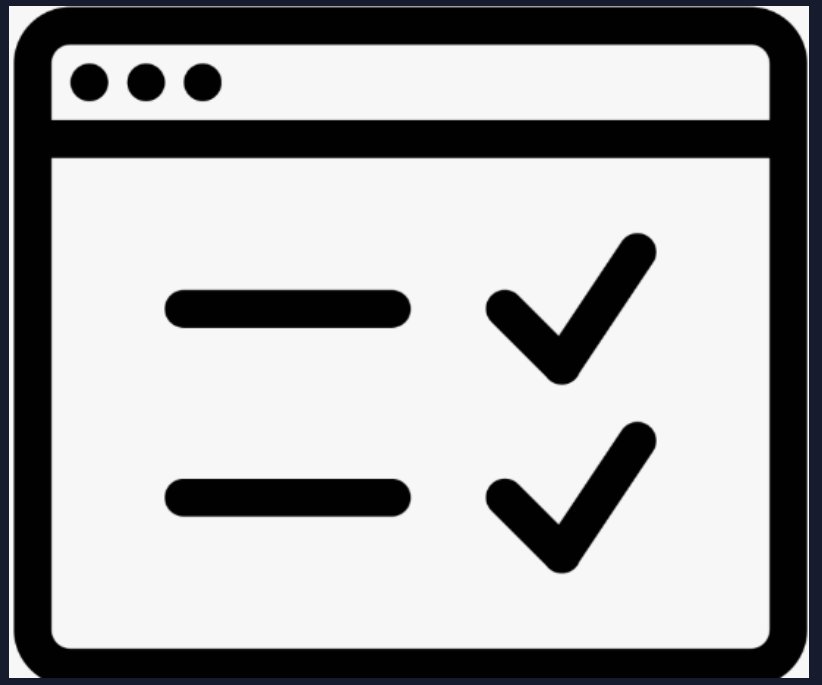




Demo: Vector Run Time Parameter (RTP)

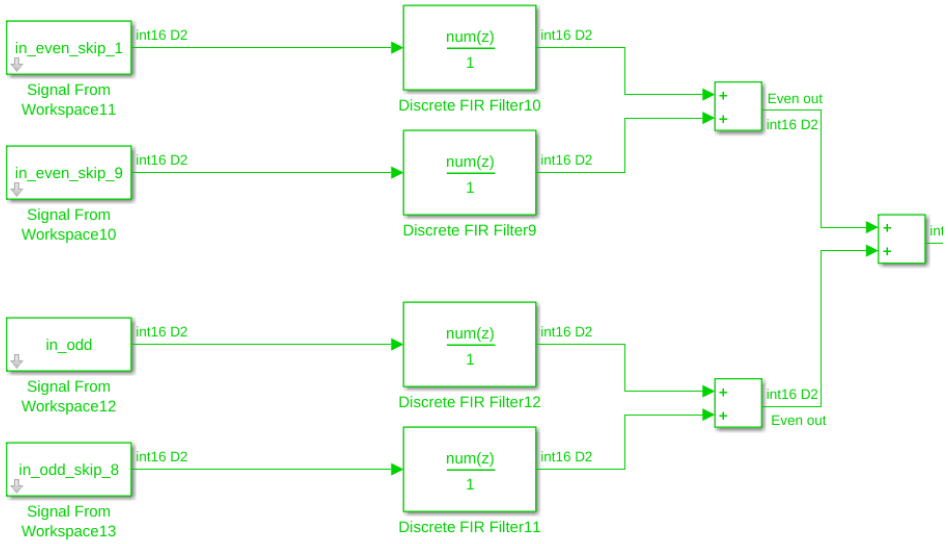
XILINX.

Verification, Test Bench Creation and Execution

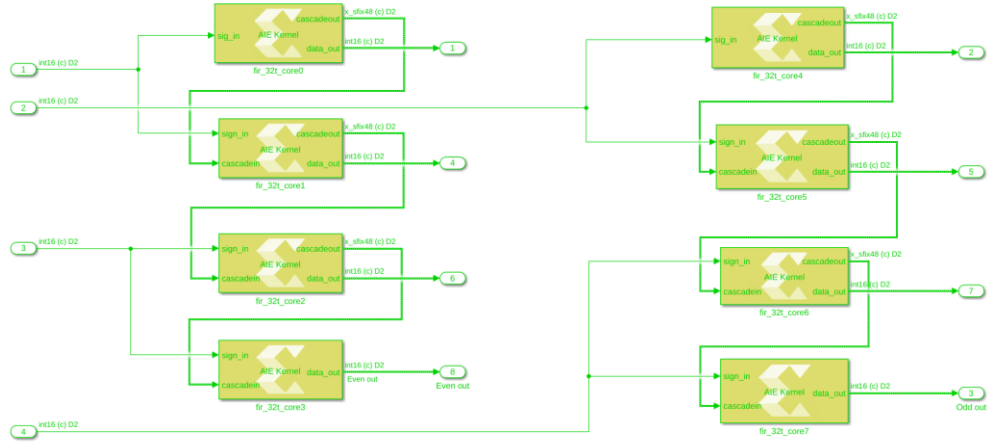


Golden Reference

Pure MATLAB and Simulink



Add-on for MATLAB and Simulink

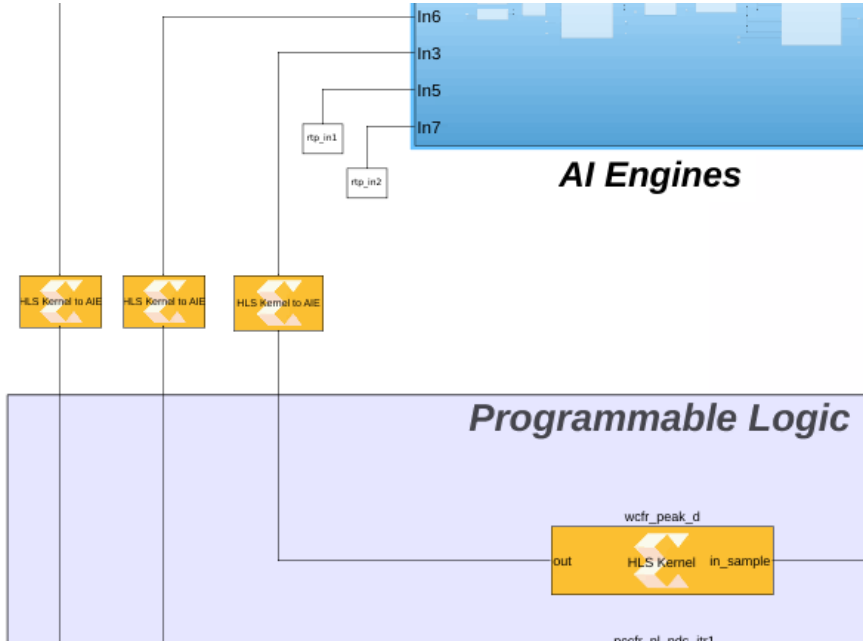


Use Scopes, Plots, to/from MATLAB workspace to evaluate the design

XILINX.

Heterogenous Simulation

Co-simulate AI Engine, HLS, and SysGen blocks all in ONE same design



System Generator

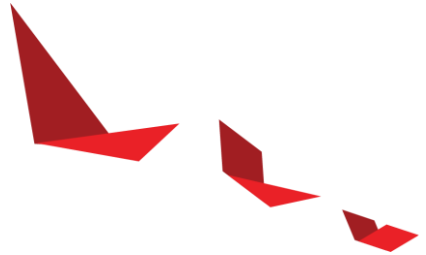
Demo: Co-simulation

Summary

Summary

- Enables rapid design exploration within the graphical Simulink environment
- Transforms algorithmic specifications to production-quality implementation through automatic optimizations
- Accelerates the path-to-production on Xilinx devices through automatic code generation
- Improves productivity significantly, 100x faster simulation
- Modeling Versal ACAP Heterogenous Device
- A single tool for all design domains

Where to find more information



- Xilinx Add-on for MATLAB and Simulink
  https://www.xilinx.com/products/design-tools/vivado/integration/addon-matlab-simulink.html
- Xilinx Versal and AI Engine
  https://www.xilinx.com/products/silicon-devices/acap/versal.html
- https://github.com/Xilinx/Model_Composer_System_Generator_Examples/blob/2020.2/README.md
- Add-on for MATLAB & Simulink video tutorial
  https://www.mathworks.com/videos/series/getting-started-with-the-avnet-ultra96-development-board.html
- Xilinx Zynq Support from MATLAB and Simulink
  https://www.mathworks.com/hardware-support/zynq.html

Thank You