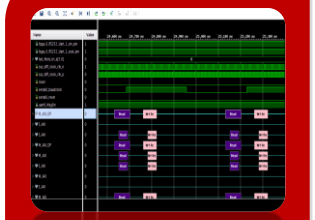
XILINX

Vivado Adapt 2021
Simulation & Hardware Debug

Satyam Jani & Matt Piazza

Overview



Simulation

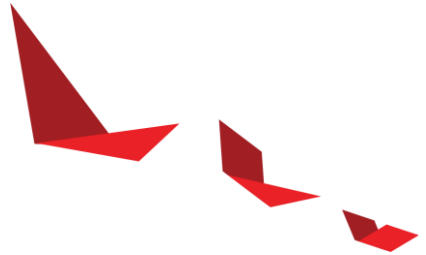
- Verification IPs, Traffic Generators
- Simulation Models – RTL & Transaction Level Models(TLMs)
- Xilinx Simulator(XSIM)
- 3rd party simulators
- Simulation Flows

Debug

- Hard Block Debug
- Fabric Debug
- High Speed Debug Connectivity
- ChipScoPy

Simulation – FPGAs & ACAP

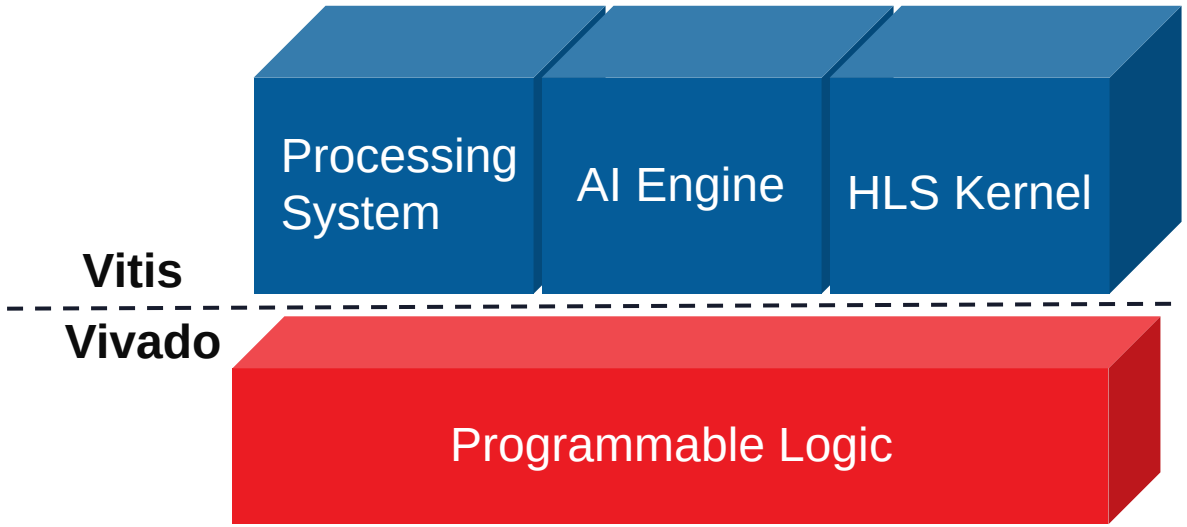
Simulation Scope



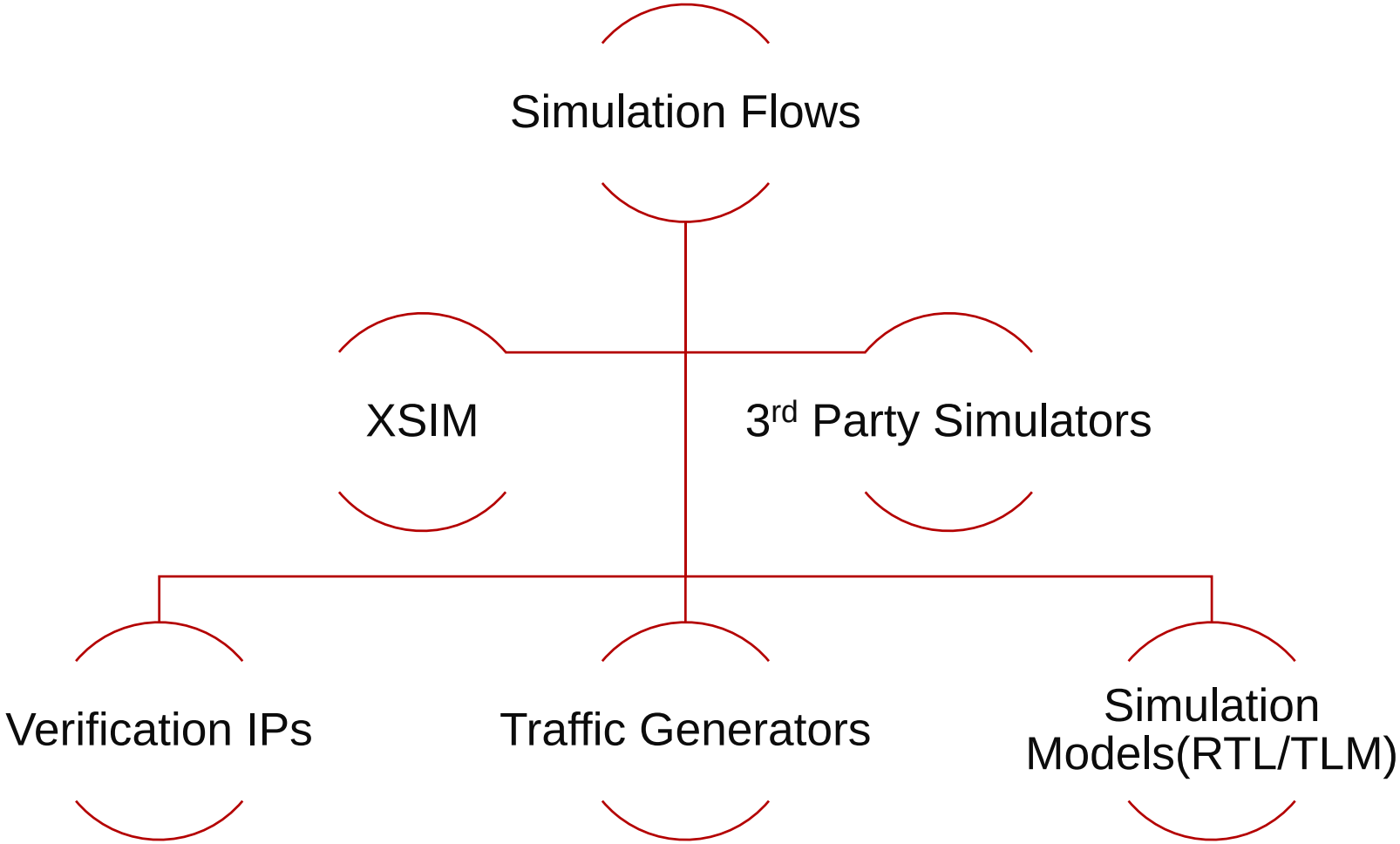
Vitis	HW Emulation	Full System Simulation with PL, PS(QEMU) & AIE blocks
	QEMU	Embedded software simulation for Processing System(PS)
	HLS Cosimulation	HLS kernel simulation with Csim or Cosim
	AIE Simulation	AI Engine simulation containing graphs and kernels
Vivado	RTL Simulation	Programmable logic simulation of hardware blocks (RTL, IPs, Sim models)

Versal ACAP Simulation

- Allows simulating individual blocks or entire system
- Simulation choice based on scope and abstraction
- Supported flows in Vitis and Vivado for any application



Simulation In Vivado



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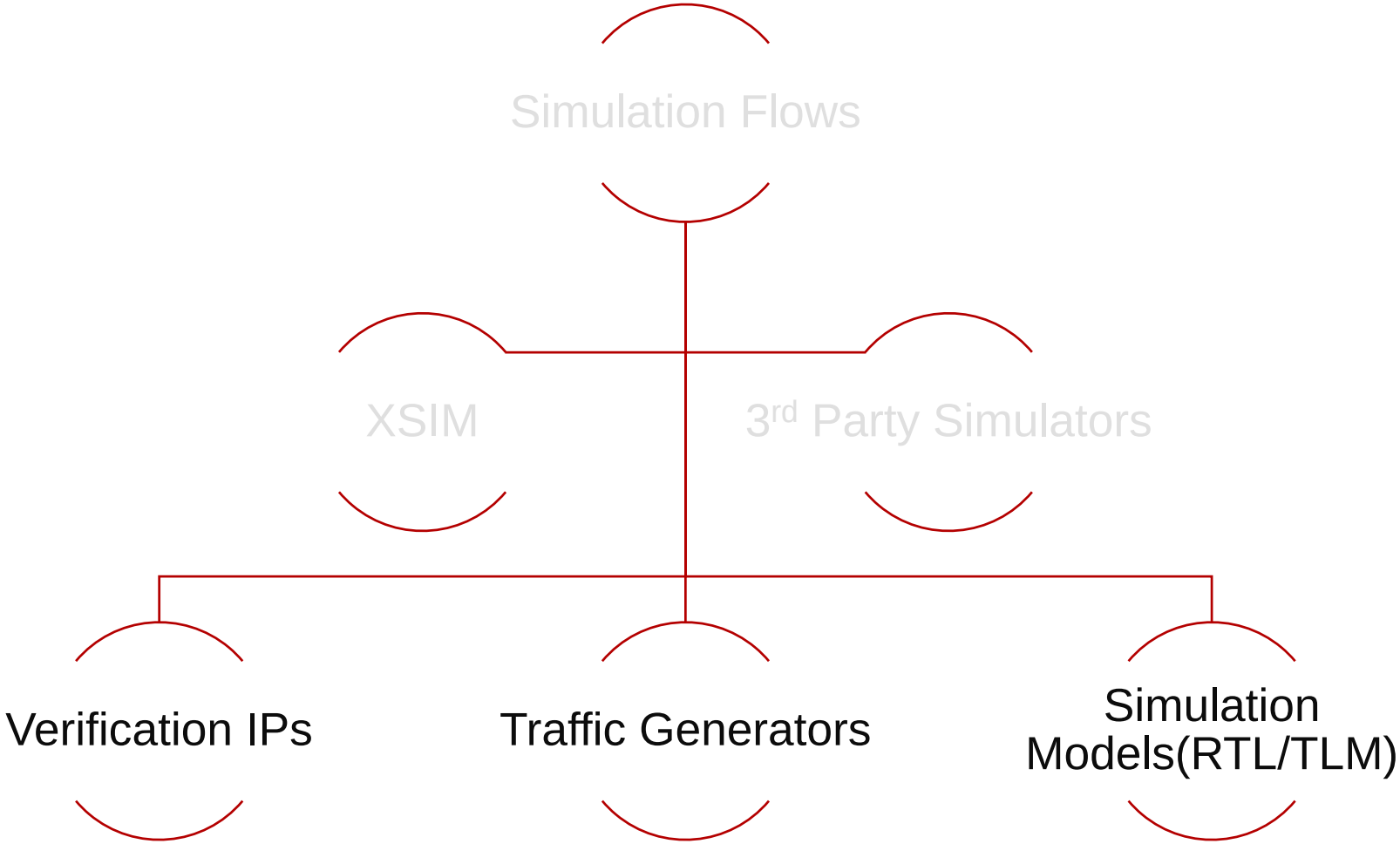
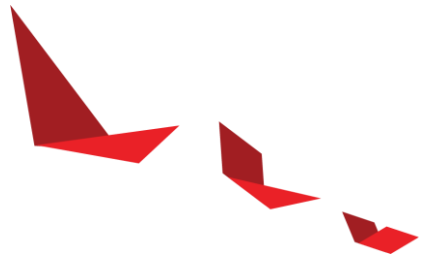


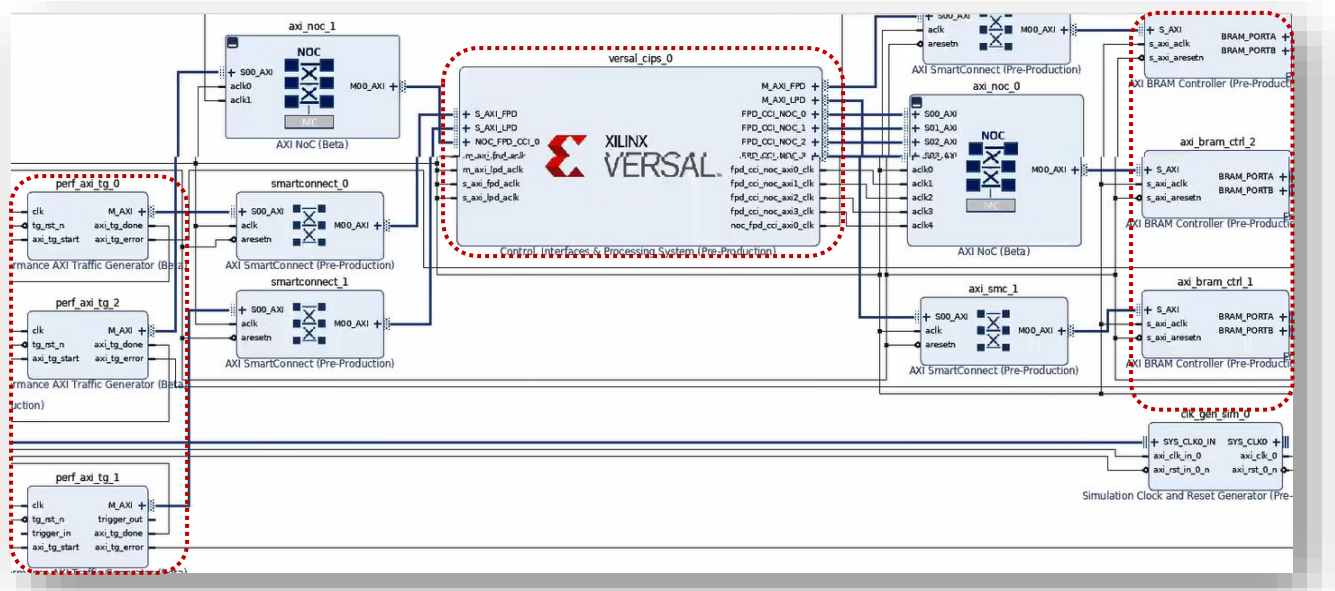
Xilinx VIPs & Traffic Generators



- Traffic Generators
  - AXI Traffic Generator for AXI4, AXI4-Stream, AXI4-Lite
- AXI VIP & AXI Stream VIP
  - Full AXI & AXI Stream Protocol Checker support
- Zynq-7000 VIP & Zynq US+ MPSoC VIP
  - Functional simulation of Zynq-7000 & Zynq US+ MPSoC based application
- Versal Control, Interfaces, and Processing System VIP
  - CIPS VIP (Early Access)

Versal CIPS VIP (Early Access)

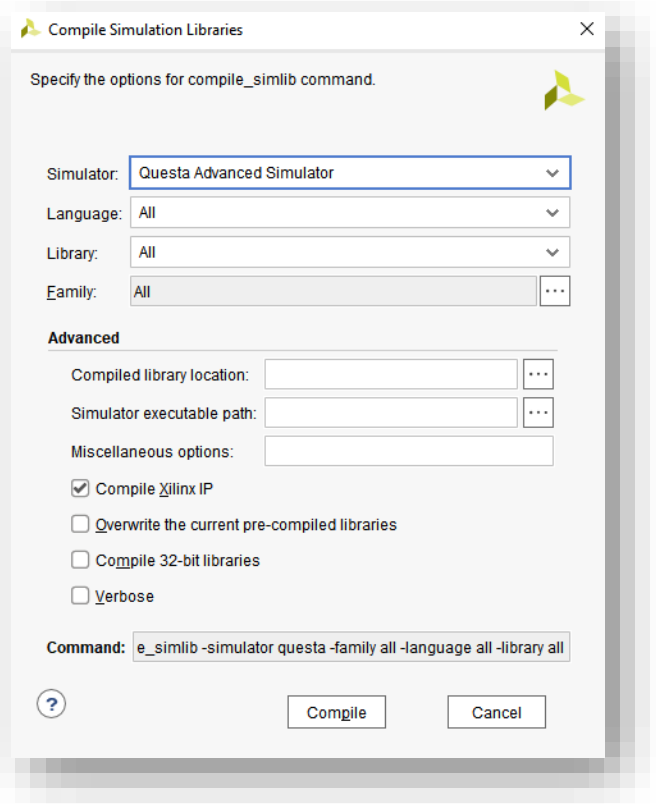
- Functional verification of Control, Interfaces, and Processing System (CIPS)
- Allows verifying PS-PL interfaces and OCM memories
- Provided as SystemVerilog model




```
launch_simulation: Time (s): cpu = 00:06:13 ; elapsed = 00:05:00 . Memory (MB): peak = 8133.281 ; gain = 242.895 ; free physical = 11984 ; free virtual = 90541
run 60 us
INFO: [VERSAL_CIPS_PS_VIP] (tb_top.DUT.design_1_i.versal_cips_0.inst.PS9_VIP_inst.inst.write_data) :: [write_data] [1615] ::: [R5_API] Done AXI Write with Starting Address(0xfffc0000) with Response 'OKAY'
Write into OCM memory
INFO: [VERSAL_CIPS_PS_VIP] (tb_top.DUT.design_1_i.versal_cips_0.inst.PS9_VIP_inst.inst.read_data) :: [read_data] [1615] ::: [R5_API] AXI Read with Starting Address(0xfffc0000) and 4 bytes
INFO: [VERSAL_CIPS_PS_VIP] (tb_top.DUT.design_1_i.versal_cips_0.inst.PS9_VIP_inst.inst.read_data) :: [read_data] [2775] ::: [R5_API] Done AXI Read with Starting Address(0xfffc0000) with Response 'OKAY'
read from OCM memory
AXI VIP Test PASSED
Simulation completed
```

Simulation Libraries & Models

- Simulation libraries for behavioral, functional and timing simulation
- Compile simulation library support for 3rd party simulators
- Pre-compiled simulation libraries for XSIM
- TLM model support to reduce simulation time



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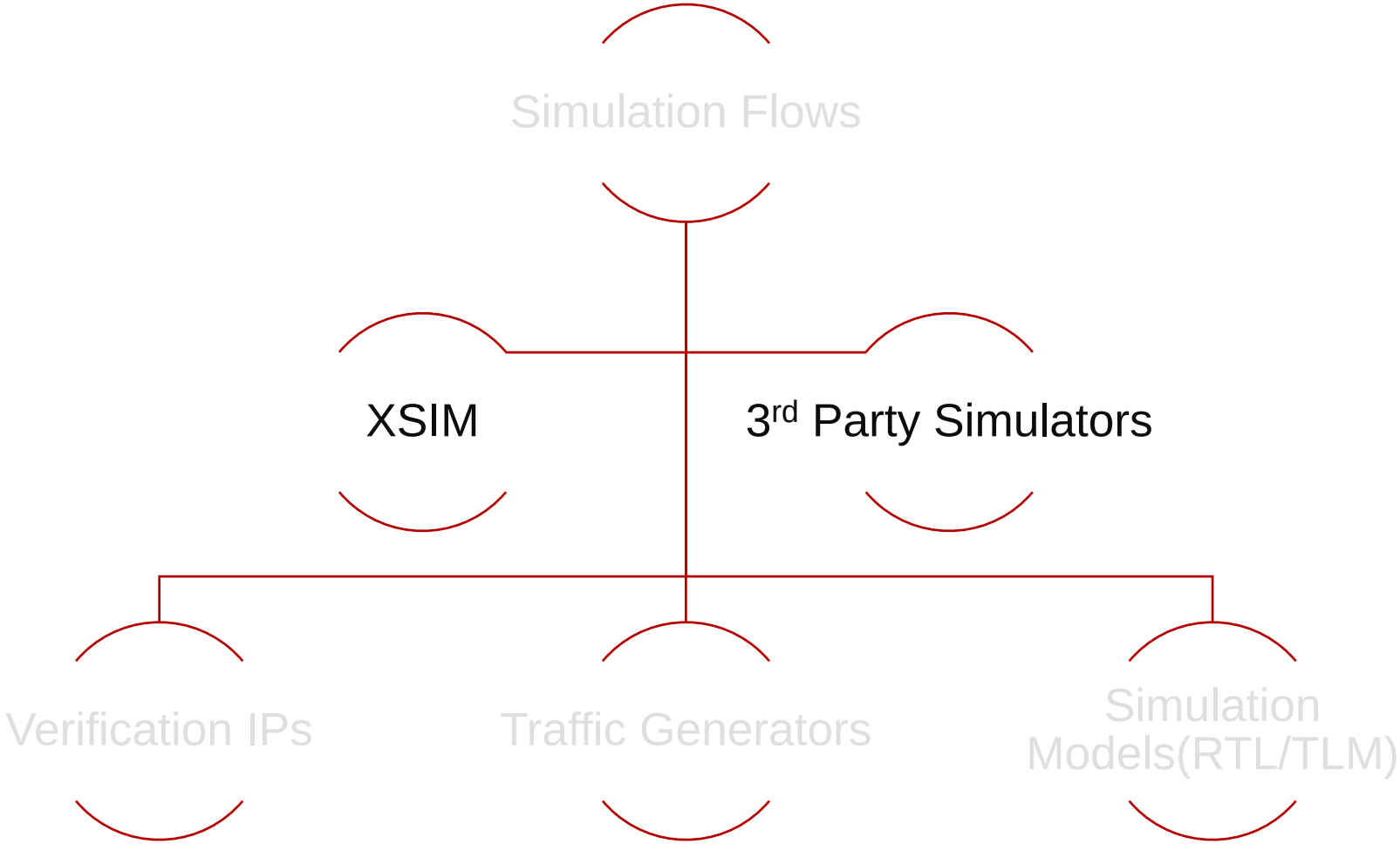
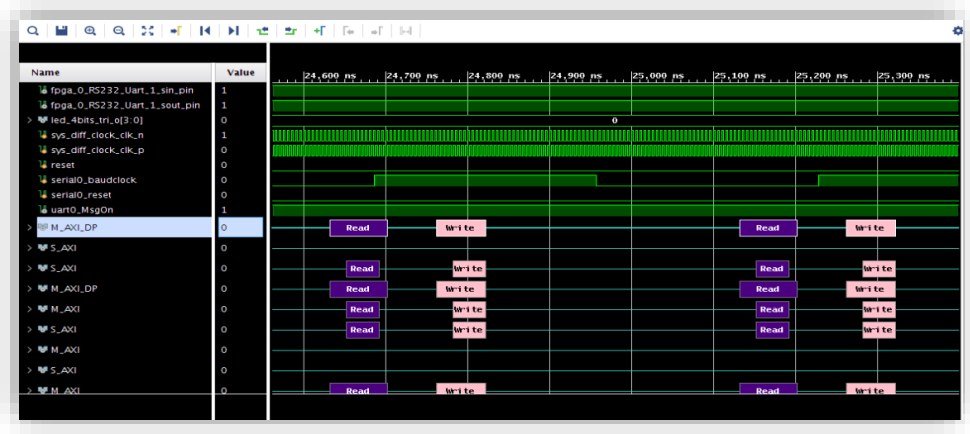
Simulation In Vivado



Xilinx Simulator (XSIM)

- Home-grown simulator with no design size limitation – no cost
- Mixed-language simulator for behavioral and timing simulation
- Support for UVM 1.2 & Functional Coverage
- Powerful waveform viewer
- Comprehensive debugging tools
- Support both GUI and batch mode with Tcl scripts



Transactions

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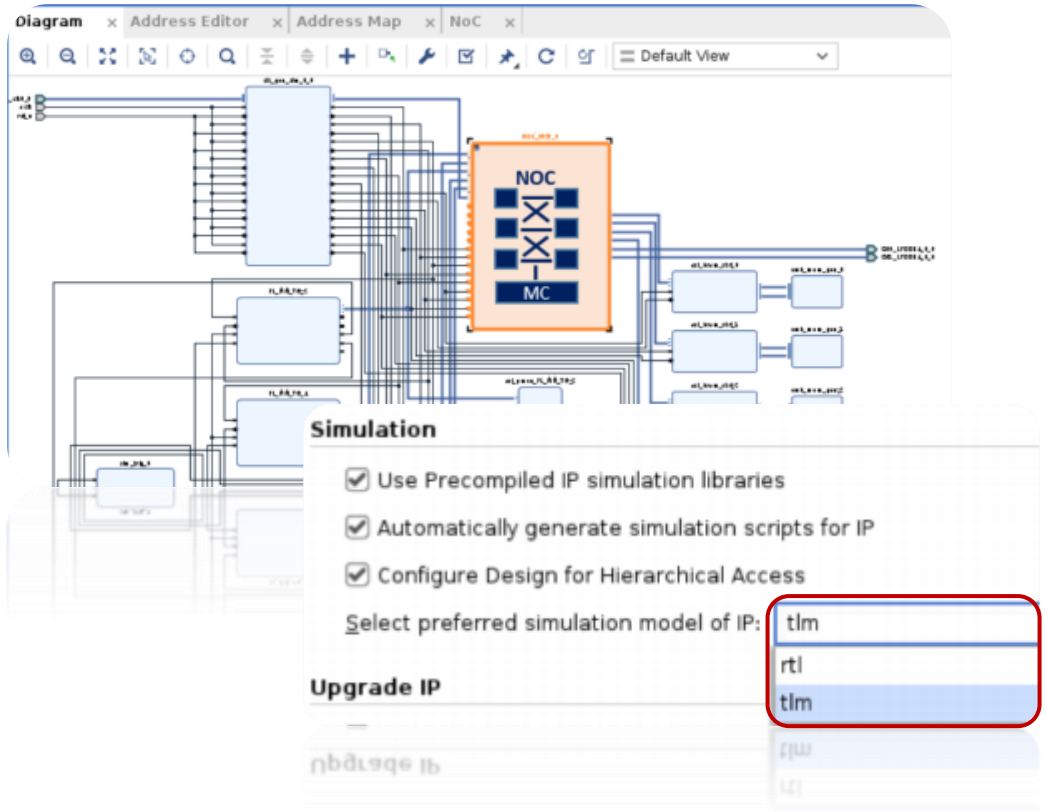
Xilinx Simulator (XSIM) - SystemC

- Mixed language simulation support for SystemVerilog & SystemC
- Pre-compiled SystemC models
- Ability to switch between RTL & SystemC models



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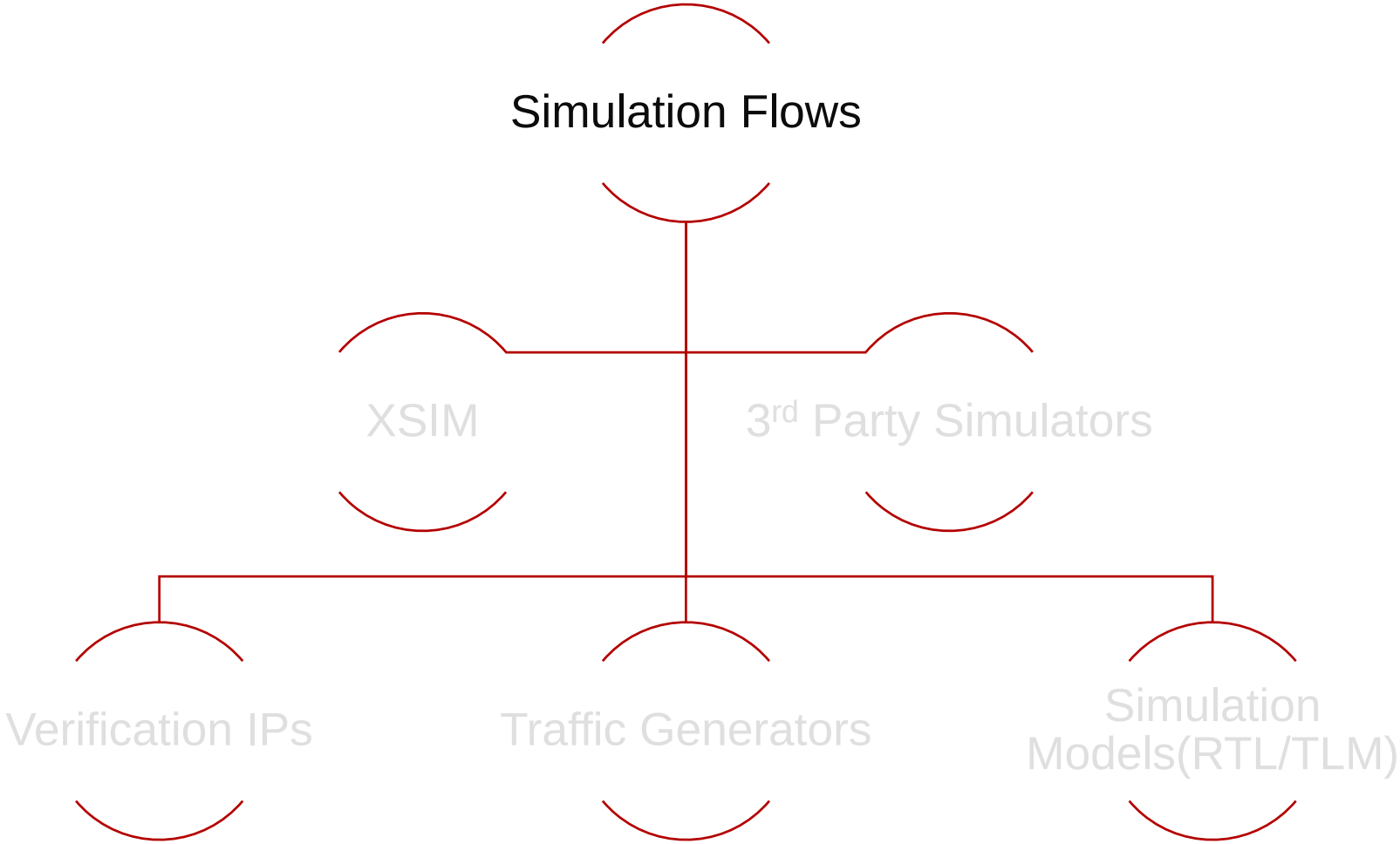
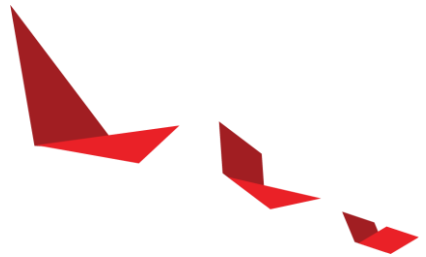
Simulation In Vivado



Simulation Flows

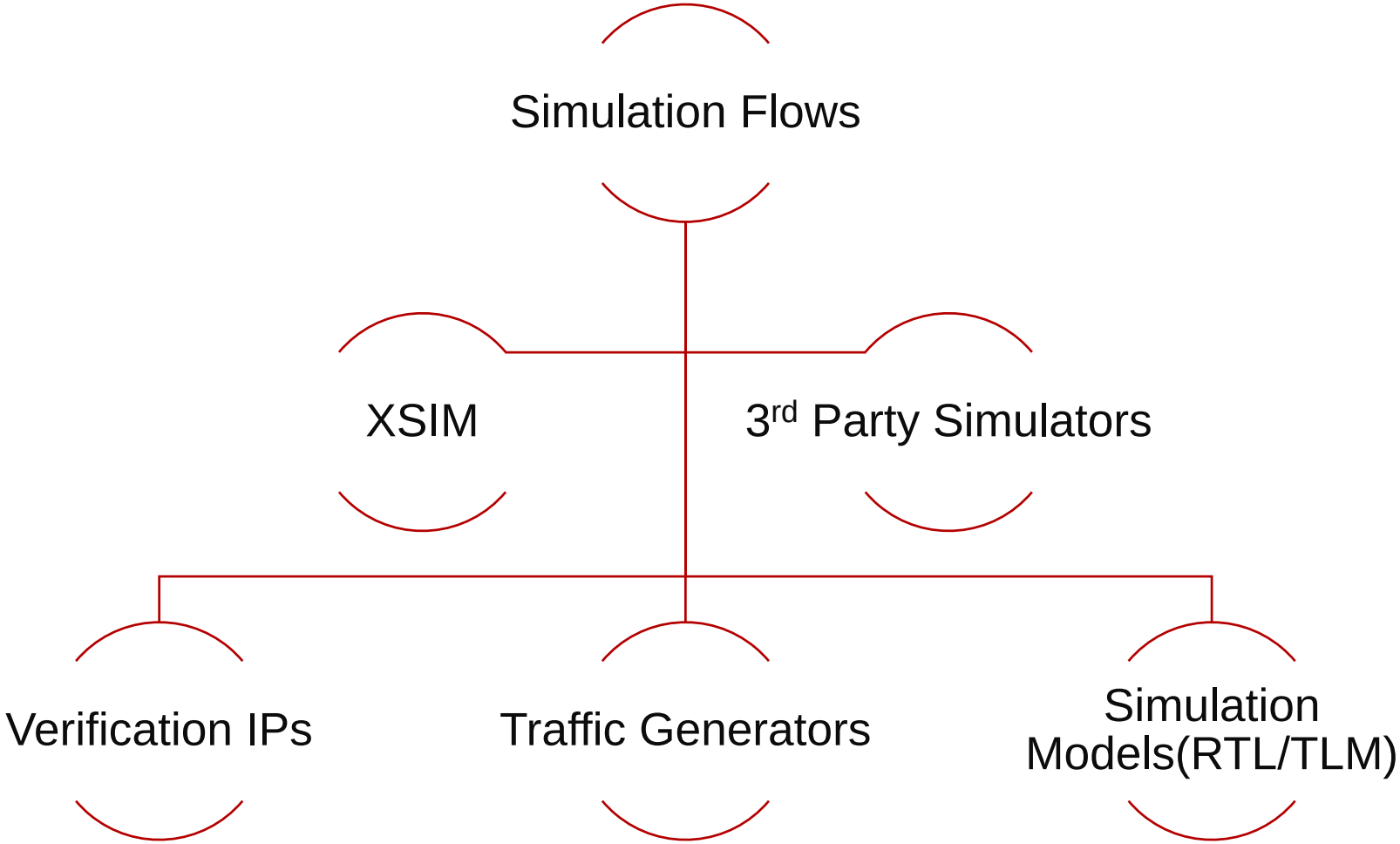


- Integrated Simulation flow – Covers from **behavioral** to **timing** simulation
- **XSIM** and **3rd party simulator** support
- Library **Compilation Utility** (Include IP simulation libraries)
- Simulation **script generation (Integrated & Export)**

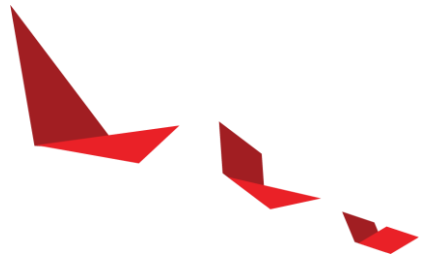
Simulation Methodology

- Compile & Simulation time
  - Use pre-compiled IP library option to cut down design compile time significantly
  - Use RTL sources for simulation and avoid netlist simulation if possible
  - Utilize SystemC model wherever available for faster simulation time
- Integrated vs Export mode
- Expand verification environment with VIPs & TCL store apps

Simulation In Vivado



Resources

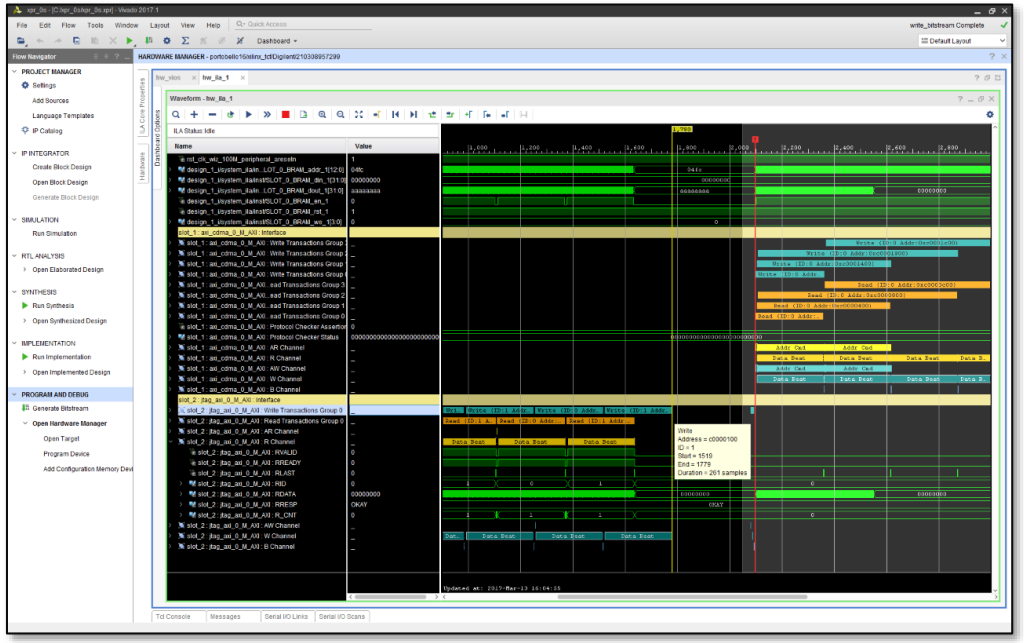


- Vivado Design Suite User Guide: Logic Simulation (**UG900**)
- Vivado Design Suite Tutorial Logic Simulation (**UG937**)
- CIPS VIP Early Access – Request Here
- AXI Verification IP (**PG267**)
- AXI4-Stream Verification IP (**PG277**)
- Zynq-7000 All Programmable SoC Verification IP (**DS940**)
- Zynq UltraScale+ MPSoC Verification IP (**DS941**)

Hardware Debugging – FPGAs & ACAPs

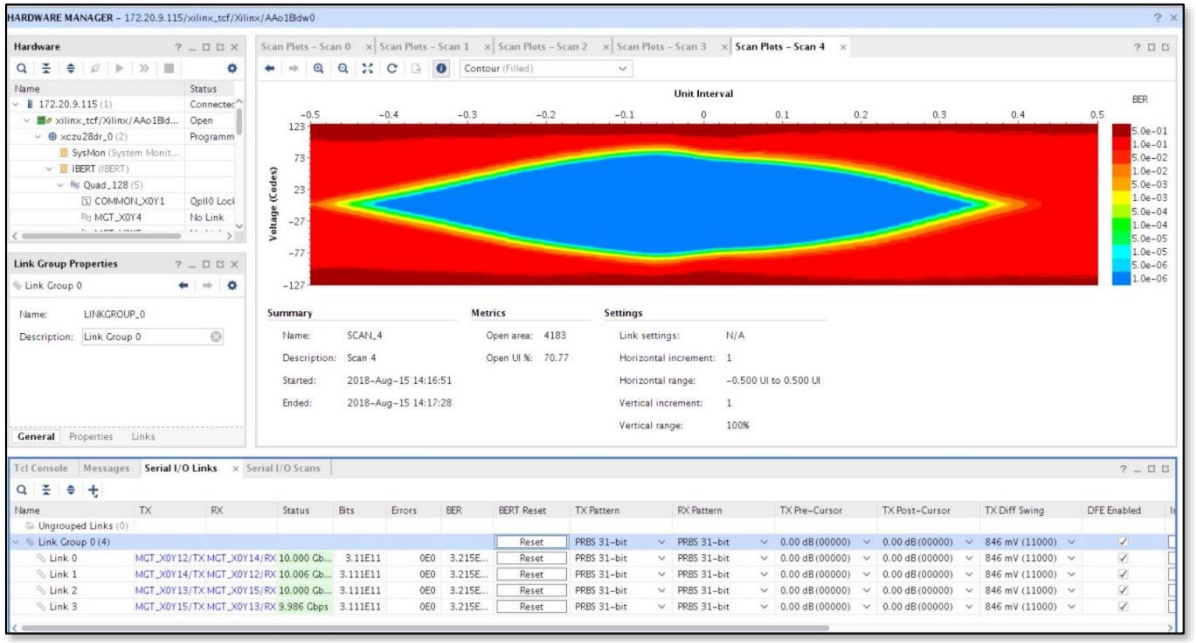
Hardware Debugging

Fabric Debug



- ILA (waveform)
- VIO (low speed I/O)
- Soft DDR (calibration)

Hard Block Debug



- IBERT (link tuning)
- PCIe (LTSSM Status)
- Hard DDR (calibration)

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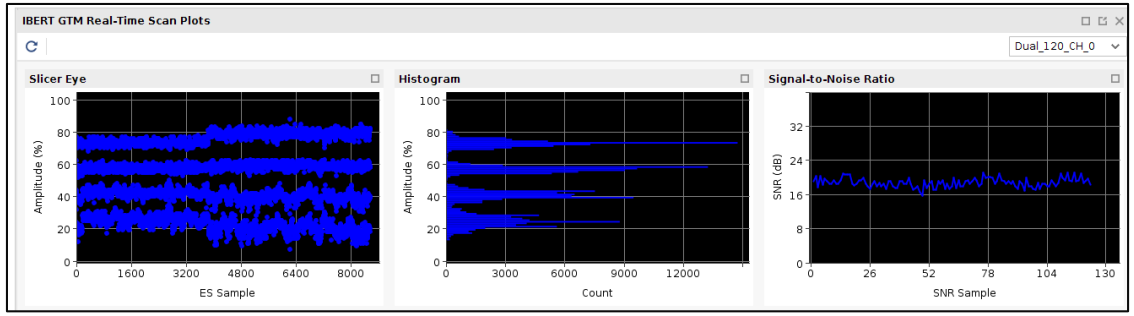
What's new in UltraScale+

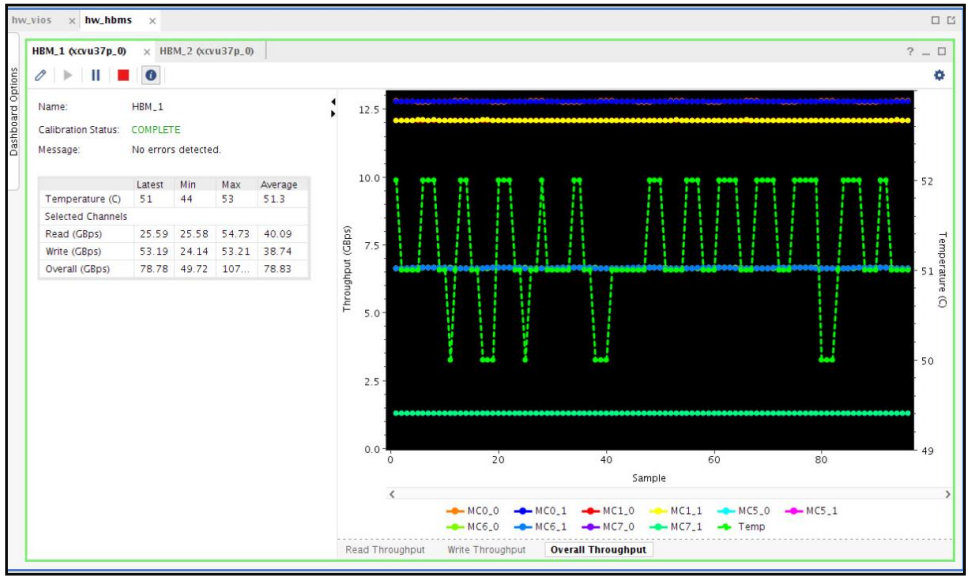
IBERT GTM

- Debug and characterization for 58 Gb/s PAM4 Transceivers
- Slicer Eye, Histogram, and Signal-to-Noise Ratio



HBM Monitor

- Optional – enable in HBM IP
- Graphical Viewer for HBM Activity Counters
- HBM Stack Temperature



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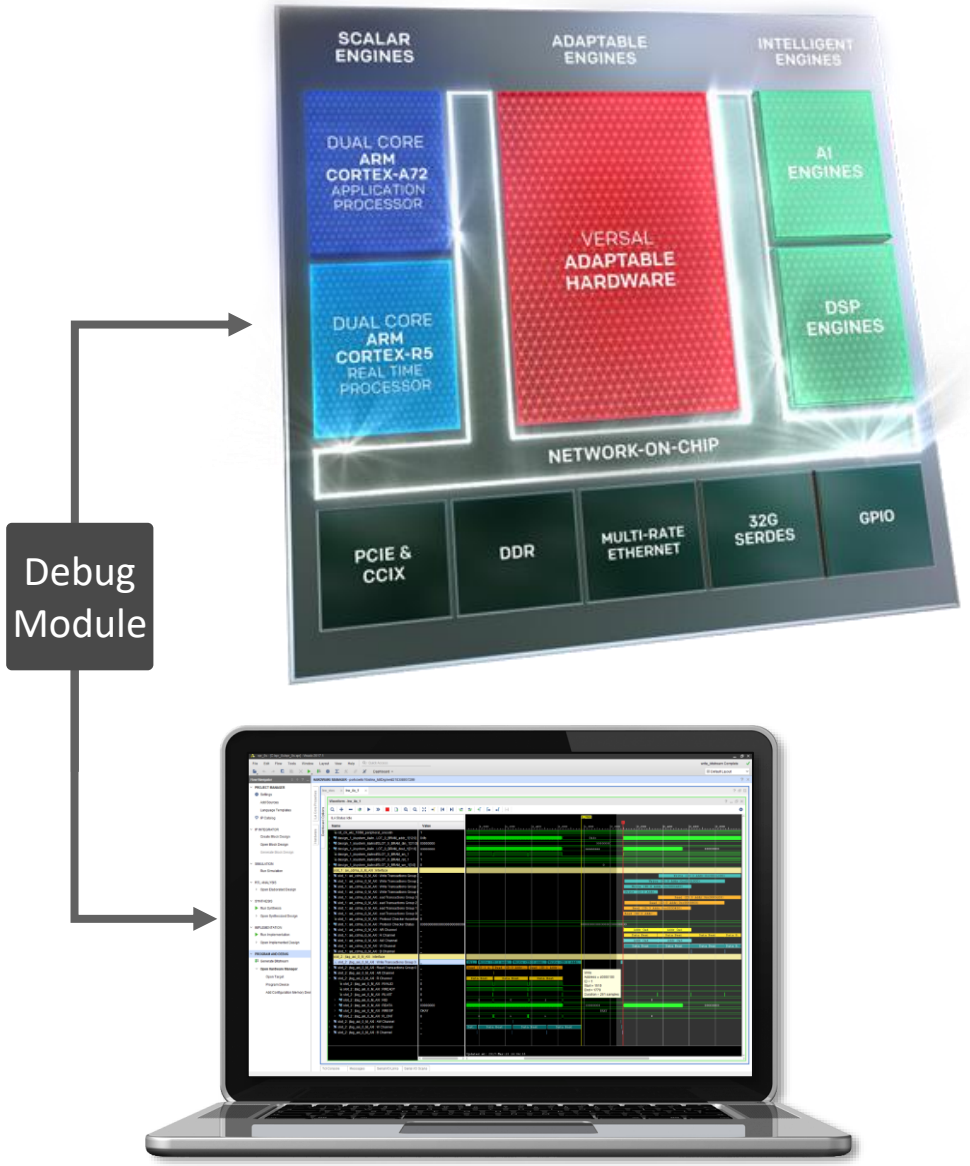
Debug Objectives for Versal

- **System-level Visibility**
  - Debug in all domains (PL/PS/AIE)
  - Integrated debug capabilities
- **Higher Performance**
  - High bandwidth and low latency debugging
  - Optimized trace and download
- **Flexibility**
  - Streamlined Connectivity
  - Integration – Python Extensions



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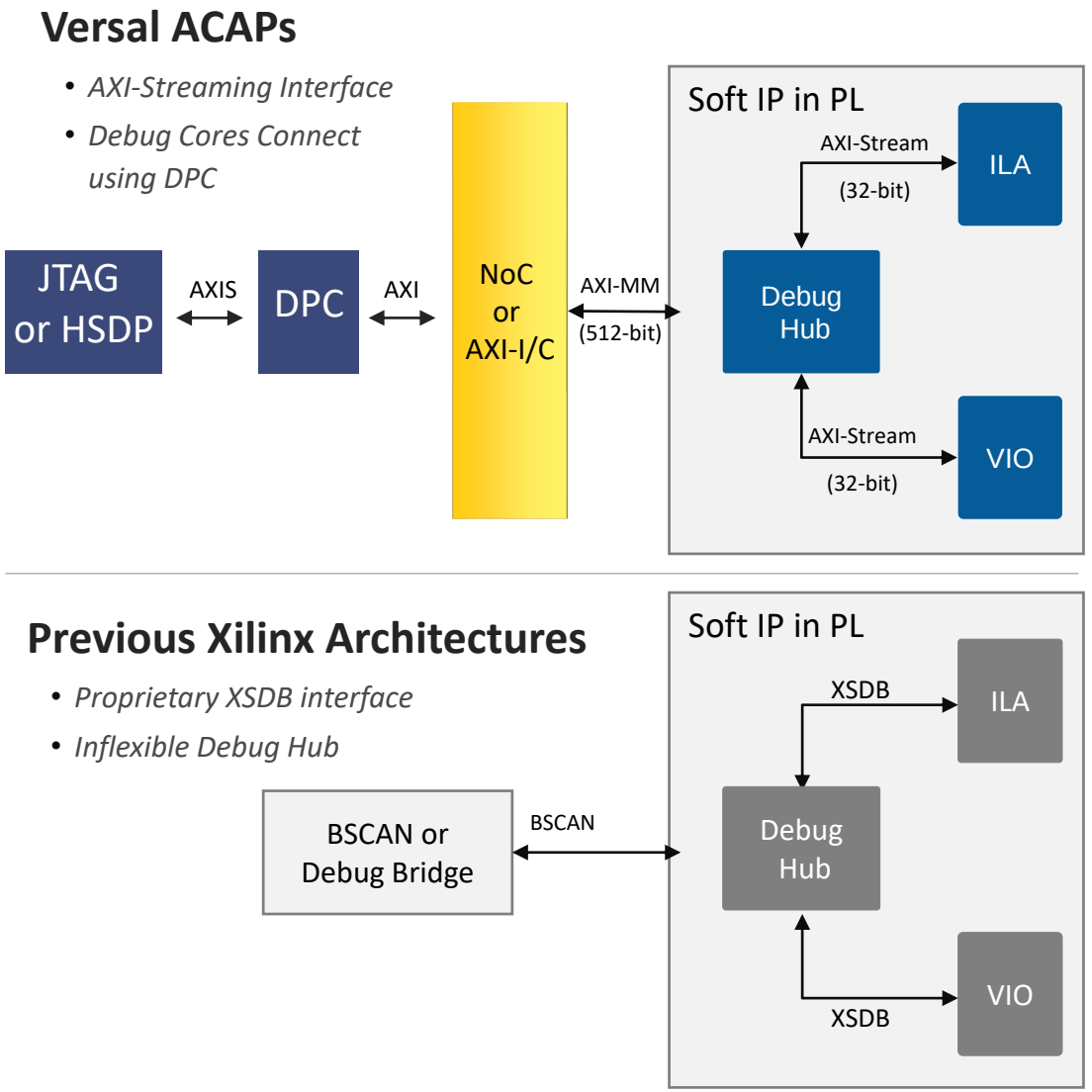
Versal – Differences in Debug Infrastructure

- **PL Debug IP**
  - Integrated Logic Analyzer (AXIS-ILA)
  - Virtual Input/Output (AXIS-VIO)
- **Hard Block Debug IP**
  - PCI Express Link Debug
  - Hardened Integrated Bit Error Ratio Test (IBERT)
  - Memory Calibration Debug Interface
- **Debug Packet Controller (DPC)**
  - Enables Multiple Access Options



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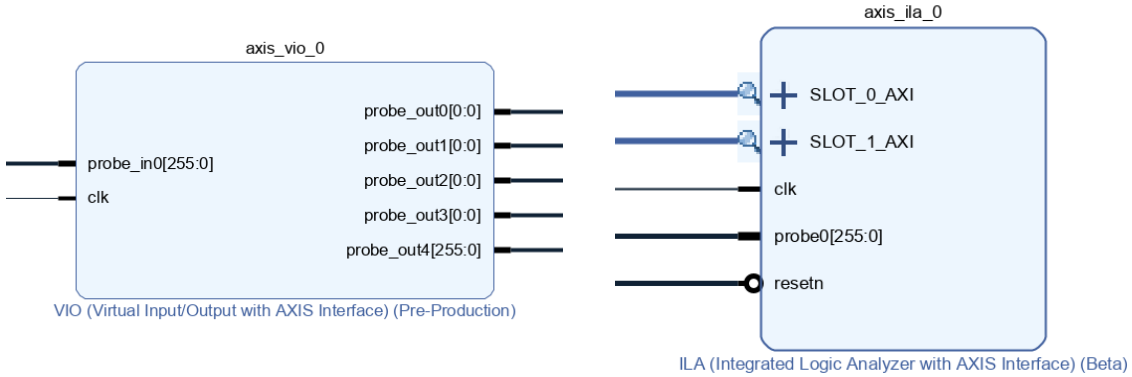
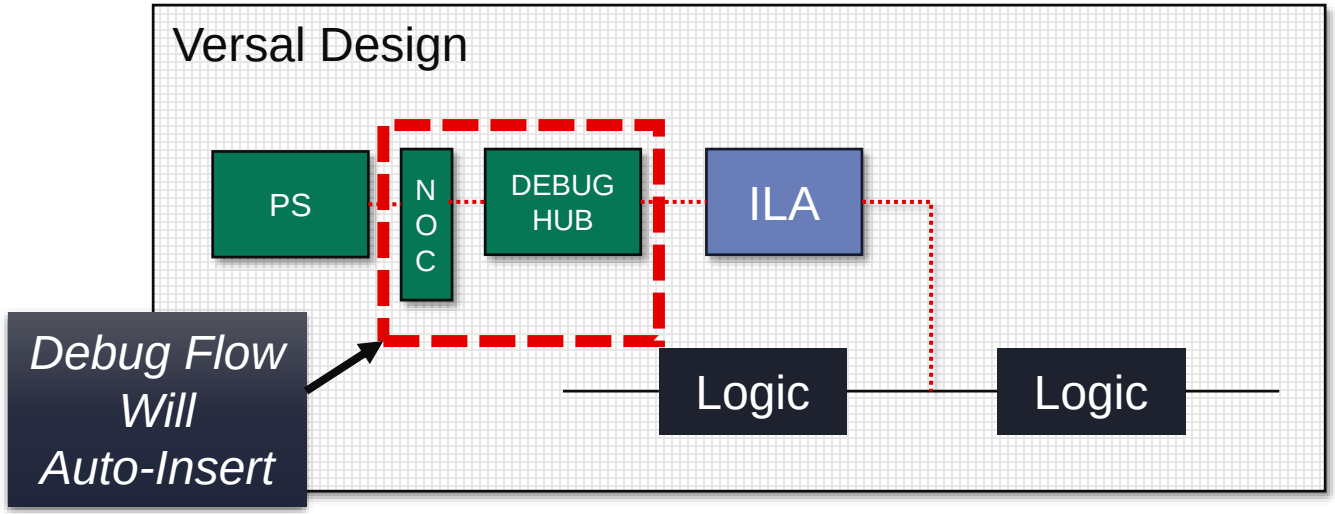
Versal PL Debug Cores

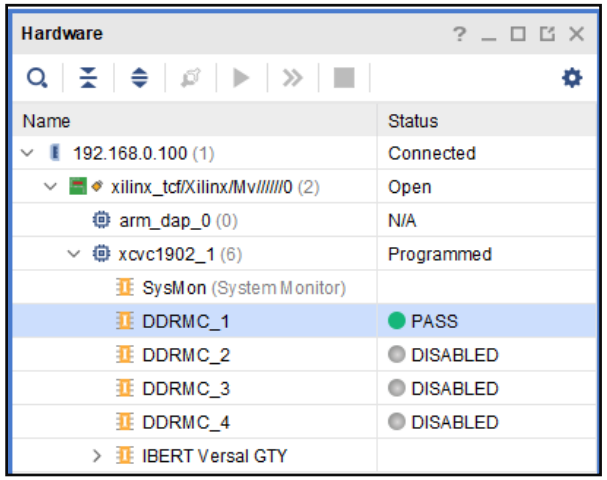
- **Integrated Logic Analyzer (ILA)**
  - Support for RTL and IPI Instantiation
  - Support for post-synthesis Netlist Insertion
  - Support for post-route ECO
  - Native and Interface Debugging – no need for separate System ILA
  - Support UltraRAM trace memory
- **Virtual Input/Output (VIO)**
- **AXI4 Debug Hub**
  - Debug hub can now be instantiated
  - AXI-Streaming Based Infrastructure
- **JTAG-to-AXI No Longer Needed**
  - Now built into DPC

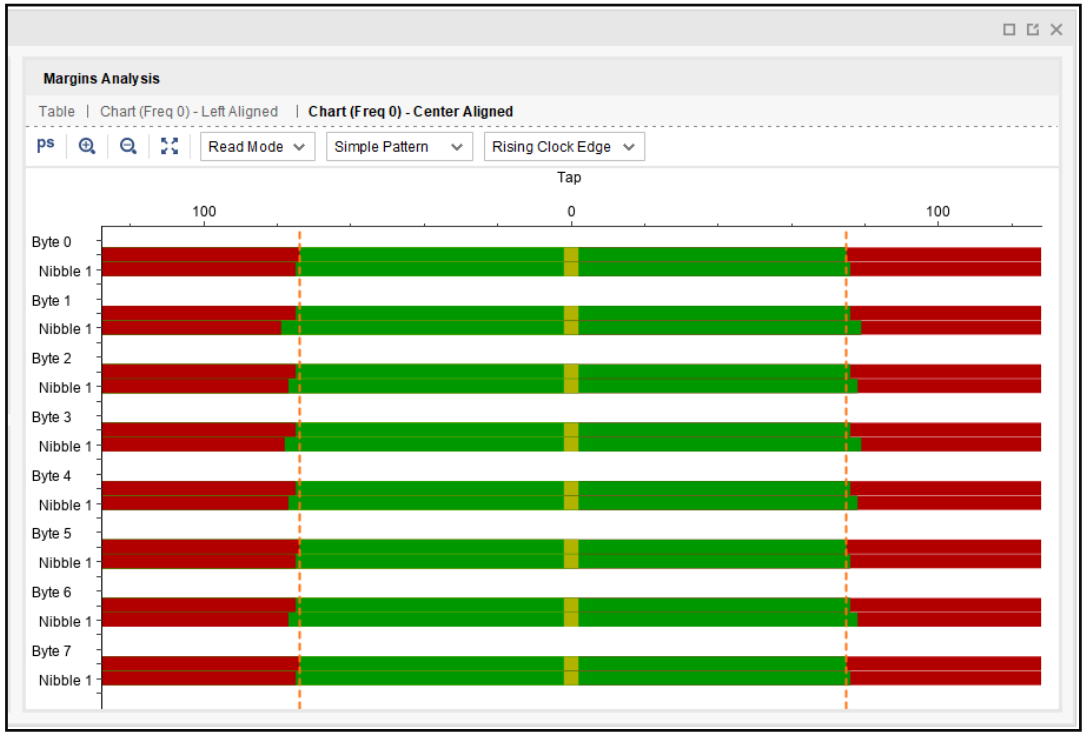




Memory Calibration for DDRMC

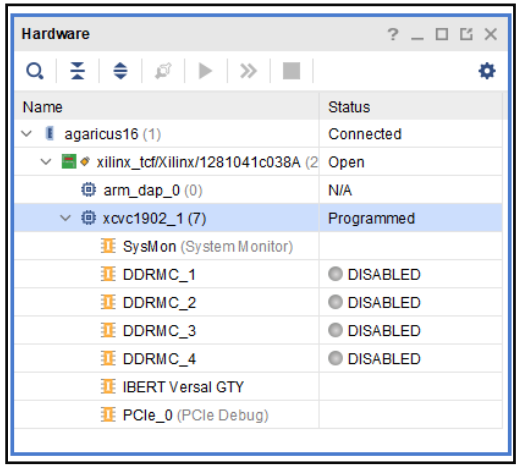
- **Integrated into Hard DDRMC**
  - No additional IP Required
- **DDRMC Status**
  - Calibration Status
  - View Status Registers
  - View Individual Calibration Stages
- **Margin Analysis**
  - View as Table / Left Aligned / Center Aligned

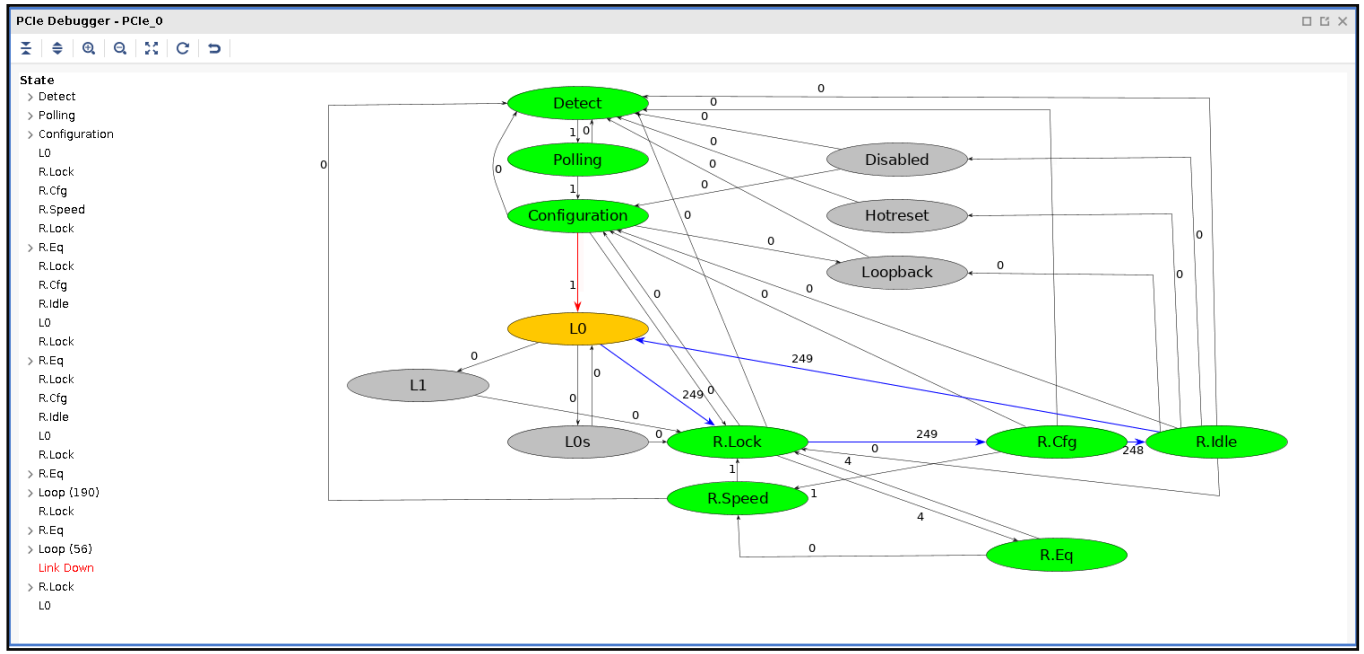




Versal PCIe Link Debug

- **Integrated in the PCI Express Integrated Block**
  - Optional – enable when configuring CPM block
  - Connect over JTAG or HSDP
- **Debugging View**
  - Current Link Speed & Width
  - LTSSM State Transitions
- **When to use**
  - Issues with PCIe Link





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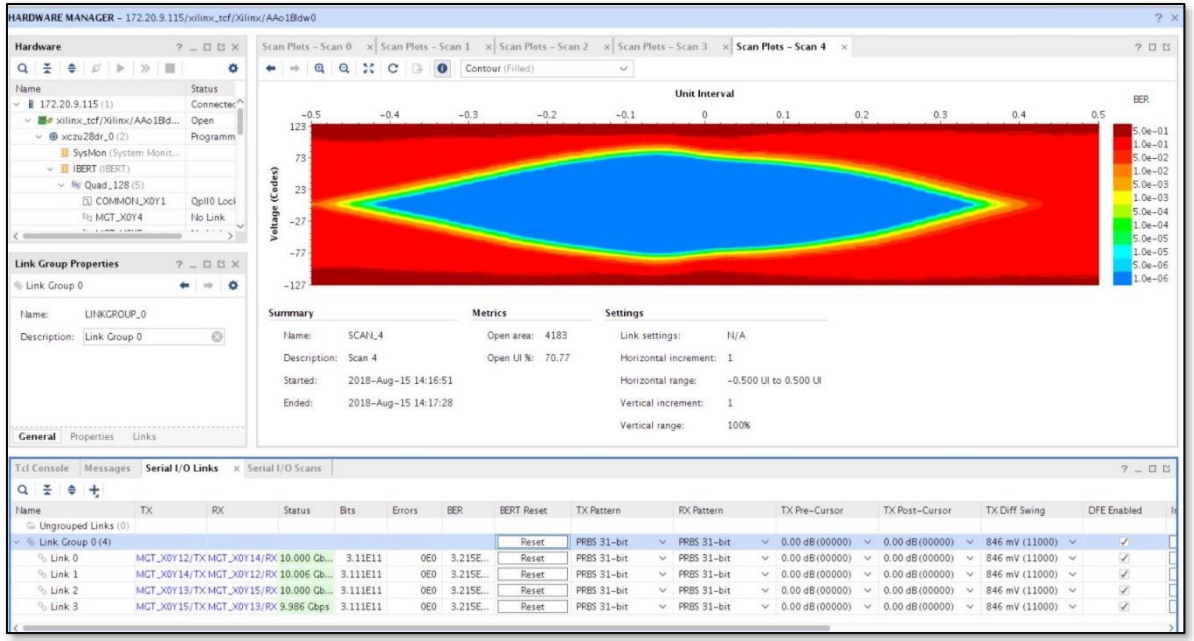
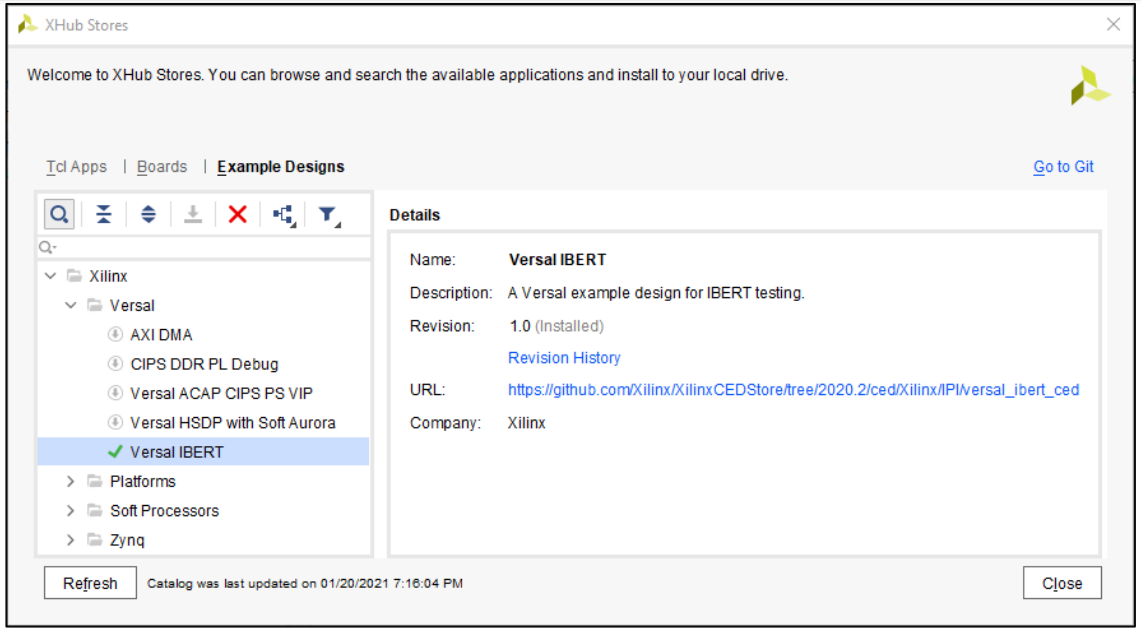
Versal IBERT

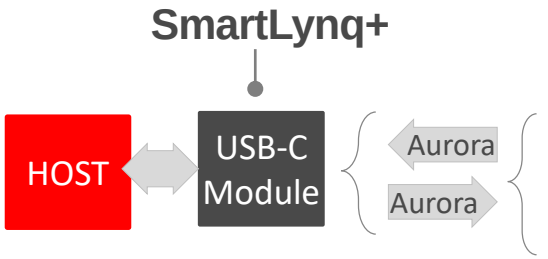
- **Differences from Legacy IBERT**
  - Integrated into GT
  - No additional IP
  - Use with any design that uses transceivers
- **Pattern Support**
  - PRBS 7, 9, 15, 23, 31
  - User Design Data
- **Versal IBERT CED**
  - Available today in XHub Store
  - Builds an IBERT capable design out of box
  - Similar interface to non-Versal IBERT IP

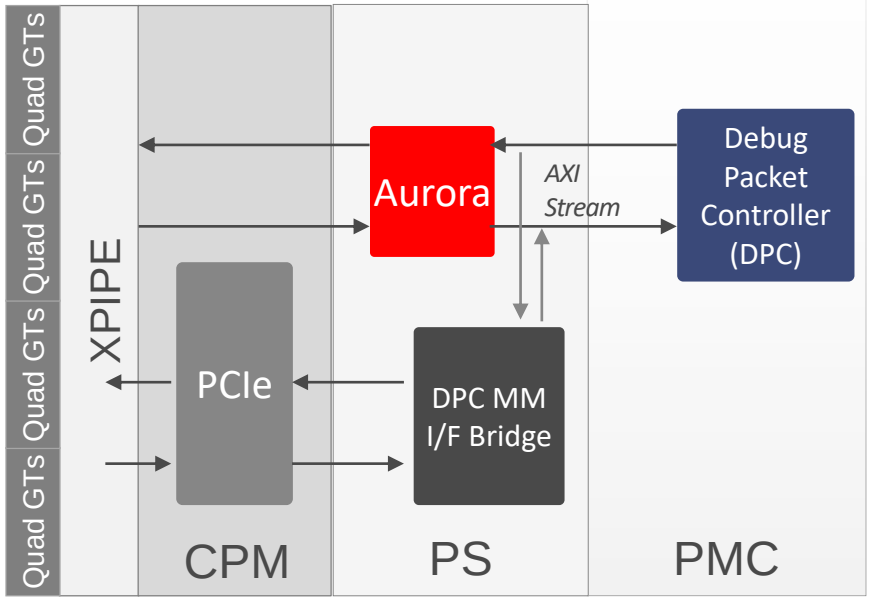




High Speed Debug Port (HSDP)

- **High Speed Interfaces to the DPC**
  - Aurora over USB-C (10 Gbps)
  - PCI-Express via. CPM (12 Gbps)
- **JTAG – 100 MHz**
- **Enabled in CIPS IP**
  - Quad / Reference Clock Selection
- **SmartLynq+**
  - Xilinx Debug Module for HSDP





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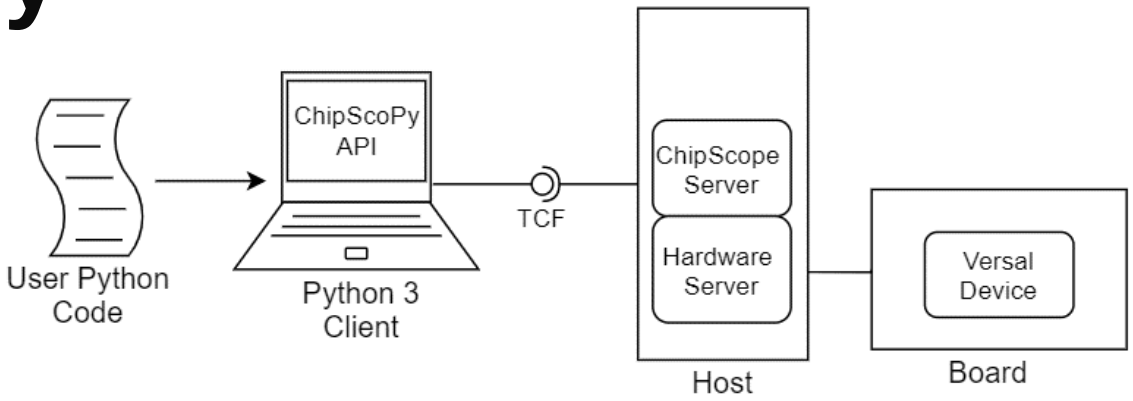
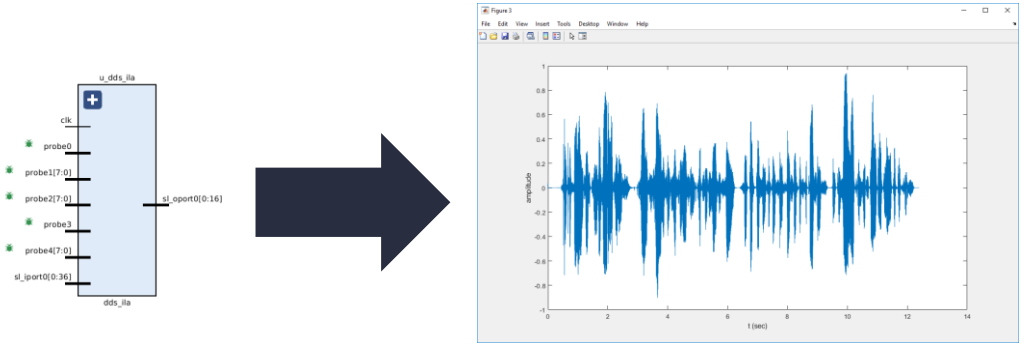
SmartLynq+ Module Overview

- **Optimized for Versal High-Speed Debug Port (HSDP)**
  - Device programming: **60X faster** than best-case JTAG
  - Memory access latency: **220X faster** than JTAG
  - Data upload & download: **200X faster** than JTAG
  - Data storage: **14GB DDR memory** on module
- **How do Versal HSDP Users Benefit?**
  - VC1902 programming in **<1s** vs **>30s** via JTAG
  - PS memory reads in **<10ms** vs **>2s** via JTAG
    - Typical debug session involves 1000's of memory reads
  - 8GB of AIE event trace offload in **<7s** vs **>21min** via JTAG
  - Linux image download in **<5s** vs. **2.5 min** via JTAG

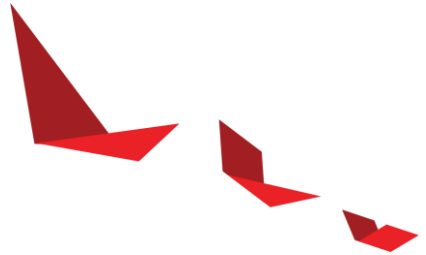
Coming Soon: ChipScoPy

- **Open-Source Python API for ChipScope**
  - Control and communicate with Versal Device and Debug Cores
  - Vivado not required to use – just need a PDI/LTX
- **Benefits**
  - Build custom debug interfaces
  - Interface with python ecosystem
- **Initial Release Will Include**
  - Device Programming
  - Versal ILA/VIO Control and Capture
  - Memory Access through DPC
  - Hard Block Debug Access (IBERT, DDRMC, PCIe)





Resources



- Vivado Design Suite User Guide – Programming and Debugging (**UG908**)
- Integrated Logic Analyzer(ILA) with AXI4-Stream InterfaceLogiCORE IP Product Guide (**PG357**)
- IBERT for UltraScale GTM Transceivers LogiCORE IP Product Guide (**PG342**)
- AXI High Bandwidth Memory Controller LogiCORE IP Product Guide (**PG276**)
- SmartLynq+ Landing Page
- Vivado Programming and Debugging Design Hub
- Xilinx Forum: Debug and Power Estimation Tools

Summary

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Q&A