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UltraScale+ Cost-Optimized Portfolio Announcement

Increasing Pressures on Edge & IoT Applications

The Need for Smarter Devices
Localized AI & Analytics

Higher Throughput
Sensor data, DSP compute, network bandwidth

Greater Power Efficiency
Battery-powered, thermal constraints

Cost Pressures
Increasingly competitive Industrial and Healthcare IoT markets

Shrinking Form Factors
Hand-held, flexible deployment & mounting

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Miniaturization at Edge and Endpoint is Becoming Pervasive across Markets

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The New UltraScale+ Cost-Optimized Portfolio

Industry Leading 16nm Perf/Watt for Cost-Sensitive Applications

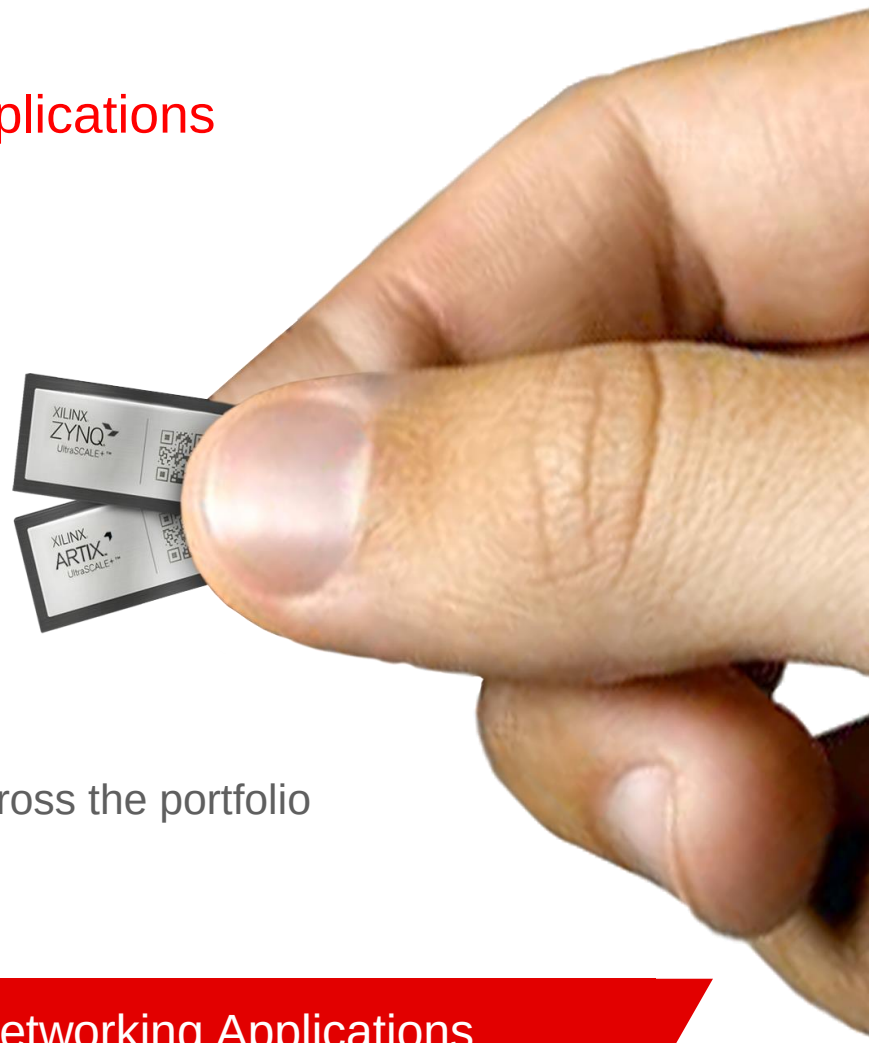
- New Zynq® UltraScale+™ SoC device optimized for power and cost
- New Artix® UltraScale+™ FPGA family for high I/O bandwidth & DSP compute

Highest Compute Density in New Form Factors

- 60% smaller, 70% thinner, lowest thermal footprint
- Highest compute, throughput, and signal processing / mm^2

Scalability across the UltraScale+ FPGA & SoC Portfolio

- Preserve & leverage investments in SW, IP, tools, and PCB design across the portfolio
- Scalable for customer's end-product portfolio



Industry's Highest Compute Density for Ultra-Compact Edge and Networking Applications

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Continuing the Success of 7 Series Cost-Optimized Portfolio

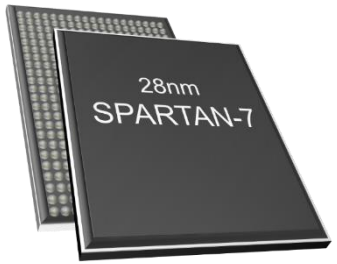
7 Series

Cost-Optimized Portfolio

28nm Performance/Watt

SPARTAN-7

Connectivity Optimized



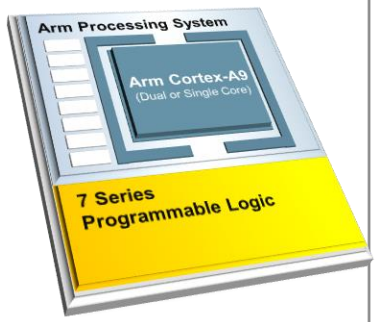
ARTIX-7

Bandwidth Optimized

ZYNQ-7000

SoC Optimized

Zynq®-7000 Devices



UltraSCALE+

Cost-Optimized Portfolio

16nm Performance/Watt

ARTIX UltraSCALE+

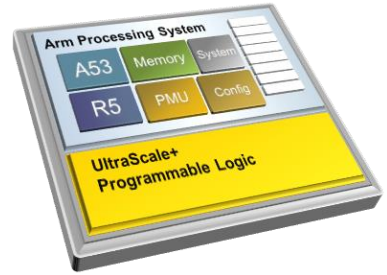
Bandwidth Optimized

- 16Gb/s Transceivers
- Multi-Level Security
- Highest DSP Compute

ZYNQ UltraSCALE+

SoC Optimized

ZU1, ZU2, ZU3 Devices



- Dual- / Quad-Core Arm® Cortex™-A53
- Scalable across ZU+ Portfolio
- Ultra-Compact Form Factor

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Enabling Ultra-Compact Edge Applications Demanding High Compute

ZYNQ UltraSCALE+

ZU1, ZU2, ZU3 Devices

ARTIX UltraSCALE+

Medical

Defibrillators

Patient Monitors

Infusion Pumps

Portable Ultrasound

Industrial

Machine Vision

Industrial Networking

Smart Sensors

Motor Control

Electric Drives

Test Equipment

Hand-Held Oscilloscopes

Application Test Equipment

AV & Broadcast

Cameras

Camera Monitors

KVM Dongles

Mini Converters

A&D

Milcom Radio

Public-Safety Radio

Munition & EW

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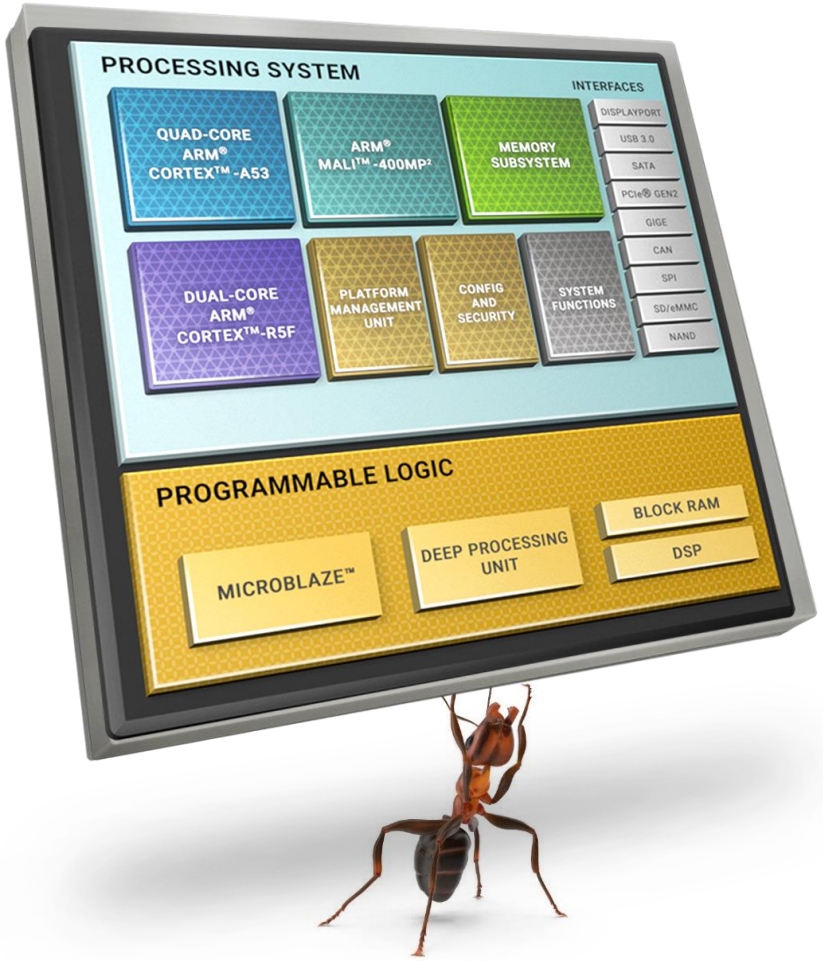
The New ZU1 Device: Small But Mighty

Lowest Cost, Lowest Power in Zynq UltraScale+ Portfolio



- Lowest Power, Lowest Cost Adaptive SoC in the Portfolio
  - Ideal for edge and battery-powered applications
- Highest I/O-to-Logic Cell Ratio
  - 400 I/Os for any-to-any connectivity
- Highest DSP-to-Logic Cell Ratio
  - Maximum compute and AI offloading for smart applications
- Same Multiprocessing Arm® processing power
  - Application software scalability across the portfolio

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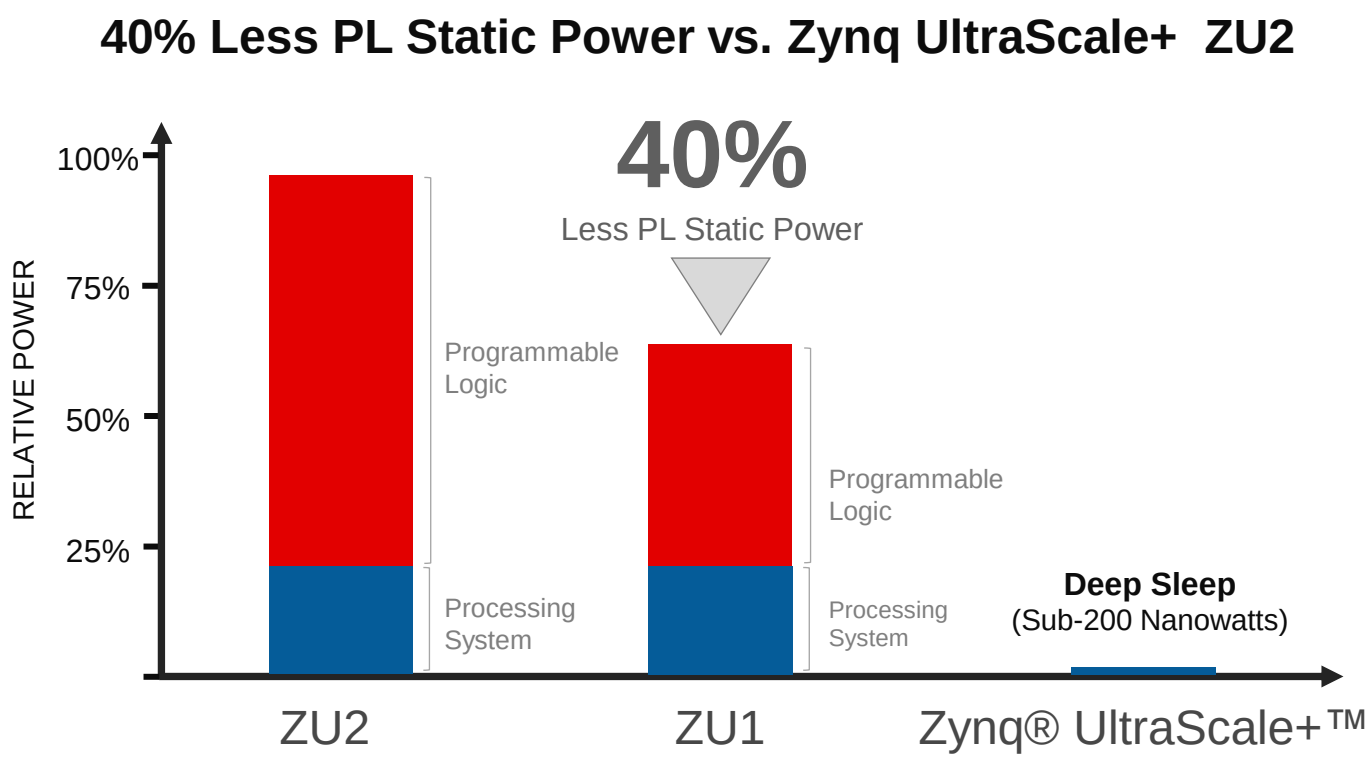
Lowest Power in Zynq UltraScale+ Portfolio

- 40% less programmable logic (PL) static power vs. ZU2 (but only 20% less fabric)
- Same Arm® processing system in a smaller overall power footprint
- Power-down unused blocks for deep sleep as low as 180 nanowatts



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The New Artix® UltraScale+™ FPGA Family

Serial I/O Performance

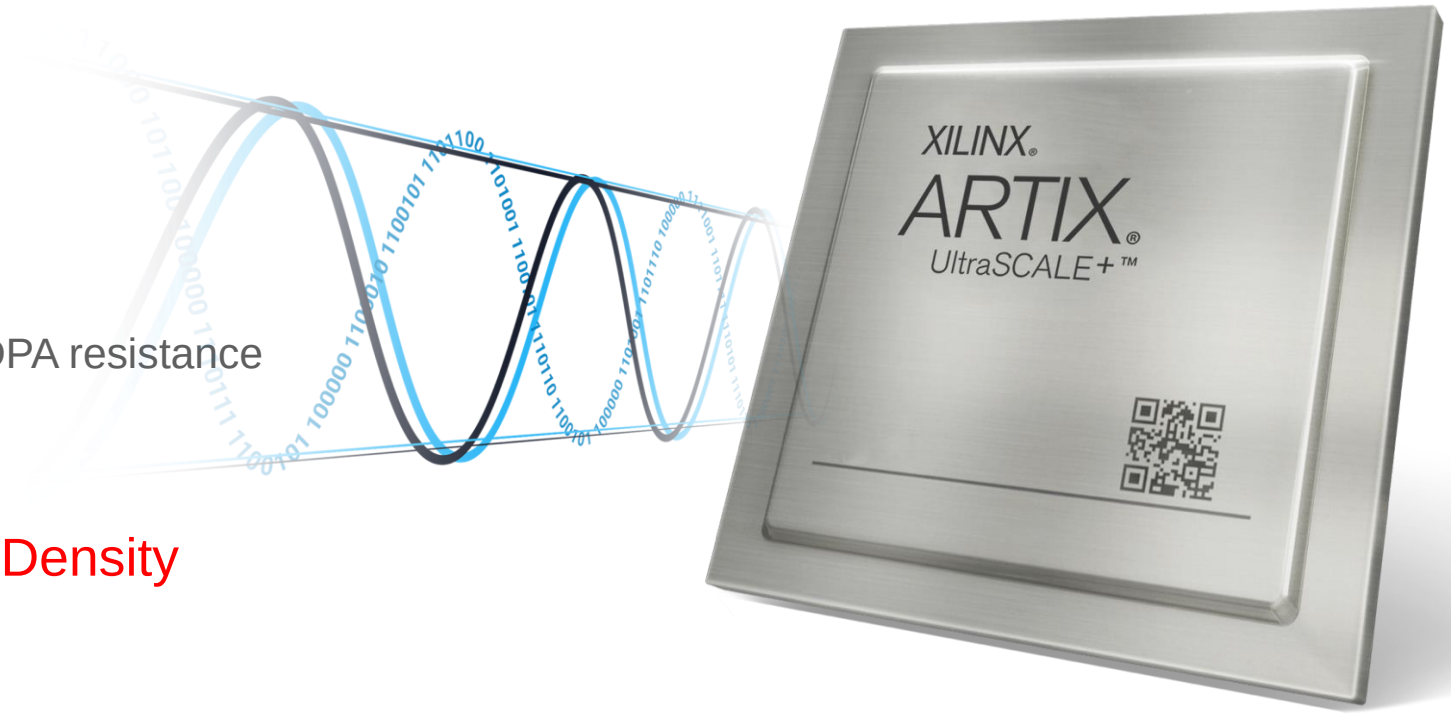
16Gb/s transceivers for advanced protocols in a cost-optimized family

Multi-Level Security

Cryptography, authentication, and DPA resistance for cybersecurity and IP protection

Signal Processing Compute Density

Best-in-Class DSP bandwidth in small form-factor packaging



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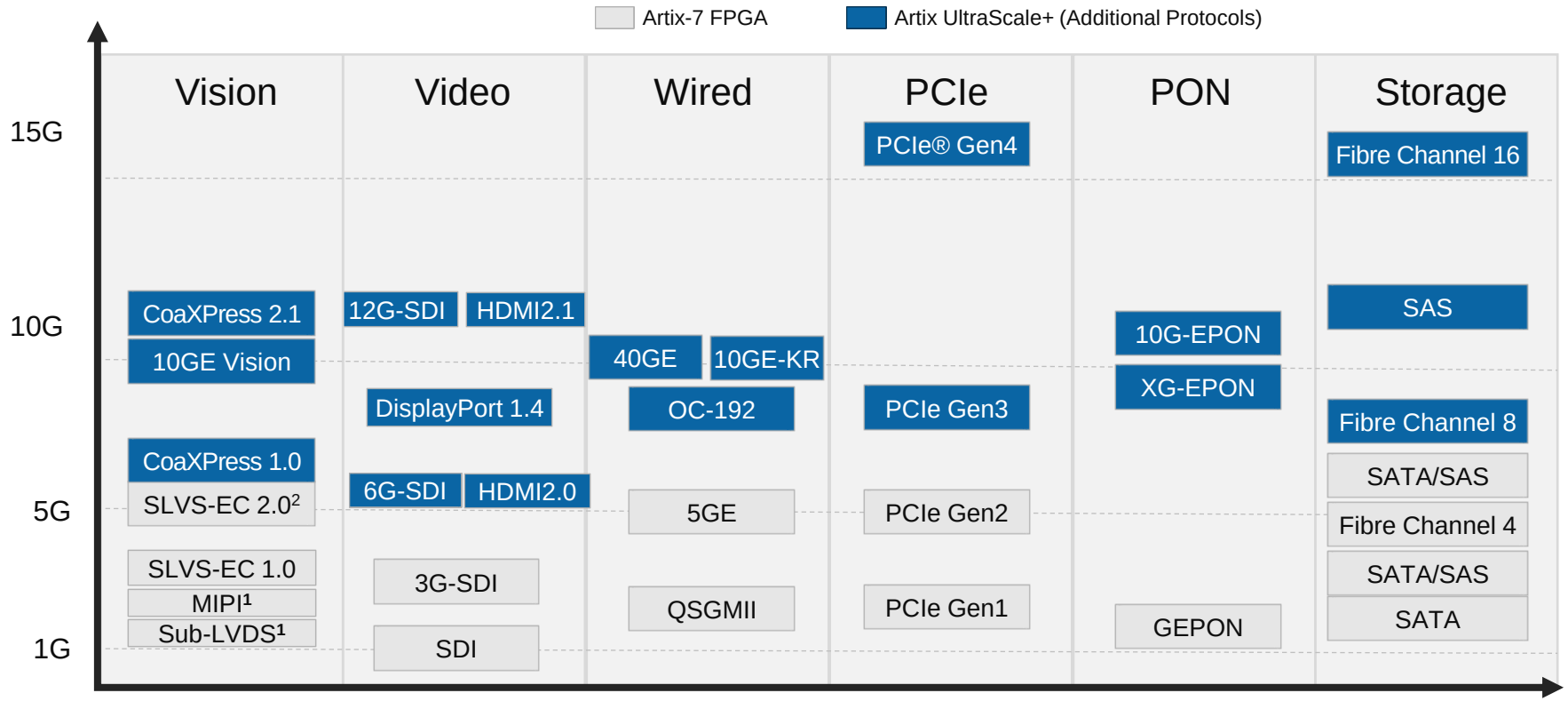
Target Artix UltraScale+ Applications and Protocols

- Up to 192 gigabits of aggregate bandwidth, including the smallest device!
- Supports emerging protocols in vision, video, networking and storage



1: Artix® UltraScale+™ delivers 2500Mb/s LVDS/MIPI performance vs. Artix-7 at 1500MB/s
2: Artix UltraScale+ supports up to 12 lanes of SLVS-EC 2.0 in 19mm package

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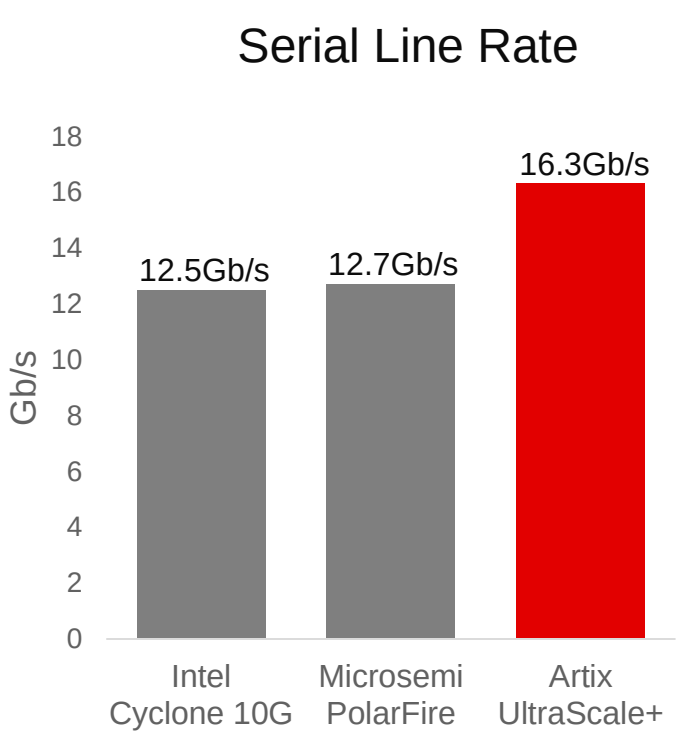
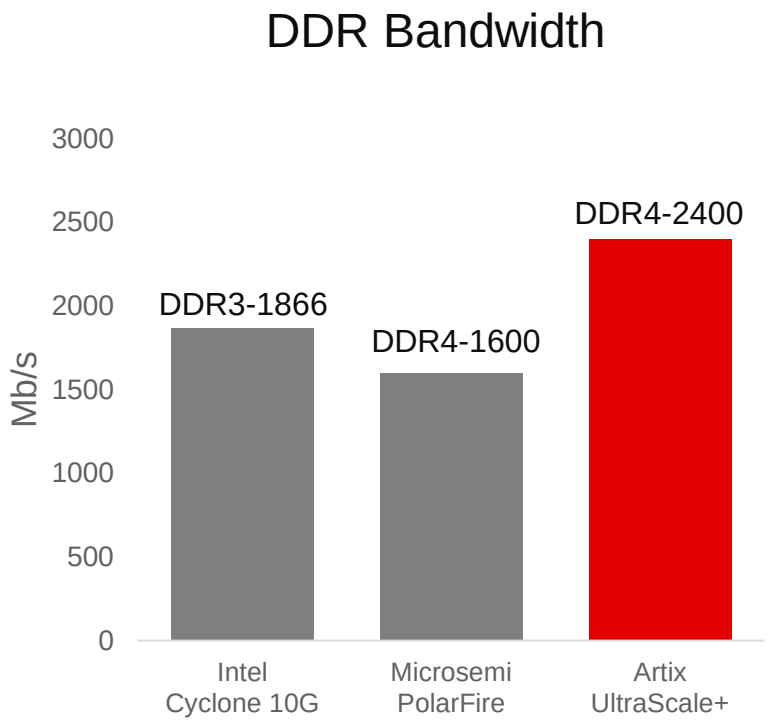
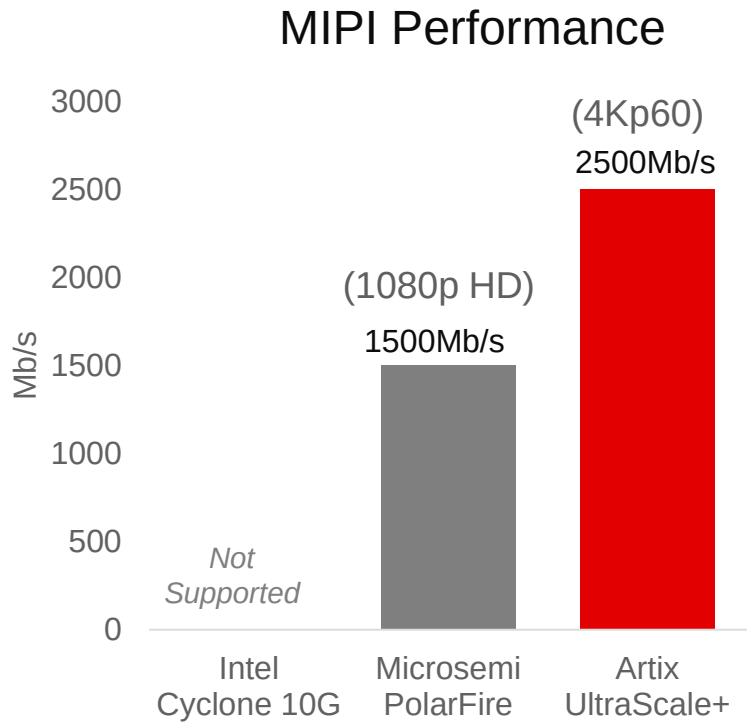
Best-in-Class FPGA I/O Performance (vs. Competition)

- Highest SerDes rates for advanced protocols (including PCIe® Gen4) in a cost-optimized device
- Highest DDR memory performance
- Highest MIPI performance for latest vision sensors (“4K/8K Ready”)







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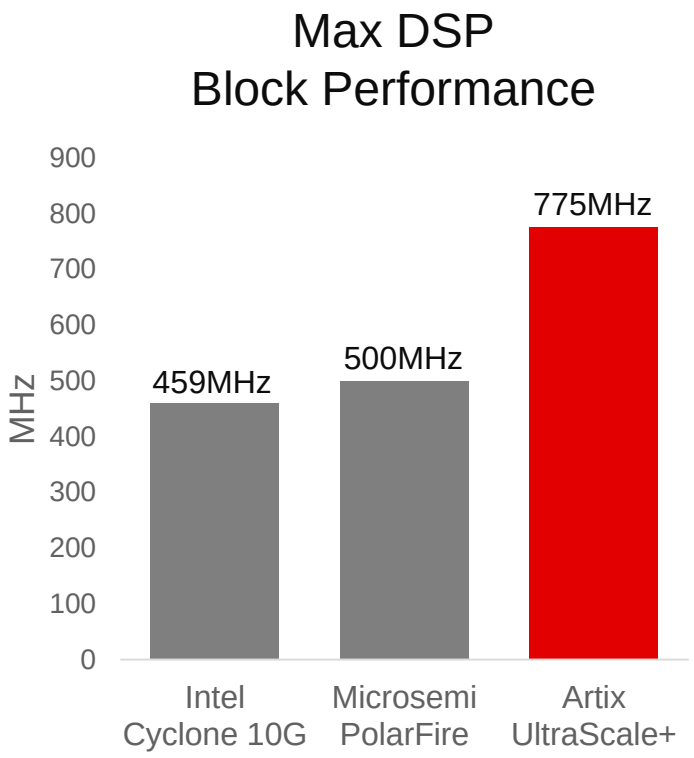
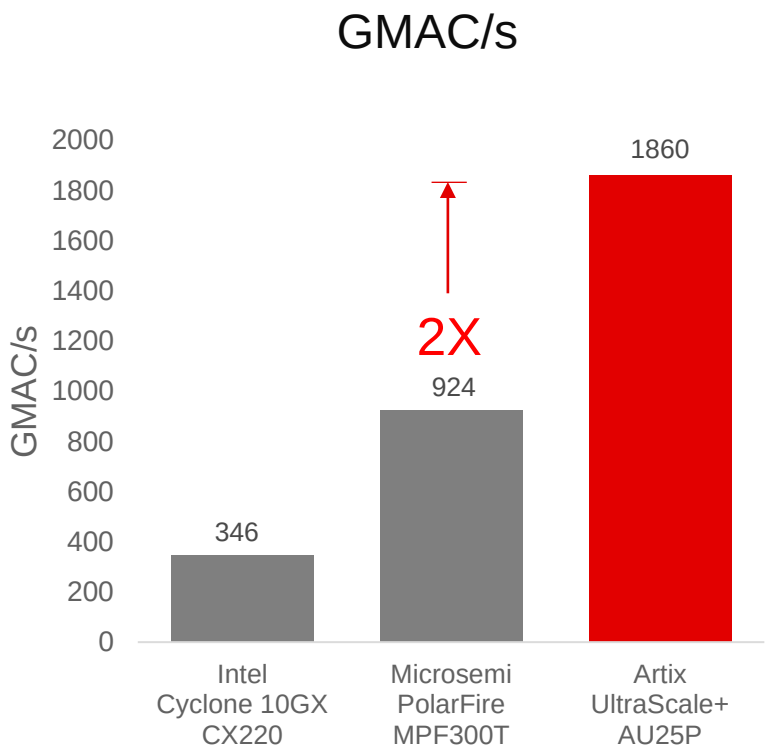
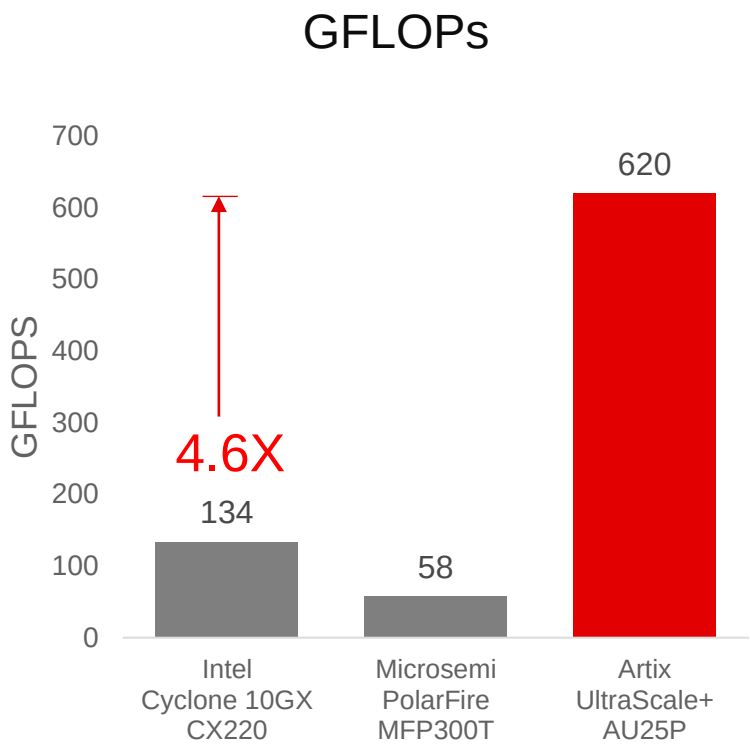
Best-in-Class FPGA Signal Processing & Compute

- Highest performance DSP, optimized for fixed-point and floating point
- Flexible for diverse forms of compute for image & video processing, real-time control, and AI inference







Source for Intel Cylcone10GX: Intel Cyclone 10 GX FPGAs Product Table
Source for Microsemi PolarFire: MicroSemi PolarFire FPGA Data Sheet, CoreFPU v2.0 Handbook,

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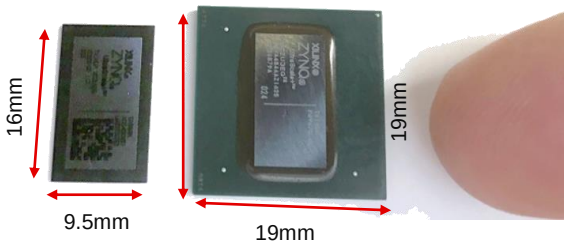
Ultra-Compact InFO (Integrated Fan-Out) Packaging

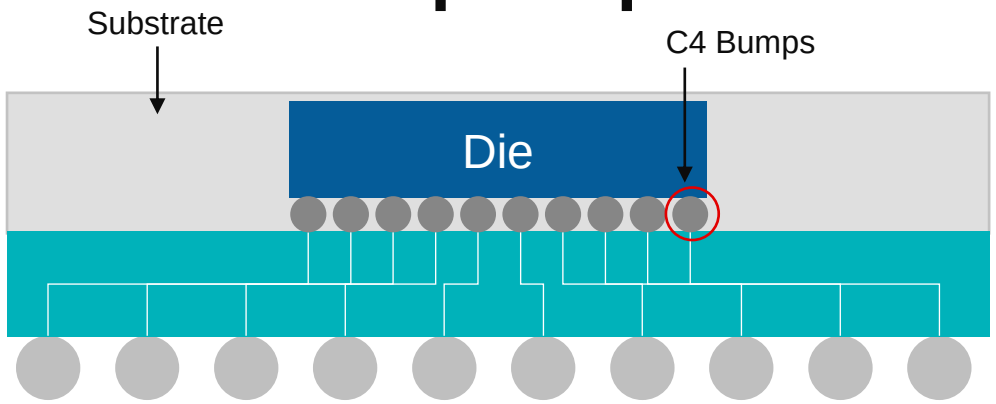
- Smaller and thinner package (no substrate or C4 bumps)
- “Near die size” ball pitch (0.5mm) for no loss of pins
- 60% less area for better thermal & power distribution
- Shorter interconnects for lower flight times and better signal integrity
- PCB and thermal guidelines available (EA)

60%
Less Area

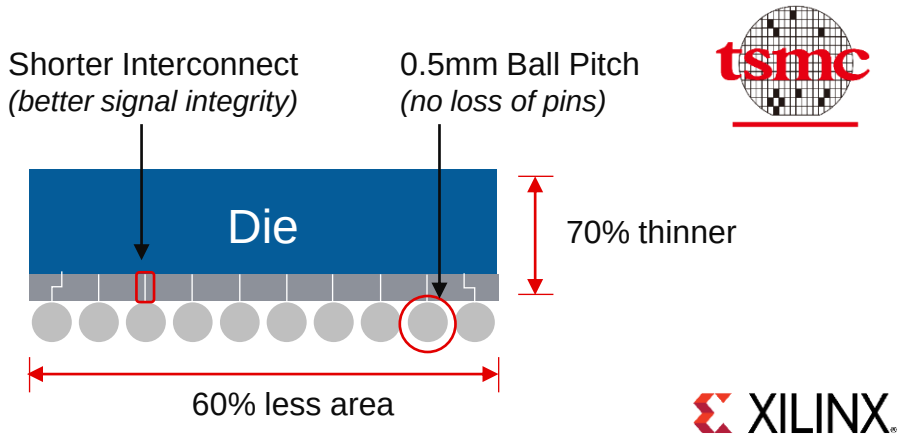


70%
Thinner

Flip Chip

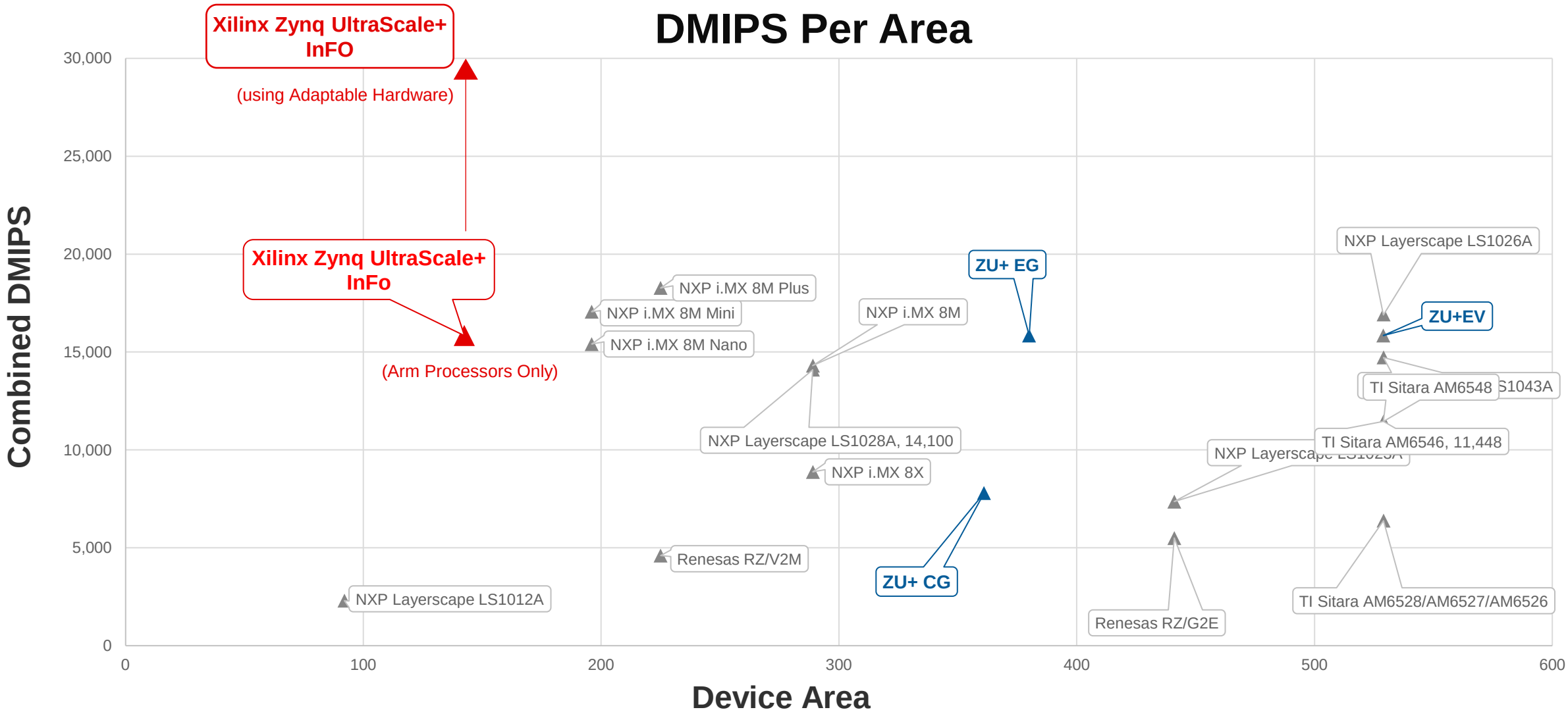


InFO



Zynq® UltraScale+™ InFO : Compute Density Like No Other

…And That's Just the Processing System!



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Scalability: Preserve Your Design Investments and Scale Your End-Products across the Same Platform

Device Architecture

- Scalable logic resources
- Scalable AI processing power
- Package & pin migration

SW & Tool Flow

- **Vivado®** for HW design
- **Vitis™** for SW developers
- **Vitis AI** for data scientists
- Same SW code base

Ecosystem

- Hardware IP
- OS support

Product Life Cycle

- Industrial grade life cycle
- Safety/Security certification

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16nm UltraScale+ FPGA and MPSoC Scalability

FPGAs

New Cost-Optimized Family

ARTIX UltraSCALE+

- Up to 309K System Logic Cells
- Up to 1,200 DSP Slices
- 16Gb/s Transceivers

Price/Performance/Watt

KINTEX UltraSCALE+

- Up to 1,843K System Logic Cells
- Up to 3,528 DSP Slices
- 32.75Gb/s Transceivers

Highest Performance and Logic Density

VIRTEX UltraSCALE+

- Up to 8,938K System Logic Cells
- Up to 12,288 DSP Slices
- Up to 58Gb/s Transceivers

Zynq UltraScale+ MPSoCs

New ZU1 Device

CG Devices

- **Dual**-Core Arm® Cortex®-A53 up to **1.3GHz**
- Dual-Core Arm Cortex-R5F up to **533MHz**
- Up to 600K System Logic Cells

EG Devices

- **Quad**-Core Arm Cortex-A53 up to **1.5GHz**
- Dual-Core Arm Cortex-R5F up to **600MHz**
- Arm Mali™-400MP2 GPU
- Up to 1,143K System Logic Cells

EV Devices

- Quad-Core Arm Cortex-A53 up to 1.5GHz
- Dual-Core Arm Cortex-R5F up to 600MHz
- Arm Mali-400MP2 GPU
- **Video Codec H.264/H.265**
- Up to 504K System Logic Cells

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Artix® UltraScale+™ Product Table

	Device	AU10P	AU15P	AU20P	AU25P
Programmable Functionality	System Logic Cells (K)	96	170	238	308
	CLB Flip-Flops (K)	88	155	218	282
	CLB LUTs (K)	44	77	109	141
Memory	Max. Distributed RAM (Mb)	1.0	2.5	3.2	4.7
	Total Block RAM (Mb)	3.5	5.1	7.0	10.5
	36K Block RAM Blocks	100	144	200	300
	UltraRAM (Mb)	-	-	-	-
Clocking	Clock Management Tiles (CMTs)	3	3	3	4
Integrated IP	DSP Slices	400	576	900	1200
	PCI Express® Gen 3x8 / Gen4x2	PCIe Gen 4	PCIe Gen 4	PCIe Gen 3	PCIe Gen 3
	AMS - System Monitor	1	1	1	1
I/O and GT	HD I/O	72	72	72	96
	HP I/O	156	156	156	208
	Gigabit Transceivers	12	12	12	12
Packaging (HD I/O, HP I/O, GT)	SFVB784 (23x23) @ 0.8mm – 12.5G			72, 156, 12	96, 208, 12
	FFVB676 (27x27) @ 1.0mm – 16.375G	72, 156, 12	72, 156, 12	72, 156, 12	72, 208, 12
	SBVB484 (19x19) @ 0.8mm – 12.5G	48, 156, 12	48, 156, 12		
	UBVA368 (11.5x9.5)@0.5mm- 12.5G	24, 104, 8	24, 104, 8		

*PCIe Compatible only (not compliance)

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Zynq® UltraScale+™ MPSoC Cost-Optimized Devices

	Devices	ZU1 CG / EG	ZU2 CG / EG	ZU3 CG / EG
APU	A53 MPCores	2 / 4	2 / 4	2 / 4
	APU L2 Cache Size (MB)	1	1	1
RPU	R5F MPCores (2)	1	1	1
GPU	Mali™-400 MP2	N / Y	N / Y	N / Y
Programmable Functionality	System Logic Cells (K)	81	103	154
	CLB Flip-Flops (K)	74	94	141
	CLB LUTs (K)	37	47	71
Memory and DSP	Max. Distributed RAM (Mb)	1.0	1.2	1.8
	Total Block RAM (Mb)	3.8	5.3	7.6
	36K BRAM Blocks	108	150	216
	DSP Slices	216	240	360
Clocking	Clock Management Tiles (CMTs)	3	3	3
Peripherals	Baseline	Baseline	Baseline	Baseline
Integrated IP	AMS - System Monitor	1	1	1
Hard PS DDR	DDR 32/64 Bit	64-bit	64-bit	64-bit
Other	USB 3.x	2	2	2
	Gigabit Ethernet	4	4	4
I/O and GT	PS I/O @ [LP] DDR4 2400	214	214	214
	HD I/O (1.2 – 3.3V)	24	96	96
	HP I/O (1.0 – 1.8V) @ DDR4	156	156	156
	PS GTR @ 6Gb/s	4	4	4
Packages (PS I/O, HD I/O, HP I/O, GTR)	SFVC784 (23x23) @ 0.8mm	214, 24, 156, 4	214, 96, 156, 4	214, 96, 156, 4
	SFVA625 (21x21) @ 0.8mm	170, 24, 156, 4	170, 24, 156, 4	170, 24, 156, 4
	SBVA484 (19x19) @ 0.8mm	170, 24, 58, 4	170, 24, 58, 4	170, 24, 58, 4
	UBVA (9.5x16) @ 0.5mm		170, 24, 58, 4	170, 24, 58, 4
	UBVA (9.5x15) @ 0.5mm	170, 24, 58, 4		

How Customers Can Get Started

ZU1, ZU2, ZU3 Devices

- Documentation Available March 26
- EA Tools Available March 26
- ZU2, ZU3 InFO Pre-Production Now
  - Prod. in Q3
- ZU1 Pre-Production in Q3'21
  - Prod. in Q4

- Documentation Available Q2'21
- Tools Available Q3'21
- AU20, AU25 Production Q3'21
- AU15, AU10 Pre-Production Q1'22

The New UltraScale+ FPGA & SoC Cost-Optimized Portfolio

Industry's Leading 16nm Performance/Watt for Cost-Sensitive Applications

New Small Form-Factor Packaging for Industry's Highest Compute Density

Scalability across the UltraScale+™ Portfolio to Preserve Your Design Investments

Industry's Highest Compute Density for Ultra-Compact Edge and Networking Applications

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Thank You