MULTI-FEATURE DRIVER ASSISTANCE PROCESSING EFFICIENCY IN A LOW-COST, LOW-POWER, FLEXIBLE SOC ARCHITECTURE

XILINX AUTOMOTIVE ZYNQ-7000 ALL PROGRAMMABLE SOCS

Xilinx Solution Highlights

- Highly integrated All Programmable system-on-a-chip (SoC) architecture
- Fully programmable hardware, software and I/O for a completely flexible platform
- Low-power and low device count, compared to traditional multi-chip designs
- Complete ecosystem of software, IP, design tools, and design services
- Part of a portfolio with a proven, industry-leading track record
- XA devices are fully automotive-qualified with extended, Q-grade temperature ranges
- Xilinx is ISO-9001 and ISO-14001 certified, and compliant to ISO-TS16949. Qualification testing for XA Zynq devices exceed AEC-Q100 requirements

Xilinx Automotive-Grade (XA) Zynq®-7000 All Programmable SoCs ideally address the technical and business challenges for one of the fastest growing automotive applications: Advanced Driver Assistance Systems (ADAS). The automotive-grade devices deliver unprecedented design flexibility as a single chip that combines a dual-core ARM® Cortex-A9 processor, high-speed programmable I/O, and flexible programmable logic including DSP blocks for hardware acceleration of critical design components.

The increased system performance and highly integrated architecture of the Xilinx All Programmable SoCs reduce overall power and bill of materials (BOM) cost. The XA Zynq-7000 devices also enable end product differentiation with complete control of IP, and help system designers keep up with constantly changing feature requirements. Both engineers and business teams benefit from the Xilinx ecosystem that lowers time to market and trims life cycle costs to contribute to profitability.

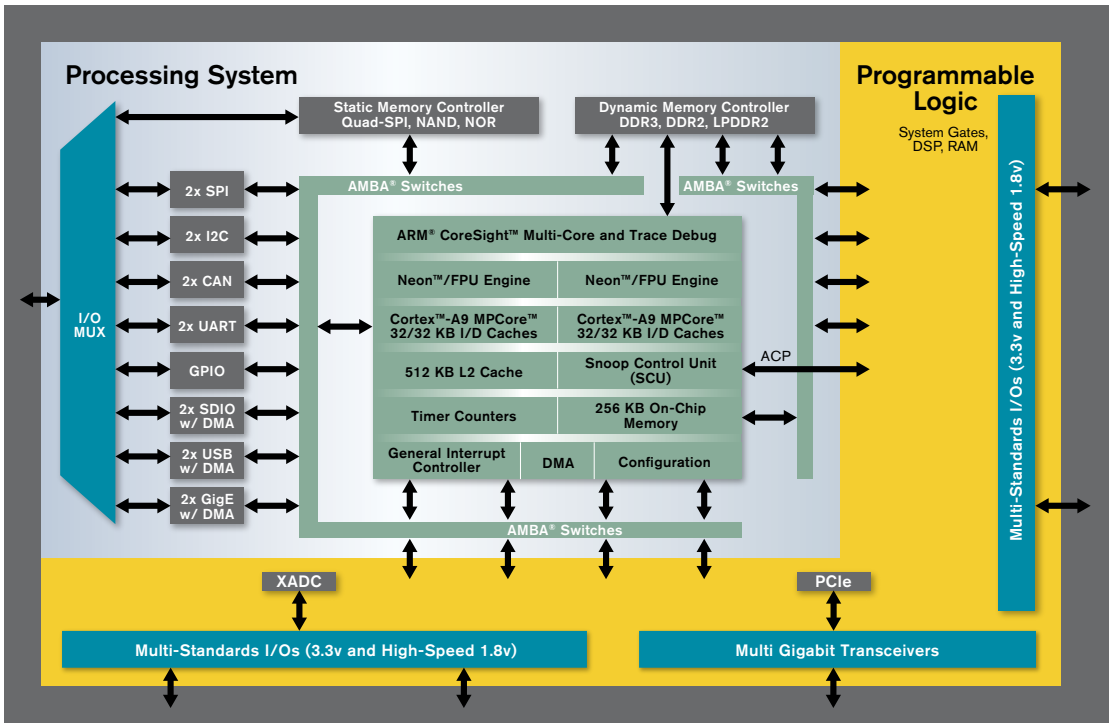
TOTAL DRIVER ASSISTANCE SOLUTION

TECHNICAL NEEDS	BUSINESS NEEDS
▪ System performance ▪ Total power ▪ System integration ▪ Total BOM cost ▪ Accelerated design time	▪ IP ownership ▪ Differentiation ▪ Total cost of ownership ▪ Time-to-market

XA Zynq-7000 All Programmable SoCs are ideally suited for meeting both the business and technical needs seen by today's advanced driver assistance system designers – making it the total driver assistance solution.

XILINX
ALL PROGRAMMABLE™

XA ZYNQ-7000 ALL PROGRAMMABLE SOC ARCHITECTURE



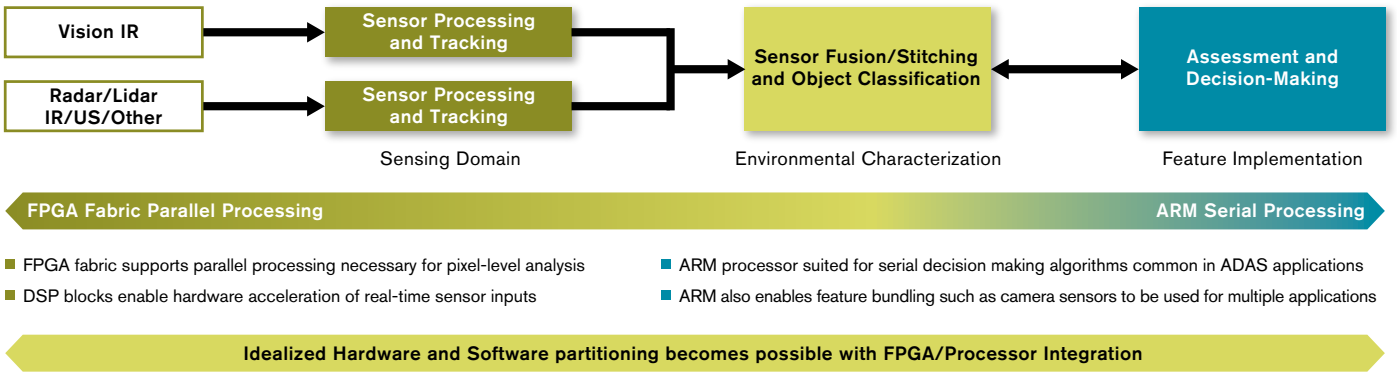
The software programmability of the dual-core ARM™ Cortex-A9 processor is combined with the hardware programmability of FPGA logic. Large amounts of on-chip programmable I/O and AXI-based interconnects complete the All Programmable SoC, enabling unprecedented advanced design possibilities. Designers can accelerate complex image and video processing with the flexibility to support 360° surround view, blind spot detection, pedestrian sensing, lane departure warning and more.

Three-to-One Device Consolidation

Four primary functional components make up most ADAS solutions. In the past, an optimal system usually required some combination of customized, parallel hardware to process high-bandwidth sensor data, another device for serial element processing, and software running on a processor to characterize the environment, make appropriate decisions and communicate to the vehicle bus.

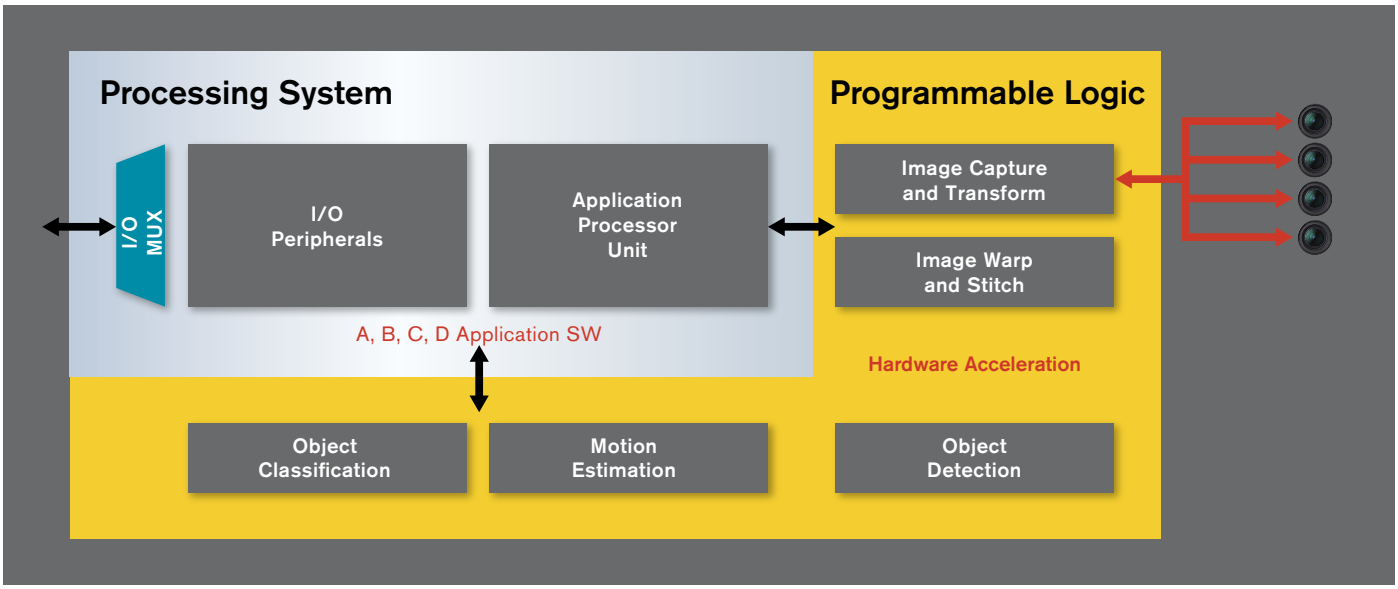
XA Zynq-7000 All Programmable SoCs radically change driver assistance design. Instead of three chips, the single device supports a homogeneous software-centric architecture with optimal hardware and software partitioning for functional acceleration.

DRIVER ASSISTANCE WORKFLOW



A sensor function processes data at a pixel level to enhance image quality or extract object information. An environmental characterization function carries out additional processing by identifying and tracking lane markers, signs, other vehicles, pedestrians, and other environmental objects. Features like vehicle rear view, or surround view, call for additional video processing, and decision-making functionality can warn the driver of potential threats.

XA ZYNQ-7000 ALL PROGRAMMABLE SOC ADAS IMPLEMENTATION



Traditionally, driver assistance solutions were implemented using multiple devices: image capture and pixel processing were often performed in hardware by an FPGA or ASIC; serial element/object processing was typically performed in software on a DSP processor; and a traditional microprocessor could handle frame-level processing and vehicle communication. Zynq-7000 All Programmable SoCs provide a high-bandwidth AXI interconnect between processor and logic, enabling a tightly integrated SoC platform for next-generation driver assistance. Traditional DSP processing can be performed in either logic (DSP slices) or in software aided by the Cortex A9 NEON vector processor.

28nm Leadership: High Performance and Low Power

The highly integrated Zynq-7000 All Programmable SoCs boost overall system performance by more than 130% compared with traditional multi-chip solutions. Power is cut in half, with the elimination of power-hungry and bandwidth-limited chip-to-chip interfaces, and BOM costs are similarly reduced by 25% with the consolidation of multiple functions on a single device.

Speed Time-To-Market and Maximize Control of Ownership

The rapidly changing Driver Assistance market calls for aggressive time to market. Designers choosing Zynq-7000 All Programmable SoCs can maximize productivity with tightly integrated development tools, and the availability of broad range of third-party software, IP, and reference designs from the Xilinx Alliance Program ecosystem. With a long history of success in the automotive industry, Xilinx also offers in-house expertise in support of designers at every phase of the design life cycle.

Unlike other platforms, Zynq All Programmable SoCs let OEM suppliers combine third-party software and IP with proprietary content that maximizes differentiation in the marketplace without the high NRE.

XA ZYNQ-7000 ALL PROGRAMMABLE SOC DEVICE FAMILY

		XA Zynq®-7000 All Programmable SoC				
	Device Name	Z-7010		Z-7020		Z-7030
	Part Number	XA7Z010		XA7Z020		XA7Z030
Processing System	Processor Core	Dual ARM® Cortex™-A9 MPCore™ with CoreSight™				
	Processor Extensions	NEON™ & Single / Double Precision Floating Point for each processor				
	Maximum Frequency	667 MHz				
	L1 Cache	32 KB Instruction, 32 KB Data per processor				
	L2 Cache	512 KB				
	On-Chip Memory	256 KB				
	External Memory Support (1)	DDR3, DDR3L, DDR2, LPDDR2				
	External Static Memory Support (1)	2x Quad-SPI, NAND, NOR				
	DMA Channels	8 (4 dedicated to Programmable Logic)				
	Peripherals	2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO				
	Peripherals w/ built-in DMA (1)	2x USB 2.0 (OTG), 2x Tri-mode Gigabit Ethernet, 2x SD/SDIO				
	Security (2)	AES and SHA 256b Decryption and Authentication for Secure Boot				
	Processing System to Programmable Logic Interface Ports (Primary Interfaces & Interrupts Only)	2x AXI 32b Master, 2x AXI 32b Slave, 4x AXI 64b/32b Memory AXI 64b ACP 16 Interrupts				
Programmable Logic	Xilinx 7 Series Programmable Logic Equivalent	Artix®-7 FPGA		Artix®-7 FPGA		Kintex®-7 FPGA
	Programmable Logic Cells (Approximate ASIC Gates (3))	28K Logic Cells (~430K)		85K Logic Cells (~1.3M)		125K Logic Cells (~1.9M)
	Look-Up Tables (LUTs)	17,600		53,200		78,600
	Flip-Flops	35,200		106,400		157,200
	Extensible Block RAM (# 36 Kb Blocks)	240 KB (60)		560 KB (140)		1,060 KB (265)
	Programmable DSP Slices (18x25 MACCs)	80		220		400
	Peak DSP Performance (Symmetric FIR)	100 GMACs		276 GMACs		593 GMACs
	PCI Express® (Root Complex and End Point)	–		–		Gen2 x4
	Analog Mixed Signal (AMS) / XADC (1)	2x 12 bit, MSPS ADCs with up to 17 Differential Inputs				
	Security (2)	AES and SHA 256b Decryption and Authentication for Secure Programmable Logic Configuration				
Speed Grades	Automotive (I-Grade) (Tj=–40°C to 100°C)	-1				
	Automotive (Q-Grade) (Tj=–40°C to 125°C)	-1				
Packages	Package Type (4)	**CLG225 (1)**	**CLG400**	**CLG400**	**CLG484**	**FBG484**
	Size (mm)	13x13	17x17	17x17	19x19	23x23
	Pitch (mm)	0.8	0.8	0.8	0.8	1.0
	Processing System User I/Os (excludes DDR dedicated I/Os) (5)	32	54	54	54	54
	Multi-Standards and Multi-Voltage SelectIO™ Interfaces (1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V)	54	100	125	200	100
	Multi-Standards and Multi-Voltage High Performance SelectIO Interfaces (1.2V, 1.35V, 1.5V, 1.8V)	–	–	–	–	63
	Serial Transceivers	–	–	–	–	4
	Maximum Transceiver Speed (Speed Grade Dependent)	NA	NA	NA	NA	6.6 Gb/s

XMP088 (v1.1DRAFT)

Notes: 1. Z-7010 in CLG225 has restrictions on PS peripherals, Memory interfaces, and I/Os. Please refer to the Technical Reference Manual for more details.

2. Security block is shared by the Processing System and the Programmable Logic.

3. Equivalent ASIC gate count is dependent of the function implemented. The assumption is 1 Logic Cell = ~15 ASIC Gates.

4. Devices in the same package are pin-to-pin compatible.

5. Static memory interface combined with the usage of many peripherals could require more than 54 I/Os. In that case, the designer can use the Programmable Logic SelectIO interface.

Preliminary product information. Subject to change. Please contact your Xilinx representative for the latest information.

Take the NEXT STEP

To learn more about the XA Zynq-7000 All Programmable SoC family, please visit **www.xilinx.com/XAZynq** or contact a local sales office.

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