Smarter Vision IP and Reference Designs – Connectivity

IP Design Target

Resource	Type	Provider	Applications	Device Family Support	Programmable Logic	ARM Processing System
1 Gigabit Ethernet AVB Endpoint • Ethernet AVB has been merged as a licensed feature in TEMAC v5.2 and higher • Designed to the following IEEE specifications: P802.1AS, P802.1Qav • Supports AVB Endpoint talker and/or listener functionality • Seamless connection to the Xilinx Tri-Mode Ethernet MAC • Supports Ethernet speeds of 100 MB/s and 1Gbps • Software drivers included to implement P802.1AS	LogiCORE IP	Xilinx, Inc.	• Advanced Driver Assistance • Professional Audio	• Zynq-7000 • Artix-7 • Kintex-7 • Virtex-7	X	
1 Gigabit Ethernet AVB IP Suite • Ethernet AVB has been merged as a licensed feature in TEMAC v5.2 and higher • Designed to the following IEEE specifications: P802.1AS, P802.1Qav • Supports AVB Endpoint talker and/or listener functionality • Seamless connection to the Xilinx Tri-Mode Ethernet MAC • Supports Ethernet speeds of 100 MB/s and 1Gbps • Software drivers included to implement P802.1AS	Alliance Member IP	Digital Design Corp.	• Advanced Driver Assistance • Professional Audio	• Spartan-6		
AFDX (ARINC 664) • DO-254 certifiable • ARINC 664 part 7 (AFDX®) defines a standard for deterministic data transfers in a network for safety-critical applications • Utilizes dedicated bandwidth-regulated traffic control while providing deterministic Quality of Service (QoS) • Based on IEEE 802.3 Ethernet, and its main aspects include full-duplex switched and profiled Ethernet, redundancy management, and high-speed performance • Guaranteed bandwidth and elimination of transmission collisions provide high data integrity and deterministic timing	Alliance Member IP	TTTech	• Aerospace & Defense	• Virtex-5	X	
Asynchronous Sample Rate Converter (ASRC) • Fully Asynchronous Up-Conversion, Down-Conversion, and 1:1 Asynchronous Conversion • -133 dB THD + N Typical (Range: -126 dB to -139 dB) • Input Rates 8 kHz to 192 kHz; Output Rates 8 kHz to 192 kHz; Conversion Ratio 1:7.5 (Down) to 8:1 (Up); All Continuous	LogiCORE IP	Xilinx, Inc.	• Broadcast Camera • Professional Audio • Video Conferencing	• Spartan-6 • Virtex-6	X	

Smarter Vision IP and Reference Designs – Connectivity

IP Design Target

Resource	Type	Provider	Applications	Device Family Support	Programmable Logic	ARM Processing System
Bridging Xilinx Streaming Video Interface with the AXI4-Stream Protocol (XAPP521) The ARM® core AMBA® specification (version 4.0) AXI interconnect standard includes three Advanced eXtensible Interface version 4 (AXI4) interconnect protocols—AXI4 interconnect, AXI4-Lite protocol, and AXI4-Stream interconnect. The Xilinx AXI video direct memory access (AXI VDMA) core is offered with an AXI4-Stream interface for video data. Video applications that require the video data to be buffered in memory need an AXI4-Stream interface to connect with the AXI VDMA. This application note details bridging an XSVI interface to an AXI4-Stream interface, enabling video designs with Xilinx video IP cores and XSVI interfaces to use the AXI VDMA.	Reference Design	Xilinx, Inc.	• Broadcast Camera • Video Conferencing • Displays/Projectors • Automotive • ISM • Aerospace & Defense	• Zynq-7000 • Artix-7 • Kintex-7 • Virtex-7	X	
CAN • Designed to ISO 11898-1, CAN2.0A and CAN2.0B specifications • Supports bit rates up to 1Mbps as per CAN2.0B specification • Transmit and Receive message FIFOs with a user configurable depth of up to 64 messages • Parameterized Acceptance Filtering of up to 4 programmable filters • Supports sleep mode with automatic wakeup • Transmit prioritization through one High Priority Transmit buffer • Maskable error and status interrupts • Automatic re-transmission on errors or arbitration loss • Compatible with 3.3V external CAN PHY chips	LogiCORE IP	Xilinx, Inc.	• Automotive • ISM	• Zynq-7000 • Artix-7 • Kintex-7 • Virtex-7	X	
CoaXPress • CoaXpress specifies a high speed protocol and direct interface to data acquisition devices • Supports transfer of data, messages and events (e.g. image data to PC frame grabber) • All communication and device power is transmitted over a single 75Ohm coaxial cable • Widely used for PAL/NTSC cameras at transfer speeds of up to 6.125GbE cable	Alliance Member IP	Sensor to Image	• ISM	• Spartan-6 • Virtex-6	X	

Smarter Vision IP and Reference Designs – Connectivity

IP Design Target

Resource	Type	Provider	Applications	Device Family Support	Programmable Logic	ARM Processing System
Display Panel Interface - LVDS Source Synchronous 7:1 Serialization and Deserialization Using Clock Multiplication (XAPP585) This application note describes how to use ISERDES and OSERDES efficiently in conjunction with the mixed-mode clock manager (MMCM) or phase-locked loop (PLL) for reception and transmission of 7:1 data using low-voltage differential signaling (LVDS) data transmission at speeds from 415 Mb/s to 1,200 Mb/s per line when using per-bit deskew.	Reference Design	Xilinx, Inc.	• Broadcast Camera • Video Conferencing • Displays/Projectors • Automotive • ISM • Aerospace & Defense	• Zynq-7000 • Artix-7 • Kintex-7 • Virtex-7	X	
DisplayPort 1.2 • Source (Tx) and Sink (Rx) controllers perform encoding/decoding • One, two or four pixel-wide main link for up to 4096x2048 monitor resolution, Quad pixel allows user to get up to 600 Mhz Video Pixel clock • Enhanced Color formats for luminance only mode & gray scale video users • Auto lane rate and width negotiation (1.6 or 2.7 or 5.4 Gbps; 1, 2 or 4 lanes)	SmartCORE IP	Xilinx, Inc.	• Broadcast Camera • Video Conferencing • Displays/Projectors • ISM	• Spartan-6 • Virtex-6 • Artix-7 • Kintex-7 • Virtex-7	X	
Gigabit Ethernet Vision • Implementation of Gigabit Ethernet Vision Protocol • Hardware Implementation of Stream Channel to reach maximum throughput • Bidirectional Streaming supported • Control Channel handled by embedded CPU • Packet Resend supported. • Tiny SDRAM controller available or MPMC supported	Alliance Member IP	Sensor to Image	• ISM	• Spartan-6 • Virtex-6	X	
HDMI 1.3 - Implementing a TMDS Video Interface in the Spartan-6 FPGA (XAPP495) This application note describes a set of reference designs able to transmit and receive DVI and HDMI data streams up to 1080 Mb/s using the native TMDS I/O interface featured by Spartan®-6 FPGAs.	Reference Design	Xilinx, Inc.	• Broadcast Camera • Video Conferencing • Displays/Projectors • Automotive • ISM • Aerospace & Defense	• Spartan-6	X	

Smarter Vision IP and Reference Designs – Connectivity

IP Design Target

Resource	Type	Provider	Applications	Device Family Support	Programmable Logic	ARM Processing System
Implementing SMPTE SDI Interfaces with Kintex-7 GTX Transceivers (XAPP592) The SMPTE SD-SDI, HD-SDI, and 3G-SDI standards are widely used in professional broadcast video equipment. This document describes how to implement SDI interfaces with GTX transceivers in Kintex-7 FPGAs.	Reference Design	Xilinx, Inc.	• Broadcast Camera • Video Conferencing • Displays/Projectors • ISM	• Kintex-7	X	
Implementing SMPTE SDI Interfaces with Virtex-7 GTX Transceivers (XAPP892) The SMPTE SD-SDI, HD-SDI, and 3G-SDI standards are widely used in professional broadcast video equipment. This document describes how to implement SDI interfaces with GTX transceivers in Virtex-7 FPGAs.	Reference Design	Xilinx, Inc.	• Broadcast Camera • Video Conferencing • Displays/Projectors • ISM	• Virtex-7	X	
Implementing Triple-Rate SDI with Spartan-6 FPGA GTP Transceivers (XAPP1076) This document describes how to implement triple-rate SDI interfaces using Spartan-6 FPGAs.	Reference Design	Xilinx, Inc.	• Broadcast Camera • Video Conferencing • Displays/Projectors • ISM	• Spartan-6	X	
Implementing Triple-Rate SDI with Virtex-6 FPGA GTX Transceivers (XAPP1075) The triple-rate serial digital interface, which supports the SMPTE SD-SDI, HD-SDI, and 3G-SDI standards, is widely used in professional broadcast video equipment. This document describes how to implement triple-rate SDI interfaces with GTX transceivers in Virtex-6 FPGAs.	Reference Design	Xilinx, Inc.	• Broadcast Camera • Video Conferencing • Displays/Projectors • ISM	• Virtex-6	X	
MIPI CSI-2 Controller IP Core • Fully CSI-2 Specification compliant • Transmit and Receive versions • Easy to use pixel-based user interface • Support for all data types • Supports high speed (1+ Gbps) and low power operation • 1-4 data lane support • Delivered fully integrated and verified with target MIPI PHY • Provided with a MIPI CSI-2 Testbench • Complete FPGA-based demonstration system available	Alliance Member IP	Northwest Logic	• Advanced Driver Assistance • Broadcast Camera • Video Conferencing • Displays/Projectors • ISM	• Zynq-7000 • Artix-7 • Kintex-7 • Virtex-7	X	

Smarter Vision IP and Reference Designs – Connectivity

IP Design Target

Resource	Type	Provider	Applications	Device Family Support	Programmable Logic	ARM Processing System
MIPI CSI-2 Demo System • Complete CSI-2 Demonstration Platform • Supports CSI-2 operation using Omnivision MIPI Camera (OV2710) • Utilizes MIPI Interface Card with PHY Test Chip from Mixel • Works with a wide variety of FPGA Mezzanine Connector (FMC) based FPGA boards • Provided with complete FPGA reference design	Alliance Member Reference Design	Northwest Logic	• Broadcast Camera • Video Conferencing • Displays/Projectors • ISM	• N/A	X	
MIPI DSI Controller Core • Fully DSI Specification compliant • Host (Tx) and Peripheral (Rx) versions • 4 data and 1 control/status packet interfaces • Optional DBI & DPI data interface and AXI control/status interface adapters • Support for all data types • Supports high speed (1+ Gbps) and low power operation • 1-4 data lane support • Delivered fully integrated and verified with target MIPI PHY • Provided with a MIPI DSI Testbench • Complete FPGA-based demonstration system available	Alliance Member IP	Northwest Logic	• Advanced Driver Assistance • Broadcast Camera • Video Conferencing • Displays/Projectors • ISM	• Zynq-7000 • Artix-7 • Kintex-7 • Virtex-7	X	
MIPI DSI Demo System • Complete DSI Demonstration Platform • Supports DSI operation using Toshiba DSI-RGB Display Bridge Chip and Seiko Display (70WW2A) • Utilizes MIPI Interface Card with PHY Test Chip from Mixel • Works with a wide variety of FPGA Mezzanine Connector (FMC) based FPGA boards • Provided with complete FPGA reference design	Alliance Member Reference Design	Northwest Logic	• Advanced Driver Assistance • Broadcast Camera • Video Conferencing • Displays/Projectors • ISM	• N/A	X	
MIPI Testbench CSI-2 / DSI • Emulates a MIPI device enabling simulation of a MIPI design • CSI-2 and DSI versions • Transmit and Receive versions • Performs automatic data logging and checking • Provided with a basic set of test cases • Specifically designed for quick out-of-the-box setup and use • Fast simulation speed • CSI and DSI specification compliant	Alliance Member IP	Northwest Logic	• Advanced Driver Assistance • Broadcast Camera • Video Conferencing • Displays/Projectors • ISM	• Zynq-7000 • Artix-7 • Kintex-7 • Virtex-7	X	

Smarter Vision IP and Reference Designs – Connectivity

					IP Design Target	
Resource	**Type**	**Provider**	**Applications**	**Device Family Support**	**Programmable Logic**	**ARM Processing System**
MOST • Adds MOST connectivity to Xilinx FPGAs • Licensed MediaLB technology from SMSC • Compliant with the MLB Specification Version 4.2 • Supports 3-pin and 6-pin interface to INICs • Supported transport methods: synchronous, asynchronous, control and isochronous	Alliance Member IP	Xylon	• Automotive	• Spartan-6	**X**	
SMPTE 2022-5/6 • Supports multiple channels of SD/HD/3G-SDI • SMPTE 2022-6 packetization and de-packetization support with automatic recognition of SDI format to be packetized • SMPTE 2022-5 FEC support with block aligned and non block aligned matrices • Handles SD/HD/3G outages during IP transmission as well as IP packet drops and out-of-order packet handling for IP reception • Timestamp generation and extraction • Stream monitoring and selection of FEC matrix parameters on a stream by stream basis • The standard SMPTE2022 IP license covers both the Tx and Rx IP cores as well as the 10Gb Ethernet MAC IP core	SmartCORE IP	Xilinx, Inc.	• Broadcast Camera • Video Conferencing • Displays/Projectors	• Kintex-7	**X**	
SMPTE 2022-5,6 - High Bit Rate Media Transport over IP Networks with Forward Error Correction (XAPP590) This application note covers the design considerations of a video over IP networks system using the performance features of the LogiCORE IP SMPTE 2022-5/6 video over IP transmitter and receiver cores.	Reference Design	Xilinx, Inc.	• Broadcast Camera • Video Conferencing • Displays/Projectors • ISM		**X**	

Smarter Vision IP and Reference Designs – Connectivity

IP Design Target

Resource	Type	Provider	Applications	Device Family Support	Programmable Logic	ARM Processing System
SMPTE SDI Standards compliance: • SMPTE 259 (SD-SDI), SMPTE 292 (HD-SDI), SMPTE 372 (Dual Link HD-SDI), SMPTE 424 and 425 (3G-SDI) including levels A, B-DL, and B-DS, SMPTE 352 (Payload ID), SMPTE RP-165 (SD-SDI EDH) Triple-Rate SDI Tx & Rx features: • A single reference clock frequency supports reception of five different bit rates o 270 Mb/s SD-SDI o 1.485 Gbps HD-SDI o 1.485/1.001 Gbps HD-SDI o 2.97 Gbps 3G-SDI o 2.97/1.001 Gbps 3G-SDI • Automatically detects incoming SDI standard and bit rate Automatically detects video transport format • Generates and inserts CRC and line numbers for HD-SDI and 3G-SDI	LogiCORE IP	Xilinx, Inc.	• Broadcast Camera • Video Conferencing • Displays/Projectors • ISM	• Zynq-7000 • Artix-7 • Kintex-7 • Virtex-7	X	
Spread-Spectrum Clock Generation in Spartan-6 FPGAs Lowers EMI in Consumer Display Applications This application note and reference design gives examples of a typical spread-spectrum clock for video applications using the Spartan-6 FPGA DCM_CLKGEN primitive. DCM_CLKGEN can be used for fixed spread-spectrum generation without any logic or in a soft spread-spectrum solution using a state machine.	Reference Design	Xilinx, Inc.	• Broadcast Camera • Video Conferencing • Displays/Projectors • Automotive • ISM • Aerospace & Defense	• Spartan-6	X	
V-by-One HS • Independent Transmitter and Receiver module • Protocol compliant with V-by-One® HS standard • Supports 1, 2, 4, and 8 lanes operations	Alliance Member IP	Inrevium	• Broadcast Camera • Video Conferencing • Displays/Projectors • Digital Television	• Spartan-6 • Kintex-7	X	
VCXO Removal (XAPP589) • Replace external voltage controlled crystal oscillator (VCXO) circuits by utilizing functionality within each serial gigabit transceiver in Xilinx FPGAs • Lock an individual GTX channel to up to ±160 ppm from the reference oscillator • Provide jitter cleaning bandwidths in the range from 0.1 Hz to 1 KHz • Typical applications include video SD/HD/3G SDI, Sync E, IEEE1588, SDH, SONET, and OTN	Reference Design	Xilinx, Inc.	• Automotive • Broadcast Camera • Video Conferencing • ISM • Aerospace & Defense	• Kintex-7	X	

Smarter Vision IP and Reference Designs – Encoding

IP Design Target

Resource	Type	Provider	Applications	Device Family Support	Programmable Logic	ARM Processing System
H.264/AVC Baseline Decoder • Supports Constrained Baseline Profile @ Level 4.2 • 8-bit color bit depth • 4:2:0 chroma format • Resolutions from QCIF (176x144) to Full HD(1920x1080) progressive • Frame-rate up to 60 fps for HD decode • Simultaneous multi-channel decode • Validated on custom-built hardware using ITU-T and Fraunhofer test streams • Optimized both for memory and performance • Lower footprint • Supports very low to very high bit-rates • Supports both Intra frame only (H.264 Intra) and Inter frame (IPB) decoding	Alliance Member IP	CoreEL	• Video Conferencing • ISM • Aerospace & Defense	• Spartan-6 • Virtex-6	X	
H.264/AVC Baseline Encoder • Fully compatible with the ITU-T H.264 specification • Profile level 3.1 is supported • Generates I and P frames • Entropy Encoding: CAVLC • Supports YUV 4:2:0 video input • Highly optimized Xilinx FPGA Footprint • Variable Bit Rate (VBR) and Constant Bit Rate (CBR) • Fully synchronous design • Search range: 80 x 48 pixels, Full, ½, ¼ pixel resolution • Support for Single or Multiple slices via firmware control • Support for intra 4 x 4 DC prediction • Supports resolutions up to 4096 x 4096 (multiple instantiations) • Supports simultaneous encoding of multiple streams of arbitrary sizes and compression ratios	Alliance Member IP	A2E	• Video Conferencing • ISM • Aerospace & Defense	• Zynq-7000 • Artix-7 • Kintex-7 • Virtex-7	X	
H.264/AVC Decoder CoreEL's H.264 Decoder IP core is highly pipelined architecture core which can run multi instances of the entropy engines for faster parallel processing. • Fully Validated on custom built hardware using ITU-T and Franhoufer test streams. • Main Profile @ L4.2 and High Profile decode @ L4.2. • Multi-channel decode: 2x1080i 60 fps / 2x1080p 30 fps. • Programmable YUV: 4:2:0, 4:2:2 and 4:4:4 chroma format support and Programmable bit depth 8, 10 or 12 bits . • Single chip FPGA solution optimized both for memory and performance. • Support up to very high bit-rate of 100 Mbps. • Supports both Intra frame only (AVC Intra) and Inter frame (IPB frames) decoding.	Alliance Member IP	CoreEL	• Broadcast Camera • Video Conferencing • Displays/Projectors • Automotive • ISM • Aerospace & Defense	• Kintex-7 • Spartan-6 • Virtex-6	X	

Smarter Vision IP and Reference Designs – Encoding

IP Design Target

Resource	Type	Provider	Applications	Device Family Support	Programmable Logic	ARM Processing System
H.264/AVC Decoder • ISO/IEC14496-10 H.264 High Profile • 1920x1080 • Up to 60 fps	Alliance Member IP	IBEX	• Broadcast Camera • Video Conferencing • Displays/Projectors • Automotive • ISM • Aerospace & Defense	• Virtex-6	X	
H.264/AVC-I Decoder CoreEL's H.264 Decoder IP core is highly pipelined architecture core which can run multi instances of the entropy engines for faster parallel processing. • Fully Validated on custom built hardware using ITU-T and Franhoufer test streams. • Main Profile @ L4.2 and High Profile decode @ L4.2. • Multi-channel decode: 2x1080i 60 fps / 2x1080p 30 fps. • Programmable YUV: 4:2:0, 4:2:2 and 4:4:4 chroma format support and Programmable bit depth 8, 10 or 12 bits . • Single chip FPGA solution optimized both for memory and performance. • Support up to very high bit-rate of 100 Mbps. • Supports both Intra frame only (AVC Intra) and Inter frame (IPB frames) decoding.	Alliance Member IP	CoreEL	• Broadcast Camera • Video Conferencing • Displays/Projectors • Automotive • ISM • Aerospace & Defense	• Kintex-7 • Spartan-6 • Virtex-6	X	
H.264/AVC-I Encoder CoreEL's Intra Frame Codec is one of industry's first FPGA based single chip I-Frame only encoding and decoding solutions and is optimized for very low latency applications. • Fully autonomous. It does not require any external processor to aid the codec operations. • High profile coding, also supports Main & Constrained Baseline Profile • Bit depth up to 10 bits • 4:2:0 and 4:2:2 Chroma format • Supports resolutions up to Full HD (1920x1080) and scalable up to 4K • Supports progressive and interlaced formats • Frame-rate up to 60 fps for progressive Full HD resolution • Simultaneous multi-channel encode-decode	Alliance Member IP	CoreEL	• Broadcast Camera • Video Conferencing • ISM • Aerospace & Defense	• Spartan-6 • Virtex-6	X	

Smarter Vision IP and Reference Designs – Encoding

IP Design Target

Resource	Type	Provider	Applications	Device Family Support	Programmable Logic	ARM Processing System
JPEG2000 Decoder • Compliant with JPEG 2000 (ISO/IEC 15444-1) and DCI (Digital Cinema Initiatives) recommendation • Customizable input bit rate up to 250Mbps / 500Mbps / 1+Gbps / lossless. • Full-frame decoding (no tiling) • Fully autonomous decoder with automatic parameter extraction, thus requiring minimal user intervention • Fully synchronous design • Multi-channel interface • Pixel depth up to 12 bits per color sample (lossless mode up to 16 bits) • Single-chip FPGA solution for single-channel or multi-channel up to 4096x2160 (4K) resolution • XYZ, RGB, YUV (4:4:4 or 4:2:2) color spaces with support for ICT/RCT color transform	Alliance Member IP	Barco-Silex	• Broadcast Camera • Video Conferencing • Displays/Projectors • Automotive • ISM • Aerospace & Defense	• Artix-7 • Kintex-7 • Virtex-7	X	
JPEG2000 Decoder • Input data-rate up to 500 Mbit/s • JPEG 2000 (ISO/IEC 15444-1) • Resolution up to 2048 x 1080 pixels , Frame rate up to 120 fps • Single or multiple tiles • Single quality layer (Multiple quality layer optional) • Single-chip FPGA solution • Up to 7 resolutions	Alliance Member IP	IntoPIX	• Broadcast Camera • Video Conferencing • Displays/Projectors • Automotive • ISM • Aerospace & Defense	• Artix-7 • Kintex-7	X	
JPEG2000 Encoder • Compliant with JPEG 2000 (ISO/IEC 15444-1) and DCI (Digital Cinema Initiatives) recommendation. • Configurable encoded bit rate with 3 selectable regulation modes up to 250Mbps / 500Mbps / 1+Gbps / lossless. • Flexible IP core with support for a wide range of JPEG 2000 options and easy to use interface for simple integration. • Full-frame encoding (no tiling). • Fully synchronous design. • Multi-channel interface. • Pixel depth up to 12 bits per color sample (lossless mode up to 16 bits). • Single-chip FPGA solution for single-channel or multi-channel up to 4096x2160 (4K) resolution. • XYZ, RGB, YUV (4:4:4 or 4:2:2) color spaces with support for ICT/RCT color transform.	Alliance Member IP	Barco-Silex	• Broadcast Camera • Video Conferencing • Displays/Projectors • ISM • Aerospace & Defense	• Artix-7 • Kintex-7 • Virtex-7	X	

Smarter Vision IP and Reference Designs – Encoding

IP Design Target

Resource	Type	Provider	Applications	Device Family Support	Programmable Logic	ARM Processing System
JPEG2000 Encoder • Data-rate up to 500 Mbit/s. • JPEG 2000 (ISO/IEC 15444-1). • Resolution up to 2048 x 1080 pixels , Frame rate up to 120 fps. • Single or multiple tiles. • Single quality layer (Multiple quality layer optional). • Single-chip FPGA solution. • Up to 7 resolutions	Alliance Member IP	IntoPIX	• Broadcast Camera • Video Conferencing • Displays/Projectors • ISM • Aerospace & Defense	• Artix-7 • Kintex-7	X	
MPEG-2 Decoder ISO/IEC13818-20 MPEG-2 Video, MP@HL, 4:2:2@HL • 1920x1080 • Up to 60 fps • 200Mbps maximum bitrate • Scalable architecture for power, area or performance	Alliance Member IP	IBEX	• Broadcast Camera • Video Conferencing • Displays/Projectors • Automotive • ISM • Aerospace & Defense	• Virtex-6	X	
MPEG-2 Decoder CoreEL's MPEG-2 decoder IP Core is a contribution grade solution delivering over 100Mbps bitrates for 1080P60 422@HL quality video. The industry proven IP Core has been designed for modularity and optimum resource utilization on Xilinx FPGAs. • Bitrate supported up to 100 Mbps. • Frame-rate up to 60 fps for progressive HD decode. • Optimized both for memory and performance, low resource utilization. • Optional support for TS input. • Simultaneous multi-channel decode. • Single chip FPGA solution. • Support both 4:2:0 & 4:2:2 chroma formats. • Supports progressive and interlaced formats. • Supports resolution up to 1920x1080 progressive.	Alliance Member IP	CoreEL	• Broadcast Camera • Video Conferencing • Displays/Projectors • Automotive • ISM • Aerospace & Defense	• Kintex-7 • Spartan-6 • Virtex-6	X	

Smarter Vision IP and Reference Designs – Image Processing

IP Design Target

Resource	Type	Provider	Applications	Device Family Support	Programmable Logic	ARM Processing System
1080p60 Camera Image Processing Reference Design (XAPP794) This application note describes how to set up and run the 1080p60 camera image processing reference design using the Zynq-7000 All Programmable SoC video and imaging kit.	Reference Design	Xilinx, Inc.	• Automotive • Consumer • ISM • Aerospace & Defense	• Zynq-7000	X	X
Color Correction Matrix (CCM) The Color Correction Matrix LogiCORE IP can be used for color correction operations such as adjusting white balance, color cast, brightness, or contrast in an RGB image. • Selectable data width (8, 10, 12 bits) • Selectable architectures using XtremeDSP Slices for optimal resource usage • Programmable matrix coefficients • Independent clipping and clamping control	LogiCORE IP	Xilinx, Inc.	• Broadcast Camera • Video Conferencing • Displays/Projectors • Automotive • ISM • Aerospace & Defense	• Zynq-7000 • Artix-7 • Kintex-7 • Virtex-7	X	
Color Filter Array Interpolation The Color Filter Array Interpolation SmartCORE IP is a high performance and resource efficient implementation for converting Bayer sensor data to the RBG color domain. • Scalable data width (8, 10, 12 bits) • Support for up to 4096 x 4096 image resolution including HD (1080P60) • High quality interpolation suppresses artifacts without the use of an external frame buffer	SmartCORE IP	Xilinx, Inc.	• Broadcast Camera • Video Conferencing • Automotive • ISM • Aerospace & Defense	• Zynq-7000 • Artix-7 • Kintex-7 • Virtex-7	X	
Defective Pixel Correction The Defective Pixel Correction LogiCORE IP performs real-time detection and correction of defective pixels in a camera image sensor array. • Scalable data width (8, 10, 12 bits) • Up to 4k x 4k resolutions supported including 1080P60 • Temporal filtering without using an external frame buffer • Programmable thresholds	LogiCORE IP	Xilinx, Inc.	• Broadcast Camera • Video Conferencing • Displays/Projectors • Automotive • ISM • Aerospace & Defense	• Zynq-7000 • Artix-7 • Kintex-7 • Virtex-7	X	

Smarter Vision IP and Reference Designs – Image Processing

IP Design Target

Resource	Type	Provider	Applications	Device Family Support	Programmable Logic	ARM Processing System
Gamma Correction The Gamma Correction LogiCORE IP is an optimized hardware block for manipulating image data to match the response of display devices. • Scalable data width (8,10, 12 bits) • Single or three color channel LUT structure • Optional interpolated output values available to reduce requirements	LogiCORE IP	Xilinx, Inc.	• Broadcast Camera • Video Conferencing • Displays/Projectors	• Zynq-7000 • Artix-7 • Kintex-7 • Virtex-7	X	

Image Characterization
The Image Characterization SmartCORE IP generates statistical data on a video stream that can be used in applications like face recognition and object detection.
 	
• Global and Block Means and Variances for:
  o Luminance/Chrominance Content
  o Frequency Content
  o Edge Content
  o Motion Content
  o Color Content
• Global histograms for Luminance, Chrominance and Hue
• Support for image sizes up to 1920x1080p @ 30 fps or 1280x720p @ 60fps
• Designed to work with the Motion Adaptive Noise Reduction and Object Segmentation IP cores
	SmartCORE IP	Xilinx, Inc.	• Broadcast Camera
			• Video Conferencing
			• Automotive
			• ISM
			• Aerospace & Defense
				• Zynq-7000
				• Artix-7
				• Kintex-7
				• Virtex-7
					X	

Image Edge Enhancement The Image Edge Enhancement SmartCORE IP is a programmable hardware block that can be used to enhance the edges of objects within each frame of video • Support for full high-definition (1080p@60fps) resolution • Programmable directional gain for edge enhancement • Selectable processor interface • 8, 10, or 12-bit input and output precision • YCrCb input	SmartCORE IP	Xilinx, Inc.	• Broadcast Camera • Video Conferencing • Automotive • ISM • Aerospace & Defense	• Zynq-7000 • Artix-7 • Kintex-7 • Virtex-7	X	

Smarter Vision IP and Reference Designs – Image Processing

IP Design Target

Resource	Type	Provider	Applications	Device Family Support	Programmable Logic	ARM Processing System
Image Noise Reduction The Image Noise Reduction SmartCORE IP provides a programmable smoothing function to reduce noise within each frame of video • Selectable smoothing filters • Selectable processor interface • 8, 10, and, 12 bit input and output precision • YCrCb input and output	SmartCORE IP	Xilinx, Inc.	• Broadcast Camera • Video Conferencing • Automotive • ISM • Aerospace & Defense	• Zynq-7000 • Artix-7 • Kintex-7 • Virtex-7	X	

Image Statistics Engine
The Image Statistics Engine SmartCORE IP provides hardware-based image analysis to support Auto-Focus, Auto-Exposure, and Auto-White balance applications.
 	
• Support for up to full high-definition (1080p60) resolutions
• 16 programmable zones
• Support for 8, 10, or 12-bit input precision
• Multiple output data values for all zones and color channels
  o Sum and sum of squares of color values
  o Low and high frequency content
  o Horizontal, vertical, diagonal and anti-diagonal edge content
• Outputs for pre-selected zone(s):
  o Y channel histogram
  o R,G,B channel histograms
  o Two dimensional Cr-Cb histogram
	SmartCORE IP	Xilinx, Inc.	• Broadcast Camera
			• Video Conferencing
			• Automotive
			• ISM
			• Aerospace & Defense
				• Zynq-7000
				• Artix-7
				• Kintex-7
				• Virtex-7
					X	

logiBAYER Color Camera Bayer Decoder • Converts camera sensor video from Bayer color space to the RGB color • Supports all possible Bayer pattern combinations (first two pixels: GB, GR, BG or BR) • Automatically recognizes input video resolution • Configurable memory interface: Xylon XMB, PLB, Xilinx MPMC NPI (AXI4 in preparation) • Optional picture's edge cropping and picture scaling • Unlimited vertical resolution horizontal resolution up to 1536 pixels	SmartCORE IP	Xylon	• Automotive • Aerospace & Defense	• Zynq-7000 • Artix-7 • Kintex-7 • Virtex-7	X	

Smarter Vision IP and Reference Designs – Image Processing

IP Design Target

Resource	Type	Provider	Applications	Device Family Support	Programmable Logic	ARM Processing System
logiCVC-ML Multi-layer Compact Video Controller • Supports LCD TFT and CRT displays • Up to 2048x2048 display resolutions (higher on request) • Supports up to 5 layers • Configurable layer's size, position and offset • Pixel, Layer, or Color Lookup Table (CLUT) alpha blending • Supported output formats: Parallel RGB, PAL/NTSC, LVDS, Camera link, DVI • Configurable AMBA AXI4, CoreConnect PLB or Xylon XMB memory interface • Software drivers for the most popular operating systems (OS)	Alliance Member IP	Xylon	• Broadcast Camera • Video Conferencing • Displays/Projectors • Automotive • ISM • Aerospace & Defense	• Zynq-7000 • Artix-7 • Kintex-7 • Virtex-7	X	
logiLMD Lane Marking Detector Accelerator for LDW • Fundamental building block for FPGA based automotive Rear Looking Lane Departure Warning System • Adopts to shadows and light changes • Hough Transform based model fitting • High input data rate > 180 180 Mpix/sec • Provides high level decision making reasoning as open source embedded software • The most demanding computing tasks implemented in programmable logic	SmartCORE IP	Xylon	• Automotive	• Artix-7 • Kintex-7 • Virtex-7	X	
logiPDET Pedestrian Detection HOG/SVM Accelerator • Advanced HOG/SVM object classification core for support of Pedestrian Detection in camera-based video systems • Supports resolutions up to 1024x1024 • Run-time variable image size • High Input Data Rate > 100 Mpixel/sec • High throughput >6.4 GMAC/sec for the classification stage • ARM AMBA AXI4 bus compliant	SmartCORE IP	Xylon	• Automotive • ISM	• Artix-7 • Kintex-7 • Virtex-7	X	

Smarter Vision IP and Reference Designs – Image Processing

					IP Design Target	
Resource	**Type**	**Provider**	**Applications**	**Device Family Support**	**Programmable Logic**	**ARM Processing System**
logiVIEW Lens correction/perspective transform/stitching • Supports perspective transformations of 2D quadrilaterals • Programmable homographic transformation matrix enables: cropping, resizing, rotating, translating, arbitrary function • Supports correction of fish eye lens distortions • Suitable for extreme wide-angle lenses (fish-eye) and other lenses • Configurable number of video inputs and outputs • Supports 2048x2048 and higher input and output resolutions • Calibration software with preview function is part of IP deliverables	SmartCORE IP	Xylon	• Broadcast Camera • Video Conferencing • Displays/Projectors • Automotive • ISM • Aerospace & Defense	• Spartan-6 • Virtex-6	**X**	
Object Segmentation The Object Segmentation SmartCORE IP provides a hardware-accelerated method for identifying objects of interest within a video stream. • Supports up to 8 sets of feature combinations (mean, variance, edge, motion and color information) • Supports up to 4 feature selects (any Boolean combination of the 8 feature combinations) • Detects up to 30 objects per feature select • Provides location of the object in the frame and density of the object in a rectangle around the object • Operates at all resolutions and frame rates supported by Image Characterization block (up to 720p60 and 1080p30)	SmartCORE IP	Xilinx, Inc.	• Broadcast Camera • Video Conferencing • Automotive • ISM • Aerospace & Defense	• Zynq-7000 • Artix-7 • Kintex-7 • Virtex-7	**X**	
Optical Flow • Used to estimate the 2D motion projected on the image plane by the objects moving in the 3D scene. • Optical flow can be illustrated with vectors that show motion that exists from a reference frame to another frame. • Used in many applications from tracking in automotive applications to explosion detection	SmartCORE IP	Digital Design Corp.	• Automotive • ISM • Aerospace & Defense	• Spartan-6	**X**	
SubLVDS Camera Sensor Interface Reference Design (XAPP582) The Compact Camera Port 2 (CCP2) protocol is used to interface between camera sensors and receivers. The signaling scheme uses SubLVDS. This application note describes the SubLVDS electrical specifications. It includes a reference design to implement resistor topology that emulates the electrical characteristics of a SubLVDS transmitter.	Reference Design	Xilinx, Inc.	• Broadcast Camera • Video Conferencing • Automotive • ISM • Aerospace & Defense	• Artix-7 • Kintex-7 • Virtex-7	**X**	

Smarter Vision IP and Reference Designs – Video Processing

					IP Design Target	
Resource	**Type**	**Provider**	**Applications**	**Device Family Support**	**Programmable Logic**	**ARM Processing System**
3D Graphics Accelerator • 3D Graphics accelerator IP designed to support the OpenGL ES 1.1 API • ARM Cortex-A9 CPU with NEON coprocessor run the geometry engine and optimizes the IP's size • Conforms to the AMBA AXI4 bus specifications from ARM • FPGA resource-effective 3D graphics acceleration • Linux compatible • support for other OSes planned for year 2012 • The logi3D GPU can be used with different CPUs	Alliance Member IP	Xylon	• Automotive • ISM • Aerospace & Defense	• Zynq-7000 • Artix-7 • Kintex-7 • Virtex-7	**X**	**X**
4K2K Up-Converter Reference Design (XAPP596) This high definition (HDTV) to 4K2K up-converter reference design enables up-conversion from 1080p HDTV to 4K2K progressive images. The up-conversion results in showing HDTV content, which is very popular in broadcasting and packaged media, on a 4K x 2K flat panel display. The reference design is built from the following SmartCORE IP in the Xilinx Video and Image Processing Pack (VIPP): • Video Scaler • On-screen Display (OSD)	Reference Design	Xilinx, Inc.	• Broadcast Camera • Video Conferencing • Displays/Projectors	• Kintex-7	**X**	
AXI VDMA Reference Design (XAPP742) This application note demonstrates the creation of video systems by using Xilinx native video IP cores such as AXI Video Direct Memory Access (VDMA), Video Timing Controller (VTC), test pattern generator (TPG), and the DDR3 memory controller to process configurable frame rates and resolutions in Kintex-7 FPGAs.	Reference Design	Xilinx, Inc.	• Broadcast Camera • Video Conferencing • Displays/Projectors • Automotive • ISM • Aerospace & Defense	• Kintex-7	**X**	

Smarter Vision IP and Reference Designs – Video Processing

					IP Design Target	
Resource	**Type**	**Provider**	**Applications**	**Device Family Support**	**Programmable Logic**	**ARM Processing System**
AXI Video DMA The AXI Video Direct Memory Access (AXI VDMA) core is a soft Xilinx SmartCORE IP core that provides high-bandwidth direct memory access between memory and AXI4-Stream type video target peripherals. The core provides efficient two dimensional DMA operations with independent asynchronous read and write channel operation. • High-bandwidth direct memory access for video streams • Efficient two-dimensional DMA operations • Independent, asynchronous read and write channel operation • Gen-Lock frame buffer synchronization option up to 32 frame stores • Supports dynamic video format changes • Optional Line Buffers with configurable thresholds for efficient video streaming • Processor accessible initialization, status, interrupt and management registers • Primary AXI Stream data width support for multiples of 8-bits: 8, 16, 24, 32, etc up to 1024 bits	SmartCORE IP	Xilinx, Inc.	• Broadcast Camera • Video Conferencing • Displays/Projectors	• Artix-7 • Kintex-7 • Virtex-7	X	
Chroma Resampler The Chroma Resampler LogiCORE IP converts video data between commonly used chroma formats. • Supports conversion between YCrCb 4:4:4, 4:2:2, and 4:2:0 • Video formats supported: o High-definition (1080p60 resolutions) o Up to 4095 total scanlines and 4095 pixels per scanline • Image edges padded to eliminate edge artifacts • Scalable data width of 8, 10 and 12-bits • Supports Progressive or Interlaced Video • Programmable clipping and clamping of output results • Three resampling options allow resource utilization trade-off	LogiCORE IP	Xilinx, Inc.	• Broadcast Camera • Video Conferencing • Displays/Projectors	• Zynq-7000 • Artix-7 • Kintex-7 • Virtex-7	X	
Chroma Resampler Reference Design (XAPP932) This application note describes the implementation of six circuits necessary to perform commonly used conversions between various chroma formats. It is accompanied by reference designs which include Generic RTL VHDL code.	Reference Design	Xilinx, Inc.	• Broadcast Camera • Video Conferencing • Displays/Projectors • Automotive • ISM • Aerospace & Defense	• Zynq-7000 • Artix-7 • Kintex-7 • Virtex-7	X	

Smarter Vision IP and Reference Designs – Video Processing

Resource	Type	Provider	Applications	Device Family Support	IP Design Target: Programmable Logic	IP Design Target: ARM Processing System
Color-Space Converter: YCrCb to RGB (XAPP931) This application note describes the implementation of a YCrCb color space to an RGB Color space conversion circuit necessary in many video designs.	Reference Design	Xilinx, Inc.	• Broadcast Camera • Video Conferencing • Displays/Projectors • Automotive • ISM • Aerospace & Defense	• Zynq-7000 • Artix-7 • Kintex-7 • Virtex-7	X	
De-interlacer Small footprint enables many channels of de-interlacing in a single FPGA for applications such as Multi-Viewing and Muti-Channel MPEG or H.264 Encoding.	SmartCORE IP	CubeVision	• Broadcast Camera • Video Conferencing • Displays/Projectors • ISM • Aerospace & Defense	• Zynq-7000 • Artix-7 • Kintex-7 • Virtex-7 • Spartan-6	X	
Designing High-Performance Video Systems in 7 Series FPGAs with the AXI Interconnect (XAPP741) • The design uses eight AXI video direct memory access (VDMA) engines to simultaneously move 16 streams (eight transmit video streams and eight receive video streams), each in 1920 x 1080 pixel format at 60 or 75 Hz refresh rates, and up to 32 data bits per pixel. • Each VDMA is driven from a video test pattern generator (TPG) with a video timing controller (VTC) block to set up the necessary video timing signals. Data read by each AXI VDMA is sent to a common on-screen display (OSD) core capable of multiplexing or overlaying multiple video streams to a single output video stream. • The output of the OSD core drives the onboard high-definition media interface (HDMI) video display interface through the color space converter.	Reference Design	Xilinx, Inc.	• Broadcast Camera • Video Conferencing • Displays/Projectors • Automotive • ISM • Aerospace & Defense	• Kintex-7	X	

Smarter Vision IP and Reference Designs – Video Processing

					IP Design Target	
Resource	**Type**	**Provider**	**Applications**	**Device Family Support**	**Programmable Logic**	**ARM Processing System**
Designing High-Performance Video Systems with the AXI Interconnect on Virtex-6 (XAPP740) This application note covers the design considerations of a system using the performance features of the LogiCORE IP Advanced eXtensible Interface (AXI) Interconnect core.	Reference Design	Xilinx, Inc.	• Broadcast Camera • Video Conferencing • Displays/Projectors • Automotive • ISM • Aerospace & Defense	• Virtex-6	X	
Designing High-Performance Video Systems with the Zynq-7000 All Programmable SoC (XAPP792) • The design uses three AXI video direct memory access (VDMA) engines to simultaneously move six streams (three transmit video streams and three receive video streams), each in 1920 x 1080p format, 60 Hz refresh rate, and up to 32 data bits per pixel. • Each VDMA is driven from a video test pattern generator (TPG) with a video timing controller (VTC) core to set up the necessary video timing signals. • Data read by each AXI VDMA is sent to a common on-screen display (OSD) core capable of multiplexing or overlaying multiple video streams to a single output video stream. • The output of the OSD core drives the HDMI video display interface on the board.	Reference Design	Xilinx, Inc.	• Broadcast Camera • Video Conferencing • Displays/Projectors • Automotive • ISM • Aerospace & Defense	• Zynq-7000	X	X
Implementing Memory Structures for Video Processing in the Vivado HLS Tool (XAPP793) Video algorithms can be quickly and efficiently implemented in Xilinx FPGAs through the use of the Vivado High-Level Synthesis (HLS) tool. This application note describes the techniques and main aspects the user needs to keep in mind when implementing this kind of algorithm in the HLS tool.	Reference Design	Xilinx, Inc.	• Broadcast Camera • Video Conferencing • Displays/Projectors • Automotive • ISM • Aerospace & Defense	• Zynq-7000 • Artix-7 • Kintex-7 • Virtex-7	X	
Motion Adaptive Noise Reduction The Motion Adaptive Noise Reduction LogiCORE IP provides system designers with an easily configurable and high quality motion detection and adaptive noise reduction core for image processing systems. - Supports resolutions up to 720P60 and 1080P30 - Configurable Noise Reduction Strength - Programmable Motion Transfer Function - YCrCb input	SmartCORE IP	Xilinx, Inc.	• Broadcast Camera • Video Conferencing • Displays/Projectors • Automotive • ISM • Aerospace & Defense	• Zynq-7000 • Artix-7 • Kintex-7 • Virtex-7	X	

Smarter Vision IP and Reference Designs – Video Processing

					IP Design Target	
Resource	**Type**	**Provider**	**Applications**	**Device Family Support**	**Programmable Logic**	**ARM Processing System**

On-Screen Display
The On-Screen Display SmartCORE IP is used for rendering text, graphics and Alpha blending in video systems.
• Hardware Accelerators
  o Alpha Blending Layer Compositor
  o Graphics Controller (including boxes and text)
• Configurable number of layers up to 8 max
• Supports video frame sizes up to 4096x4096 pixels and frame rates up to 60fps including 1080P60
• Provides configurable internal text string memory with 1-bit or 2-bit per pixel color depth and scaling text by 1x, 2x, 4x or 8x
• Provides configurable internal font memory for 8x8 or 16x16 pixel fixed distance fonts
• Color Spaces: RGB, RGBA, YUV-4:4:4, YUVa-4:4:4, YUV-4:2:2, YUVa-4:2:2, YUV-4:2:0, YUVA-4:2:0
• Number of color components: 2 or 3; Bits per color component: 8, 10 or 12
	SmartCORE IP	Xilinx,Inc.	• Broadcast Camera
			• Video Conferencing
			• Displays/Projectors
			• Automotive
			• ISM
			• Aerospace & Defense
				• Zynq-7000
				• Artix-7
				• Kintex-7
				• Virtex-7
					X	

OSVP (OmniTek Scalable Video Processor) • Chroma resampling • De-interlacing • Resizing • Composite onto video output with graphic overlay • Video resolutions up to 2048x2048 • YUV and RGB colour in 4:2:2 or 4:4:4 format • 8, 10 or 12 bit colour depth per plane • Interlaced, progressive and progressive segmented frame (PsF) support • Motion and low angle edge adaptive de-interlacing	SmartCORE IP	OmniTek	• Broadcast Camera • Video Conferencing • Displays/Projectors • Automotive • ISM • Aerospace & Defense	• Zynq-7000 • Kintex-7	X	
Real Time Video Engine on Spartan-6 (XAPP898) The Real-Time Video Engine (RTVE) provides a professional grade and highly demonstrable video processing reference design targeted to the broadcast market. The reference design is built from IP cores using the Xilinx Video and Image Processing IP Pack. The reference design performs video de-interlacing and scaling functions, and also provides many other features:	Reference Design	Xilinx, Inc.	• Broadcast Camera • Video Conferencing • Displays/Projectors • Automotive • ISM • Aerospace & Defense	• Spartan-6	X	

Smarter Vision IP and Reference Designs – Video Processing

					IP Design Target	
Resource	**Type**	**Provider**	**Applications**	**Device Family Support**	**Programmable Logic**	**ARM Processing System**
Real Time Video Engine on Virtex-6 (XAPP889) The Real-Time Video Engine (RTVE) provides a good quality and highly demonstrable video processing reference design targeted to the broadcast market. The reference design is built from IP cores using the Xilinx Video and Image Processing IP Pack (VIPP). The reference design performs video de-interlacing and scaling functions and also provides many other features.	Reference Design	Xilinx, Inc.	• Broadcast Camera • Video Conferencing • Displays/Projectors • Automotive • ISM • Aerospace & Defense	• Virtex-6	**X**	
Real Time Video Engine 2.0 on Kintex-7 (XAPP1091) The objective of this reference design is to provide a highly demonstrable, broadcast-quality video processing reference design targeted to a wide range of video applications. The Real-Time Video Engine Reference Design version 2.0 performs the video processing function in a scalable fashion with capability supporting 2x, 4x and up to 8x parallel video pipelines.	Reference Design	Xilinx, Inc.	• Broadcast Camera • Video Conferencing • Displays/Projectors • Automotive • ISM • Aerospace & Defense	• Kintex-7	**X**	

RGB to YCrCb Color-Space Converter
The Xilinx RGB to YCrCb Color Space Conversion LogiCORE IP is an optimized hardware block for converting RGB video data to the YCrCb color space.
 	
• Scalable Data Width (8, 10, 12 bits)
• Supports multiple color space conversions
  o SD (ITU 601)
  o HD (ITU 709) PAL
  o HD (ITU 709) NTSC
  o YUV
• User defined conversion matrices
	LogiCORE IP	Xilinx, Inc.	• Broadcast Camera
			• Video Conferencing
			• Displays/Projectors
				• Zynq-7000
				• Artix-7
				• Kintex-7
				• Virtex-7
					X	

Smarter Vision IP and Reference Designs – Video Processing

					IP Design Target	
Resource	**Type**	**Provider**	**Applications**	**Device Family Support**	**Programmable Logic**	**ARM Processing System**
Test Pattern Generator Xilinx Test Pattern Generator IP Core provides convenient generation of test patterns for Video System bring up, evaluation and debug. • Supports generation of a wide variety of test patterns including solid colors, color bars, tartan bars, vertical, horizontal and temporal ramps, zone plate, crosshairs, moving box, addition of noise, insertion of stuck pixels, etc. • Supports YCC 4:2:2 and RGB • Scalable data width of 8, 10 and 12-bits • Supports pass through of video signals in addition to test pattern generation • Supports AXI4-Lite control interface and AXI4-Stream Video Protocol • Supports 1080p60 data rates in Artix-7 family devices and higher data rates in high performance Xilinx devices	LogiCORE IP	Xilinx, Inc.	• Broadcast Camera • Video Conferencing • Displays/Projectors • Automotive • ISM • Aerospace & Defense	• Zynq-7000 • Artix-7 • Kintex-7 • Virtex-7	**X**	
Video De-interlacer The Video De-interlacer SmartCORE IP converts live incoming interlaced video streams into progressive video streams. This process is performed in real time as the input video passes through the Video De-interlacer. It also uses additional motion tracking and diagonal edge enhancement techniques to ensure that motion artifacts are removed where possible. This results in a high-quality progressive output image. • Supports a wide range of industry standard video encoding and packing methods, including: o 8, 10 or 12 bits per pixel o YUV or RGB color spaces (static or dynamically configurable) o 4:2:0, 4:2:2 or 4:4:4 packing (static or dynamically configurable) • Supports highly scalable resolutions from 128x128 up to 2048x2048, such as: o Standard SD formats: 480i, 480p, 576i, 576p o Standard HD formats: 720p, 1080i, 1080p o Digital Cinema 2K o All PC resolutions: e.g. 640x480, 1024x768, 1280x1024, 1920x1200 • Supports progressive pass through, "Progressive Segmented Frames" (PSF) and "Pull down" encoded streams • Highly configurable and can be optimized for the smallest FPGA footprint	SmartCORE IP	Xilinx, Inc.	• Broadcast Camera • Video Conferencing • Displays/Projectors • Automotive • ISM • Aerospace & Defense	• Zynq-7000 • Artix-7 • Kintex-7 • Virtex-7	**X**	

Smarter Vision IP and Reference Designs – Video Processing

IP Design Target

Resource	Type	Provider	Applications	Device Family Support	Programmable Logic	ARM Processing System

Video Scalar
The Video Scalar SmartCORE IP is an optimized hardware block that converts an input color image of one size to an output image of a different size.
• Support for -8, -10, -12 bit video data
• Video resolutions up to 4094x4094
  o Includes standard high-definition formats (1080i/60, 720P/60, 1080P/30, 1080P/60)
• Configurable up to 64 phases and 12 taps
• Supports multiple algorithms
  o Bilinear, bicubic, and polyphase scaling
• Programmable scaling factor in both horizontal and vertical directions
• Support for YUV4:4:4, RGB YUV4:2:2 or YUV4:2:0
• Programmable or user input coefficient parameters
• Coefficient sharing for Luminance/Chrominance and Horizontal/Vertical filters
	SmartCORE IP	Xilinx, Inc.	• Broadcast Camera
			• Video Conferencing
			• Displays/Projectors
			• Automotive
			• ISM
			• Aerospace & Defense
				• Zynq-7000
				• Artix-7
				• Kintex-7
				• Virtex-7
					X	

Video Timing Controller Xilinx provides a Video Timing Controller LogiCORE IP for use in imaging systems which allows easy timing configuration and system control. • Automatic detection of horizontal and vertical blanking, synchronization pulses, and active video pixels • In-system programmable for easy configuration • Generation of horizontal, vertical and field ID pulses • Full interrupt support for system event control	LogiCORE IP	Xilinx, Inc.	• Broadcast Camera • Video Conferencing • Displays/Projectors • Automotive • ISM • Aerospace & Defense	• Zynq-7000 • Artix-7 • Kintex-7 • Virtex-7	X	

YCrCb to RGB Color-Space Converter
The Xilinx YCrCb to RGB Color Space Conversion LogiCORE IP is an optimized hardware block for converting YCrCb video data to the RGB color space.
• Scalable Data Width (8, 10, 12 bits)
• Supports multiple color space conversions
  o SD (ITU 601)
  o HD (ITU 709) PAL
  o HD (ITU 709) NTSC
  o YUV
• User defined conversion matrices
	LogiCORE IP	Xilinx, Inc.	• Broadcast Camera
			• Video Conferencing
			• Displays/Projectors
				• Zynq-7000
				• Artix-7
				• Kintex-7
				• Virtex-7
					X	

Zynq All Programmable SoC Sobel Filter Implementation Using the Vivado HLS Tool (XAPP890) This application note describes how to generate the Sobel edge detection filter in the Zynq-7000 All Programmable SoC ZC702 Base Targeted Reference Design (TRD) using the Vivado High-Level Synthesis (HLS) tool.	Reference Design	Xilinx, Inc.	• Broadcast Camera • Video Conferencing • Displays/Projectors • Automotive • ISM • Aerospace & Defense	• Zynq-7000	X	X

Smarter Vision IP and Reference Designs – Transmission

Resource	Type	Provider	Applications	Device Family Support	IP Design Target: Programmable Logic	IP Design Target: ARM Processing System
ATSC Modulator Supports ATSC A/53 Part 2 The MVD modulator cores can be delivered with an Intermediate Frequency output or a RF output when using Analog Devices or Maxim RF DACs • Single clock • Robust SPI input (null packet deletion in option) • PCR re-stamping • 19.39Mbits maximum input rate for 8-VSB • Possibility of supporting a variable symbol rate • Intermediate frequency output for single DAC (14 bits) or baseband outputs (2 x 16 bits) • Single / multi channel	Alliance Member IP	MVD	• Broadcast	• Zynq-7000 • Artix-7 • Kintex-7 • Virtex-7	X	
ATSC Modulator The MW_8-VSB core implements the terrestrial broadcast mode (known as 8 VSB) compliant to ATSC Standard A/53, part of the VSB subsystem of the Digital Television Standard • Input: 19.39…Mbps serial data stream. • 207/187 Reed Solomon Encoder • 52 data segment (intersegment) convolutional byte interleaver • Interleaving depth: 1/6 of a data field (4ms deep). • 2/3 rate trellis code. 8-level (3 bit) one dimensional constellation.	Alliance Member IP	Mindway	• Broadcast	• Spartan-6	X	
DVB-C Modulator The MW_DVB-C modulator core performs the digital baseband function required for the transmission side of Digital Video Broadcasting cable link. It accepts a MPEG-2 transport stream and produces a I/R filtered output which should be used by an external modulator. • Compliant to ETSI EN 300 429 v.1.2.1 • 204/188 Reed Solomon Outer Coder • Selectable QAM Modulation between 16, 32 or 64 • Fully synchronous design • High speed: more than 20 MHz Cable symbol rate	Alliance Member IP	Mindway	• Broadcast	• Spartan-6	X	

Smarter Vision IP and Reference Designs – Transmission

Resource	Type	Provider	Applications	Device Family Support	IP Design Target: Programmable Logic	IP Design Target: ARM Processing System
DVB-C Modulator • Fully synthetizable RTL VHDL design (not delivered) for easy customization • Intermediate frequency output for single DAC (14 bits) or baseband outputs (2 x 16 bits) • MER > 42dB • PCR re-stamping • Programmable 16, 32, 64, 128 and 256 QAM Symbol Mapping • Robust SPI input (discarding incorrect input packets) • Single / multi channel • Single clock (up to 140 MHz+ for Spartan-3/6, 180 MHz+ for Virtex-5/6) • Supports programmable symbol rates	Alliance Member IP	MVD	• Broadcast	• Zynq-7000 • Artix-7 • Kintex-7 • Virtex-7	X	
DVB-S Modulator The MW_DVB-S modulator core performs the digital baseband function required for the transmission of a Digital Video Broadcasting satellite link. It accepts a MPEG-2 transport stream and produces a I/Q filtered output which should be used by an external modulator. • Compliant to ETSI EN 300 421 v1.1.2 • 204/188 Reed Solomon Outer Coder • Selectable code rates of 1/2 , 2/3, 3/4, 5/6, 7/8 • Fully synchronous design • High speed: up to 80 MHz Ru rates	Alliance Member IP	Mindway	• Broadcast	• Spartan-6	X	
DVB-S Modulator • Baseband or Intermediate frequency output for complex DAC (2 x 16 bits) • DVB-S (ETS 300 421) Compliant baseband transmitter for Satellite Modem Termination Systems (SMTS) • Design delivered as Netlist • Drop-in module • Flexible input and symbol rates • Fully synthetizable RTL VHDL design (not delivered) for easy customization • MER > 40dB • PCR re-stamping • PCR re-stamping • Programmable 1/2, 2/3, 3/4, 5/6 and 7/8 punctured FEC • Ready to use DVB-S compliant modulator core	Alliance Member IP	MVD	• Broadcast	• Zynq-7000 • Artix-7 • Kintex-7 • Virtex-7	X	

Smarter Vision IP and Reference Designs – Transmission

IP Design Target

Resource	Type	Provider	Applications	Device Family Support	Programmable Logic	ARM Processing System
DVB-T2 Modulator • FFT sizes: 1K, 2K, 4K, 8K, 8K extended, 16K, 16K extended, 32K, 32K extended. • Guard-interval fractions: 1/128, 1/32, 1/16, 19/256, 1/8, 19/128, 1/4. Guard interval processing may need an external memory depending on the amount of memory available on your FPGA. • Scattered-pilot patterns: 8 different versions (PP1... PP8) matched to guard intervals. • Continual pilots with improved optimization to reduce overhead, with respect to DVB-T. • Supported code rates: 1/2, 3/5, 2/3, 3/4, 4/5 and 5/6 with normal and short FECFRAME. • Supported modulation format: QPSK, 16-QAM, 64-QAM and 256-QAM. • Rotated constellations, which provide a form of modulation diversity, to assist in the reception of higher-code-rate signals in adverse channel condition. • Extended interleaving, including bit, cell, time and frequency interleavers. The time interleaver requires external memory.	Alliance Member IP	Binary Core	• Broadcast	• Artix-7 • Kintex-7 • Virtex-7	X	
DVB-T/H Modulator • Fully compliant with ETSI EN 300 744 V1.5.1 (2004-11) • Support DVB-H functionality • Configurable for 2K, 4K and 8K OFDM modes. • Support Hierarchical Mode • Supplied with build script using Synplify Pro® • Optional SFN functional mode could be added • Optional Linear and Not Linear Pre-Distortion • could be added • Internal or external microcontroller interface is available • Status and control registers are available for start up and continuous test and management	Alliance Member IP	Mindway	• Broadcast	• Spartan-6	X	
DVB-T/H Modulator • ETSI, DVB-T/H (EN 300 744 V1.5.1) Compliant baseband transmitter for Digital Terrestrial Television. • MER > 41dB. • PCR restamping. • Programmable symbol mapping, OFDM mode, guard interval and convolutional rate - Supports variable channel width 5 MHz to 8 MHz. • Robust SPI input (discarding of incorrect input packets). • Single channel, supports hierarchical transmission.	Alliance Member IP	MVD	• Broadcast	• Zynq-7000 • Artix-7 • Kintex-7 • Virtex-7	X	