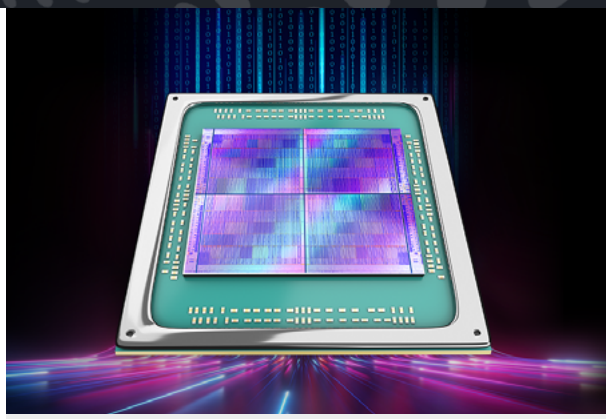
VERSAL™ PREMIUM VP1902 ADAPTIVE SOC



OVERVIEW

The Versal™ Premium VP1902 adaptive SoC offers the highest logic capacity, interconnect, and external memory bandwidth available in the Versal portfolio. With over 18.5M logic cells, over 2,000 I/Os, and up to 160 high-speed transceivers capable of operating up to 112 Gbps, the VP1902 device is designed for applications that stretch the boundaries of engineering.

Built on the proven Versal architecture, the VP1902 not only delivers industry-leading capacity[1], but also integrates Arm® scalar processors, hardened IP for PCIe® Gen5, Ethernet, and memory interfacing, all tied together by the Versal programmable network on chip (NoC) for simplified data movement across the massive device.

The VP1902 is a sixth-generation emulation-class device[2] from AMD and the first adaptive SoC to leverage a novel two-by-two SLR architecture, where the programmable logic dies are oriented in a quadrant configuration. This greatly simplifies routing between SLRs and reduces latency for signals traversing the device.

HIGHLIGHTS

Extreme Capacity and Interconnect

- 18.5 million system logic cells
- 2,328 SelectIO™ resources capable of operation up to 3.2 Gbps
- Up to 160 high-speed serial transceivers, including 112G PAM-4 GTMs and 32.75G GTYPs
- Integrated hard IP for PCIe Gen5, 10-400G Ethernet, and DDR memory interfacing
- Dual-core Arm scalar processors

Built on 4th Generation Stacked Silicon Interconnect Technology

- Two-by-two SLR configuration for enhanced routability and reduced latency
- Programmable NoC provides inter- and intra-SLR connectivity
- Enhanced Laguna connection technology expanded to two dimensions for reduced SLR-crossing congestion

Comprehensive Tools and IP

- Co-optimized with the Vivado™ design suite
- Enhanced visibility and debug with low resource utilization
- Novel place-and-route tuned for multi-SLR designs

TARGET APPLICATIONS

EMULATION AND PROTOTYPING

- Desktop Prototyping
- Enterprise Prototyping
- ASIC/SoC Emulation

TEST AND MEASUREMENT

- Protocol Analyzers
- RF Instrumentation

AEROSPACE

WIRED COMMUNICATION

DATA CENTER

DEVICE RESOURCES

VERSAL PREMIUM VP1902 ADAPTIVE SOC		
Adaptable Engines	System Logic Cells (K)	18,507
	LUTs (K)	8,460
Intelligent Engines	DSP Engines	6,864 (DSP58)
Scalar Engines	Application Processing Unit	Dual-Core Arm® Cortex®-A72
	Real-Time Processing Unit	Dual-Core Arm Cortex-R5F
Memory	Hardened DDR Memory Controllers	14
	Block RAM (Mb)	239
	UltraRAM (Mb)	619
Transceivers	GTYP Transceivers (32.75 Gbps)	Up to 128
	GTM Transceivers (58G (112G))	32 (16)
Hardened IP	100G Multirate Ethernet MAC	12
	600G Ethernet MAC	4
	PCI Express®	16 x Gen5 x 4
Packaging	XPIO (Fabric Facing)	Up to 264 DDR-only, 2064 DDR + PL
	HDIO	88
	Footprint	77.5 x 77.5 mm

NEXT STEPS

• For more information about the AMD Versal Premium VP1902 device, visit www.amd.com/vp1902.

[1]Based on AMD internal analysis in May 2023 with a 6-input LUT count to compare the Versal Premium VP1902 device versus the Intel Stratix 10 GX 10M FPGA. (VER-002)
[2]Based on AMD internal analysis, May 2023. (VER-009)