PRODUCT BRIEF

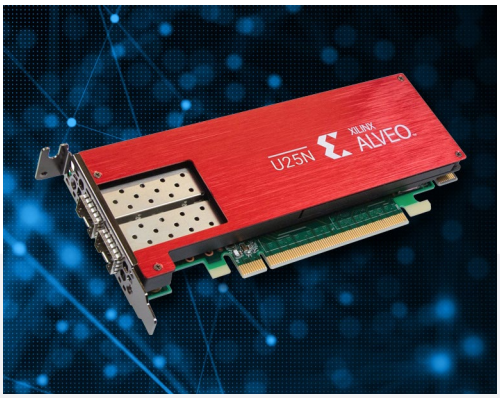
ALVEO™ U25N

2x25GbE SmartNIC for Turnkey Network and Security Acceleration

OVERVIEW

For cloud and enterprise architects building modern data centers, the Alveo U25N provides a comprehensive SmartNIC platform that brings true convergence of network and security acceleration functions into a single platform.

The U25N SmartNIC platform is based on the fusion of three technologies, a powerful System on a Chip (SoC) that includes an FPGA and multi-core Arm processors, and a proven XtremeScale™ X2 Ethernet Controller. The FPGA enables in-line hardware acceleration and offload with maximum efficiency while avoiding unnecessary data movements. The Arm cores handle exception traffic processing, and FPGA-related management and statistics. The X2 Ethernet Controller chip provides a platform for processing two ports of 25 Gigabit Ethernet via field proven software drivers.



XILINX ADVANTAGE

- Bump-in-the-wire model to offload and accelerate networking and security functions
- Includes turnkey advanced network accelerations including Open vSwitch (OvS), IPsec, Firewall, and QoS
- Application customization programmability enables flexibility to add custom workloads
- Baseline NIC feature parity with field proven XtremeScale™ Ethernet controllers

FEATURES AND BENEFITS

Enabling the Fastest, Most Secure Networks

Powerful SmartNIC

The U25N delivers ultra-high throughput, small packet performance and low-latency. The host interface supports standard NIC drivers as well as Onload® kernel bypass to provide both TCP and packet- based APIs for network application acceleration. The U25N is also tamper resistant and provides secure flow monitoring with enforcement via a stateless firewall.

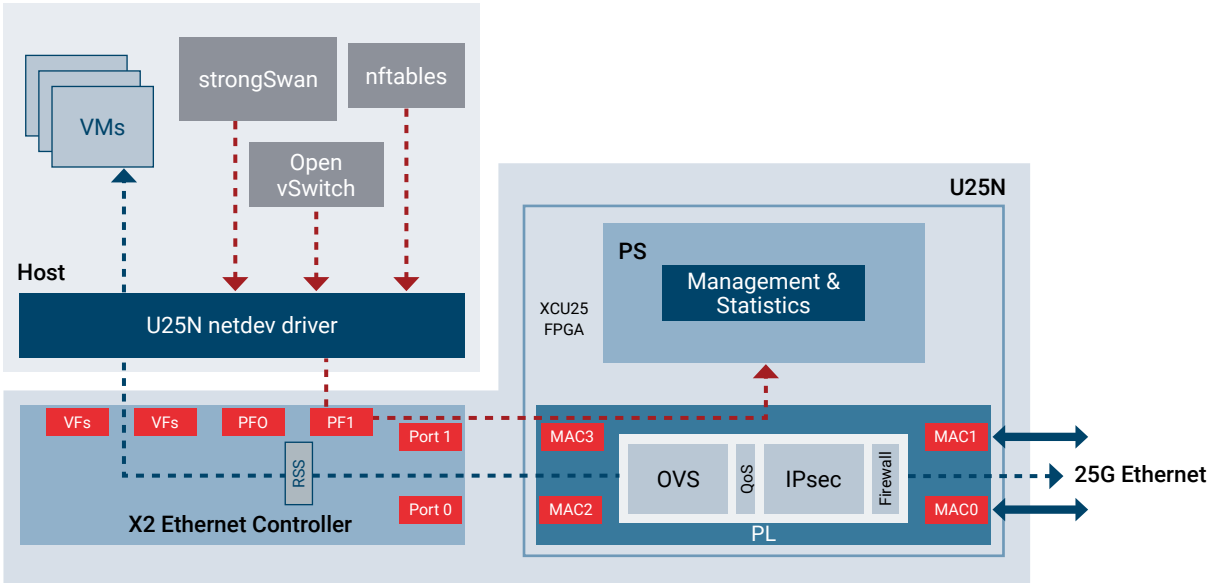
Programmable Fabric

The U25N SmartNIC contains a programmable FPGA processing all the network flows. Each flow can be individually delivered to the host and/or streamed in hardware through bump-in-the-wire network acceleration functions. The platform also enables ability for customers to accelerate custom workloads.

A Platform for Hardware Accelerated Clouds

Cloud service providers are deploying SmartNIC fabrics to achieve virtual switching and micro- segmentation of services that scale linearly with CPU cores and network links. The U25N is a platform for the industry's first converged SmartNIC fabric, including shrink-wrapped applications.

Adaptable. Intelligent.



U25N Architectural Block Diagram

ALVEO U25N PLATFORM ARCHITECTURE

The U25N has three computational components, the X2 Ethernet Controller, the Arm cores represented by the PS block, and the FPGA programmable logic (PL).

Most of the data plane processing tasks of the U25N SmartNIC are handled within the X2 or the FPGA. Both blocks were designed to handle wire-rate traffic at 25Gbps/port. The X2 processes standard network tasks, and Single Root Input Output Virtualization (SR-IOV) requests to setting up physical functions (PFs) and virtual functions (VFs).

The FPGA is the home to several data plane pipeline stages. These include the Match Action Engine (MAE) which handles network virtualization tasks like VXLAN and L2GRE.

The Internet Protocol Security (IPsec) block which offloads this layer of protocol processing by leveraging the strongSwan application for configuring rules. There is also a stateless firewall executing within the FPGA that can support rules passed down from the hosts nftables entries. Finally, quality of service (QoS) is supported by a hierarchical token bucket (HTB) implementation to guarantee egress traffic shaping and priority control.

The Arm cores of the U25N are primarily used as a management agent for receiving control plane management traffic from the host CPU. of the FPGAs programmable logic. Agent applications running on the Arm cores update tables used by the MAE, IPsec and the firewall, while these programmable logic blocks are running. They also gather various statistics used to improve the overall processing within the U25N SmartNIC platform.

Network Acceleration

- DPDK Poll Mode Driver - Packet (Cloud, Telco)
- Onload® – TCP (Cloud, Telco, Enterprise)
- Onload®/TCPDirect - TCP/UDP (Fintech)

Stateless Offloads

- TTCP/UDP Checksum Offload (CSO) TCP Segmentation Offload (TSO) Giant Send Offload (GSO)
- Large Send Offload (LSO) Large Receive Offload (LRO) Receive Side Scaling (RSS)
- Receive Segment Coalescing (RSC)

Hardware-based Packet Processing

- Open Virtual Switch (OVS) data plane offload
- Connection Tracking (Stateful Firewall)
- Quality of service (QoS) to guarantee egress traffic shaping and priority control

Security

- Inline hardware IPsec encryption & decryption
  • AES-GCM 256 bit key
- strongSwan Plugin for IPsec offload support
- nftables hardware accelerated filtering
- Tamper resistant X2 firmware – Digitally signed and secured via private keys

Manageability and Remote Boot

- UEFI
- NC-SI over MCTP SMBus
- PLDM over MCTP SMBus MCTP PCIe VDM

Management and Utilities

- Ethtool Support
- Boot Manager

Adapter Hardware

- PCIe Gen 3 x8 interface to host (Gen 3 x16 PCIe connector)
- 2x10/25G SFP28 DA copper or optical transceiver;
- XtremeScale™ X2 Ethernet Controller
- Zynq® UltraScale+™ XCU25N FPGA
- 1x 2GB x 40 DDR4-2666 for use by the Arm cores
- 2x 4GB x 72 DDR4-2666 for use by the FPGA

Traffic Engineering

- XtremePacket™ Engine for parsing, filtering, and flow steering
- TCP/UDP/IP, MAC, VLAN, RSS filtering Accelerated Receive Flow Steering (ARFS) Transmit Packet Steering

Virtualization

- Linux Multi-Queue
- SR-IOV: 2 physical functions; 240 virtual functions
- VXLAN, L2GRE tunneling offloads; adaptable to custom overlays

Ethernet Standards

- IEEE802.3-2018 Ethernet Base Standard
- IEEE 802.3by Ethernet consortium 25 Gigabit Ethernet
- IEEE 802.3ad, 802.1AX Link Aggregation
- IEEE 802.1Q, 802.1P VLAN Tags and Priority
- Jumbo Frame support (9000 bytes)

OS Support

- Ubuntu, Red Hat RHEL and Linux variants

Physical Dimensions

- L: 6.60 inch (167.65 mm)
- W: 2.54 inch (64.4 mm)

Hardware Certifications

- FCC, UL, CE
- RoHS - Complies with EU directive 2011/65/EU

Environmental Requirements

Temperature:

- Operating: 0°C to 55°C (32°F to 131°F)
- Storage: –40°C to 65°C (–40°F to 149°F)

Humidity:

- Operating: 10% to 80%
- Storage: 5% to 90%

Ordering Information

- A-U25N-P06G-PQ-G

TAKE THE NEXT STEP

Learn more about the Xilinx Alveo SmartNIC Accelerator Cards

Notes:
Feature availability is software release dependent. Please check release notes or contact Xilinx Support for more information.

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