

5G Beamforming with Versal AI Core Series

- > 2X TMACs/watt vs. competing FPGAs¹
- > Support for adaptable ORAN O-DU and O-RU functional partitioning
- > Adaptable beamforming for evolving algorithms

CHALLENGE

5G New Radio (NR) beamforming is the key to enabling a dramatic increase in network capacity. Beamforming technology, however, requires significant compute density and advanced high-speed connectivity to meet 5G throughput and low-latency requirements, making it extremely challenging for FPGAs to implement using traditional programmable logic and multiplier blocks alone.

Massive MIMO radio is the leading form factor for 5G commercial deployments, using 32 or 64 antenna elements for beamforming steered towards one or multiple users while using the same spectral resources. For typical radio configuration of a 64 antenna 200MHz system, the beamforming device in the radio needs to perform over 1.5 tera multiply and add (TMAC) operations per second for downlink. Additional compute is needed to perform beamforming in the uplink direction, all while meeting stringent thermal and system footprint constraints.



SOLUTION: VERSAL AI CORE ACAP FOR BEAMFORMING

The Versal[™] AI Core adaptive compute acceleration platform (ACAP) is a highly integrated, multicore, heterogeneous platform that delivers exceptional compute density at low power consumption to perform the real-time, low-latency signal processing demanded by beamforming algorithms in massive MIMO radios. Central to the platform are the AI Engines—a tiled array of C-programmable vector processors with flexible interconnect and distributed memory—ideal for implementing beamforming algorithms that can easily be reprogrammed after deployment.

AI Engines for Performance/Watt

Al Engines provide system-level compute far beyond that of traditional FPGA-based multipliers and DSP blocks, enabling 2X TMACs/watt over competing 10nm FPGAs¹, allowing more programmable logic resources to be used for additional functionality.

Adaptable ORAN

By using Versal AI Core ACAPs in conjunction with other Xilinx adaptable solutions, network suppliers and OEMs can split baseband processing across distributed units (DU) and radio units (RU) to realize fully adaptable networks.

Adaptable Beamforming

With 5G specifications in flux and beamforming techniques evolving, Versal AI Core ACAPs offer adaptive compute for different algorithm implementations to address a wide range of processing performance and compute precision.

1: Versal AI Core VC1902 ACAP vs. Intel Agilex AGF027 FPGA

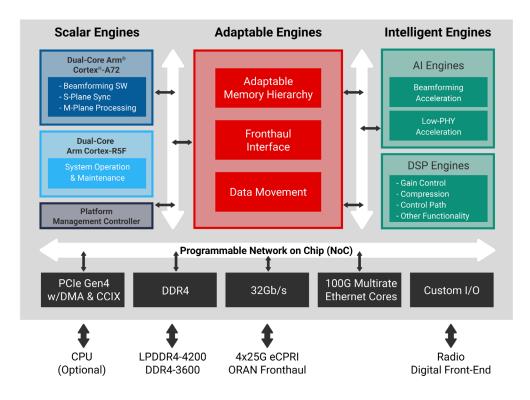




VERSAL ACAP IMPLEMENTATION

64TRX 200MHz+ Massive MIMO Beamformer Device

An ACAP implementation provides software programmability for C/C++ developers, hardware adaptability to evolve with beamforming algorithms, and hard IP integration for the on- and off-chip performance/watt and low latency required for 5G.

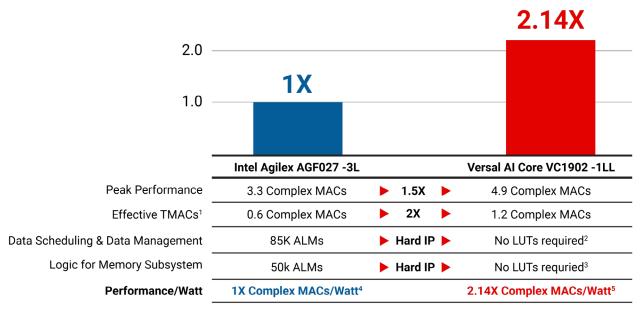


| PLATFORM HIGHLIGHTS | |
|---------------------------------|---|
| Al Engines | > Tiled array of vector processors capable of fixed- and floating-point signal processing and massive parallelism > Perform on-the-fly calculation of phase and gain coefficients for beamforming and Low-PHY acceleration > C/C++ programmable with 1GHz performance |
| Adaptable Engines | Manage ingress and egress data movement, dynamically controlling accelerators based on radio configuration Fine grained memory hierarchy to optimize accelerator performance Fronthaul interface logic—including eCPRI & 1588-PTP packet filter & framer/de-framer, xRAN pre-processing, and more |
| Scalar Engines | Manage initial system configuration and run-time control Perform system operation and maintenance (OA&M), S-Plane sync, and M-Plane processing Run beamforming application software |
| Programmable Network on Chip | Seamlessly integrates all engines and key interfaces Simplifies kernel and IP placement, reducing soft logic needed for connectivity Streamlines programming experience for software and hardware developers |
| Integrated Shell | Comprises hardened interface (PCIe[®] w/DMA, DDR4 controllers) and programmable network on chip (NoC) Ensures streamlined device bring-up and connectivity to off-chip interfaces-making the platform available at boot Delivers pre-engineered timing closure and logic resource savings |
| Multirate 100G Ethernet | Enables 10G/25G/50G eCPRI over Ethernet Optional built-in RS-FEC / FEC and IEEE Std 1588 hardware timestamping |

BENCHMARK

Shown below is a comparison of projected results for a 7nm production Versal VC1902 device vs. a 10nm Intel Agilex FPGA. Xilinx Versal AI Engine technology increases desired compute density while reducing power in contrast to an Agilex AGF027 based on traditional FPGA fabric, multipliers, memory, and soft interconnect.

64TRX 200MHz+ Massive MIMO Beamformer Device



RELATIVE MACS/WATT

1: Assumes 75% DSP utilization for 17,056 Intel Agilex FPGA 18x19 multipliers and 300 of 400 available Versal ACAP AI Engines 2: Versal ACAP AI Engines and AI Engine Interconnect provide data movement for compute

3: Versal ACAP hardened memory subsystem comprises network on chip and DDR controllers - no programmable logic required

4: Based on Quartus Power & Thermal Calculator 2021.2, assumes SmartVID and claimed static power savings

5: Based on Xilinx Power Estimator (XPE) available at https://www.xilinx.com/products/technology/power/xpe.html

TAKE THE NEXT STEP

- > To learn more about beamforming with AI Engines, read the application note or watch the video
- > To try the above benchmark yourself, visit www.xilinx.com/versal-performance-elevated
- > For more information on the Versal AI Core series, visit www.xilinx.com/versal-ai-core
- > To contact your local Xilinx sales representative, visit Contact Sales

Versal AI Core ACAP VCK190 Evaluation Kit <u>www.xilinx.com/vck190</u>



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