SOLUTION BRIEF

SmartPHY for DCI and Transport with Versal Premium Series

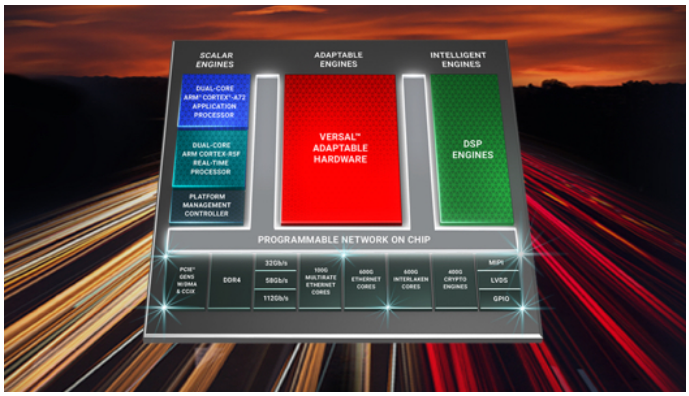
> Networked, power-optimized cores deliver 2.2X higher performance/watt vs. competing 10nm FPGAs[1]

> Scalable SerDes for emerging optical modules and a wide range of client rates and protocols

> Hardware adaptability for custom bridging and transport functions

CHALLENGE

As data centers move to 400G and beyond, data center interconnect (DCI) technology is at the heart of the cloud-centric world, providing the network capacity for users and applications to connect to compute, network, and storage resources. Bridging various client interfaces to line-side interfaces requires adjusting the SerDes rates and changing the FEC as needed. Due to the mismatch between coherent and clients, the need for multiplexing multiple clients or inverse multiplexing a client over multiple line interfaces has increased in many transport applications. In addition, many data centers are multi-tenant sites that exchange sensitive information, so encryption is required on all interfaces.



SOLUTION: SMARTPHY FOR DCI AND TRANSPORT WITH VERSAL PREMIUM SERIES

Versal™ Premium adaptive compute acceleration platform (ACAP) is a highly integrated, multicore, heterogeneous platform that enables implementation of a single card DCI bridging solution, providing up to 2.4Tb/s of network interfaces to client-side and transport-side optics (for a total of 4.8Tb/s bi-directional throughput). With the breakthrough integration of connectivity cores and High-Speed Crypto (HSC) Engines, the Xilinx SmartPHY solution implemented on Versal Premium ACAPs provides the highest bridging bandwidth density per device in the industry by far, enabling differentiated products for OEM system providers by accommodating a variety of server-side and transport-side optics and protocols support in a single platform.

Scalable SerDes for Diverse Client Interfaces

While coherent optic chipsets are deployed to overcome capacity limitations to provide 400G and beyond, client optics still use 25G NRZ transceivers in many transport applications. Versal Premium devices feature a broad mix of 25G NRZ, 58G PAM4, and 112G PAM4 transceivers to enable unmatched scalability from 10G to 800G to support both existing optics, next-generation NPUs, and coherent ASICs without hardware redesign.

Dedicated Power-Optimized Hard IP for Greater Performance/Watt

Versal Premium devices integrate power-optimized cores such as 100G/600G Ethernet cores, High-Speed Crypto (HSC) Engines, and integrated PCIe® Gen5 with DMA to provide system-level advantages, enabling 2.2X performance/watt over competing 10nm FPGAs[1]. Flexible configuration of Ethernet subsystems provides dynamic connectivity for Ethernet/non-Ethernet transponders that use different protocols and multiple FECs without consuming valuable programmable logic resources.

Hardware Adaptability Enabling Value Added Features

By integrating dedicated connectivity IP, Versal Premium ACAPs significantly lower logic utilization, retaining more resources for additional functionality such as IEEE Std 1588 timestamping, OTN wrapping, multiplexing, gearboxing, protocol translation, and snooping to address a wide range of dynamic network configurations.

2.2X

Performance/Watt[1]

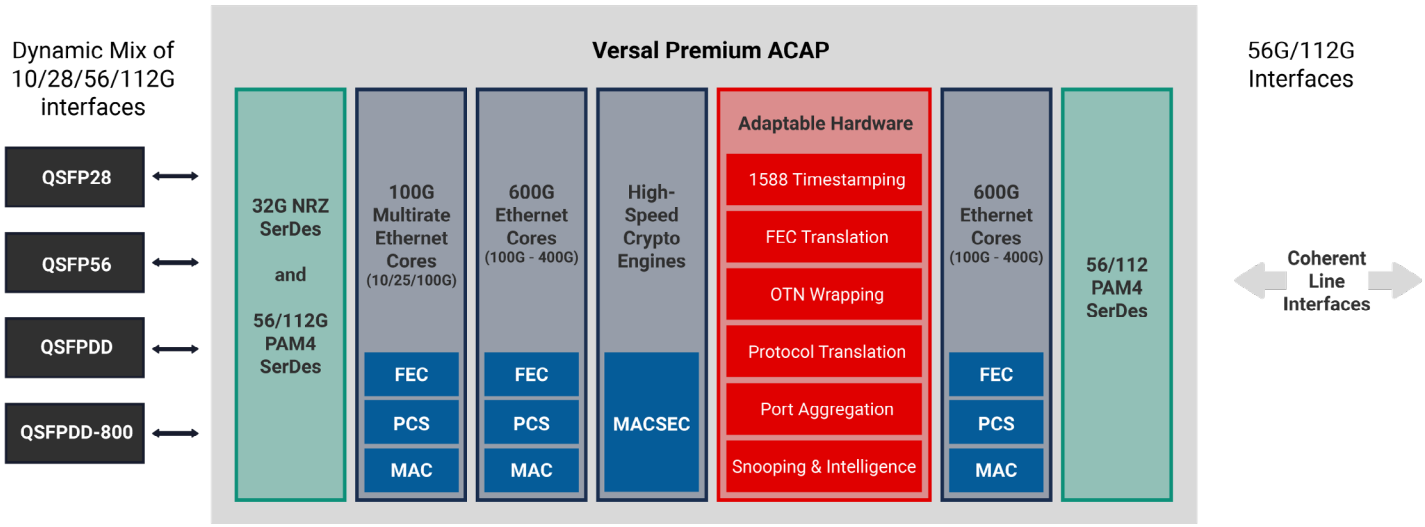
Versal Premium ACAP for Single-Chip DCI Line Card Implementation

1: Versal Premium VP1402 ACAP vs. Intel Agilex AGF022 FPGA implementation

VERSAL ACAP IMPLEMENTATION

DCI Bridging and Transport Application

The SmartPHY solution on the Versal Premium device features heterogeneous engines for efficient implementation, a dedicated connectivity IP for power-optimized interconnect and versatile client interfaces, and adaptable hardware for custom transponder applications to deliver multi-terabit DCI bridging and transport applications. With the right combination of SmartPHY and security technologies in a single platform, hyperscale data center operators and service providers gain the capacity and flexibility to interconnect data centers and build metro / core networks.

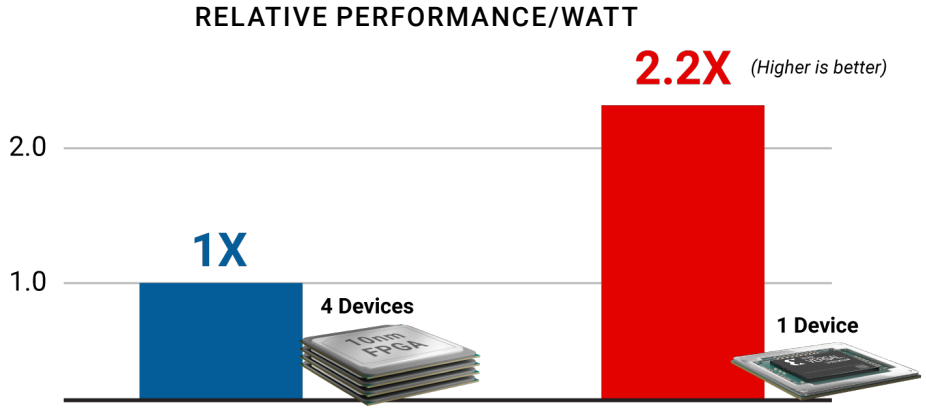


PLATFORM HIGHLIGHTS	
Adaptable Engines	> Adaptable to a wide range of complex bridging workloads including IEEE Std 1588 timestamping, OTN wrapping, protocol translation, FEC translation, and more > Custom transponders for non-Ethernet clients
100G/600G Ethernet Cores	> Channelized configuration for signal multiplexing between coherent and client interfaces running at different rates > Gearboxing for different electrical connectivity rates > Built-in FEC for robust error correction in optical links > Stand-alone MAC, FEC, and PCS for OTN or custom protocol implementation
Transceivers	> Mix of 32G NRZ, 58G PAM4, and 112G PAM4 transceivers for diverse client interfaces and rates > Single-lane 100G deployment for 400G and beyond
High-Speed Crypto (HSC) Engines	> Up to 1.6Tb/s of line-rate encryption throughput > AES-GCM-256/128 engine for encryption/decryption > 400G of MACsec, IPsec, and bulk encryption per engine for DCI-optimized security
Programmable Network on Chip (NoC)	> Seamless on-chip data movement for all engines and key interfaces > Simplifies kernel and IP placement, reducing soft logic needed for connectivity > Streamlines programming experience for software and hardware developers

BENCHMARK

1.6Tb/s Example: SmartPHY for DCI and Transport Application

Shown below is a comparison of estimated power consumption of an equivalent DCI Bridging design on Versal Premium devices vs. the projected performance of competing programmable devices. Versal architectural features, e.g., high-density, hardened Ethernet interfaces, crypto engines, and best in-class 112G PAM4 SerDes technology, drive a 2.2X better performance-per-watt against the equivalent Intel Agilex 10nm FPGA implementation. In addition, the Versal Premium VP1402 ACAP can scale to 2.4Tb/s in a single device, achieving even greater performance, area, and power advantages.



	Intel Agilex AGF022 -3E		Versal Premium VP1402 -2LL
# of Devices	4 devices	▶ 75% Less ▶	1 device
Area	10,080mm^2	▶ 70% Less ▶	3,025mm^2
4X 400G Crypto Engines	800k ALMs per device[1]	▶ Hard IP ▶	No LUTs required[2]
Power	212 watts[3]	▶ 51% Less ▶	104 watts[3]
Throughput	1.6Tb/s	◀ Equivalent ▶	1.6Tb/s[4]

1: Intel Agilex I series device with 200G half-duplex crypto was not available in the tools

2: Versal Premium ACAP features multiple hardened 400G High-Speed Crypto Engines – no programmable logic required

3: Based on Quartus Power & Thermal Calculator 2021.2 including SmartVID and static power savings, Xilinx XPE 2020.3

4: For ease of comparison, the example is limited to 1.6Tb/s throughput

TAKE THE NEXT STEP

> To learn more about the breakthrough integration of Versal Premium series, watch the video

> To try the above benchmark yourself, visit www.xilinx.com/versal-performance-elevated

> For more information on the Versal Premium series, visit www.xilinx.com/versal-premium

> To apply to the Versal Premium Evaluation Kit Early Access Program, visit Contact Sales

Versal Premium Evaluation Kit
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