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AXI Chip2Chip Aurora Reference Design for Real-Time Video Applications

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Summary

The Xilinx® LogiCORE™ IP AXI Chip2Chip core provides bridging between systems using the Advanced eXtensible Interface (AXI) for multi-device system-on-chip solutions. This application note demonstrates real time video traffic between two Kintex®-7 FPGA KC705 evaluation boards or one KC705 board and one Zynq®-7000 All Programmable (AP) SoC ZC706 evaluation board. The AXI Chip2Chip core provides connectivity between the two boards using SMA data connector cables.

The Reference Design Files for this application note can be downloaded from the Xilinx website. For detailed information about the design files, see Reference Design.

Included Systems

The reference design includes two integrated systems created with the Vivado® Design Suite: System Edition 2014.1 IP Integrator (IPI) feature. The Vivado Design Suite helps simplify the task of instantiating, configuring, and connecting IP blocks to form complex integrated systems. The design also includes a software application created with the Xilinx Software Development Kit (SDK). The application runs on either the MicroBlaze™ embedded processor or the ARM® Cortex™-A9 MPCore™ application processor and implements control, status and monitoring functions. Complete IP integrator and SDK project files are provided with the reference design to allow easy examination and modification of the design or to provide a template for beginning a new design.
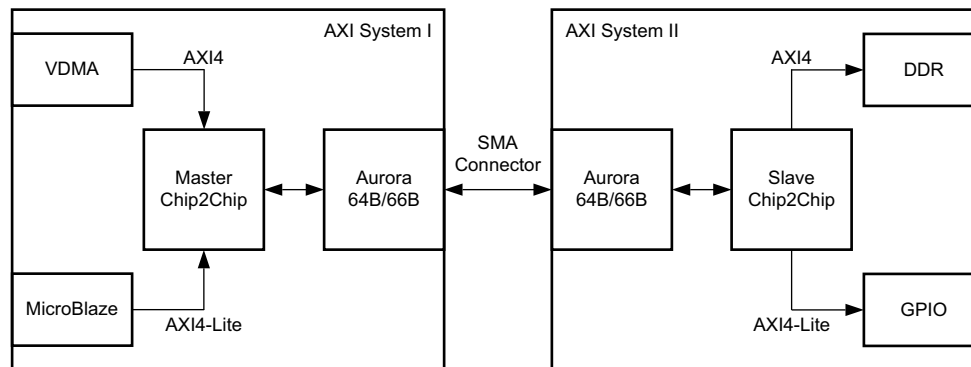
Introduction

The AXI Chip2Chip core bridges AXI4 transactions between multiple devices in compliance with the AXI protocol specifications to provide a low pin count, high-performance AXI chip-to-chip bridging solution (see AMBA AXI4 Specifications [Ref 1] and *LogiCORE IP AXI Chip2Chip Product Guide* (PG067) [Ref 2]).

The core supports these PHY layer interface types:

• Single Data Rate (SDR) SelectIO™ interface

• Double Data Rate (DDR) SelectIO interface

• Aurora 64B/66B serial data stream

This reference design demonstrates the capabilities of the AXI Chip2Chip core using the LogiCORE IP Aurora 64B/66B core as the PHY layer.

The reference design is implemented as two platforms named *AXI System I* and *AXI System II* (see Figure 1).

Figure 1:   **AXI Chip2Chip Core Typical Interconnections**

Each platform is implemented on a separate hardware evaluation kit board. Two versions of the reference design are included:

1. Demonstrates the connectivity between two Kintex-7 FPGA KC705 evaluation boards.

2. Demonstrates the connectivity between one KC705 board and one Zynq-7000 AP SoC ZC706 evaluation board.

The reference design implements a video system in which the source video signal is created by a Test Pattern Generator (TPG) core. Two instances of the AXI Chip2Chip core are instantiated, one as master and one as slave. Both master and slave instances of the AXI Chip2Chip core connect to an Aurora 64B/66B core through an AXI4 streaming interface. The master Chip2Chip core connects to the Aurora 64B/66B core in AXI Master mode, while the slave Chip2Chip core connects to the Aurora 64B/66B core in AXI Slave mode. The Aurora cores interface with each other using SMA connectors and cables.

The AXI System I platform contains the AXI Video Direct Memory Access (VDMA) reference design [Ref 4] in which the master Chip2Chip core replaces the AXI 7 series FPGA DDRx memory controller. The AXI System II platform contains the actual AXI 7 series FPGA DDRx memory controller connected to the slave Chip2Chip core in AXI Slave mode. By mapping the memory region of the AXI slave peripheral on the AXI System II platform to the Master Chip2Chip core, the AXI master peripherals on the AXI System I platform can access the slave peripherals on the AXI System II platform.

The AXI System I platform is designated the Master platform because it contains the AXI Chip2Chip core in master mode. Similarly, the AXI System II platform is designated the Slave platform.

Figure 2 shows a detailed block diagram of the reference design and its interconnections. The AXI VDMA block on the AXI System I platform (board A) writes and reads the video data from the external memory on the AXI System II platform (board B) through the AXI4 interfaces of the master and slave Chip2Chip cores. The MicroBlaze processor on board A configures the video

peripherals attached to the local AXI4-Lite interconnect. The ARM/MicroBlaze processor on board B configures the peripherals attached to the local AXI4-Lite interconnect.
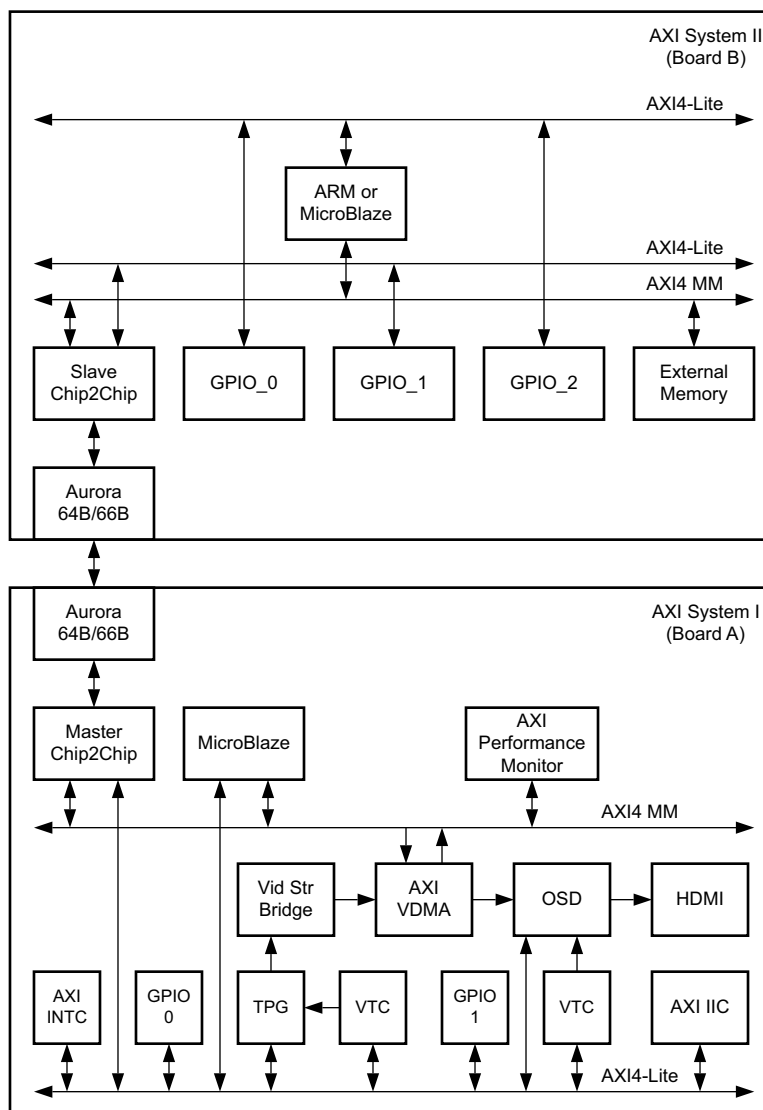

Figure 2: **Reference Design Detailed Block Diagram**

The ZC706 slave platform version of the design requires two external 125 MHz reference clock sources. *Any suitable conditioned 125 MHz clock source can be used to replicate this example test setup.*

Similar designs can be created with the AXI Chip2Chip core by replacing the AXI VDMA block with any master that generates AXI transactions. Similarly, the External Memory block can be replaced with any slave that receives AXI transactions.

Hardware Requirements

KC705 Slave Platform Version

- Two Kintex-7 FPGA KC705 evaluation boards.

- Two power adaptors for the evaluation boards

- One HDMI™ cable

- Display monitor supporting configurable resolutions (tested with Dell U2410F monitor using an HDMI cable)

- One USB Type-A to Mini-B 5-pin cable

- Two JTAG platform USB cables

- Four SMA connector cables for serial data

ZC706 Slave Platform Version

- One Kintex-7 FPGA KC705 evaluation board and one Zynq-7000 AP SoC ZC706 evaluation board.

- Two power adaptors for the evaluation boards

- One HDMI™ cable

- Display monitor supporting configurable resolutions (tested with Dell U2410F monitor using an HDMI cable)

- One USB Type-A to Mini-B 5-pin cable

- Two JTAG platform USB cables

- Two external differential 125 MHz SMA clock sources

- Four SMA connector cables for serial data

- Four SMA connector cables for external clock sources

Software Requirements

Software tool requirements for the AXI Chip2Chip reference design:

• Vivado Design Suite 2014.1: System Edition

Reference System Specifics

Two versions of the reference design are included:

1. Demonstrates the connectivity between two Kintex-7 FPGA KC705 evaluation boards.

2. Demonstrates the connectivity between one KC705 board and one Zynq-7000 AP SoC ZC706 evaluation board.

Each version of the reference design includes one Master platform and one Slave platform. The Master platforms of both versions of the reference design are similar and include these cores:

• AXI Chip2Chip

• Aurora 64B/66B

• AXI Interconnect

• Clock Generator

• Processor System Reset Module (`proc_sys_reset`)

• AXI IIC Bus Interface

• AXI GPIO

• AXI Interrupt Controller (INTC)

• Video Timing Controller (VTC)

• Test Pattern Generator (TPG)

• AXI Video Direct Memory Access (VDMA)

• AXI Performance Monitor

• On-Screen Display (OSD)

• HDMI Interface cores

• External SMA Clock source

Table 1 lists the peripheral address mapping for the Master platform.

Table 1: **AXI System I Platform Address Map**

Peripheral	Instance	Interface	Base Address	High Address
axi_chip2chip	axi_chip2chip_0	s_axi	0x20000000	0x3FFFFFFF
bram_if_cntlr	lmb_bram_if_cntlr_1	slmb	0x00000000	0x0001FFFF
mig_7series	mig_7series_0	s_axi	0x80000000	0x9FFFFFFF
axi_gpio	axi_gpio_0	s_axi	0x40000000	0x4000FFFF
axi_gpio	axi_gpio_1	s_axi	0x40010000	0x4001FFFF
axi_iic	axi_iic_1	s_axi	0x40800000	0x4080FFFF
axi_intc	axi_intc_1	s_axi	0x41200000	0x4120FFFF
axi_perf_mon	axi_perf_mon_0	s_axi	0x44A10000	0x44A1FFFF
axi_timer	axi_timer_1	s_axi	0x41C00000	0x41C0FFFF
axi_uartlite	axi_uartlite_1	s_axi	0x40600000	0x4060FFFF
axi_vdma	axi_vdma_1	s_axi_lite	0x44A20000	0x44A2FFFF
mdm	mdm_1	s_axi	0x41400000	0x41400FFF
v_cresample	v_cresample_0	ctrl	0x44A30000	0x44A3FFFF
v_osd	v_osd_1	ctrl	0x44A40000	0x44A4FFFF
v_rgb2ycrcb	v_rgb2ycrcb_0	ctrl	0x44A50000	0x44A5FFFF
v_tc	v_tc_1	ctrl	0x44A60000	0x44A6FFFF
v_tpg	v_tpg_1	ctrl	0x44A70000	0x44A7FFFF
axi_chip2chip	axi_chip2chip_0	s_axi_lite	0x50000000	0x5000FFFF

The Slave platform for the Kintex-7 FPGA includes these cores:

- 7 series Devices Memory Interface Solutions

- AXI Chip2Chip (in slave mode)

- Aurora 64B/66B

- MicroBlaze Processor

- AXI Interconnect

- AXI GPIO

- Clock Generator

- Processor System Reset Module

Table 2 lists the peripheral address mapping for the Kintex-7 FPGA Slave platform.

Table 2: **AXI System II Platform (KC705) Address Map**

Peripheral	Instance	Interface	Base Address	High Address
axi_bram_ctrl	axi_bram_ctrl_0	s_axi	0xE0000000	0xE000FFFF
axi_gpio	axi_gpio_0	s_axi	0x40000000	0x4000FFFF
axi_gpio	axi_gpio_2	s_axi	0x40010000	0x4001FFFF
axi_uartlite	axi_uartlite_0	s_axi	0x40600000	0x4060FFFF
bram_if_cntlr	microblaze_0_local_memory	slmb	0x00000000	0x00001FFF
axi_intc	microblaze_0_axi_intc	s_axi	0x41200000	0x4120FFFF
mig_7series	mig_7series_0	s_axi	0x20000000	0x3FFFFFFF

The Zynq-7000 AP SoC includes a processing system (PS). For the Slave platform, the PS is configured to include the UART and the DDR memory controller. The DDR memory controller is accessed through the HP0 port. The PS controls the AXI4-Lite video peripherals on the Master platform board through the M_AXI_GP1 port.

The Slave platform for the Zynq-7000 AP SoC includes these cores:

• AXI Interconnect

• AXI Chip2Chip (in slave mode)

• Aurora 64B/66B

• AXI GPIO

• Clock Generator

• Processor System Reset Module

Table 3 lists the peripheral address mapping for the Zynq-7000 AP SoC Slave platform.

Table 3: **AXI System II Platform (ZC706) Address Map**

Peripheral	Instance	Interface	Base Address	High Address
axi_gpio	axi_gpio_0	s_axi	0x41200000	0x4120FFFF
axi_gpio	axi_gpio_1	s_axi	0x41210000	0x4121FFFF
Mig_7series	Processing_system7_1	s_axi	0x00000000	0x3FFFFFFF

The KC705 and ZC706 evaluation kit boards contain LEDs which are used to indicate the status of the reference system during execution. Table 4 shows the LED assignment used for each platform.

Table 4:   **Platform LED Assignment**

Pin Name	LOC Value	LED
KC705 Master Platform		
axi_c2c_link_status_out	AA8	GPIO_LED_1
axi_c2c_config_error_out	AB8	GPIO_LED_0
axi_c2c_link_error_out	AE26	GPIO_LED_4
axi_c2c_multi_bit_error_out	AC9	GPIO_LED_2
KC705 Slave Platform		
axi_c2c_link_status_out	AA8	GPIO_LED_1
axi_c2c_config_error_out	AB8	GPIO_LED_0
axi_c2c_multi_bit_error_out	AC9	GPIO_LED_2
ZC706 Slave Platform		
axi_c2c_config_error_out	G2	GPIO_LED_CENTER
axi_c2c_link_status_out	Y21	GPIO_LED_LEFT
axi_c2c_multi_bit_error_out	W21	GPIO_LED_RIGHT

Hardware System Specifics

This section describes the configuration of the AXI Chip2Chip core. For information on hardware system specifics for VDMA configuration and other video-related IP cores, see the *AXI VDMA Reference Design Application Note* (XAPP742) [Ref 4]. For information on AXI system optimization and design trade-offs, see the *Vivado Design Suite: AXI Reference Guide* (UG1037) [Ref 6].

Configuring the AXI System I Platform

AXI Chip2Chip Core Master Instance (master_c2c)

When operating in master mode, the AXI Chip2Chip core can be configured as a slave for one or more AXI master peripherals. When operating in slave mode, the core can be configured as a master for one or more AXI slave peripherals.

The AXI Chip2Chip core can also be configured to act in independent or common clocking mode. In independent clocking mode, the physical layer interface can be operated at a higher or lower frequency compared to the AXI clock. In the common clocking mode, clock domain crossing latencies are reduced.

An AXI data width of 32 or 64 bits can be selected based on the system requirements. The Chip2Chip PHY type and PHY width parameters determine the number of I/O pins used for device-to-device interfacing. Three PHY layer interface types are supported:

- SDR SelectIO interface
- DDR SelectIO interface
- Aurora 64B/66B serial data stream

Compact 2:1 and 4:1 options reduce the number of I/O pins needed. Not all compact ratios are supported by all PHY layer interfaces. For example, with the Aurora PHY layer interface, only compact 2:1 and compact 1:1 are supported.

In this reference design, the 64-bit AXI Chip2Chip core master instance is configured for Independent clocking mode with the PHY layer operating at a frequency of 125 MHz. The AXI4 and AXI4-Lite interfaces of the AXI Chip2Chip core are configured in Master mode. The PHY Type is configured as Aurora 64B/66B with Compact 2:1 PHY Width to obtain a good data rate for transmitting and receiving the 720p real-time video traffic signals. The AXI WUser Width is set to one bit (see Figure 3).
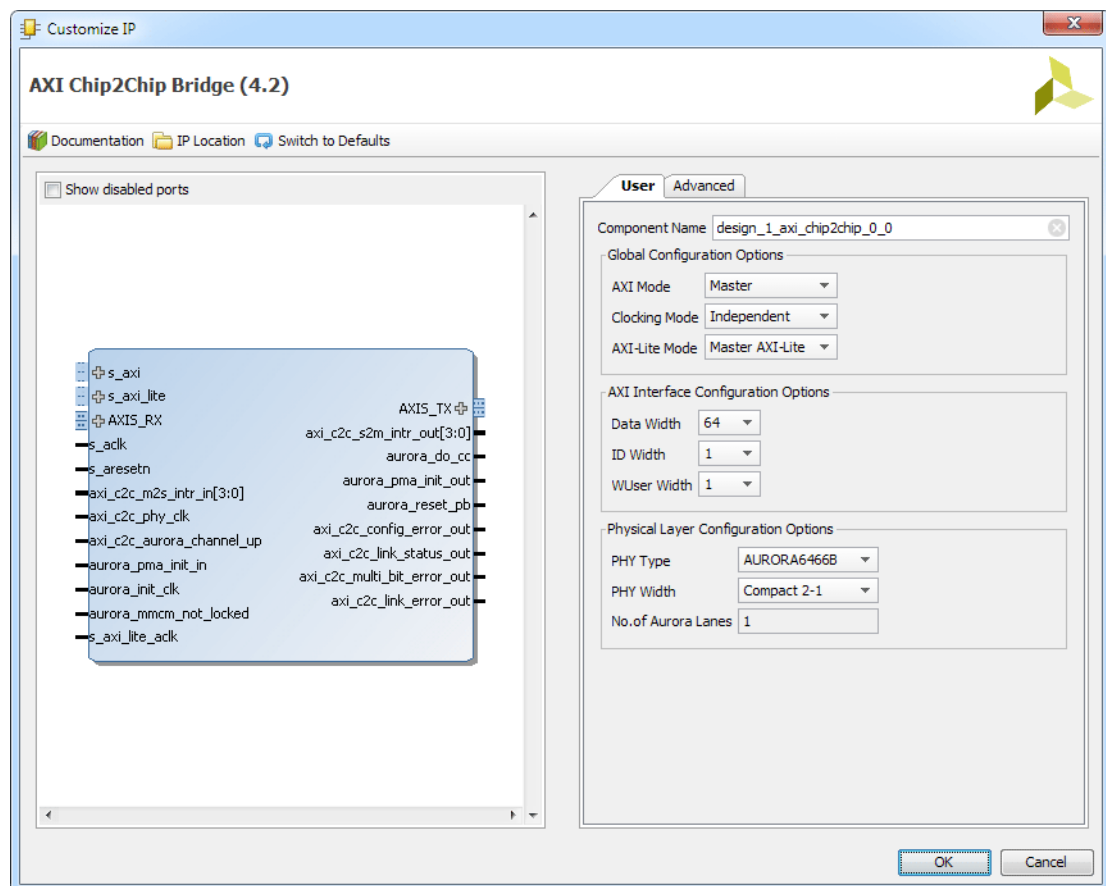

Figure 3:   **AXI Chip2Chip Core Master Mode Configuration**

Aurora 64B/66B

The Aurora 64B/66B core acts as the PHY layer in this configuration of the AXI Chip2Chip core. The Aurora core uses an external SMA clock of 125 MHz for the GT reference clock. The line rate is configured for 6.25 Gb/s with Duplex data flow mode. Both master platforms share the same configuration. The Aurora Core Options settings for the master platform should match those shown in Figure 4. On the GT Selections tab, ensure that the lane is assigned to the transceiver in Quad-2 (GTXQ2) as shown in Figure 5.

Note: The GTXQ2 transceiver is the only transceiver pinned out to SMA connectors on the KC705 board. When placing the cursor over the list box setting, a tooltip appears to verify the location of the selected transceiver.

On the Shared Logic tab, ensure that **include Shared Logic in core** is selected as shown in Figure 6.
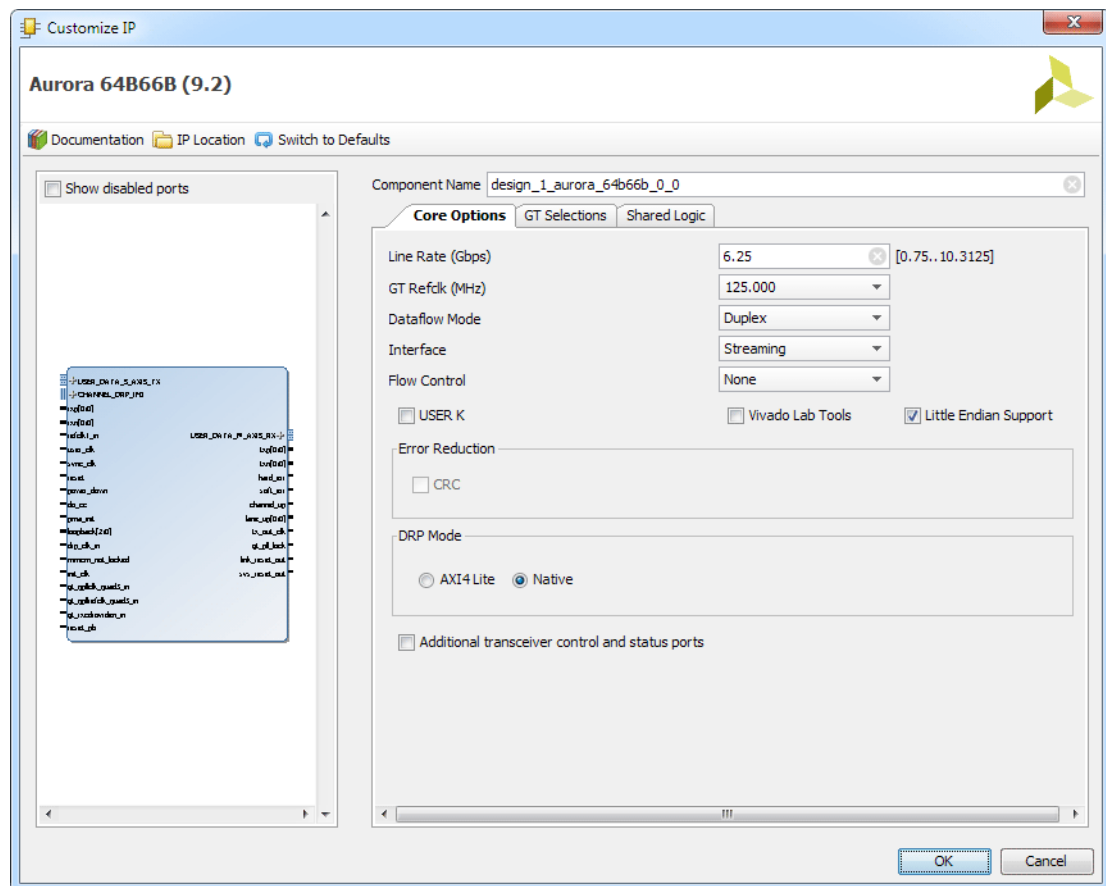

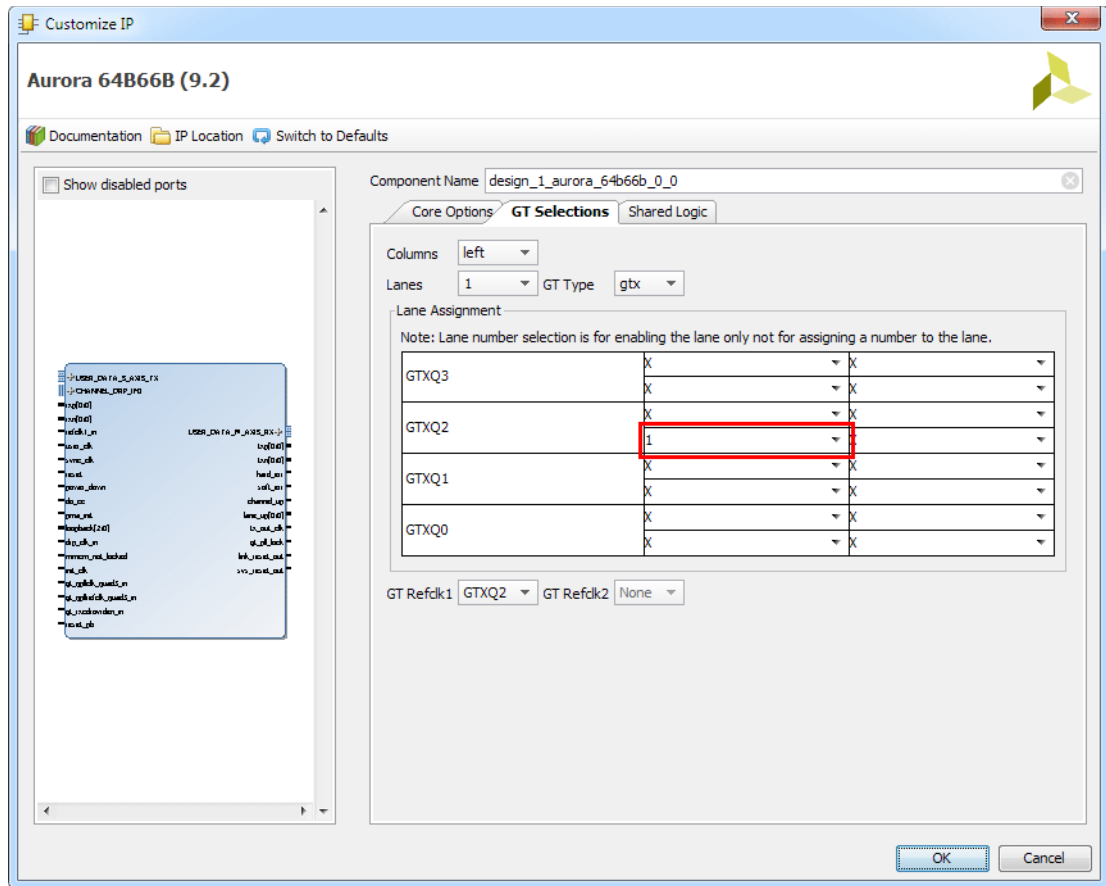*Figure 4:*   **Aurora 64B/66B Core Options for Master Platform**

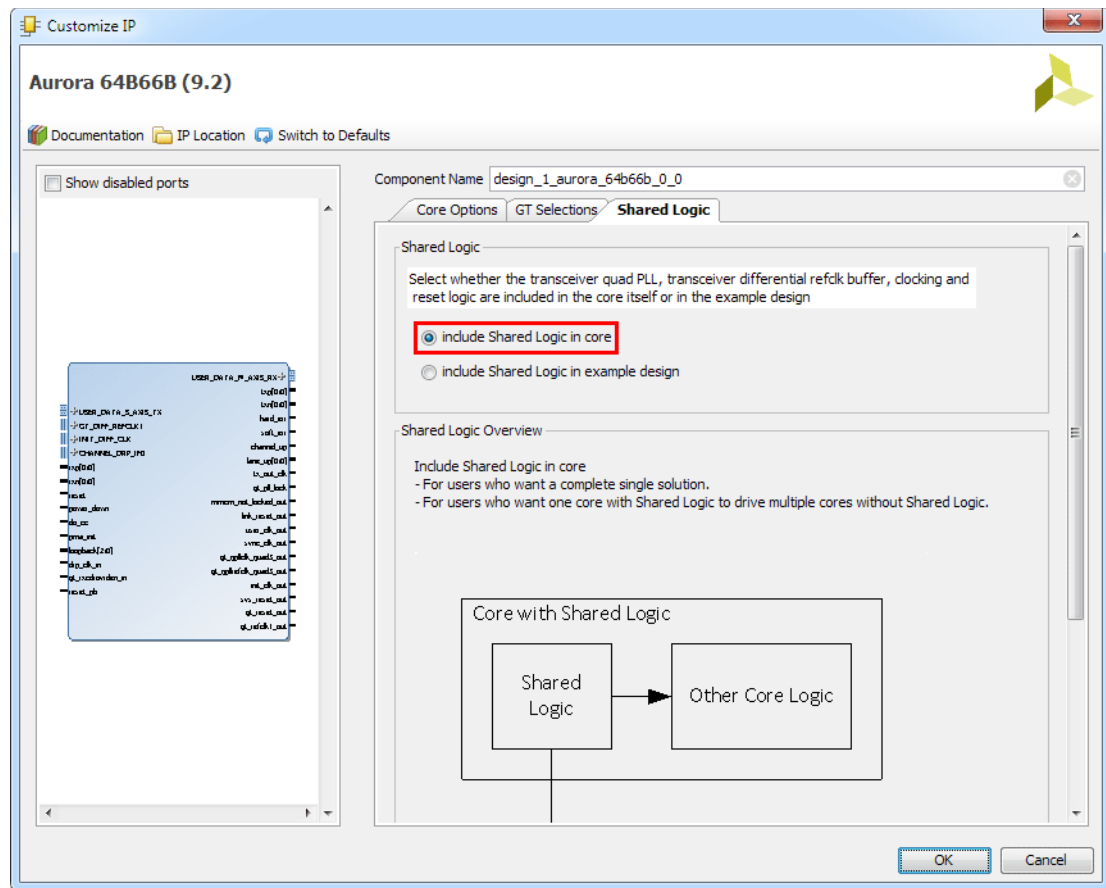*Figure 5:* **Aurora 64B/66B GT Selections for Master Platform**

Figure 6: **Aurora 64B/66B Shared Logic Setting for Master Platform**

AXI Performance Monitor

The AXI Performance Monitor core measures major performance metrics within the AXI4 interconnect system. The core consists of a slave AXI4-Lite interface which allows the processor to access the registers. The AXI performance monitor core only monitors the read and write channels between the AXI slave and the AXI interconnect. The core does not modify any of the AXI transactions it is monitoring.

The AXI Performance Monitor core is capable of measuring various performance metrics. For example:

- Total read byte count
- Total write byte count
- Read requests
- Write requests
- Write responses

Count start and count end conditions are provided by the processor through the register interface. The core global clock counter measures the number of clocks between count start and count end events. The counters used for the performance monitor can be configured for 32 or 64 bits using the register interface. Final user-selectable metrics can also be read through the register interface.

In this reference design, the slave AXI4 interface of the master AXI Chip2Chip core is monitored and the performance metrics are reported.

Master System Clocking

The clocking requirements for the master platforms vary depending on the version of the reference design. The Aurora 64B/66B core on the KC705 board uses an internal clock on the KC705 board slave platform version. On the ZC706 slave platform version, an external SMA clock of 125 MHz is required for the GT Reference clock. The KC705 board accepts an external SMA clock on connectors J15 and J16.

SMA Data Connections

SMA data cables are connected between the master and slave platform boards using KC705 connectors J17, J18, J19 and J20.

Configuring the AXI System II Platform

AXI Chip2Chip Core Slave Instance (slave_c2c)

In this reference design, the 64-bit AXI Chip2Chip core slave instance is configured for Independent clocking mode with the PHY layer operating at a frequency of 125 MHz. The AXI4 and AXI4-Lite interfaces of the AXI Chip2Chip core are configured in Slave mode. The PHY Type is configured as Aurora 64B/66B with Compact 2:1 PHY Width to obtain a good data rate for transmitting and receiving the 720p real-time video traffic signals. The AXI WUser width is set to one bit (see Figure 7). In general, all parameters except the AXI4 and AXI4-Lite modes are set to match the master instance of the AXI Chip2Chip core.
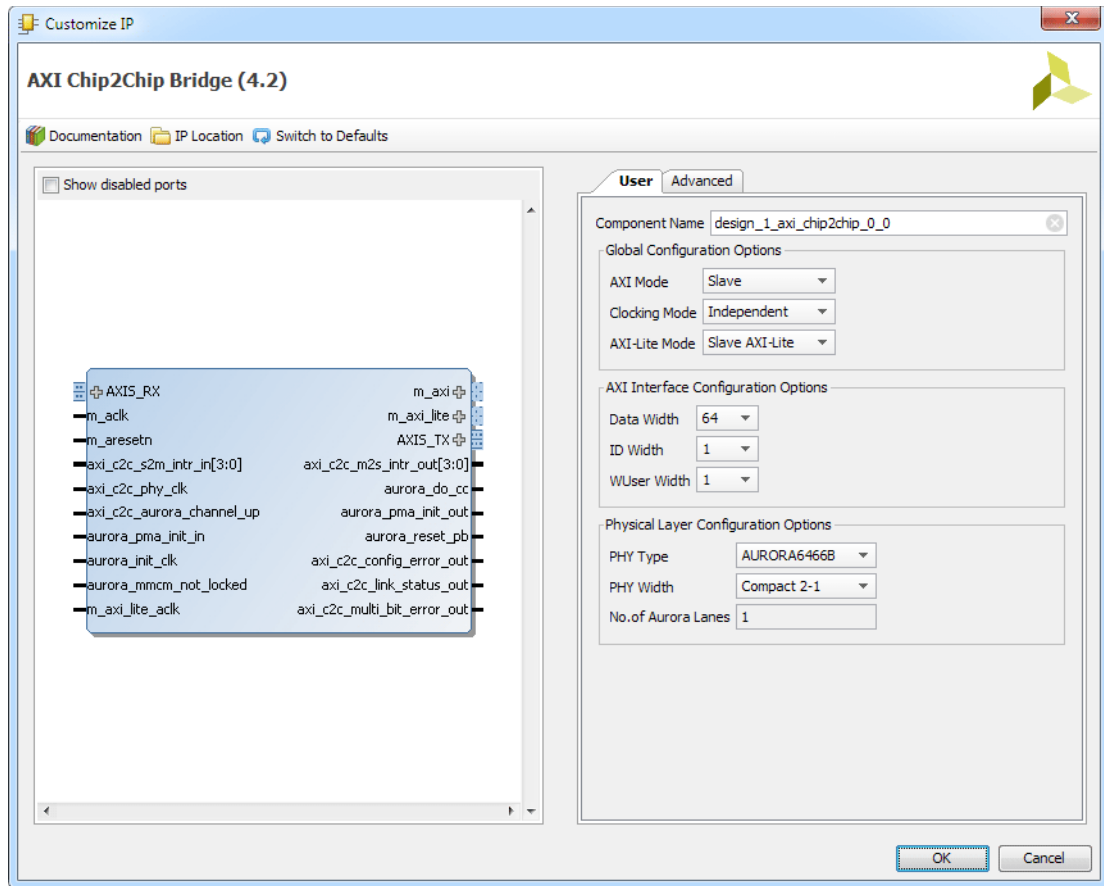
Figure 7: **AXI Chip2Chip Core Slave Mode Configuration**

Aurora 64B/66B

The Aurora 64B/66B core acts as the PHY layer in this configuration of the AXI Chip2Chip core. The Aurora core uses an external SMA clock of 125 MHz for the GT reference clock. The line rate is configured for 6.25 Gb/s with duplex data flow mode. Both slave platforms share the same configuration as that of the master platform. The Aurora Core Options settings for the slave platform using either the KC705 board or the ZC706 board should match those shown in Figure 8.
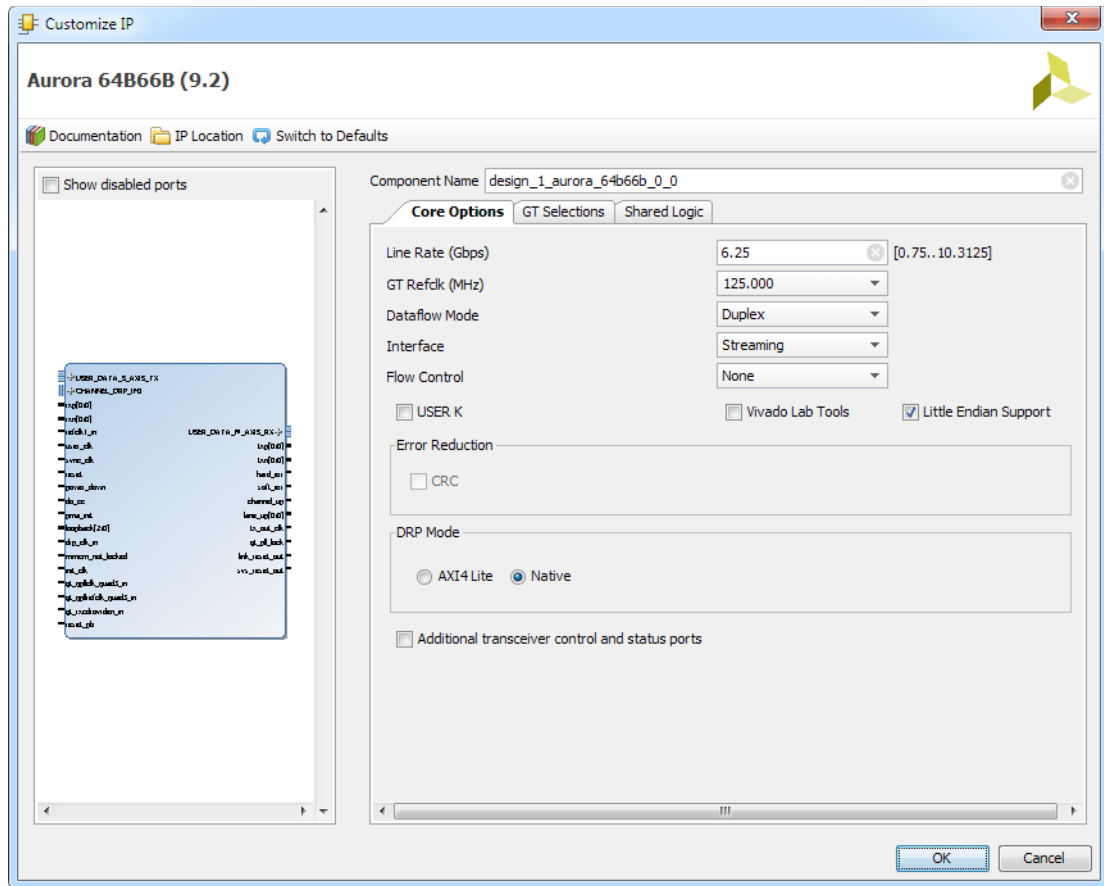
Figure 8: **Aurora 64B/66B Core Options for Slave Platform**

The Aurora GT Selections for the slave platform using the KC705 board should match those shown in Figure 9. Ensure that the lane is assigned to the first transceiver in Quad-2 (GTXQ2) as shown.

Note: The GTXQ2 transceiver is the only transceiver pinned out to SMA connectors on the KC705 board. When placing the cursor over the list box setting, a tooltip appears to verify the location of the selected transceiver.

Figure 9: **Aurora 64B/66B GT Selections for KC705 Slave Platform**

The Aurora GT Selections for the slave platform using the ZC706 board should match those shown in Figure 10. Ensure that the lane is assigned to the second transceiver in Quad-2 (GTXQ2) as shown.
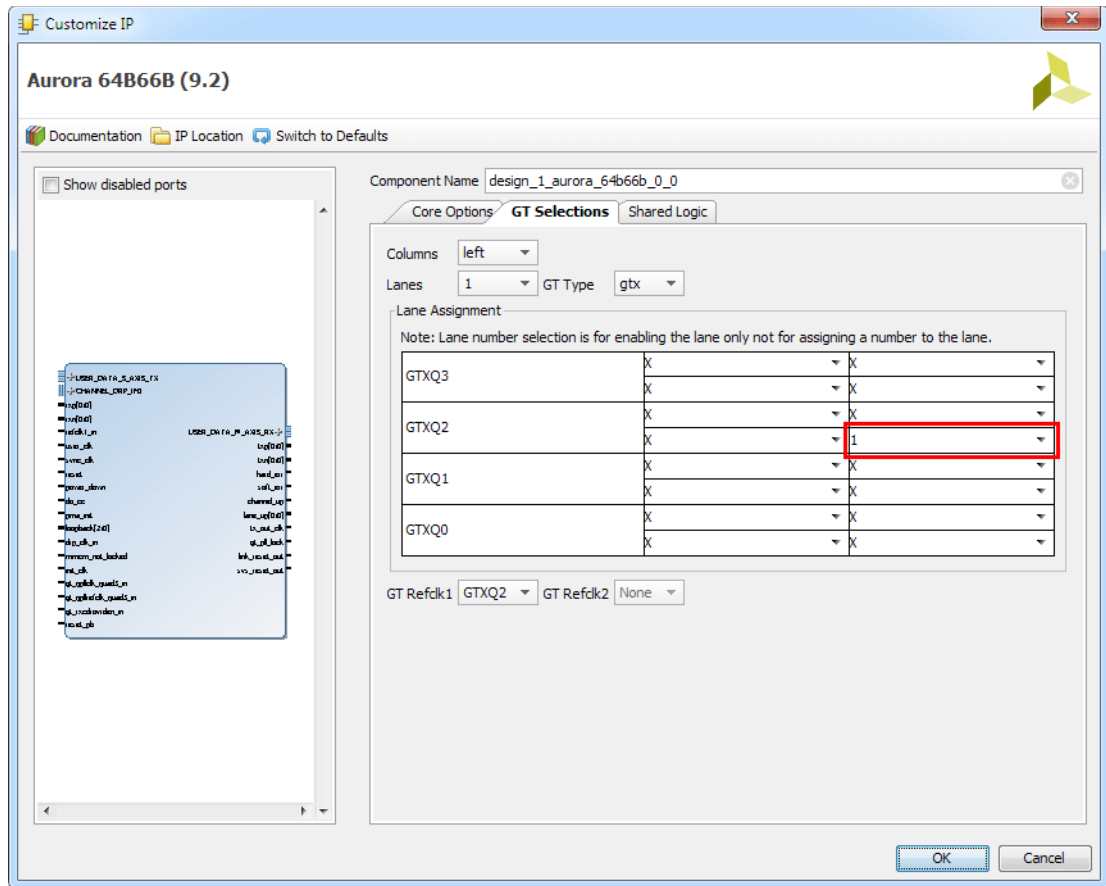
Figure 10: **Aurora 64B/66B GT Selections for ZC706 Slave Platform**

On the Shared Logic tab, ensure that **include Shared Logic in core** is selected as shown in Figure 11.
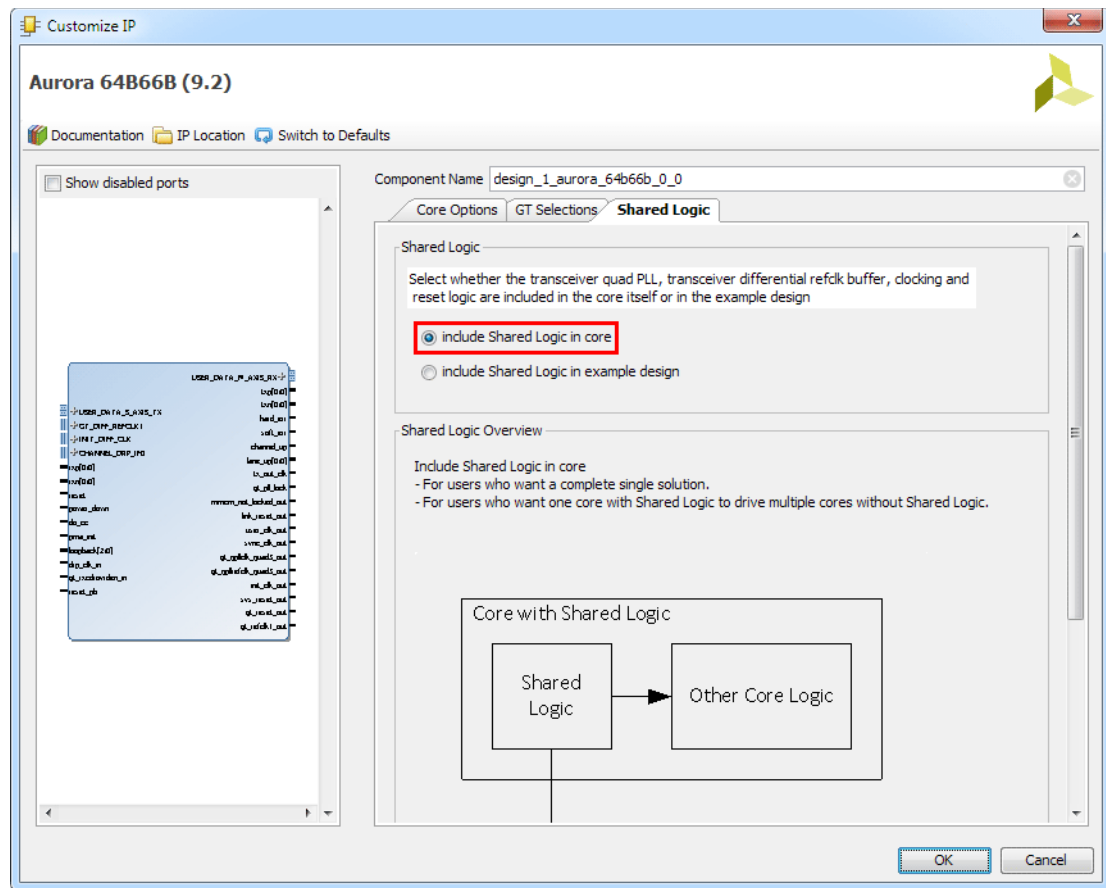
Figure 11: **Aurora 64B/66B Shared Logic Settings for Slave Platform**

Slave Platform Memory System

On the KC705 slave platform, the 7 series devices memory interface solutions core is used to create an interface with the DDR3 SDRAM device. The AXI4 interface is configured as 64 bits running at 200 MHz. The 7 series devices memory interface solutions core is configured for a write/read acceptance of two and 512-deep write/read. The AXI4 interconnect memory controller port FIFOs are enabled. See the *Zynq-7000 SoC and 7 Series Devices Memory Interface Solutions User Guide* (UG586) [Ref 7] for more details on the memory interface solutions core.

On the ZC706 slave platform, the AXI Chip2Chip core connects to the high-performance (HP) slave AXI4 interface of the PS. The HP port enables a high-throughput datapath between the AXI4 masters in the programmable logic (PL) and the DDR3 memory of the PS.

Slave System Clocking

The clocking requirements for the slave platforms vary depending on the version of the reference design. The Aurora 64B/66B core on the KC705 board uses an internal clock on the KC705 board slave platform version. On the ZC706 slave platform version, an external SMA clock of 125 MHz is required for the GT reference clock. Clocking for the KC705 slave platform is the same as for the KC705 master platform. The external SMA clock is connected to J15 and J16 on the KC705 board.

On the ZC706 slave platform, the external SMA clock is connected to J36 and J31 on the ZC706 board.

Serial Transceiver Connectors

SMA data cables are connected between the master and slave platform boards. Data cables are connected to J17, J66, J19 and J20 on the KC705 board, and to J32, J33, J34 and J35 on the ZC706 board.

Software Application

The application software for the master platform (Board-A) configures the AXI4-Lite slaves. See the *AXI VDMA Reference Design Application Note* (XAPP742) [Ref 4] for more details on the software application.

Building Hardware

This section describes how to rebuild the hardware designs. Before rebuilding the projects, Ensure that Vivado design suite 2014.1: System Edition is properly installed.

Rebuilding the Master Platform

1. Unzip the reference design files accompanying this application note (see Reference Design, page 29). The local folder into which the design files are placed is subsequently referred to as <unzip dir>.

   Note: On Windows workstations, it might be necessary to place the design files in the root directory of the selected drive to accommodate the longer path names present in the source folders.

2. Launch Vivado Design Suite.

3. Click **Open Project** and select the following workspace path:

   For KC705 slave platform:

   ```
   <unzip_dir>/c2c_aurora/kintex-kintex/HW/master/project_1/project_1.xpr
   ```

   For ZC706 slave platform:

   ```
   <unzip_dir>/c2c_aurora/kintex-zynq/HW/master/project_1/project_1.xpr
   ```

4. Click **OK**.

5. Select **Flow > Generate Bitstream** or click **Generate Bitstream** under **Program and Debug** in the Flow Navigator pane. Click **Yes** if prompted to run Synthesis and Implementation.

Rebuilding the Slave Platform

1. If necessary, unzip the reference design files accompanying this application note (see Reference Design, page 29). The local folder into which the design files are placed is subsequently referred to as <unzip dir>.

2. Launch Vivado Design Suite.

3. Click **Open Project** and select the following workspace path:

    For KC705 slave platform:

    ```
    <unzip_dir>/c2c_aurora/kintex-kintex/HW/slave/project_1/project_1.xpr
    ```

    For ZC706 slave platform:

    ```
    <unzip_dir>/c2c_aurora/kintex-zynq/HW/slave/project_1/project_1.xpr
    ```

4. Click **OK**.

5. Select **Flow > Generate Bitstream** or click **Generate Bitstream** under **Program and Debug** in the Flow Navigator pane. Click **Yes** if prompted to run Synthesis and Implementation.

Compiling the Software Application in SDK

1. Launch SDK.

2. In the Workspace Launcher, select the following workspace path and click **OK**:

    For KC705 slave platform:

    ```
    <unzip_dir>/c2c_aurora/kintex-kintex/SW/master/SW
    ```

    For ZC706 slave platform:

    ```
    <unzip_dir>/c2c_aurora/kintex-zynq/SW/master/SW
    ```

3. Select **Project > Build All**.

4. If the SDK project is *not* visible in the workspace, import the SDK project by following these steps:

    a. Select **File > Import**.

    b. Select **General > Existing Projects into Workspace**.

    c. Click **Next**.

    d. Change Root Directory to:

        For KC705 slave platform:

        ```
        <unzip_dir>/c2c_aurora/kintex-kintex/SW/master/SW
        ```

        For ZC706 slave platform:

        ```
        <unzip_dir>/c2c_aurora/kintex-zynq/SW/master/SW
        ```
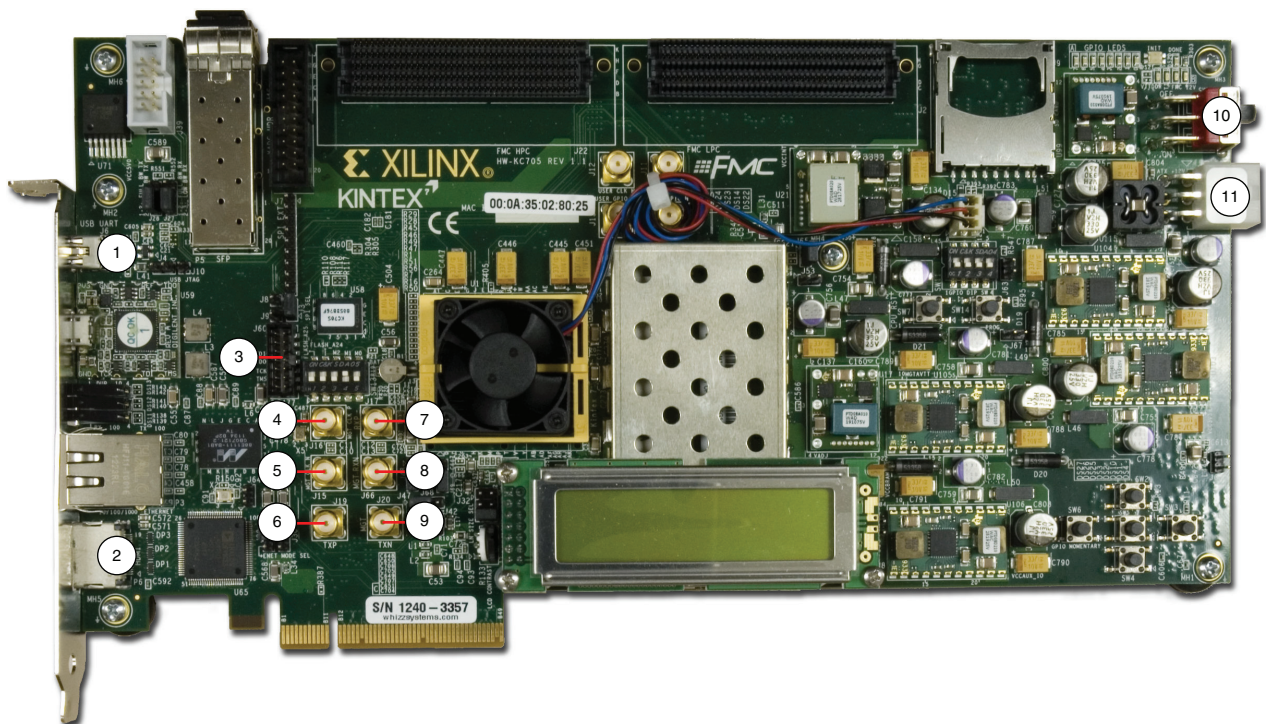
e. Click **Finish**.

The board support package (BSP) and software applications are compiled at this step. The process can take up to five minutes. Upon completion, existing applications can be modified and new applications can be created using the SDK.

Executing the Reference Design in Hardware

Setting Up the KC705 Slave Platform System

This example illustrates real time video traffic between two Kintex-7 FPGA KC705 evaluation boards serving as the master and slave platforms (see Figure 2, page 3). The master platform, AXI System I, Board A, connects to the slave platform, AXI System II, Board B, using SMA data cables. The KC705 board connectors are shown in Figure 12.

Figure 12:   **KC705 Board Connectors**

In these instructions, numbers in parentheses correspond to callout numbers in Figure 12. Make these connections using the SMA to SMA connector cables:

1. Connect TXP (6) from Board A to RXP (7) of Board B.

2. Connect TXN (9) from Board A to RXN (8) of Board B.

3. Connect TXP (6) from Board B to RXP (7) of Board A.

4. Connect TXN (9) from Board B to RXN (8) of Board A.

Make these connections using the specified cables:

1. Connect a USB Type-A to Mini-B 5-pin cable from the host PC to the USB UART port of Board A (1). Ensure that the appropriate device drivers are installed on the host PC. See *Kintex-7 FPGA KC705 Evaluation Kit Getting Started Guide* (UG883) [Ref 11].

2. Connect a JTAG platform USB cable to the platform cable header of Board A (3).

3. Connect a JTAG platform USB cable to the platform cable header of Board B (3).

4. Connect an HDMI video cable from the HDMI connector (2) of Board A to a monitor capable of displaying a 1280 x 720p 60Hz video signal.

5. Connect a KC705 Universal 12v power adapter cable to the power connector (11) of both boards.

6. Set the power switch (10) of both boards to the ON position.

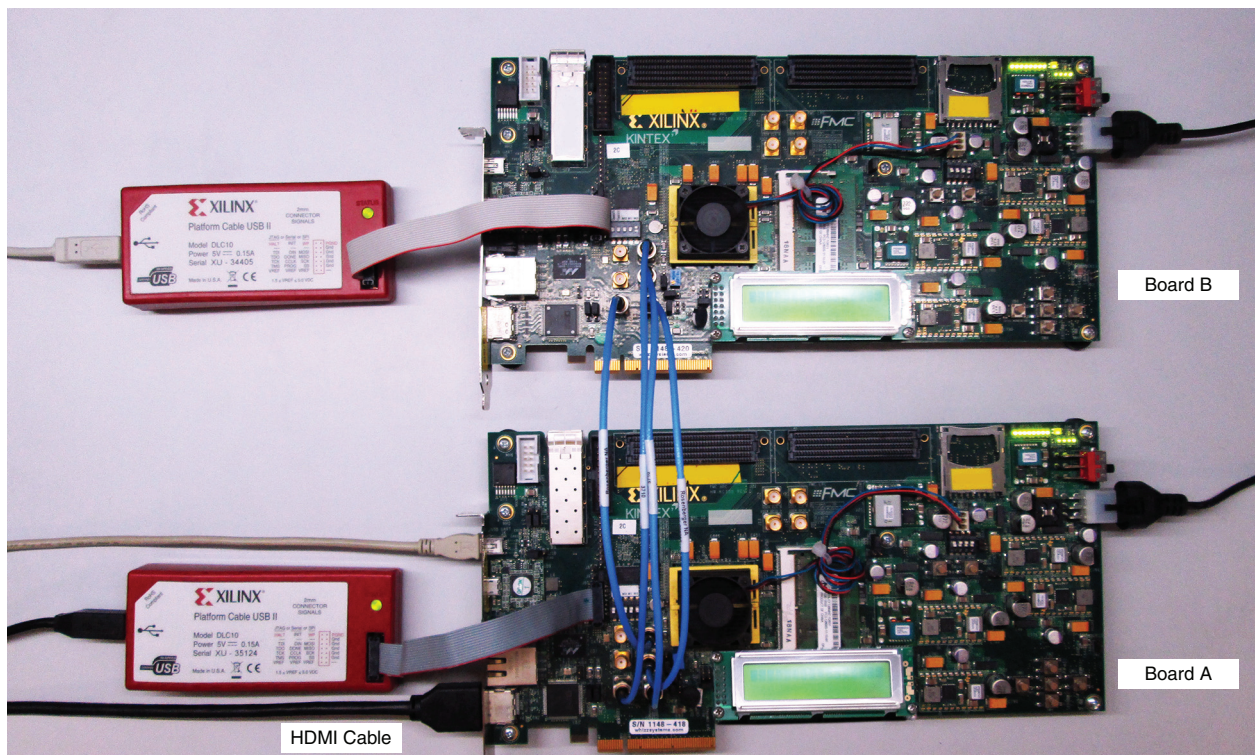The completed setup should resemble that shown in Figure 13.

Figure 13: **KC705 Master Platform to KC705 Slave Platform Setup**

Executing the KC705 Slave Platform Reference Design

1. Start a terminal program such as HyperTerminal on the host PC using these settings:

   - Baud rate: **9600**
   - Data bits: **8**
   - Parity: **None**
   - Stop bits: **1**
   - Flow control: **None**

2. Connect the Board B JTAG platform USB cable to the host PC.

3. In the command shell or terminal window, change to the slave download directory:

   ```
   % cd <unzip_dir>/c2c_aurora/kintex-kintex/ready_for_download/slave
   ```

4. Launch the Xilinx Microprocessor Debugger:

   Windows:

   Select **Start > All Programs > Xilinx Design Tools > SDK 2014.1 > Xilinx Microprocessor Debugger 2014.1**

   Linux:

   ```
   % xmd
   ```

5. Download the bitstream file to Board B:

   ```
   XMD% fpga -f design_1_wrapper.bit
   ```

6. Exit the XMD command prompt:

   ```
   XMD% exit
   ```

7. Connect the Board A JTAG platform USB cable to the host PC.

8. In the command shell or terminal window, change to the master download directory:

   ```
   % cd <unzip_dir>/c2c_aurora/kintex-kintex/ready_for_download/master
   ```

9. Launch the Xilinx Microprocessor Debugger:

   Windows:

   Select **Start > All Programs > Xilinx Design Tools > SDK 2014.1 > Xilinx Microprocessor Debugger 2014.1**

   Linux:

   ```
   % xmd
   ```

10. Download the bitstream file to Board A:

    ```
    XMD% fpga -f design_1_wrapper.bit
    ```

11. Connect the processor:

    ```
    XMD% connect mb mdm
    ```

12. Disable entire system reset on software download:

    ```
    XMD% debugconfig -reset_on_run system disable
    ```

13. Reset the processor:

    ```
    XMD% rst -processor
    ```

14. Download the processor code file:

    ```
    XMD% dow app_vp.elf
    ```

15. Execute the reference system:

    ```
    XMD% run
    ```

16. Observe that the `axi_c2c_link_status_out` LED (AA8) is glowing on both boards. See Table 4, page 8 for LED assignment.

17. Select one of the patterns from the menu displayed on the HyperTerminal console.

Continue to Hardware and Software Execution Results, page 28.

Setting Up the ZC706 Slave Platform System

This example illustrates real time video traffic between one Kintex-7 FPGA KC705 evaluation board serving as the master platform and one Zynq-7000 AP SoC ZC706 evaluation board serving as the slave platform (see Figure 2, page 3). The master platform, AXI System I, Board A, connects to the slave platform, AXI System II, Board B, using SMA data cables. Additionally, a 125 MHz external clock source is connected to the master and slave platform boards using SMA cables. The KC705 board connectors are shown in Figure 12, page 21. The ZC706 board connectors are shown in Figure 14.
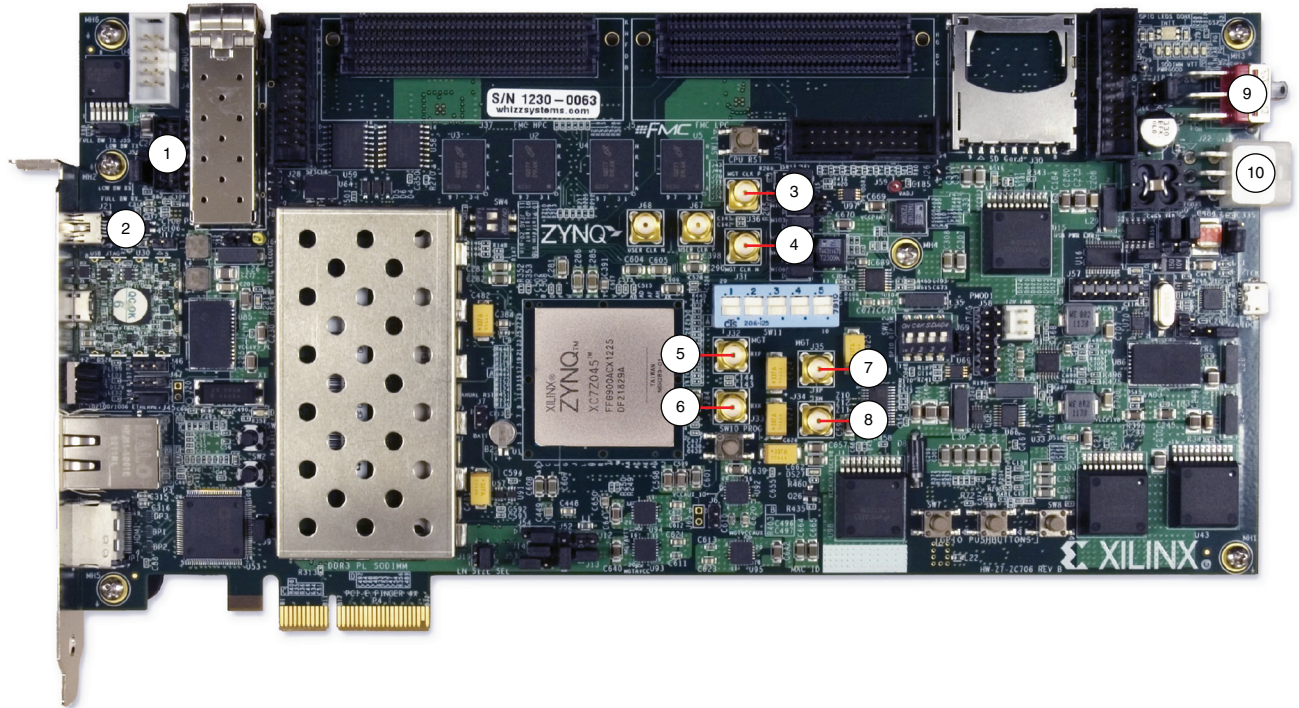
Figure 14: **ZC706 Board Connectors**

In these instructions, numbers in parentheses correspond to callout numbers in Figure 12, page 21 for KC705 (Board A) and Figure 14 for ZC706 (Board B). Make these connections using the SMA to SMA connector cables:

1. Connect TXP (6) from Board A to RXP (5) of Board B.

2. Connect TXN (9) from Board A to RXN (6) of Board B.

3. Connect TXP (7) from Board B to RXP (7) of Board A.

4. Connect TXN (8) from Board B to RXN (8) of Board A.

5. Connect CLKP from clock source 1 to MGT CLK P (4) of Board A.

6. Connect CLKN from clock source 1 to MGT CLK N (5) of Board A.

7. Connect CLKP from clock source 2 to MGT CLK P (3) of Board B.

8. Connect CLKN from clock source 2 to MGT CLK N (4) of Board B.

Make these connections using the specified cables:

1. Connect a USB Type-A to Mini-B 5-pin cable from the host PC to the USB UART port of Board A (1). Ensure that the appropriate device drivers are installed on the host PC. See *Kintex-7 FPGA KC705 Evaluation Kit Getting Started Guide* (UG883) [Ref 11].

2. Connect a JTAG platform USB cable to the platform cable header of Board A (3).

3. Connect a JTAG platform USB cable to the platform cable header of Board B (1).

4. Connect an HDMI video cable from the HDMI connector (2) of Board A to a monitor capable of displaying a 1280 x 720p 60Hz video signal.

5. Connect a KC705 Universal 12v power adapter cable to the power connector (11) of Board A.

6. Connect a ZC706 12v AC adapter cable to the power connector (10) of Board B.

7. Set the power switch (10) of Board A and (9) of Board B to the ON position.

The completed setup should resemble that shown in Figure 15.

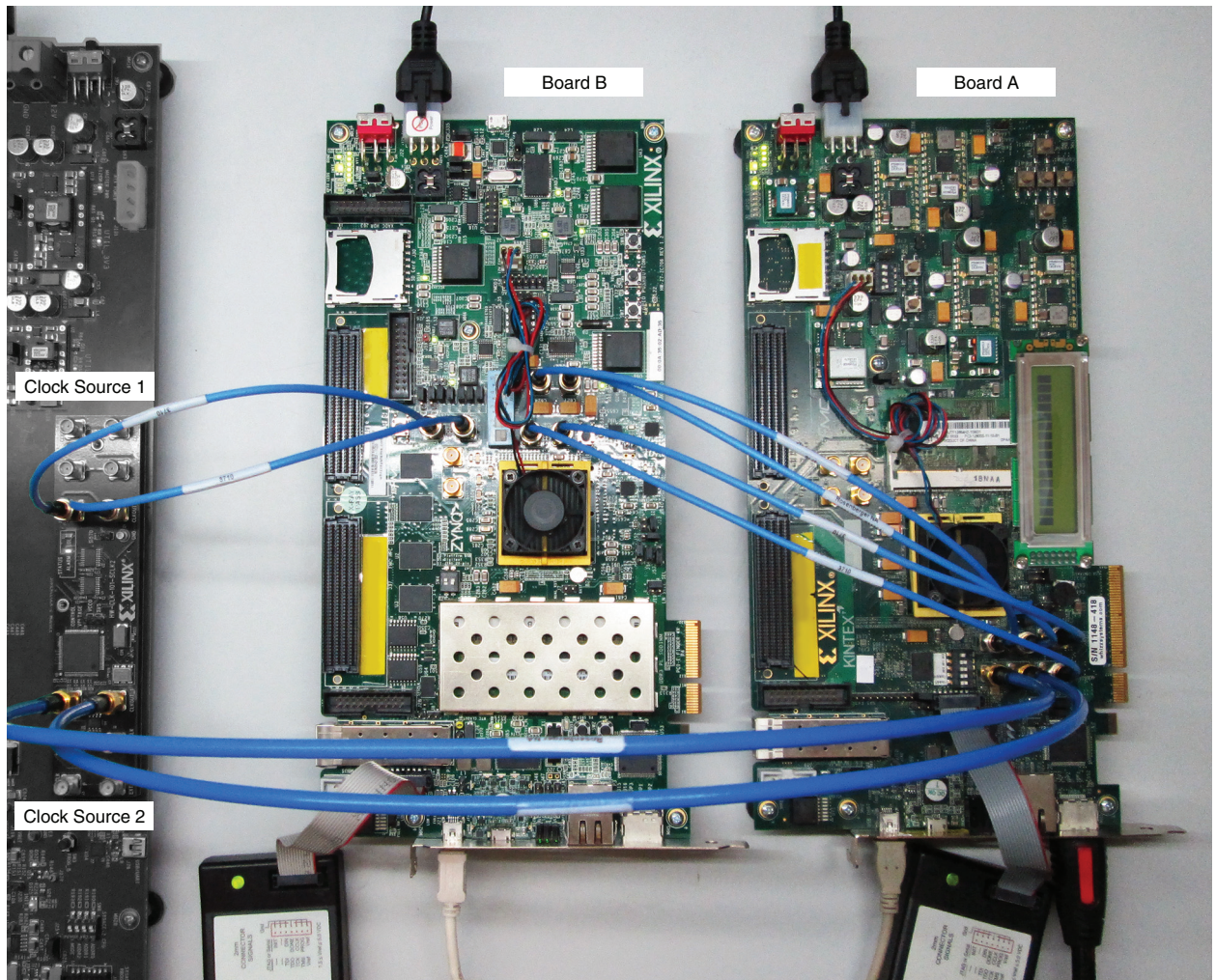*Figure 15:*   **KC705 Master Platform to ZC706 Slave Platform Setup**

Executing the ZC706 Slave Platform Reference Design

1. Start a terminal program such as HyperTerminal on the host PC using these settings:

    ◦   Baud rate: **9600**

    ◦   Data bits: **8**

    ◦   Parity: **None**

    ◦   Stop bits: **1**

    ◦   Flow control: **None**

2. Connect the JTAG platform USB cable from Board B to the host PC.

3. In the command shell or terminal window, change to the slave download directory:

   ```
   % cd <unzip_dir>/c2c_aurora/kintex-zynq/ready_for_download/slave
   ```

4. Launch the Xilinx Microprocessor Debugger:

   Windows:

   Select **Start > All Programs > Xilinx Design Tools > SDK 2014.1 > Xilinx Microprocessor Debugger 2014.1**

   Linux:

   ```
   % xmd
   ```

5. Source the Tcl file for Board B:

   ```
   XMD% source slave.tcl
   ```

6. Exit the XMD command prompt:

   ```
   XMD% exit
   ```

7. Connect the JTAG platform USB cable from Board A to the host PC.

8. In the command shell or terminal window, change to the master download directory:

   ```
   % cd <unzip_dir>/c2c_aurora/kintex-zynq/ready_for_download/master
   ```

9. Launch the Xilinx Microprocessor Debugger:

   Windows:

   Select **Start > All Programs > Xilinx Design Tools > SDK 2014.1 > Xilinx Microprocessor Debugger 2014.1**

   Linux:

   ```
   % xmd
   ```

10. Download the bitstream file to Board A:

    ```
    XMD% fpga -f design_1_wrapper.bit
    ```

11. Connect the processor:

    ```
    XMD% connect mb mdm
    ```

12. Disable entire system reset on software download:

    ```
    XMD% debugconfig -reset_on_run system disable
    ```

13. Reset the processor:

    ```
    XMD% rst -processor
    ```

14. Download the processor code file:

    ```
    XMD% dow app_vp.elf
    ```

15. Execute the reference system:

    ```
    XMD% run
    ```

16. Observe that the `axi_c2c_link_status_out` LED (AA8 on KC705, Y21 on ZC706) is glowing on both boards. See Table 4, page 8 for LED assignment.

17. Select one of the patterns from the menu displayed on the HyperTerminal console.

Hardware and Software Execution Results

Both platform versions of the reference design produce the same results. Only 720p resolution is supported in this example. When the design is executed, the HyperTerminal console display should match that shown in Figure 16.

```
--- Entering main() ---
HDMI Config done
4
Resolution: 1280x720
Initializing Video Pipe
VDMA initialization done
Starting TPG
--------------------------------------------------
--                            Pattern Menu            --
--------------------------------------------------

 Selection option
 0 = Horizontal RAMP
 1 = Vertical RAMP
 2 = Flat RED
 3 = Flat GREEN
 4 = Flat BLUE
 5 = Color Bars
 6 = Zone Plates
 7 = Tartan Bars
 8 = Cross Hatch
 9 = DDR Bandwidth

 q = exit
 ?  = help
--------------------------------------------------
>
```

Figure 16:   **HyperTerminal Output: Pattern Selection Menu**

1. Using the HyperTerminal console, select one of the options and observe the monitor display:

   ◦ 0: Displays horizontal ramp pattern

   ◦ 1: Displays vertical ramp pattern

   ◦ 2: Displays flat red frame

   ◦ 3: Displays flat green frame

   ◦ 4: Displays flat blue frame

   ◦ 5: Displays color bar pattern

   ◦ 6: Displays zone plates

   ◦ 7: Displays "tartan" bar pattern

   ◦ 8: Displays cross-hatch pattern

   ◦ 9: Displays performance-related metrics on terminal

After selecting these options, the HyperTerminal console display should resemble that shown in Figure 17.

```
>0
>1
>2
>3
>4
>5
>6
>7
>8
>9
--GlblCnt : 08F0D1D7 , Slot1 Wr Byte 0 , Rd Byte:0--
Slave DDR Throughput:-> 390389736

 ---------DDR3, AXI4 Slave Profile Summary........

Theoretical DDR Bandwidth                                    = 6400000000

Practical DDR bandwidth                                      =  390389736 bytes/sec

Resolution: 1280x720 @ 60 Hz

Percentage of DDR Bandwidth consumed by frame of resolution (1280x720) @ 60 Hz) (Approx.)= 6.09
>
```

Figure 17:   **Terminal Output: Menu Selection**

The theoretical bandwidth of the Chip2Chip configuration used in the reference design is 1.5 GB/s. The bandwidth needed for 720p video traffic is 0.332 GB/s. The percentage of available DDR bandwidth used is 6.09% (0.390/6.4). The numbers shown on the HyperTerminal console might vary from the example shown here.

Reference Design

The Reference Design Files for this application note can be downloaded from the Xilinx website.

Table 5 shows the reference design matrix.

Table 5:   **Reference Design Matrix**

Parameter	Description
General	
Target devices	Kintex-7 FPGAs and Zynq-7000 AP SoC
Source code provided	Yes
Source code format	VHDL/Verilog
Design uses code and IP from existing Xilinx application note and reference designs or third party	Yes

Table 5: **Reference Design Matrix** *(Cont'd)*

Parameter	Description
Simulation	
Functional simulation performed	N/A
Timing simulation performed	N/A
Test bench used for functional and timing simulations	N/A
Test bench format	N/A
Simulator software/version used	N/A
SPICE/IBIS simulations	N/A
Implementation	
Synthesis software tools/versions used	Vivado synthesis
Implementation software tools/versions used	Vivado Design Suite 2014.1
Static timing analysis performed	Yes (passing timing in place and route)
Hardware Verification	
Hardware verified	Yes
Hardware platform used for verification	Two KC705 evaluation boards and one ZC706 evaluation board

Design Characteristics

The reference design is implemented using Vivado Design Suite 2014.1, a Kintex-7 FPGA (XC7K325T-2FFG900) target device, and, optionally, a Zynq-7000 AP SoC (XC7Z045-2FFG900C) target device.

Utilization and Performance

The resource utilization of the KC705 slave platform reference design is shown in Table 6.

Table 6: **KC705 Slave Platform Reference Design Resource Utilization**

Mode	LUTs	Slice Regs	Memory	DSP	IO	Transceiver Channels	Clocking
Master	42,636	47,797	88	15	154	1	15
Slave	21,491	21,633	6	0	16	1	10

The resource utilization of the ZC706 slave platform reference design is shown in Table 7.

Table 7: **ZC706 Slave Platform Reference Design Resource Utilization**

Mode	LUTs	Slice Regs	Memory	DSP	IO	Transceiver Channels	Clocking
Master	42,636	47,797	88	15	154	1	15
Slave	2,739	5,417	6	0	16	1	10

Table 8 and Table 9 list the device resource utilization values for the master and slave instances of the AXI Chip2Chip core for both versions of the reference design. The information in these tables is taken from the XPS Design Summary tab which can be found by selecting **Design Overview > Module Level Utilization**. The utilization information is approximate due to cross-boundary logic optimizations and logic sharing between modules.

Table 8: **KC705 Slave Platform Reference Design Module-Level Resource Utilization**

IP Core	Mode	LUTs	Slice Regs	Memory	DSP	IO	Transceiver Channels	Clocking
AXI Chip2Chip	Master	1,165	2,201	5	0	N/A	0	0
AXI Chip2Chip	Slave	1,069	2,121	5	0	N/A	0	0

Table 9: **ZC706 Slave Platform Reference Design Module-Level Resource Utilization**

IP Core	Mode	LUTs	Slice Regs	Memory	DSP	IO	Transceiver Channels	Clocking
AXI Chip2Chip	Master	1,165	2,201	5	0	N/A	0	0
AXI Chip2Chip	Slave	1,099	2,187	5	0	N/A	0	0

Note: Slices can be packed with basic elements from multiple IP cores and hierarchies. Therefore, a slice is counted for each hierarchical module that shares packed basic elements belonging to that module. This results in some double-counting of slices when totaling the slice counts for all modules.

The KC705 slave platform board setup uses the 64-bit AXI configuration in compact 2:1 Aurora 64B/66B mode with the physical layer clocked at 125 MHz. The Aurora 64B/66B core is configured for a line rate of 6.5 Gb/s which requires a user clock of 101.56 MHz (6.5 Gb/s/64 bits). The AXI Chip2Chip core and the Aurora 64B/66B core should be configured so that the theoretical throughput (see Equation 1) is higher than the average traffic sent as input to the master AXI Chip2Chip core.

$$Throughput = \frac{0.75 \times AXIDataWidth}{MuxingRatio} \times PHYFrequency \qquad \textit{Equation 1}$$

The Chip2Chip core overhead is 12.5% protocol and 12.5% ECC. For example, given a 64-bit AXI data width configuration with compact 2:1 and Aurora PHY layer operating at 125 MHz, the theoretical throughput of the core is 375 MB/s. Thus, this configuration cannot support a frame resolution of 1920x1080, which requires a bandwidth of 0.747 GB/s for 1080p60. For a higher bandwidth requirement, the Aurora 64B/66B core must be configured for a higher line rate.

The muxing ratio dictates the setting of the AXI Chip2Chip core PHY width parameter:

- **1**: compact 1:1
- **2**: compact 2:1
- **4**: compact 4:1

Equation 1 applies to systems with a burst length of 1. The reference design implements a priority encoding scheme for multiplexing AW, AR, and W (or AR and B) AXI4 interface data. That is, for systems with a larger burst length, when a defined slot is empty, data from an available channel is multiplexed and transmitted. For example, if data is not available at the AW and AR channels, data from the W channel is transmitted. Hence, the theoretical bandwidth for systems with larger burst lengths are greater than the value in Equation 1, allowing the 0.75 factor to be ignored.

Table 10 lists the number of input and output I/Os required for the different AXI Chip2Chip core configurations. The shaded row shows the selected configuration for the reference design. If a lower data rate or pin count is required, Table 10 and Equation 1 can be used to determine the appropriate configuration.

Table 10: **FPGA I/O Utilization for AXI Chip2Chip Core Configurations**

AXI Data Width	Chip2Chip PHY Type	Muxing Ratio	Number of Input I/Os	Number of Output I/Os
32	SelectIO SDR	Compact 4:1	19	19
		Compact 2:1	31	31
	SelectIO DDR	Compact 4:1	10	10
		Compact 2:1	16	16
		Compact 1:1	29	29
64	SelectIO SDR	Compact 4:1	26	26
		Compact 2:1	45	45
	SelectIO DDR	Compact 4:1	14	14
		Compact 2:1	23	23
		Compact 1:1	42	42
	Aurora 64b/66b	Compact 2:1	1 lane	1 lane
		Compact 1:1	2 lanes	2 lanes

References

1. AMBA AXI4 specifications

2. *LogiCORE IP AXI Chip2Chip Product Guide* (PG067)

3. *LogiCORE IP Aurora 64B/66B Product Guide* (PG074)

4. *AXI VDMA Reference Design Application Note* (XAPP742)

5. *Designing a System Using the Aurora 64B66B Core (Duplex) on the KC705 Evaluation Kit Application Note* (XAPP1192)

6. *Vivado Design Suite: AXI Reference Guide* (UG1037)

7. *Zynq-7000 SoC and 7 Series Devices Memory Interface Solutions User Guide* (UG586)

8. *Vivado Design Suite User Guide: Designing IP Subsystems Using IP Integrator* (UG994)

9. *Vivado Design Suite Tutorial: Designing IP Subsystems Using IP Integrator* (UG995)

10. *KC705 Evaluation Board for the Kintex-7 FPGA User Guide* (UG810)

11. *Kintex-7 FPGA KC705 Evaluation Kit Getting Started Guide* (UG883)

12. *ZC706 Evaluation Board for the Zynq-7000 XC7Z045 All Programmable SoC User Guide* (UG954)

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
08/12/2014	1.0	Initial Xilinx release.

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