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Simulating High Performance Video Systems with Bus Functional Models

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Summary

When designing high performance systems, simulation can be used to determine system bottlenecks more efficiently than hardware analysis. Bus Functional Models (BFMs) can be configured to mimic traffic patterns that are expected out of the hardware modules.

High performance video systems can be created using Xilinx® AXI IP cores. AXI Interconnect cores, AXI3 ports on the Zynq-7000 device, and AXI VDMA IP blocks can form the core of video systems capable of handling multiple video streams and multiple video frame buffers sharing a common DDR3 SDRAM. Xilinx also provides IP cores that provide BFMs for the Zynq®-7000 All Programmable (AP) SoC device and for the AXI3, AXI4, AXI4-Stream, and AXI4-Lite protocols.

Video designs, which are sensitive to both system latency and system bandwidth, require system analysis and the use of Xilinx BFMs provides an effective way to simulate performance without the need for hardware.

The reference design described in this application note uses one 1080p video pipeline to show how video designs are simulated using BFMs. The reference design is targeted for simulation only using the Vivado® Simulator, but the project can be re-targeted for the Zynq-7000 AP SoC ZC702 evaluation board.

You can download the Reference Design Files for this application note from the Xilinx website. For detailed information about the design files, see Reference Design.

Reference Design

This section describes the high-level features of the reference design, including how to configure the main IP blocks including the Processing System core. Information about useful IP features, performance, and other configuration information are also provided. This information is applied to a video system, but the principles used to optimize the system performance are applicable to a wide range of high performance AXI systems. For information about AXI system optimization and design trade-offs, see the *Vivado Design Suite AXI Reference Guide* (UG1037) [Ref 1]. This application note assumes the user has some general knowledge of the Zynq-7000 architecture, the AXI protocol, the Vivado Design Suite and IP integrator. See the *Vivado Design Suite Tutorial: Embedded Processor Hardware Design* (UG940) [Ref 2] for more information about IP integrator.

Table 1 shows the reference design matrix.

Table 1: **Reference Design Matrix**

Parameter	Description
General	
Developer name	James Lucero
Target devices	Zynq-7000 AP SoC
Source code provided	Yes
Source code format	VHDL/Verilog
Design uses code and IP from existing Xilinx application note and reference designs or third party	No
Simulation	
Functional simulation performed	Yes
Timing simulation performed	N/A
Test bench used for functional and timing simulations	Yes
Test bench format	Verilog
Simulator software/version used	Vivado Simulator
SPICE/IBIS simulations	N/A
Implementation	
Synthesis software tools/versions used	N/A
Implementation software tools/versions used	N/A
Static timing analysis performed	N/A
Hardware Verification	
Hardware verified	N/A
Hardware platform used for verification	N/A

A video pipeline could consist of a Timing Controller IP core, Test Pattern Generator IP core, and On Screen Display IP core. Within a BFM simulation environment, as described in this application note, these IP cores can be replaced with a Verilog process to generate 1080p timing, an AXI4-Stream master BFM to write data into memory, and an AXI4-Stream slave BFM to read data from memory using the AXI Video Direct Memory Access (VDMA) core. A Zynq-7000 BFM core is used to configure the video pipeline using the `M_AXI_GP0` interface and system memory is accessed through the `S_AXI_HP0` interface. These blocks are shown in Figure 1 and comprise the reference design delivered with this application note.

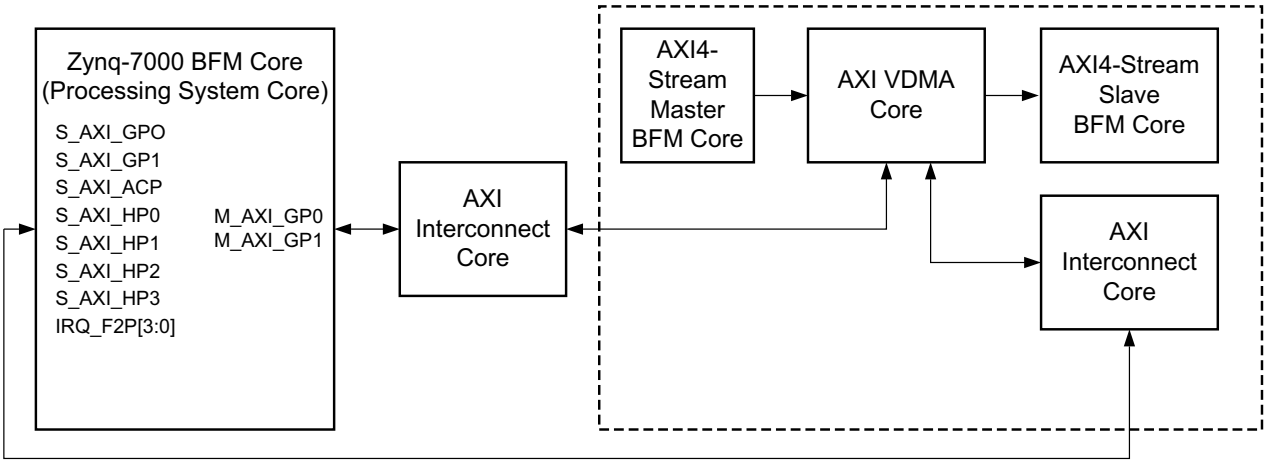

Figure 1: **Reference System Block Diagram**

In this application note, reference is made to the Processing System core which is the Zynq-7000 BFM core but can also mean the Processing System 7 core, if hardware is targeted. The Zynq-7000 BFM core is used for the simulation described in this application note. During simulation this core replaces the Processing System 7 core, but takes its settings from the Processing System 7 core. The Processing System core supplies clocks and resets throughout the system including the general interconnect.

To mimic video traffic behavior in the design, APIs are used to control the BFMs. To see a full frame in simulation time, the number of vertical lines is reduced.

The performance of the video pipeline is reported out with a test bench function and the waveforms are analyzed to ensure video traffic requirements are met.

The AXI interface protocol standard is defined in the ARM® AMBA4 and ARM AMBA3 AXI specifications (see the *Vivado Design Suite AXI Reference Guide* (UG1037) [Ref 1] for more information). The AXI interfaces used in this design are the AXI4, AXI3, AXI4-Lite, and AXI4-Stream interfaces. These interfaces provide a common IP interface protocol for building the design.

Both the AXI Interconnect core and the AXI HP ports on the Processing System core implement a high bandwidth Multi-Port Memory Controller (MPMC); this is used in applications where multiple devices share a common memory controller. This is a requirement in many video, embedded, and communications applications where data from multiple sources move through a common memory device, typically DDR3 SDRAM.

The AXI VDMA core implements a high performance video optimized DMA engine with frame buffering, Scatter Gather (SG), and 2-Dimensional DMA features. The AXI VDMA core transfers video data streams to and from memory and operates under dynamic software control or static configuration modes.

The design is built using the Vivado Design Suite, System Edition 2015.1, Vivado Simulator feature, and the Vivado IP integrator feature. IP integrator simplifies the task of instantiating, configuring, and connecting IP cores together to form complex integrated systems. The complete IP integrator project and simulation environment are provided with this application note to allow the designer to examine and rebuild this design or use the files as a template for

starting a new design. Included with this application note is one reference system, `zc702_zynq_axi_bfm_sim`, available in the ZIP file.

Processing System Core

In the block diagram in Figure 1, adding the Processing System core allows for either generation of the hardware wrapper (using the Processing System 7 core) or simulation (using the Zynq-7000 BFM core) of the Zynq-7000 device. After generating the design in the Vivado Design Suite, the Zynq-7000 BFM core wrapper is generated in the `sim` directory of the core, based on the hardware configuration of the Processing System 7 core. Only the simulation features of the Zynq-7000 BFM core are covered in this application note.

The Processing System core is configured for the ZC702 board with UART 1 and the DDR3 Controller for the I/Os. The `M_AXI_GP0` interface and `S_AXI_HP0` interface (64-bits) are enabled for the AXI interfaces.

One general interconnect clock is generated with a frequency of 50 MHz. The 50 MHz clock is connected to the Clocking Wizard core to generate the 148.5 MHz used for the video pipeline. The 50 MHz clock is used for the AXI4-Lite slave interfaces (AXI VDMA AXI4-Lite slave interface, `M_AXI_GP0` interface) and the 148.5 MHz clock is used for the video pipeline (AXI VDMA AXI4 MM/AXI4-Stream interfaces, `S_AXI_GP0` interface).

Zynq-7000 BFM Memory Controller

A sparse memory model for OCM/DDR is included with the Zynq-7000 BFM core. An API call allows for AXI slaves on the Processing System core accessing the memory to have best case, average case, or worst latency to have a general idea of latency in hardware. This application note covers the best case latency. No APIs are needed when accessing the `S_AXI_HP0` interface because the BFM automatically responds.

Video Configuration

The reference design implements one video pipeline running at a modified configuration for 1080p60 (1920x1080 pictures at 60 frames/s). Each picture consists of 4 bytes per pixel (3-bytes for RGB, and 1-byte for padding to show extra throughput) to represent an upper bound for high quality video streams such as RBGA or YUVA 4:4:4 with alpha channel information.

The AXI BFM cores are used to mimic video traffic by writing into (AXI4-Stream master BFM) and reading from (AXI4-Stream slave BFM) memory using the AXI VDMA core. The AXI BFM cores are configured in the simulation environment to send or receive one horizontal line of the frame. The AXI BFM cores are configured for a 32-bit interface and a maximum packet size of 1920.

This design is targeting a 1080p60 video pipeline which takes $1/60^{th}$ of a second to see the next `fsync` pulse. To reduce this time for simulation purposes, the number of horizontal lines is reduced from 1080 to 24 and the number of horizontal blanking lines is reduced from 45 to 1.

The following computations are used for the expected performance of the video pipeline in simulation:

Horizontal Line: 280 clocks blanking period (no active video) + 1920 clocks (active video)

Vertical Lines: 24 horizontal lines + 1 line blanking (no active video for 2200 clocks)

Clocks of Active Video per Frame: 1920x24 = 46,080 clocks

Total Clocks per Frame: 25 lines x (1920+280) = 55,000 clocks

148,500,000 Clocks per second/Total Clocks per Frame = 2,700 frames/s

Bandwidth per Channel = 1920x4 bytes per pixel (horizontal line) * 24 (active vertical lines) * 2,700 Frames per second = 497.664 MB/s

The bandwidth in this design is analyzed with a Verilog function on the `S_AXI_HP0` interface which computes the throughput continuously based on one frame (55,000 total clocks).

AXI Interconnect (processing_system7_0_axi_periph Instance)

This AXI Interconnect `processing_system7_0_axi_periph` instance does not use a strategy because of the 1 master/1 slave configuration. APIs use the `M_AXI_GP0` interface to write and read to all AXI4-Lite slave registers in the design (control and status registers). In addition, this portion of the design is clocked at 50 MHz which is a slower clock relative to the rest of the system.

AXI Interconnect (axi_mem_intercon Instance)

The AXI Interconnect `axi_mem_intercon` instance is configured for the Maximize Performance strategy. This allows for the AXI VDMA AXI4 MM2S/AXI4 S2MM master interfaces to issue up to four outstanding transactions and for the `S_AXI_HP0` slave interface to have an acceptance of eight transactions. These issue/accept settings are required to handle the bandwidth requirements of the video pipeline.

AXI VDMA Instance

The AXI VDMA core is designed to provide video read and write transfer capabilities to and from the AXI4 memory-mapped domain to AXI4-Stream interface. The AXI VDMA core provides high-speed data movement between system memory and the AXI BFM cores. AXI4 memory-mapped interfaces are used for high-speed data movement and buffer description fetches across the AXI interface. With this design, register direct mode is used for the buffer descriptors which eliminates the need for the SG interface in the system.

The design incorporates video-specific functionality such as Frame Sync (FSYNC) for fully synchronized frame DMA operations as well as two-dimensional DMA transfers. FSYNC is enabled for both write and read channels where the signal is generated in the test bench.

The AXI VDMA core instance is set for a maximum burst of 32 for both write and read channels. The AXI3 protocol only supports a maximum burst of 16. However, because the Zynq-7000 HP

interface 0 is 64-bits, this interface supports a transfer size of 64 bits x 16 data beats (32 bits x 32 data beats). The Line Buffer depths for both channels are configured for 1024 which is about half a horizontal line.

Block Design Connections for Simulation

An input port `fsync` is added that is driven by the `bfm_test.v` module to generate the frame sync for the video pipeline.

The output ports `reg_clk` and `reg_rst_n` are used by the `bfm_test.v` module to control the slave register Verilog process.

The output ports `vid_clk`, and `vid_rst_n` are used by the `bfm_test.v` module to control the video pipeline Verilog processes.

Simulation Environment

The following is an overview of the simulation environment.

Test bench (`system_tb.v`)

- Generates system clocks/resets
- Instantiates the IP integrator top level wrapper and connects the `bfm_test` module

Defines (`axi_bfm_defines.v`, `zynq_bfm_defines.v`, `axi_bfm_s_defines.v`)

- Contains protocol constants and tasks for the APIs

BFM API calls (`bfm_test.v`)

- See Overview of bfm_test.v

Overview of bfm_test.v

This file contains the API commands to control the Zynq-7000 BFM core (setup and `M_AXI_GP0` APIs), AXI BFM cores, `fsync` signal and performance measuring for the video pipeline. See the *Zynq-7000 All Programmable SoC Bus Functional Model v2.0* (DS897) [Ref 3]and the *AXI BFM Cores v5.0* (PG129) [Ref 4] to get a full listing of all APIs and descriptions.

The following initial configuration is used to configure the Zynq-7000 BFM core. The `set_slave_profile` API is used for `S_AXI_HP0` to enable best case latency. The `pre_load_mem` API is used to generate random data to the three frame buffers used in the design. After the main test bench reset is deasserted (active-Low reset), the `fpga_soft_reset` API is called to deassert the Programmable Logic (PL) reset.

When the system is out of reset, the Zynq-7000 BFM `write_data` API allows writes from the `M_AXI_GP0` interface to the control registers of the AXI VDMA core to enable 1920 horizontal lines and 24 vertical lines.

After configuration of the AXI VDMA core, the FSYNC process is started. The FSYNC process issues the assertion of the `fsync` signal 2700 times per second.

The AXI4-Stream process waits for the assertion of `fsync`, waits for 280 clocks for the horizontal line blanking period, sends and receives data within a parallel Verilog process, and stops sending out horizontal lines when the vertical line number of the frame is met (24 in this case). The `send_packet` API is used for the AXI4-Stream master BFM to write data to the AXI VDMA core. The `receive_transfer` API is used for the AXI4-Stream slave BFM to read data from the AXI VDMA core where the `last` output of the API is used to determine when the line is complete.

The performance function is executed after the assertion of the first `fsync` and monitors one frame continuously on the `S_AXI_HP0` interface. The function counts the number of clocks with valid data (`wvalid`/`wready` and `rvalid`/`rready`) divided by the number of total clocks. The computation of MB/s is determined and the result is displayed in the transcript of the simulator.

A result is given for the read and the write interface on `S_AXI_HP0` which should match the result in the Video Related IP section (497.664 MB/s). If this number is not achieved, the system needs to be analyzed for system bottlenecks or other functional issues.

Requirements

Hardware

Not required but can be re-targeted for use with the Zynq-7000 AP SoC ZC702 evaluation board.

IP

The reference system requires the following LogiCORE™ IP cores:

- Zynq-7000 BFM
- AXI Interconnect
- AXI Video Direct Memory Access
- AXI4 BFM Cores
- Clocking Wizard
- Processor System Reset

See Figure 1 for the block diagram and Table 2 for the address map of the system.

Software

The installed software tool requirements for building and simulating this reference system are:

- Vivado Design Suite, System Edition 2015.1
- AXI and Zynq Bus Functional Model LogiCORE IP License

The address map for the reference system is shown in Table 2.

Table 2: **Reference System Address Map**

Peripheral	Instance	Base Address	High Address
processing_system7	processing_system7_1 (M_AXI_GP0)	0x40000000	0x7FFFFFFF
processing_system7	processing_system7_1 (S_AXI_HP0)	0x00000000	0x3FFFFFFF
axi_vdma	axi_vdma_0	0x40000000	0x4000FFFF

Reference Design Files

You can download the Reference Design Files for this application note from the Xilinx website.

Included with this application note is one reference system, `zc702_zynq_axi_bfm_sim`, available in the ZIP file.

The following is the directory structure of the reference design. The `sim` directory files are described in Simulation Environment.

```
xapp1250/
    zc702_zynq_axi_bfm_sim/
        HW/
            sim/
```

Licensing

Click the following link for details for obtaining the AXI and Zynq-7000 BFM LogiCORE IP cores:

http://www.xilinx.com/products/intellectual-property/zynq_bfm/zynq_bfm-order.html

Reference Design Steps

This section includes details about running the reference design from setup to results.

Running the Reference Design

1. Open `zc702_zynq_axi_bfm_sim/HW/project_1.xpr` in the Vivado Design Suite.
2. In the Sources tab, expand `design_1_wrapper`. Right-click `design_1_i` and select **Generate Output Products...** Select **Generate**.

3. In Flow Navigator, expand Simulation. Select **Run Simulation** and then select **Run Behavioral Simulation**. This starts the Vivado Simulator. This step can take up to 10 minutes depending on the machine.
4. When the Vivado Simulator is invoked, run the simulation for 400 µs to get one frame of transactions. The provided waveform contains all AXI VDMA top level signals (AXI4LITE, AXI4 MM2S, AXI4 S2MM, AXI4S MM2S, AXI4S S2MM interfaces). This step can take up to 30 minutes depending on the machine. When the simulation is finished, the following should be seen in the Tcl console:

```
387704000 HP0 Rd: 497.664000 MB/s
387704000 HP0 Wr: 497.664000 MB/s
```

Results

1. Double-click the system_tb_behav.wcfg tab which makes the waveform window expand. The waveform is organized into five groups (AXI4_LITE, AXI4_MM2S, AXI4_S2MM, AXI4S_MM2S, AXI4S_S2MM).
2. Expand the AXI4_LITE group and zoom in between 10.8 µs and 17.5 µs. During this time period, the Zynq-7000 BFM `M_AXI_GP0` is writing to the slave registers on the AXI VDMA core to configure the core for the video pipeline. After writing the vertical size into an AXI VDMA register, the VDMA is activated and the `fsync` signal is generated by the test bench. This is shown in Figure 2.

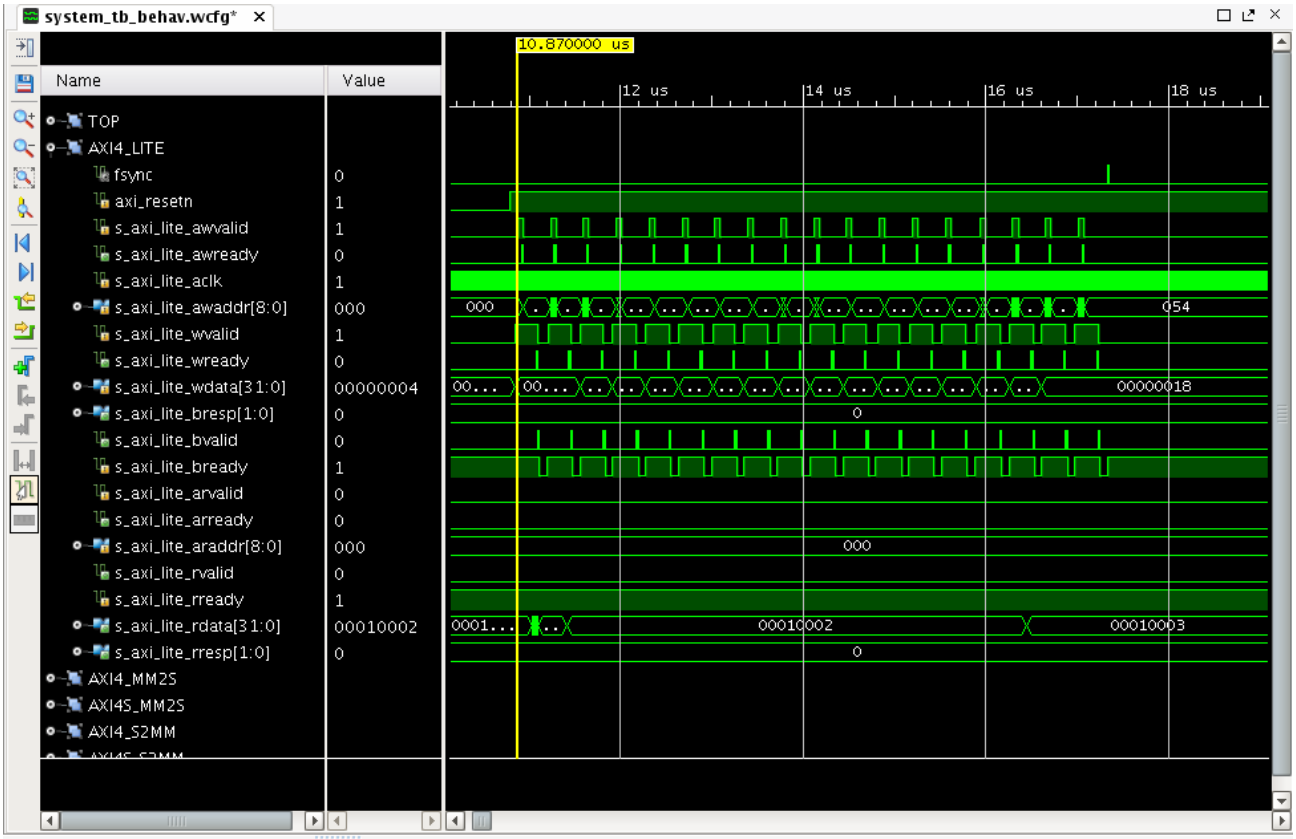

Figure 2: **AXI4_LITE–fsync Generated by Test Bench**

3. Expand the AXI4_MM2S group and zoom in between 17.3 µs and 18.2 µs, This shows the first read transitions after `fsync`. Four read transactions (address phase) are accepted by the AXI Interconnect core while the fifth transaction is throttled until `rvalid` is asserted for the data phase. `rlast` is asserted after 32 data beats are received by the core (the maximum burst of the AXI VDMA core is set to 32 data beats). This is shown in Figure 3.

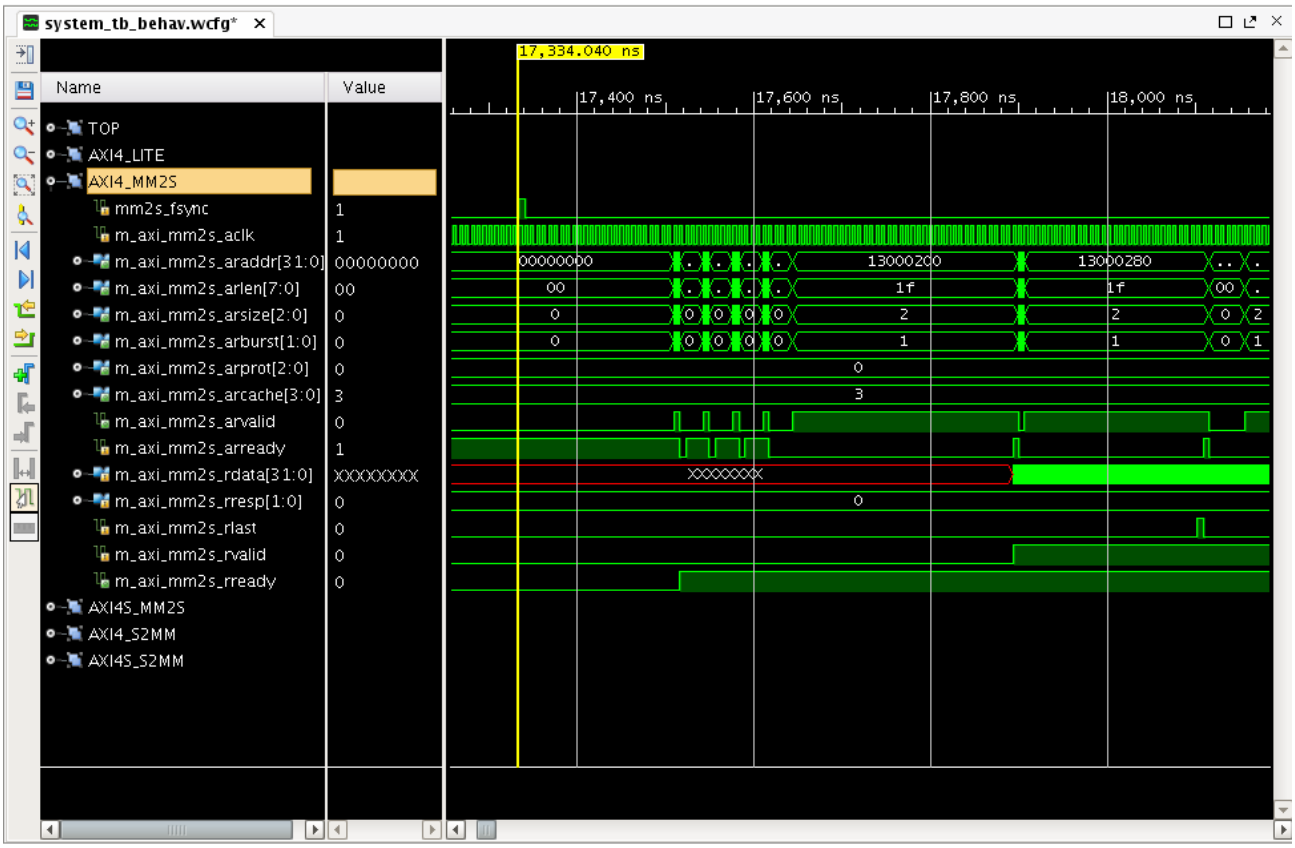

Figure 3: **AXI4_MM2S–First Reads after fsync**

4. Expand the AXI4_S2MM group and zoom in between 19.5 µs and 19.8 µs. This shows the first write transaction. Only one write transaction (address phase) occurs on the write side because the AXI VDMA core is concurrently getting write data from the AXI4-Stream master BFM. `wlast` is asserted after the 32 data beats are written to the Zynq-7000 BFM `S_AXI_HP0` interface (the maximum burst of the AXI VDMA core is set to 32 data beats). This is shown in Figure 4.

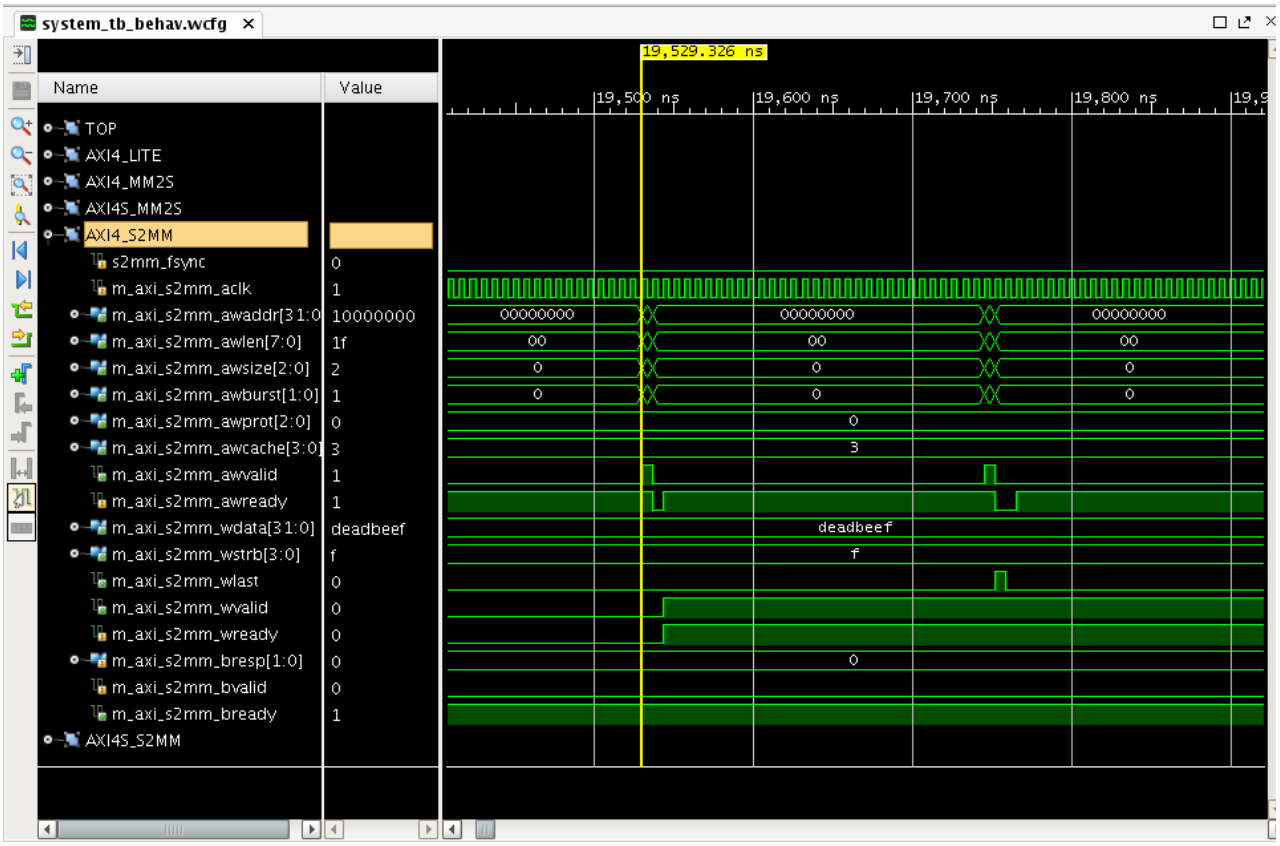

Figure 4: **AXI4_S2MM–First Write**

5. Expand the AXI4S_MM2S group and zoom in between 17.3 µs and 34.0 µs. In this time range, `fsync` is asserted and `tready` (asserted by the AXI4-Stream slave BFM) is asserted 280 clocks after `fsync`. `tvalid` (generated by the AXI VDMA core) and `tready` (generated by the AXI4-Stream slave BFM) is asserted for 1920 clocks and `tlast` is asserted on the 1920th clock to signify that the horizontal line is complete. This behavior continues for the next line (280 clocks blanking period and then 1920 clocks of `tready` for one line). This is shown n Figure 5.

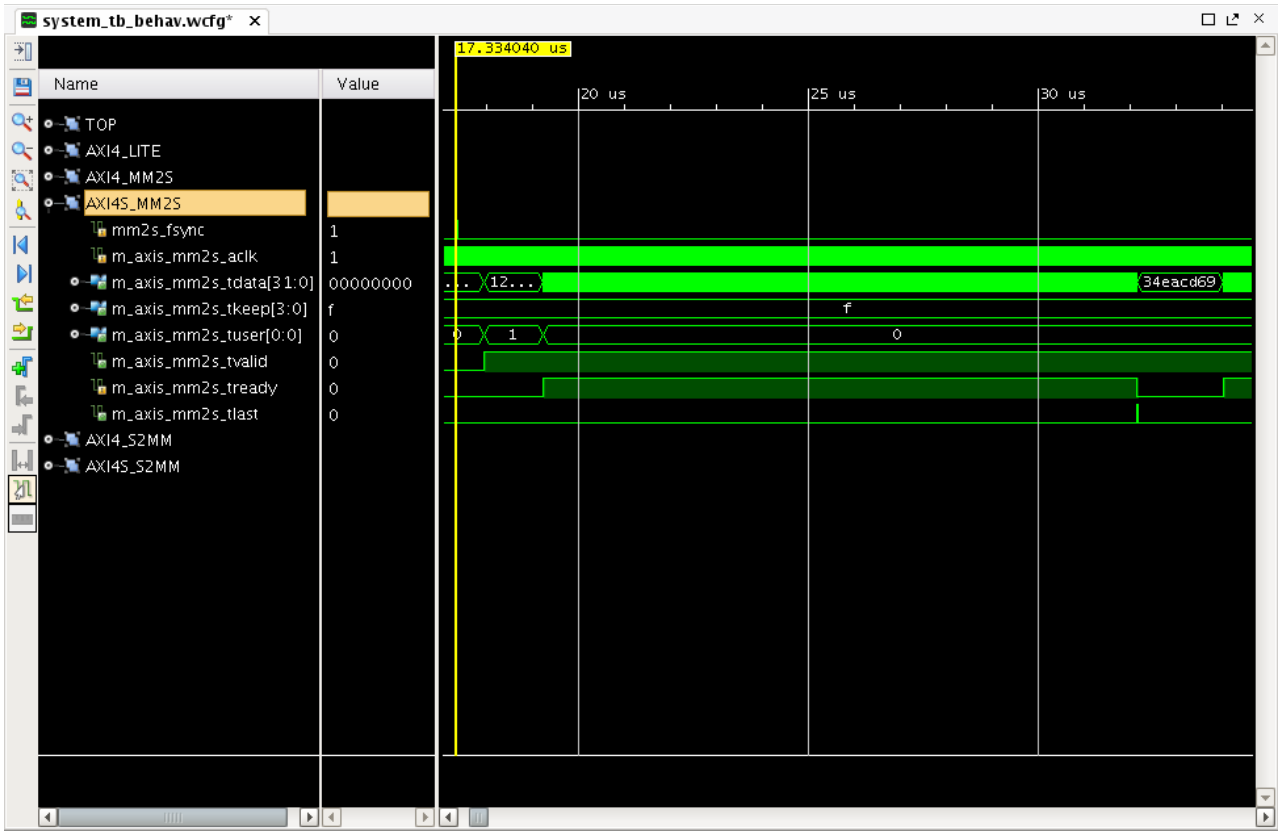

Figure 5: **AXI4S_MM2S–Horizontal Line Complete**

If `tready` is asserted (1) and `tvalid` is deasserted (0), this is a condition for the video pipeline to be throttled. In video applications this can cause flickering on the screen or other similar behavior.

6. Expand the AXI4S_S2MM group and zoom in between 17.3 µs and 34.0 µs. In this time range, `fsync` is asserted and `tvalid` (asserted by the AXI4-Stream master BFM) is asserted 280 clocks after `fsync`. `tvalid` is asserted for 1920 clocks and `tlast` is asserted on the 1920th clock to signify that the horizontal line is complete. `tready` (generated by the AXI VDMA core) is asserted before `fsync` indicating that the core is ready for write data from the AXI4-Stream interface. This behavior continues for the next line (280 clocks blanking period and then 1920 clocks of `tvalid` for one line). This is shown n Figure 6.

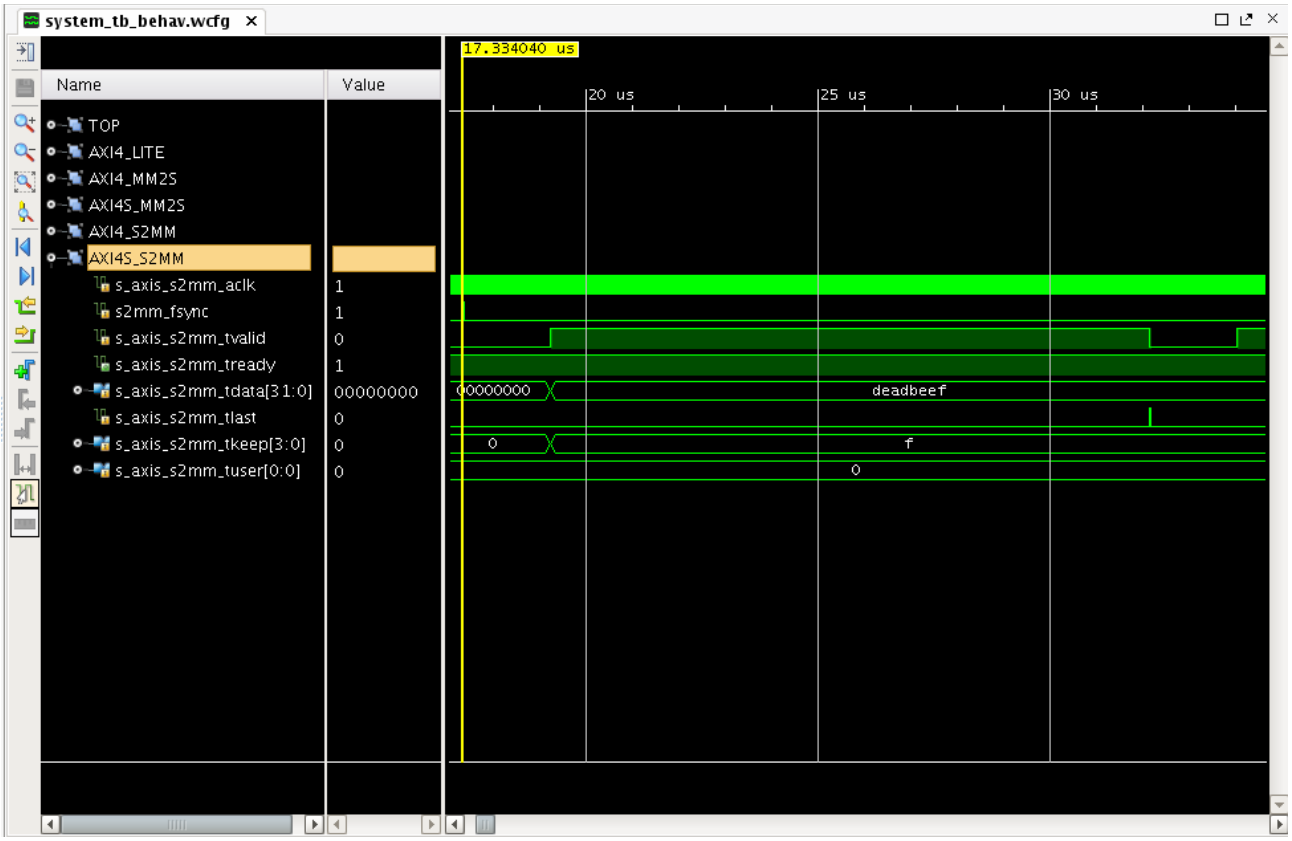

Figure 6: **AXI4S_S2MM–Horizontal Line Complete**

If `tvalid` is asserted (1) and `tready` is deasserted (0), this is a condition for the video pipeline to be throttled. In video applications this can cause flickering on the screen or other similar behavior.

References

1. *Vivado Design Suite AXI Reference Guide* (UG1037)
2. *Vivado Design Suite Tutorial: Embedded Processor Hardware Design* (UG940)
3. *Zynq-7000 All Programmable SoC Bus Functional Model v2.0* (DS897)
4. *AXI BFM Cores v5.0* (PG129)
5. *Zynq-7000 All Programmable SoC Technical Reference Manual* (UG585)
6. *LogicCORE IP AXI Interconnect Product Guide* (PG059)
7. *LogiCORE IP AXI Video Direct Memory Access Product Guide* (PG020)
8. *LogiCORE IP Processing System 7 Product Guide* (PG082)

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
05/15/2015	1.0	Initial Xilinx release.

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