XAPP555 (v1.1) December 12, 2012

Lowering Power using the Voltage Identification Bit

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Summary

Voltage identification is a form of adaptive voltage scaling (AVS). The voltage-identification technique described in this application note enables certain devices in the Virtex®-7 family to be operated at a lower voltage of 0.9V while delivering the same specified performance as that of a device operating at the nominal supply voltage of 1.0V. Voltage identification capable devices consume approximately 30% lower worst case (maximum) static power and correspondingly dissipate less heat.

Reduced power consumption is a desirable characteristic and one that Xilinx 7 series FPGAs fulfill in multiple ways. The primary purpose of the voltage-identification technique is to reduce the worst-case power consumption of -1C devices. However, the significance of the voltage-identification technique goes beyond an individual device dissipating less energy, it also can lower the overall system cost.

Power supplies and thermal management requirements are normally specified based on the worst-case power demands of all the system's components. Although the 7 series FPGAs -1C devices are the most cost-effective, the total cost of a product is the sum of all parts, and costs associated with the power supply and thermal management can be significant. The voltage-identification technique specifically reduces worst-case power consumption, which reduces the overall costs associated with specifying a larger power supply, requiring a heat sink, adding forced air cooling, or including similar devices.

This application note shows the technical aspects of implementing the voltage-identification technique and introduces a reference design for the VC707 evaluation kit. It also explains how voltage identification fits into the complete power portfolio of Virtex-7 FPGAs and highlights the benefits of using the voltage-identification technique to reduce power consumption and system costs.

Introduction

The power consumption of 7 series FPGAs is significantly lower than that of previous generations of Xilinx FPGAs and equivalent devices offered by other vendors. What really matters is how much power the user's particular product consumes and how much the final product costs. The voltage-identification scheme in this application note will further lower worst-case static power consumption by ~30% and in turn, lower the final cost of the end product.

Devices with VID Bits

Table 1 lists the seven Virtex-7 devices with voltage identification (VID) bits. The scheme in this application note only applies to the commercial temperature range -1C speed specification devices. When the voltage-identification technique is applied, the performance available is consistent with the -1 speed specification. This application note also explains the reasoning for the speed grade restriction. All of the -1C devices listed in Table 1 come with the VID bit feature built into the device. These are not special parts with special ordering codes, but simply standard devices. All of these devices will see lower worst-case static power when taking advantage of the VID bit feature.

Table 1: **Virtex-7 Devices with VID Bits**

XC7V585T-1C	XC7VX330T-1C	XC7VX550T-1C
	XC7VX415T-1C	XC7VX690T-1C
	XC7VX485T-1C	XC7VX980T-1C

Reading the Bit

The VID bit is a single bit of nonvolatile information programmed into each device during production testing. While it can only have two values (`0` or `1`), its value is specific to each individual device and part of the device's identity. This bit of information contributes to the Device DNA value that is programmed during production testing.

The VID bit is bit 1 of the 57-bit Device DNA value, which is defined as having bits 0 to 56 and accessed via the DNA_PORT primitive. The DNA_PORT is arranged as a serial shift register into which the DNA value is first loaded by driving the READ control High as one rising edge is applied to the CLK input. After loading the shift register, the MSB (bit 56) is present at the DOUT port for reading. When the READ control is Low, the shift register is advanced by driving the SHIFT control High and applying a rising edge to the CLK input. After 55 shift cycles, the DOUT output presents the VID bit (bit 1) for reading and based upon its value, the voltage-identification technique can be used.

The user must ensure that the correct *bit 1* is extracted from the DNA value. A fundamental flaw in the design performing this task or a totally unexpected event that interferes with the normally reliable operation of the circuitry can lead to interpreting the incorrect bit as being that of the VID bit information. Designing for reliable operation from the outset ensures that the read process is logically correct.

The challenge is that every device contains a unique 57-bit value and there is no direct way of knowing when the correct DNA value is read. However, this can be done indirectly by injecting a known data pattern into the DNA shift register through the DIN input of the DNA_PORT primitive (while it is shifting), and then shifting beyond the 57th bit to confirm the same pattern emerges when expected. The DNA value, especially bit 1, must be stored somewhere when it is read and only used after the known pattern is used to verify the DNA read operation.

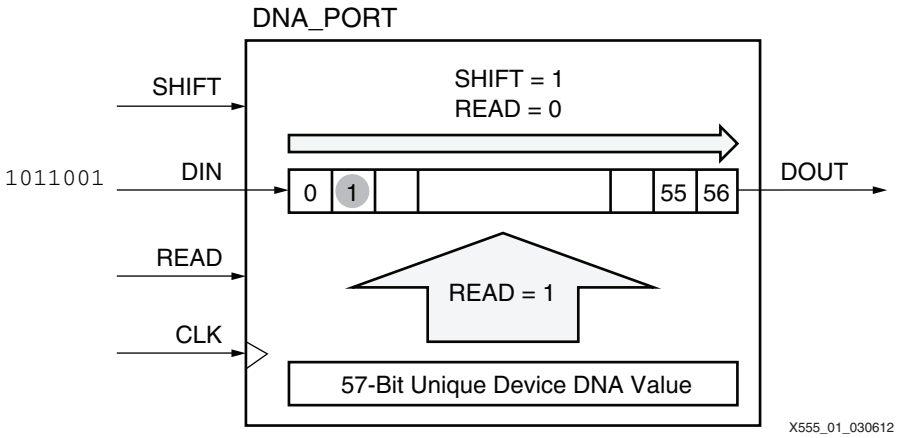

Figure 1: **Extracting the Voltage Identification Bit from Device DNA**

Figure 1 shows the VID bit extraction. To extract the VID bit from Device DNA:

1. Load the SHIFT register with DNA value.
2. Shift while injecting a known 7-bit pattern (e.g., `1011001`) and capturing the bits presented at the output.
3. After reading 64 bits, verify that the last 7 bits match the known (injected) pattern.
4. If the read process is verified good, use the captured DNA value. Bit 1 of the Device DNA is the VID bit.

Lowering V_{CCINT} and V_{CCBRAM} to 0.9V

When the VID bit has the value of `0`, the device must be operated with the V_{CCINT} and V_{CCBRAM} supplies at 1.0V nominal. A VID bit with the value of `1` indicates that the V_{CCINT} and V_{CCBRAM} supplies can be reduced to 0.9V nominal. The device still operates at 1.0V, but lowering the V_{CCINT} and V_{CCBRAM} supplies to 0.9V, when possible, results in lower static and dynamic power consumption. Most importantly, the device continues to meet all performance specifications expected of the commercial temperature range -1C speed specification.

To support this voltage-identification scheme, there must be a way for the V_{CCINT} and V_{CCBRAM} supplies to provide either 0.9V or 1.0V. Both voltages must be supportable since not all -1C devices are able to support 0.9V operation. Some board designs contain power supplies that allow the voltage level to be set. This feature is sometimes used in production to set each supply rail to the level required for normal operation. However, when only fixed output power supplies are used, a different solution for the V_{CCINT} and V_{CCBRAM} supplies should be considered.

In most cases, V_{CCINT} and V_{CCBRAM} would be connected to a common supply requiring only that supply be set to either 0.9V or 1.0V. Whether there is one common supply or separate supplies for V_{CCINT} and V_{CCBRAM}, there are two fundamental schemes to consider to service this voltage-identification technique:

- Production test method
- Adaptive voltage scaling

Production Test Method

The VID bit in each device is set during production testing of the device at the Xilinx factory and can never change. A device with the VID bit set to `1` can operate at 0.9V at all times, meaning that the V_{CCINT} and V_{CCBRAM} supplies to that specific device could be set permanently to 0.9V rather than 1.0V. In this method, the value of the VID bit is determined and the V_{CCINT} and V_{CCBRAM} supplies are set as part of the end-customer production testing of each product. Initially, the Virtex-7 device needs to be supplied with 1.0V supplies to read the Device DNA value. In this situation, there is the ability to read the Device DNA via JTAG using the XSC_DNA command or a test design can also be loaded into the device. Depending on the VID bit value, the V_{CCINT} and V_{CCBRAM} supplies can be programmed appropriately to 0.9V or 1.0V, or a suitable select on test (SOT) component or link can be inserted.

Adaptive Voltage Scaling

Adaptive voltage scaling (AVS) is a technique used within the industry to adjust the voltage supplied to devices. Each particular device delivers the performance required at each point in time, typically with a goal to keep power consumption (heat) within limits. AVS voltage adjustments tend to be made continuously, often using a closed-loop control algorithm. Using the VID bit is a form of AVS, requiring a single reduction of the V_{CCINT} and V_{CCBRAM} supplies from a default startup value of 1.0V down to 0.9V. This method can be easier to implement and can even be an open loop process. The key is to have a controllable power supply, but with AVS in general use, this does not present a significant challenge. The reference design described in this application note illustrates how the power supplies on the 7 series FPGA evaluation kits, that feature Texas Instruments UCD9248 controllers, can be controlled through the power-management bus (PMBus) using an area-efficient PicoBlaze™ controller. An alternative power supply arrangement uses the direct output of the VID bit from the Virtex-7 FPGA to switch the V_{CCINT} and V_{CCBRAM} supplies down to 0.9V (e.g., the VID bit is used to adjust the voltage feedback to the sense input of an otherwise fixed output supply).

Advantages of Voltage Identification

As this voltage-identification technique is a simple form of AVS, in the same way that AVS is applied to application-specific integrated circuit (ASIC) devices, it ultimately reduces power consumption. However, there are fundamental differences between ASIC and FPGA technology and the reasons to use AVS in conjunction with an FPGA are completely different.

The benefits of using the voltage-identification technique are further understood when applied to the commercial temperature range -1C speed specification Virtex-7 FPGAs. The voltage-identification technique is just one of several power-saving options available. This technique focuses on the power features of the pure silicon. There are various power-saving options available within the design tools that can further enhance the power properties of the end system.

When silicon devices are manufactured, there are manufacturing process variables (P). These variables lead to variations in the performance and power consumption of devices. The performance and power consumption of any device is also subject to the operating voltage (V) and temperature (T). These effects are generally known as variation over PVT. To fully understand how the voltage-identification technique applies, each parameter is considered separately.

The dominant influence on the voltage-identification scheme is P. Virtex-7 devices employ a 28 nm high-performance and low-power (HPL) process, which delivers an attractive level of both performance and power consumption, but for purposes of voltage-identification, the focus is on variability within that process. Although the precise distribution curves can look rather different, a normal distribution curve (shown in Figure 2) is provided as a useful reference example when focusing on the VID bit for -1C devices.

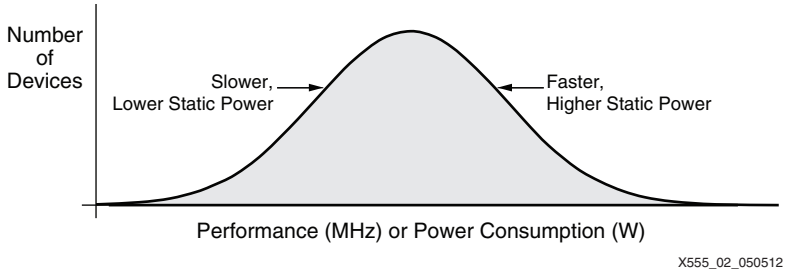

Figure 2: **Representation of Variation Across Many Devices Due to Manufacturing Process**

The curve in Figure 2 is a general representation of the performance variance between of a large number of devices from different wafers. A majority of devices fall into the middle of the range. Generally, the higher device performance, the higher its static power consumption.The range of -1C devices can fall anywhere on this curve. While the slower devices need to run at 1.0V the faster devices can achieve the same performance while running at 0.9V.

During production testing, Xilinx determines which -1C devices are fast enough to meet -1 performance specifications while running at 0.9V. Then, if the devices meet all the -1 specifications when operated at 0.9V, Xilinx programs the nonvolatile VID bit in the Device DNA with a `1`. Running the device at a lower voltage essentially shifts the curve to the left as the part slows down with a lower voltage.

In addition to moving the upper range of distribution downward, the voltage-identification technique has a minimum impact on cost. The VID bit is a standard feature in all -1C devices listed in Table 1. Using VID avoids the requirement for another ordering code and the costs associated with inventory and ordering. The simple form of AVS that the voltage-identification technique employs (that V_{CCINT} and V_{CCBRAM} have to be reduced once from 1.0V to 0.9V) also minimizes the design effort and costs in the final product. It can also be less expensive compared to ordering a device with the lower power screening already built in, like an industrial temperature range device, or a -2L device. See WP389, *Lowering Power at 28 nm with Xilinx 7 Series FPGAs* for more details on devices that are process screened for lower static power.

With direct costs associated with the VID bit for specific -1C devices kept to a minimum, an overall cost saving can be achieved in the final product. A power supply must be designed and implemented based on the worst-case current consumption of the components. The

voltage-identification technique reduces the worst-case power consumption figure on all devices, reducing the worst-case current that the supply must provide. Specifying this lower power supply could represent significant cost savings.

As thermal management of a product must be designed and implemented based on the worst-case power consumption of all components in the system, the reduction in worst-case power consumption figures when using the voltage-identification technique could be enough to avoid the need for a heat sink or a cooling fan, items that add a significant cost to every product.

For lower power consumption and ease of design, the -2L device is an alternative compared to using a -1C device and the voltage-identification technique. However, the VID bit comes built into all -1C devices at no extra charge. Therefore, for designs using Virtex-7 devices, the voltage-identification technique is a low-cost option for lower worst-case static power.

Cost Reduction

The voltage-identification technique is useful for engineers designing products with both power and cost budgets. Although the -1C devices are already lower cost, the voltage-identification technique also can reduce the overall cost of a product. The benefits of the voltage-identification technique must be considered in the context of cost-effective design.

The Virtex-7 data sheet (DS183), in conjunction with the Xilinx Power Estimator (XPE) or Xilinx Power Analyzer (XPA) tools, should be consulted to confirm precise values, but the voltage-identification technique reduces worst-case power consumption associated with the V_{CCINT} and V_{CCBRAM} supplies by ~30% on all devices. Reducing the V_{CCINT} and V_{CCBRAM} supplies from 1.0V to 0.9V corresponds to a worst-case reduction in V_{CCINT} and V_{CCBRAM} supply current of 22.5%. The reduced voltage further reduces the dynamic power consumption.

The primary benefit of implementing the voltage-identification technique is that it reduces the worst-case static current that the V_{CCINT} and V_{CCBRAM} supplies are required to deliver to the FPGA. Power supplies are designed and implemented based on the worst-case current consumption. The power reduction enabled by the voltage-identification technique allows a lower cost, lower capacity supply to be specified. Since that same supply can be used for all devices, the cost saving applies to *all* products and not just those with VID bit = `1`.

The secondary benefit of the voltage-identification technique is the reduction in worst-case power consumption of the device, and therefore, less heat dissipated. As with power-supply design, the thermal management of a product must be designed to meet the worst-case specifications. Cost savings include not adding a heat sink for every device or avoiding the requirement to upgrade from the lowest cost commercial temperature range (C) device to extended temperature range (E) or industrial temperature range (I) devices. The voltage-identification technique should interest designers of commercial products that must operate in a totally enclosed environment where there is a continuous balancing between power (heat) and cost.

Although not a direct benefit of voltage-identification, if a PicoBlaze controller is used to implement the voltage-identification process, the controller can perform other useful functions during the operation of the product. This is illustrated in the reference design that accompanies this application note, where a PicoBlaze controller implements the PMBus protocol to control the voltage of the V_{CCINT} and V_{CCBRAM} supplies and then subsequently monitors all the supplies on the board.

It would also be possible to connect the PicoBlaze controller to the on-chip XADC primitive. Measurement of die temperature could be used to control a cooling fan or *throttle* the design. The V_{CCINT} and V_{CCBRAM} supply voltages could also be internally monitored and used in the control of external power supplies in a non-PMBus arrangement.

Considerations and Precautions

The voltage-identification technique is straightforward to apply. However, potential issues can arise and measures should be taken to prevent them. Designs should include the following considerations:

- The voltage-identification technique only applies to -1C devices from the Virtex-7 family listed in Table 1.
- The V_{CCINT} and V_{CCBRAM} supplies can only be reduced to 0.9V when the VID bit is set. If there are multiple Virtex-7 devices in a system each must be supplied with an appropriate V_{CCINT} and V_{CCBRAM} supply corresponding with its VID bit. In practice, this requires an independent and controllable supply for each device.
- When the VID bit is `0`, the device must be operated with 1.0V V_{CCINT} and V_{CCBRAM} supplies. If a device with a VID bit = `0` is supplied with 0.9V, it can fail to provide the performance required by the design. The most likely cause of this happening is a fundamental failure to read the Device DNA value correctly. This can be prevented by following the recommendations described in Reading the Bit, page 2, to inject and verify a known pattern as part of the DNA read process.
- When the voltage-identification technique facilitates the specification of a lower capacity power supply or a reduction in thermal management features, it becomes vital that a device with a VID bit = `1` is operated with 0.9V V_{CCINT} and V_{CCBRAM} supplies. If the device continues to operate at 1.0V, it has the potential to consume a higher current than expected, to overload the supply, and to dissipate more heat than anticipated. As with the previous case, a fundamental failure to extract the VID bit correctly from the Device DNA is the most likely reason for this occurring, and the problem should be avoided by using good design practices. However, there is a small risk that a hardware or manufacturing defect associated with the board or the supply prevents correct voltage control. Including a power supply check in the testing of the end product should prevent this issue. An FPGA design (e.g., PicoBlaze controller code) could also be crafted to assist with that testing process.
- In a typical voltage-identification implementation, a supply common to V_{CCINT} and V_{CCBRAM} is adjusted according to the VID bit after the product is powered on. The V_{CCINT} and V_{CCBRAM} supply must start at 1.0V and can only be reduced to 0.9V after the state of the VID bit has been extracted from the Device DNA and found to be `1`. This means that during the time that a VID bit = `1` device is being supplied with 1.0V, it will also consume more power. However, because total power consumption is a combination of static and dynamic power, it is unlikely that the design enters its peak power-consuming state before the switch to 0.9V is accomplished (that is, most systems take a relatively long time to initialize and ramp up after being turned on, and dynamic power consumption rises slowly). If the design demands high-power levels almost immediately, the corresponding demand for current could exceed the capacity of the common V_{CCINT} and V_{CCBRAM} supply, causing it to shut down. This situation must be avoided. One solution is to prevent some of the highest power-consuming sections from operating until the operational level of the supply is established. For example, the design can exploit the control inputs provided on global clock buffers to gate the distribution of clocks to high-frequency circuits. In a typical implementation, the V_{CCINT} and V_{CCBRAM} supply is reduced to 0.9V in much less than one second, which allows any heating effects as a result of the higher power when operating at 1.0V for such a short period to be ignored.

Reference Design

The reference design files for this application note can be downloaded from:

https://secure.xilinx.com/webreg/clickthrough.do?cid=185933

Figure 3 shows an overview of the reference design presented on the VC707 evaluation kit.

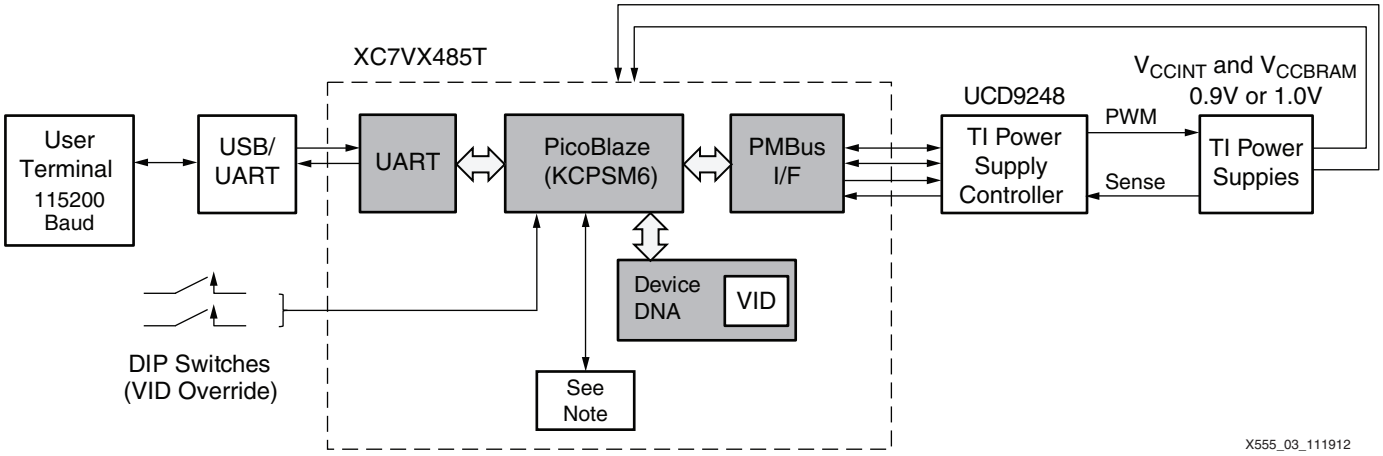

Figure 3: **Overview of the Reference Design on a VC707 Board**

Note: In Figure 3, the *See Note* box references circuits that enable experiments to be performed while operating at 0.9V or 1.0V. These circuits are somewhat representative of a real application and occupy the majority of the device. The activity of these circuits can be adjusted to increase or decrease dynamic power consumption of the device as well as to verify the device performance.

The Reference Design works with the VC707 evaluation kit. More importantly, the voltage-identification related sections of the design are intended to provide a starting point for the implementation of the voltage-identification technique in the user's product and can even be considered a drop-in solution, especially if the end product's board employs a similar power supply arrangement to the one provided on the VC707 evaluation kit.

In terms of the voltage-identification technique itself, a single PicoBlaze controller is used to read the Device DNA, extract the VID bit, and adjust the V_{CCINT} and V_{CCBRAM} supplies. Inspection of the source code would reveal that the most significant task is the implementation of the PMBus signalling and the command protocol required to communicate with the Texas Instruments UCD9248 power controller. The PicoBlaze controller is ideally suited to this class of application. In some systems it makes the actual voltage-identification task appear larger than expected. However, the PicoBlaze controller KCPSM6 occupies just 26 slices and requires a minimum of peripheral logic. The voltage-identification technique has a very small overhead, even taking into account the relatively complex requirements of the PMBus.

Besides implementing the voltage-identification technique, the reference design also includes additional features that enable the user to see how the voltage-identification technique works and to perform experiments to evaluate the power reduction of the device on their board when the voltage of the V_{CCINT} and V_{CCBRAM} supplies are reduced to 0.9V. The design also enables the user to confirm the performance of the device. The USB/UART in conjunction with PicoTerm or a similar terminal application on a PC allows information and results to be displayed. A menu facilitates user control over the evaluation circuits, for user conducted experiments.

All source code contains extensive comments to help the user get the most out of their experiments and to quickly identify sections they would like to reuse in their designs. The experimental circuits and features are enormous compared to the fundamental voltage-identification control elements of the reference design. When first looking at the reference design, remember that voltage-identification is the smaller, simpler part of the source code and everything else is to encourage designer experimentation. Other features include the ability to monitor and display the voltage, current, and power associated with all the supply rails

on the VC707 board. They are a good illustration of how much more the PicoBlaze controller can add to a product, having already performed the primary voltage-identification task immediately after being turned on.

The Voltage Identification Emulation Feature

One crucial feature of the reference design is a voltage-identification override using two of the general purpose DIP switches on the board. As described, the Virtex-7 FPGAs outlined in Table 1 contain a unique factory-programmed Device DNA value where the VID bit is one bit of the DNA value, as a constant, reflecting the qualities of the particular device. Hence, the outcome of the voltage-identification technique should always be the same for the device on the evaluation board. That would be the correct behavior, but it also means that unless the device had a VID bit set to `1`, the user would never see the V_{CCINT} and V_{CCBRAM} supplies automatically switch to 0.9V or see the reduction in power consumption. The VID bit override provides an ability to emulate a different VID bit value, allowing a user to conduct more experiments using the device on their board. A device with VID bit = `0` is only guaranteed to meet -1C specifications when the V_{CCINT} and V_{CCBRAM} supplies are 1.0V, so operating a VID bit = `0` device at 0.9V could fail speed tests. In addition, observed power reductions can be greater than or less than the worst-case figures specified for a device operating at 1.03V and 85°C.

Executing the Reference Design

The reference design matrix is shown in Table 2.

Table 2: **Reference Design Matrix**

Parameter	Description
General	
Developer name	Xilinx
Target devices	See Table 1, commercial temperature range -1C speed specification.
Source code provided	Yes
Source code format	VHDL and PSM
Design uses code and IP from existing Xilinx application note and reference designs, CORE Generator software, or third party	Yes, incorporates PicoBlaze controller
Simulation	Verified in hardware (interaction and dependence on external power supplies)
Functional simulation performed	
Timing simulation performed	
Test bench used for functional and timing simulations	
Test bench format	
Simulator software/version used	
SPICE/IBIS simulations	
Implementation	
Synthesis software tools/version used	XST Vivado® synthesis
Implementation software tools/versions used	ISE® Design Suite, version 14.3 Vivado Design Suite, version 2012.3
Static timing analysis performed	
Hardware Verification	
Hardware verified	Yes (reference design provided to facilitate further experiments)
Hardware platform used for verification	Virtex-7 FPGA VC707 evaluation kit

Conclusion

The voltage-identification technique described in this application note is a low cost method to save power. Designing with Virtex-7 FPGAs using the commercial temperature range -1C speed specification and applying the voltage-identification technique reduces the worst-case maximum supply current and power consumption. The system-wide reduction in power allows designers to minimize thermal management requirements in a system, leading to smaller power supplies and overall product cost savings.

Revision History

The revision history for this document in the following table.

Date	Version	Revisions
05/10/2012	1.0	Initial Xilinx release.
12/12/2012	1.1	This version reflects updates to v1.8 of the Virtex-7 FPGA data sheet (DS183). In this specification, V_{CCBRAM} can also be reduced to 0.9V in devices where the VID bit = 1. See the new Reference Design update which includes Vivado Design Suite files.

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