AC701 Evaluation Board for the Artix-7 FPGA

User Guide

UG952 (v1.4) August 6, 2019

XILINX®

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
10/23/2012	1.0	Initial Xilinx release.
01/30/2013	1.1	Updated photograph in Figure 1-2, page 11 to revision 1.0 of the AC701 board. Revised Figure 1-3. Revised last paragraph under DDR3 Memory Module, page 15, fourth paragraph under USB JTAG Module, page 23, third paragraph under GTP Transceivers, page 35, first paragraph under U3 IN0: 125 MHz Clock Generator, page 33, first, second and third paragraphs under U3/U4 IN2: FMC HPC GBT Clocks, page 35, fourth paragraph under PCI Express Edge Connector, page 38, and the first paragraph under SFP/SFP+ Connector, page 39. Revised third and fourth rows in Table 1-13, page 40 and the fifth row in Table 1-14, page 40. Revised second paragraph and added fourth paragraph under LCD Character Display, page 47. Revised first paragraph under I2C Bus Switch, page 49. Added Figure 1-32, page 53, Figure 1-34, page 53 and Figure 1-35, page 54. Revised Figure 1-41, page 57. Added section AC701 Board Power System, page 67 and section XADC Power System Measurement, page 72. Added third paragraph under Power Management, page 62. Revised Figure 1-49, page 78. Revised Figure A-2, page 82. Updated the Xilinx Design Constraints in Appendix C. Added Appendix F, Regulatory and Compliance Information.
08/28/2013	1.2	Added Figure 1-10. Revised Figure 1-2, Figure 1-49, and Figure 1-50.

Date	Version	Revision
04/07/2015	1.3	Replaced the board photo in Figure 1-2 with the Rev 2.0 board. Added callout row to GTP transceiver clock multiplexers in Table 1-1. Replaced Table 1-4, Table 1-5, Table 1-7, and Table 1-8. Replaced I/O banks 32, 33, and 34 with banks 33, 34, and 35 in DDR3 Memory Module, page 15. Updated Figure 1-10. Major revision of GTP Transceiver Clock Multiplexer section, starting on page 28. Added note to Table 1-13. Replaced Table 1-16, Table 1-19, Table 1-21, Table 1-23, and Table 1-26. Updated Figure 1-42. Voltage regulators changed in section AC701 Board Power System, page 67. Updated device types and footnotes in Table 1-27 to reflect device changes. Updated Figure 1-44 and Figure 1-45. Changed Texas Instruments parts numbers to LMZ31710 and LMZ31704 in [Ref 22]. Changed XADC_GPIO_3, 2, 1, 0 description in Table 1-35. Added Figure A-3 to show board components called out in Table A-3. Updated the Artix-7 FPGA AC701 Declaration of Conformity link in Appendix F, Regulatory and Compliance Information.
08/06/2019	1.4	Updated DDR3 Memory Module section. Changed Appendix C, Xilinx Design Constraints. Updated the Appendix F, Regulatory and Compliance Information.

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Chapter 1

AC701 Evaluation Board Features

Overview

The AC701 evaluation board for the Artix®-7 FPGA provides a hardware environment for developing and evaluating designs targeting the Artix-7 XC7A200T-2FBG676C FPGA. The AC701 board provides features common to many embedded processing systems, including a DDR3 SODIMM memory, an 4-lane PCI Express® interface, a tri-mode Ethernet PHY, general purpose I/O, and a UART interface. Other features can be added by using an FPGA mezzanine card (FMC) attached to the VITA-57 FPGA mezzanine connector provided on the board. A high pin count (HPC) FMC connector is provided. See AC701 Board Features for a complete list of features. The details for each feature are described in Feature Descriptions.

Additional Information

See Appendix G, Additional Resources for references to documents, files and resources relevant to the AC701 board.

AC701 Board Features

- Artix-7 XC7A200T-2FBG676C FPGA
- 1 GB DDR3 memory SODIMM
- 256 Mb quad serial peripheral interface (quad SPI) flash memory
- Secure Digital (SD) connector
- USB JTAG through Digilent module
- Clock generation
  - Fixed 200 MHz LVDS oscillator
  - I2C programmable LVDS oscillator
  - SMA connectors
  - SMA connectors for GTP transceiver clocking
- GTP transceivers
  - FMC HPC connector (two GTP transceivers)
  - SMA connectors (one pair each for TX, RX and REFCLK)
  - PCI Express (four lanes)
  - Small form-factor pluggable plus (SFP+) connector
  - Ethernet PHY RGMII interface (RJ-45 connector)
- PCI Express endpoint connectivity
  - Gen1 4-lane (x4)

- Gen2 4-lane (x4)
- SFP+ connector
- 10/100/1,000 tri-speed Ethernet PHY
- USB-to-UART bridge
- High-Definition Multimedia Interface (HDMI™) technology codec
- I2C bus
  - I2C MUX
  - I2C EEPROM (1 KB)
  - User I2C programmable LVDS oscillator
  - DDR3 SODIMM socket
  - HDMI codec
  - FMC HPC connector
  - SFP+ connector
  - I2C programmable jitter-attenuating precision clock multiplier
- Status LEDs
  - Ethernet status
  - Power good
  - FPGA INIT
  - FPGA DONE
- User I/O
  - User LEDs (four GPIO)
  - User pushbuttons (five directional)
  - CPU reset pushbutton
  - User DIP switch (4-pole GPIO)
  - User SMA GPIO connectors (one pair)
  - LCD character display (16 characters x 2 lines)
- • Switches
  - Power on/off slide switch
  - FPGA_PROG_B pushbutton switch
  - Configuration mode DIP switch
- VITA 57.1 FMC HPC connector
- Power management
  - PMBus voltage and current monitoring through TI power controller
- XADC header
- Configuration options
  - Quad SPI flash memory
  - USB JTAG configuration port
  - Platform cable header JTAG configuration port

The AC701 board block diagram is shown in Figure 1-1. The AC701 board schematics are available for download from the AC701 Evaluation Kit product page.

Electrostatic Discharge Caution

Caution! ESD can damage electronic components when they are improperly handled, and can result in total or intermittent failures. Always follow ESD-prevention procedures when removing and replacing components.

To prevent ESD damage:

- Use an ESD wrist or ankle strap and ensure that it makes skin contact. Connect the equipment end of the strap to an unpainted metal surface on the chassis.
- Avoid touching the adapter against your clothing. The wrist strap protects components from ESD on the body only.
- Handle the adapter by its bracket or edges only. Avoid touching the printed circuit board or the connectors.
- Put the adapter down only on an antistatic surface such as the bag supplied in your kit.
- If you are returning the adapter to Xilinx Product Support, place it back in its antistatic bag immediately.
- If a wrist strap is not available, ground yourself by touching the metal chassis before handling the adapter or any other part of the computer/server.

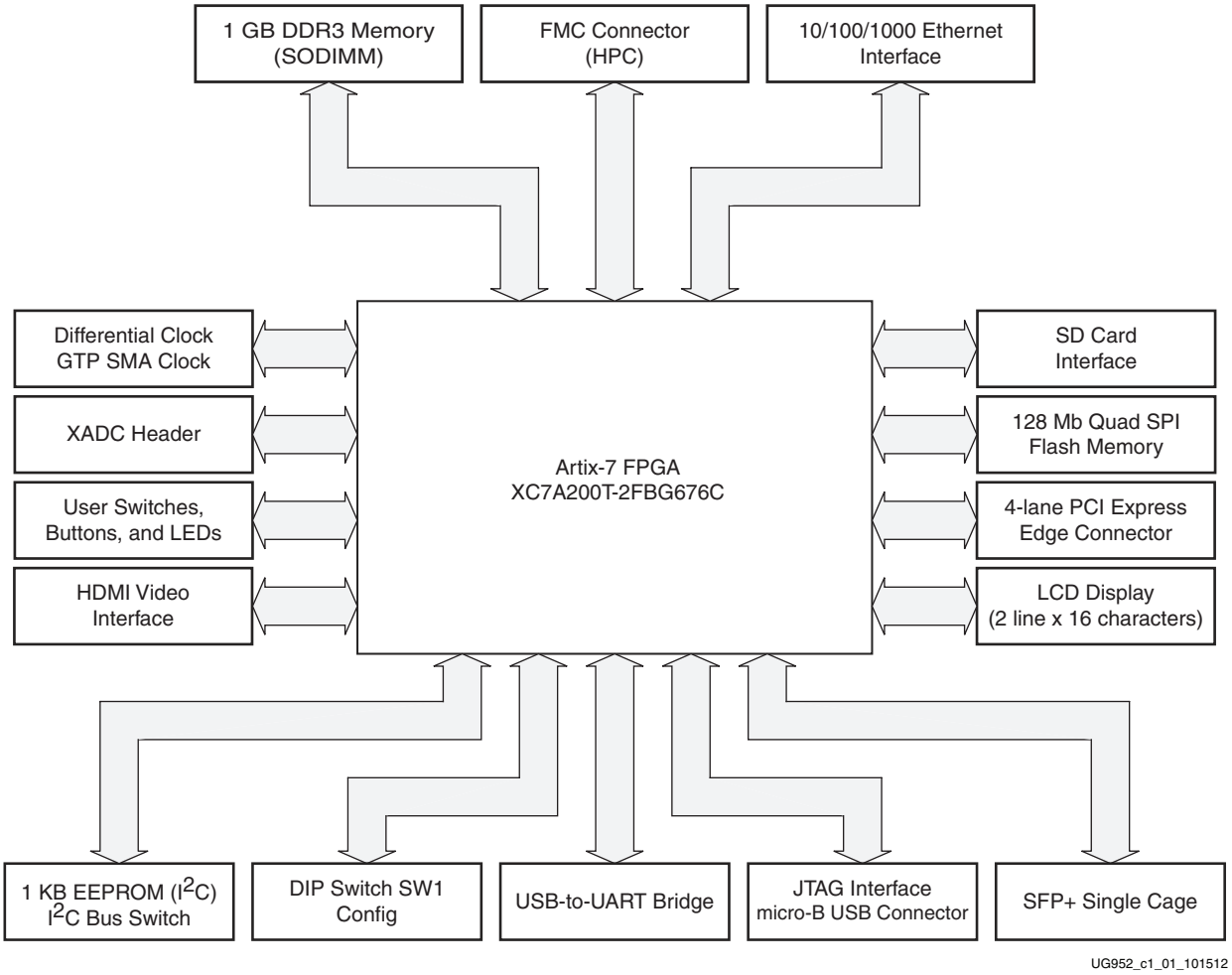


Figure 1-1: **AC701 Board Block Diagram**

Feature Descriptions

Figure 1-2 shows the AC701 board. Each numbered feature that is referenced in Figure 1-2 is described in the sections that follow.

Note: The image in Figure 1-2 is for reference only and might not reflect the current revision of the board.

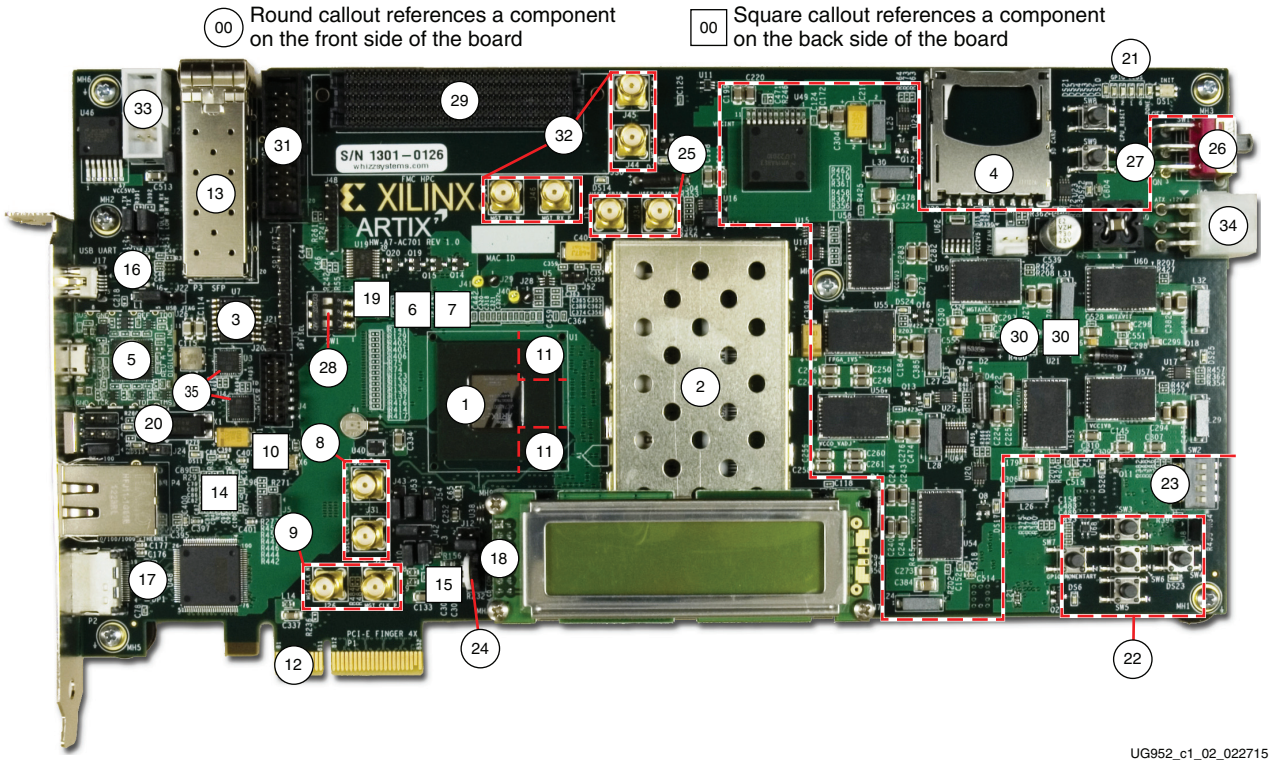


Figure 1-2: **AC701 Board Components (Rev. 2.0)**

Table 1-1: **AC701 Board Component Descriptions**

Callout	Reference Designator	Component Description	Notes	Schematic 0381502 Page Number
1	U1	Artix-7 FPGA	Xilinx XC7A200T-2FBG676C	
2	J1	DDR3 SODIMM socket with memory	Micron MT8JT12864HZ-1G6G1	10
3	U7	Quad SPI flash memory	Micron N25Q256A13ESF40G	4
4	U29	SD card interface connector	Molex 67840-8001	14
5	U26	USB-JTAG module	Digilent USB JTAG module (with micro-B receptacle)	4
6	U51	System clock source (back side of board)	SiTime SIT9102AI-243N25E200.0000	3
7	U34	Programmable user clock source 10 MHz-810 MHz (back side of board)	Silicon Labs SI570BAB000544DG (default 156.250 MHz)	3
8	J31, J32	SMA user clock input	Rosenberger 32K10K-400L5	3

Table 1-1: **AC701 Board Component Descriptions *(Cont'd)***

Callout	Reference Designator	Component Description	Notes	Schematic 0381502 Page Number
9	J25, J26	SMA GTP reference clock input	Rosenberger 32K10K-400L5	3
10	U24	Jitter attenuated clock (back side of board)	Silicon Labs SI5324-C-GM	16
11	U1	GTP transceivers	Embedded within FPGA U1	30
12	P1	PCI Express® edge connector	4-lane card edge connector	28
13	P3	SFP/SFP+ connector	Molex 74441-0010	20
14	U12	10/100/1000 tri-speed Ethernet PHY	Marvell 88E1116RA0-NNC1C000	15
15	U2	GTP transceiver clock generator 125 MHz	ICS ICS84402IAGI-01LF	3
16	J17, U44	USB-to-UART bridge (back side of board) and mini-B receptacle (front side of board)	Silicon Labs CP2103GM	5
17	P2, U48	HDMI video connector and device	Molex 500254-1927, Analog Devices ADV7511KSTZ-P	19, 18
18	J23	LCD character display connector	2 x 7 0.1 in male pin header	14
19	U52	I2C bus switch (back side of board)	TI PCA9548ARGER	6
20	DS11–DS13	Ethernet PHY status LEDs, green	Lumex SML-LX0603GW	15
21	DS2–DS5	User GPIO LEDs, green	Lumex SML-LX0603GW	21
22	SW3 – SW7	User pushbuttons E-switch	E-Switch TL3301EF100QG	21
23	SW2	GPIO DIP switch, 4-pole	C&K SDA04H1SBD	21
24	SW10	User rotary switch	Panasonic EVQ-WK4001	21
25	J33, J34	SMA user GPIO	Rosenberger 32K10K-400L5	3
26	SW15	Power on/off slide switch	C&K 1201M2S3AQE2	38
27	SW9	FPGA_PROG_B pushbutton switch (active-Low)	E-Switch TL3301EF100QG	7
28	SW1	Configuration mode DIP switch, 3-pole	C&K SDA03H1SBD	7
29	J30	FMC HPC connector	Samtec ASP_134486_01	24–27
30	U8, U9, U49, U53-U60	Power management (voltage regulators front side of board, controllers back side of board)	TI UCD90120ARGC controllers in conjunction with various regulators	39–50
31	J19	XADC header	2X10 0.1 inch male header	31
32	J44, J45, J46, J47	MGT transmit, receive SMA pairs	Rosenberger 32K10K-400L5	3
33	J2	PMBus connector	Assmann AWHW10G-0202-T-R	38
34	J49	6 pin Molex mini-fit Jr. connector for 12V	Molex 39-30-1060	38

Table 1-1: **AC701 Board Component Descriptions *(Cont'd)***

Callout	Reference Designator	Component Description	Notes	Schematic 0381502 Page Number
35	U3, U4	GTP transceiver clock multiplexers	Micrel SY89544UMG	30

Notes:

1. Jumper header locations are identified in Default Jumper Settings in Appendix A.

Artix-7 FPGA

[Figure 1-2, callout 1]

The AC701 board is populated with the Artix-7 XC7A200T-2FBG676C FPGA.

For further information on Artix-7 FPGAs, see *7 Series FPGAs Overview* (DS180) [Ref 2].

FPGA Configuration

The AC701 board supports two of the five 7 series FPGA configuration modes:

- Master SPI flash memory using the onboard Quad SPI flash memory
- JTAG using a standard-A to micro-B USB cable for connecting the host PC to the AC701 board configuration port or by J4 Platform Cable USB/Parallel Cable IV flat cable connector

Each configuration interface corresponds to one or more configuration modes and bus widths as listed in Table 1-2. The mode switches M2, M1, and M0 are on SW1 positions 1, 2, and 3 respectively, as shown in Figure 1-3.

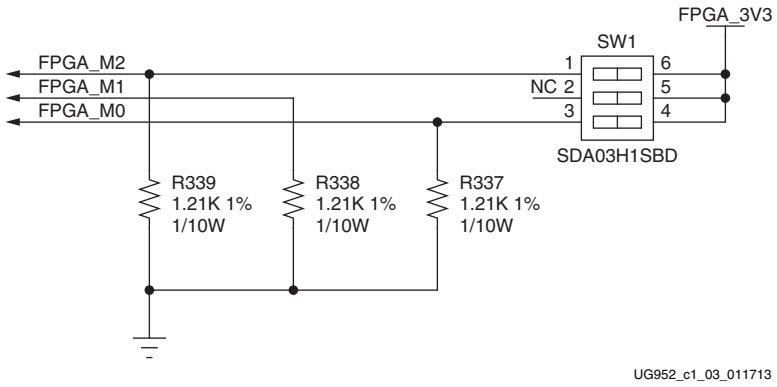


Figure 1-3: **SW1 Default Settings**

The default mode setting is M[2:0] = `001`, which selects Master SPI flash memory at board power-on. See Configuration Options for more information about the mode switch SW1.

Table 1-2: **AC701 Board FPGA Configuration Modes**

Configuration Mode	SW1 DIP switch Settings (M[2:0])	Bus Width	CCLK Direction
Master SPI flash memory	`001`	x1, x2, x4	Output
JTAG	`101`	x1	Not applicable

For full details on configuring the FPGA, see *7 Series FPGAs Configuration User Guide* (UG470) [Ref 6].

Encryption Key Backup Circuit

FPGA U1 implements bitstream encryption key technology. The AC701 board provides the encryption key backup battery circuit shown in Figure 1-4. The rechargeable 1.5V lithium button-type battery B1 is soldered to the board with the positive output connected to FPGA U1 VCCBATT pin G14. The battery supply current I_{BATT} specification is 150 nA maximum when board power is off. B1 is charged from the VCC1V8 1.8V rail through a series diode with a typical forward voltage drop of 0.38V and 4.7 kΩ current limit resistor. The nominal charging voltage is 1.62V.

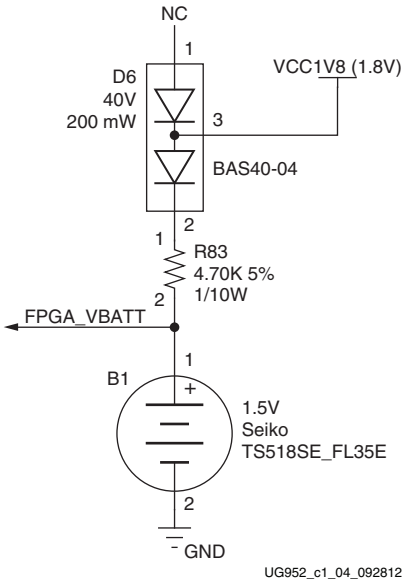


Figure 1-4: **Encryption Key Backup Circuit**

I/O Voltage Rails

In addition to Bank 0, there are eight I/O banks available on the Artix-7 device. The voltages applied to the FPGA I/O banks used by the AC701 board are listed in Table 1-3.

Table 1-3: **FPGA Bank Voltage Rails**

U1 FPGA Bank	Power Supply Rail Net Name	Voltage
Bank 0	FPGA_3V3	3.3V
Bank 12	VCCO_VADJ	2.5V
Bank 13	FPGA_1V8	1.8V
Bank 14	FPGA_3V3	3.3V
Bank 15	VCCO_VADJ	2.5V
Bank 16	VCCO_VADJ	2.5V
Bank 33	FPGA_1V5	1.5V

Table 1-3: **FPGA Bank Voltage Rails *(Cont'd)***

U1 FPGA Bank	Power Supply Rail Net Name	Voltage
Bank 34	FPGA_1V5	1.5V
Bank 35	FPGA_1V5	1.5V

DDR3 Memory Module

[Figure 1-2, callout 2]

The memory module at J1 is a 1 GB DDR3 small outline dual-inline memory module (SODIMM). It provides volatile synchronous dynamic random access memory (SDRAM) for storing user code and data. The SODIMM socket has a perforated EMI shield surrounding it as seen in Figure 1-2.

- Part number: MT8JTF12864HZ-1G6G1 (Micron Technology)
- Configuration: 1GB (128 Mb x 64)
- Supply voltage: 1.5V
- Datapath width: 64 bits
- Data rate: up to 1,600 MT/s

The AC701 XC7A200T FPGA memory interface performance is documented in the Artix-7 FPGAs Data Sheet: DC and AC Switching Characteristics (DS181) [Ref 4].

The DDR3 interface is implemented across I/O banks 33, 34, and 35. An external 0.75V reference VTTREF is provided for these banks. Any interface connected to these banks that requires a reference voltage must use this FPGA voltage reference. The connections between the DDR3 memory and the FPGA are listed in Table 1-4.

Table 1-4: **DDR3 Memory Connections to the FPGA**

FPGA Pin (U1)	Schematic Net Name	I/O Standard	J1 DDR3 Memory	
			Pin Number	Pin Name
M4	DDR3_A0	SSTL15	98	A0
J3	DDR3_A1	SSTL15	97	A1
J1	DDR3_A2	SSTL15	96	A2
L4	DDR3_A3	SSTL15	95	A3
K5	DDR3_A4	SSTL15	92	A4
M7	DDR3_A5	SSTL15	91	A5
K1	DDR3_A6	SSTL15	90	A6
M6	DDR3_A7	SSTL15	86	A7
H1	DDR3_A8	SSTL15	89	A8
K3	DDR3_A9	SSTL15	85	A9
N7	DDR3_A10	SSTL15	107	A10/AP
L5	DDR3_A11	SSTL15	84	A11
L7	DDR3_A12	SSTL15	83	A12_BC_N

Table 1-4: **DDR3 Memory Connections to the FPGA *(Cont'd)***

FPGA Pin (U1)	Schematic Net Name	I/O Standard	J1 DDR3 Memory	
			Pin Number	Pin Name
N6	DDR3_A13	SSTL15	119	A13
L3	DDR3_A14	SSTL15	80	A14
K2	DDR3_A15	SSTL15	78	A15
N1	DDR3_BA0	SSTL15	109	BA0
M1	DDR3_BA1	SSTL15	108	BA1
H2	DDR3_BA2	SSTL15	79	BA2
AB6	DDR3_D0	SSTL15	5	DQ0
AA8	DDR3_D1	SSTL15	7	DQ1
Y8	DDR3_D2	SSTL15	15	DQ2
AB5	DDR3_D3	SSTL15	17	DQ3
AA5	DDR3_D4	SSTL15	4	DQ4
Y5	DDR3_D5	SSTL15	6	DQ5
Y6	DDR3_D6	SSTL15	16	DQ6
Y7	DDR3_D7	SSTL15	18	DQ7
AF4	DDR3_D8	SSTL15	21	DQ8
AF5	DDR3_D9	SSTL15	23	DQ9
AF3	DDR3_D10	SSTL15	33	DQ10
AE3	DDR3_D11	SSTL15	35	DQ11
AD3	DDR3_D12	SSTL15	22	DQ12
AC3	DDR3_D13	SSTL15	24	DQ13
AB4	DDR3_D14	SSTL15	34	DQ14
AA4	DDR3_D15	SSTL15	36	DQ15
AC2	DDR3_D16	SSTL15	39	DQ16
AB2	DDR3_D17	SSTL15	41	DQ17
AF2	DDR3_D18	SSTL15	51	DQ18
AE2	DDR3_D19	SSTL15	53	DQ19
Y1	DDR3_D20	SSTL15	40	DQ20
Y2	DDR3_D21	SSTL15	42	DQ21
AC1	DDR3_D22	SSTL15	50	DQ22
AB1	DDR3_D23	SSTL15	52	DQ23
Y3	DDR3_D24	SSTL15	57	DQ24
W3	DDR3_D25	SSTL15	59	DQ25

Table 1-4: **DDR3 Memory Connections to the FPGA *(Cont'd)***

FPGA Pin (U1)	Schematic Net Name	I/O Standard	J1 DDR3 Memory	
			Pin Number	Pin Name
W6	DDR3_D26	SSTL15	67	DQ26
V6	DDR3_D27	SSTL15	69	DQ27
W4	DDR3_D28	SSTL15	56	DQ28
W5	DDR3_D29	SSTL15	58	DQ29
W1	DDR3_D30	SSTL15	68	DQ30
V1	DDR3_D31	SSTL15	70	DQ31
G2	DDR3_D32	SSTL15	129	DQ32
D1	DDR3_D33	SSTL15	131	DQ33
E1	DDR3_D34	SSTL15	141	DQ34
E2	DDR3_D35	SSTL15	143	DQ35
F2	DDR3_D36	SSTL15	130	DQ36
A2	DDR3_D37	SSTL15	132	DQ37
A3	DDR3_D38	SSTL15	140	DQ38
C2	DDR3_D39	SSTL15	142	DQ39
C3	DDR3_D40	SSTL15	147	DQ40
D3	DDR3_D41	SSTL15	149	DQ41
A4	DDR3_D42	SSTL15	157	DQ42
B4	DDR3_D43	SSTL15	159	DQ43
C4	DDR3_D44	SSTL15	146	DQ44
D4	DDR3_D45	SSTL15	148	DQ45
D5	DDR3_D46	SSTL15	158	DQ46
E5	DDR3_D47	SSTL15	160	DQ47
F4	DDR3_D48	SSTL15	163	DQ48
G4	DDR3_D49	SSTL15	165	DQ49
K6	DDR3_D50	SSTL15	175	DQ50
K7	DDR3_D51	SSTL15	177	DQ51
K8	DDR3_D52	SSTL15	164	DQ52
L8	DDR3_D53	SSTL15	166	DQ53
J5	DDR3_D54	SSTL15	174	DQ54
J6	DDR3_D55	SSTL15	176	DQ55
G6	DDR3_D56	SSTL15	181	DQ56
H6	DDR3_D57	SSTL15	183	DQ57

Table 1-4: **DDR3 Memory Connections to the FPGA *(Cont'd)***

FPGA Pin (U1)	Schematic Net Name	I/O Standard	J1 DDR3 Memory	
			Pin Number	Pin Name
F7	DDR3_D58	SSTL15	191	DQ58
F8	DDR3_D59	SSTL15	193	DQ59
G8	DDR3_D60	SSTL15	180	DQ60
H8	DDR3_D61	SSTL15	182	DQ61
D6	DDR3_D62	SSTL15	192	DQ62
E6	DDR3_D63	SSTL15	194	DQ63
AC6	DDR3_DM0	SSTL15	11	DM0
AC4	DDR3_DM1	SSTL15	28	DM1
AA3	DDR3_DM2	SSTL15	46	DM2
U7	DDR3_DM3	SSTL15	63	DM3
G1	DDR3_DM4	SSTL15	136	DM4
F3	DDR3_DM5	SSTL15	153	DM5
G5	DDR3_DM6	SSTL15	170	DM6
H9	DDR3_DM7	SSTL15	187	DM7
W8	DDR3_DQS0_N	SSTL15	10	DQS0_N
V8	DDR3_DQS0_P	SSTL15	12	DQS0_P
AE5	DDR3_DQS1_N	SSTL15	27	DQS1_N
AD5	DDR3_DQS1_P	SSTL15	29	DQS1_P
AE1	DDR3_DQS2_N	SSTL15	45	DQS2_N
AD1	DDR3_DQS2_P	SSTL15	47	DQS2_P
V2	DDR3_DQS3_N	SSTL15	62	DQS3_N
V3	DDR3_DQS3_P	SSTL15	64	DQS3_P
B1	DDR3_DQS4_N	SSTL15	135	DQS4_N
C1	DDR3_DQS4_P	SSTL15	137	DQS4_P
A5	DDR3_DQS5_N	SSTL15	152	DQS5_N
B5	DDR3_DQS5_P	SSTL15	154	DQS5_P
H4	DDR3_DQS6_N	SSTL15	169	DQS6_N
J4	DDR3_DQS6_P	SSTL15	171	DQS6_P
G7	DDR3_DQS7_N	SSTL15	186	DQS7_N
H7	DDR3_DQS7_P	SSTL15	188	DQS7_P
R2	DDR3_ODT0	SSTL15	116	ODT0
U2	DDR3_ODT1	SSTL15	120	ODT1

Table 1-4: **DDR3 Memory Connections to the FPGA *(Cont'd)***

FPGA Pin (U1)	Schematic Net Name	I/O Standard	J1 DDR3 Memory	
			Pin Number	Pin Name
N8	DDR3_RESET_B	LVCMOS15	30	RESET_B
T3	DDR3_S0_B	SSTL15	114	S0_B
T2	DDR3_S1_B	SSTL15	121	S1_B
U1	DDR3_TEMP_EVENT	LVCMOS15	198	EVENT_B
R1	DDR3_WE_B	SSTL15	113	WE_B
T4	DDR3_CAS_B	SSTL15	115	CAS_B
P1	DDR3_RAS_B	SSTL15	110	RAS_B
P4	DDR3_CKE0	SSTL15	73	CKE0
N4	DDR3_CKE1	SSTL15	74	CKE1
L2	DDR3_CLK0_N	DIFF_SSTL15	103	CK0_N
M2	DDR3_CLK0_P	DIFF_SSTL15	101	CK0_P
N2	DDR3_CLK1_N	DIFF_SSTL15	104	CK1_N
N3	DDR3_CLK1_P	DIFF_SSTL15	102	CK1_P

The AC701 board DDR3 memory interface adheres to the constraints guidelines documented in the DDR3 Design Guidelines section of the *7 Series FPGAs Memory Interface Solutions User Guide* (UG586) [Ref 4]. The AC701 board DDR3 memory interface is a 40 Ω impedance implementation. Other memory interface details are available in the *7 Series FPGAs Memory Interface Solutions User Guide* (UG586) and the *7 Series FPGAs Memory Resources User Guide* (UG473) [Ref 5]. For more DDR3 SODIMM details, see the Micron MT8JTF12864HZ-1G6G1 data sheet [Ref 15].

Quad SPI Flash Memory

[Figure 1-2, callout 3]

The Quad SPI flash memory U7 provides 256 Mb of nonvolatile storage that can be used for configuration and data storage.

- Part number: N25Q256A13ESF40G (Micron)
- Supply voltage: 3.3V
- Datapath width: 4 bits
- Data rate: various depending on Single/Dual/Quad mode and CCLK rate

Four data lines and the FPGA CCLK pin are wired to the Quad SPI flash memory. The connections between the SPI flash memory and the FPGA are listed in Table 1-5.

Table 1-5: **Quad SPI Flash Memory Connections to the FPGA**

FPGA Pin (U1)	Schematic Net Name	I/O Standard	U7 Quad SPI Flash Memory	
			Pin Number	Pin Name
R14	FLASH_D0	LVCMOS33	15	DQ0
R15	FLASH_D1	LVCMOS33	8	DQ1
P14	FLASH_D2	LVCMOS33	9	DQ2
N14	FLASH_D3	LVCMOS33	1	DQ3
H13	FPGA_CCLK	LVCMOS33	16	C
P18	QSPI_IC_CS_B	LVCMOS33	7	S_B

The configuration section of the *7 Series FPGAs Configuration User Guide* (UG470) [Ref 6] provides details on using the Quad SPI flash memory. Figure 1-5 shows the connections of the Quad SPI flash memory on the AC701 board. For more details, see the Micron N25Q256A13ESF40G data sheet [Ref 15].

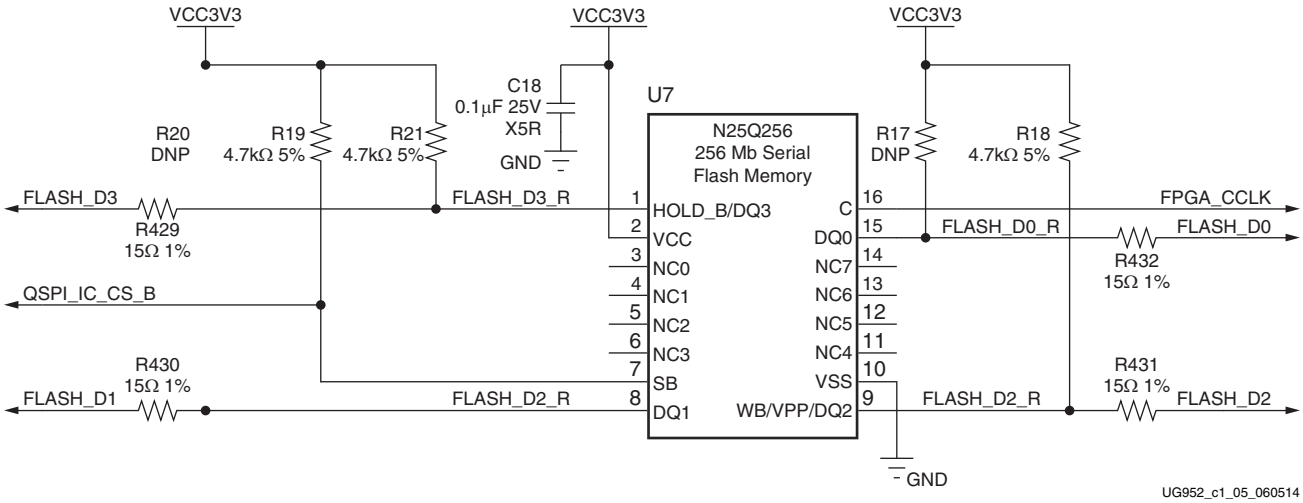


Figure 1-5: **256 Mb Quad SPI Flash Memory**

SPI Flash Memory External Programming Header

In addition to the Quad SPI device FPGA U1 connections shown in Table 1-5, the FPGA U1 SPI flash memory interface is connected to an external programming header J7.

Table 1-6 shows the SPI flash memory J7 connections to FPGA U1.

Table 1-6: **SPI Flash Memory J7 Connections to the FPGA**

U1 FPGA Pin	Schematic Net Name	J7 Pin
AE16	FPGA_PROG_B	1
N14	FLASH_D3	2
P14	FLASH_D2	3
J3.2	QSPI_CS_B	4
R14	FLASH_D0	5
R15	FLASH_D1	6
H13	FPGA_CCLK	7
NA	GND	8
NA	VCC3V3	9

Figure 1-6 shows the J7 SPI flash memory external programming connector.

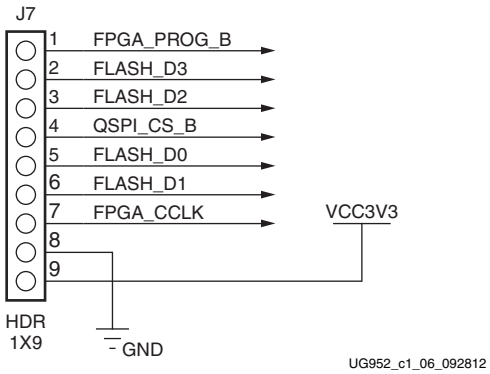


Figure 1-6: **SPI Flash Memory J7 External Programming Connector**

SD Card Interface

[Figure 1-2, callout 4]

The AC701 board includes a secure digital input/output (SDIO) interface to provide user-logic access to general purpose nonvolatile SDIO memory cards and peripherals. The SD card slot is designed to support 50 MHz high speed SD cards.

The SDIO signals are connected to I/O bank 14, which has its VCCO set to 3.3V. Figure 1-7 shows the connections of the SD card interface on the AC701 board.

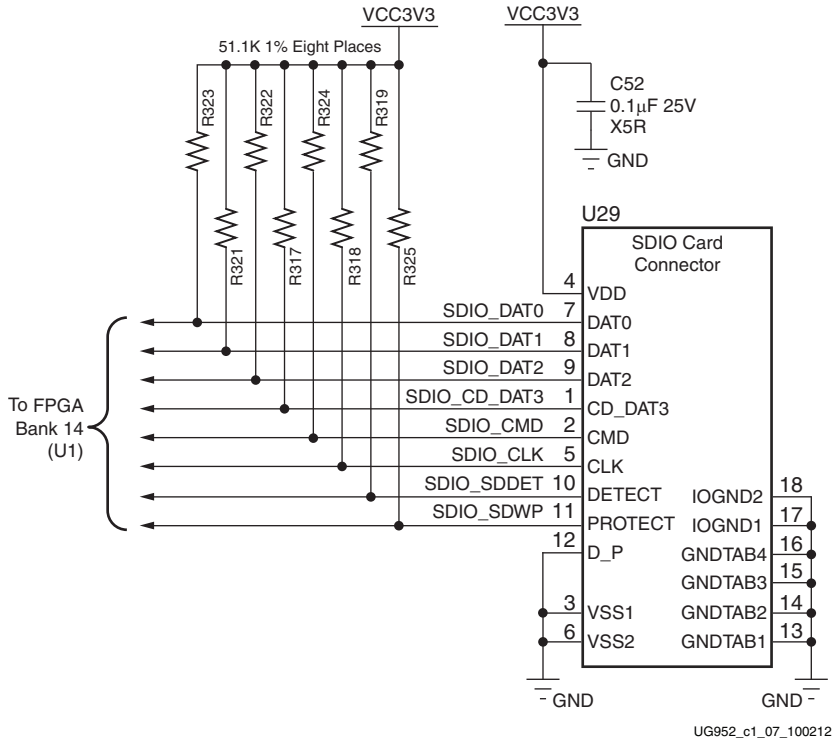


Figure 1-7: **SD Card Interface**

Table 1-7 lists the SD card interface connections to the FPGA.

Table 1-7: **SDIO Connections to the FPGA**

FPGA Pin (U1)	Schematic Net Name	I/O Standard	U29 SDIO Connector	
			Pin Number	Pin Name
R20	SDIO_SDWP	LVCMOS33	11	SDWP
P24	SDIO_SDDET	LVCMOS33	10	SDDET
N23	SDIO_CMD	LVCMOS33	2	CMD
N24	SDIO_CLK	LVCMOS33	5	CLK
P23	SDIO_DAT2	LVCMOS33	9	DAT2
N19	SDIO_DAT1	LVCMOS33	8	DAT1
P19	SDIO_DAT0	LVCMOS33	7	DAT0
P21	SDIO_CD_DAT3	LVCMOS33	1	CD_DAT3

USB JTAG Module

[Figure 1-2, callout 5]

JTAG configuration is provided through a Digilent onboard USB-to-JTAG configuration logic module (U26) where a host computer accesses the AC701 board JTAG chain through a standard-A plug (host side) to micro-B plug (AC701 board side) USB cable.

A 2-mm JTAG header (J4) is also provided in parallel for access by Xilinx download cables such as the Platform Cable USB II and the Parallel Cable IV.

The JTAG chain of the AC701 board is illustrated in Figure 1-8. JTAG configuration is allowed at any time regardless of FPGA mode pin settings. JTAG initiated configuration takes priority over the configuration method selected through the FPGA mode pin settings at SW1.

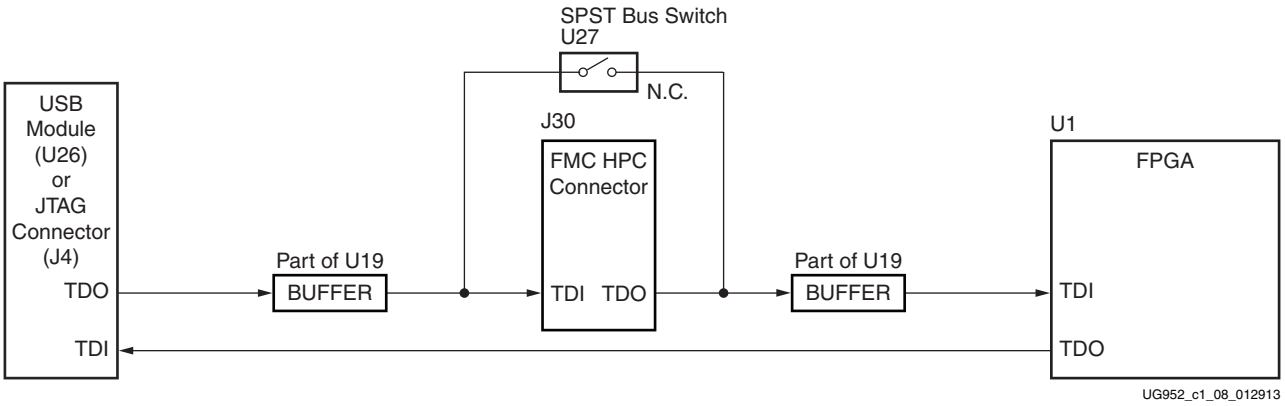


Figure 1-8: **JTAG Chain Block Diagram**

When an FMC card is attached to the AC701 board, it is automatically added to the JTAG chain through electronically controlled single-pole single-throw (SPST) switch U27. The SPST switch is in a normally closed state and transitions to an open state when an FMC card is attached. Switch U27 adds an attached FMC HPC mezzanine card to the FPGAs JTAG chain as determined by the FMC_HPC_PRSNT_M2C_B signal. The attached FMC card must implement a TDI-to-TDO connection through a device or bypass jumper in order for the JTAG chain to be completed to the FPGA U1.

The JTAG connectivity on the AC701 board allows a host computer to download bitstreams to the FPGA using Xilinx software tools. In addition, the JTAG connector allows debug tools or a software debugger to access the FPGA. Xilinx software tools can also indirectly program the Quad SPI flash memory. To accomplish this, Xilinx software configures the FPGA with a temporary design to access and program the Quad SPI flash memory device. The JTAG circuit is shown in Figure 1-9.

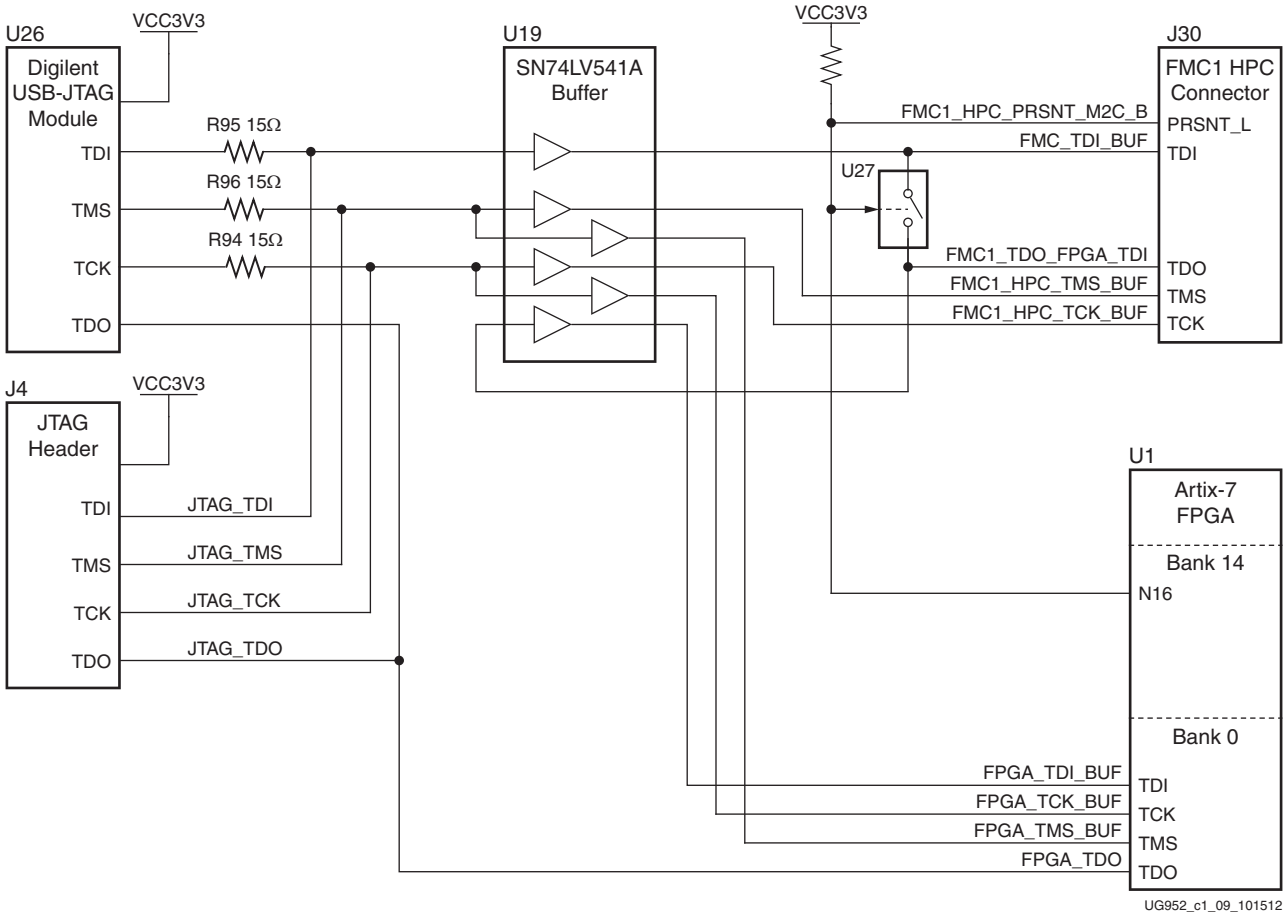


Figure 1-9: **JTAG Circuit**

Clock Generation

There are three clock sources available for the FPGA logic on the AC701 board (see Table 1-8).

Table 1-8: **AC701 Board Clock Sources**

FPGA Pin (U1)	Schematic Net Name	I/O Standard	Clock Reference	Pin	Description
R3	SYSCLK_P	LVDS_25	U51	4	SiT9102 2.5V LVDS 200 MHz Fixed Frequency Oscillator (SiTime). See System Clock Source.
P3	SYSCLK_N	LVDS_25		5	

Table 1-8: **AC701 Board Clock Sources *(Cont'd)***

FPGA Pin (U1)	Schematic Net Name	I/O Standard	Clock Reference	Pin	Description
M21	USER_CLOCK_P	LVDS_25	U34	4	Si570 3.3V LVDS I2C Programmable Oscillator (Silicon Labs). Default power-on frequency 156.250 MHz. See Programmable User Clock Source.
M22	USER_CLOCK_N	LVDS_25		5	
P16	FPGA_EMCCLK	LVCMOS33	U40	3	SiT8103 3.3V Single-Ended LVCMOS 90 MHz Fixed Frequency Oscillator (SiTime). See System Clock Source.

The AC701 clocking diagram is shown in Figure 1-10. The FPGA logic clock source circuits are detailed first after Figure 1-10, followed by the GTP clock sources circuitry descriptions in the GTP Transceivers section.

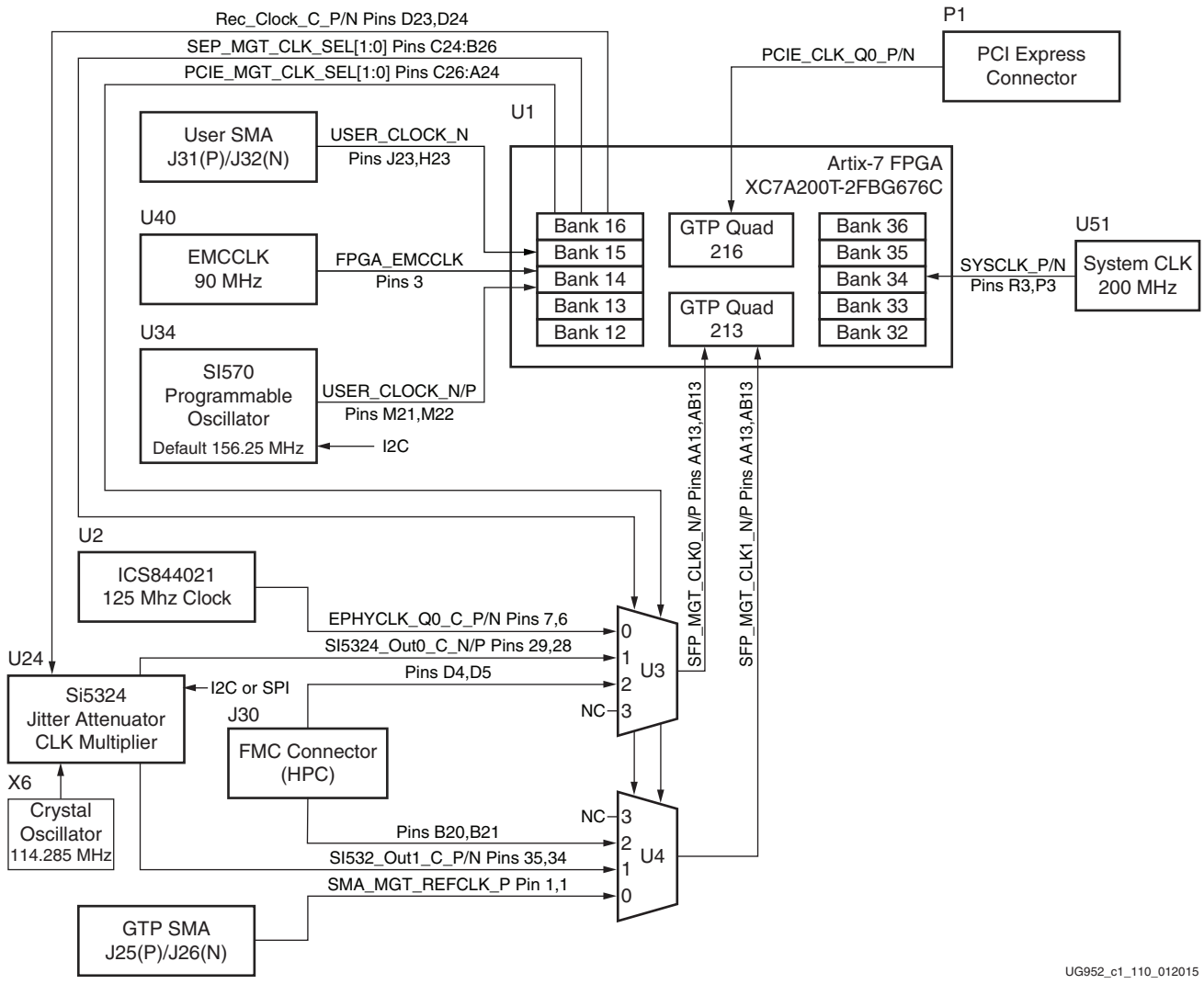


Figure 1-10: **AC701 Board Clocking Diagram**

System Clock Source

[Figure 1-2, callout 6]

The AC701 board has a 2.5V LVDS differential 200 MHz oscillator (U51) soldered onto the back side of the board and wired to an FPGA MRCC clock input on bank 34. This 200 MHz signal pair is named SYSCLK_P and SYSCLK_N, which are connected to FPGA U1 pins R3 and P3 respectively.

- Oscillator: Si Time SiT9102AI-243N25E200.00000 (200 MHz)
- PPM frequency tolerance: 50 ppm
- Differential output

For more details, see the Si Time SiT9102 data sheet [Ref 20]. The system clock circuit is shown in Figure 1-11.

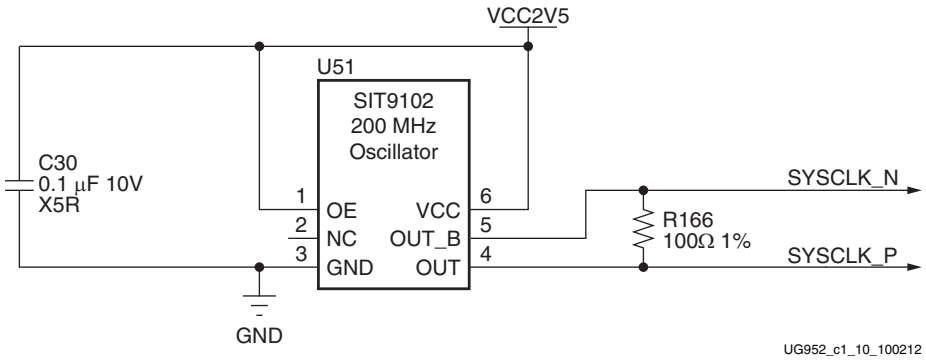


Figure 1-11: **System Clock Source**

Programmable User Clock Source

[Figure 1-2, callout 7]

The AC701 board has a programmable low-jitter 3.3V differential oscillator (U34) driving the FPGA MRCC inputs of bank 14. This USER_CLOCK_P and USER_CLOCK_N clock signal pair are connected to FPGA U1 pins M21 and M22 respectively. On power-up, the user clock defaults to an output frequency of 156.250 MHz. User applications can change the output frequency within the range of 10 MHz to 810 MHz through an I2C interface. Power cycling the AC701 board reverts the user clock to its default frequency of 156.250 MHz.

- Programmable oscillator: Silicon Labs Si570BAB000544DG (10 MHz–810 MHz)
- Differential output

The user clock circuit is shown in Figure 1-12.

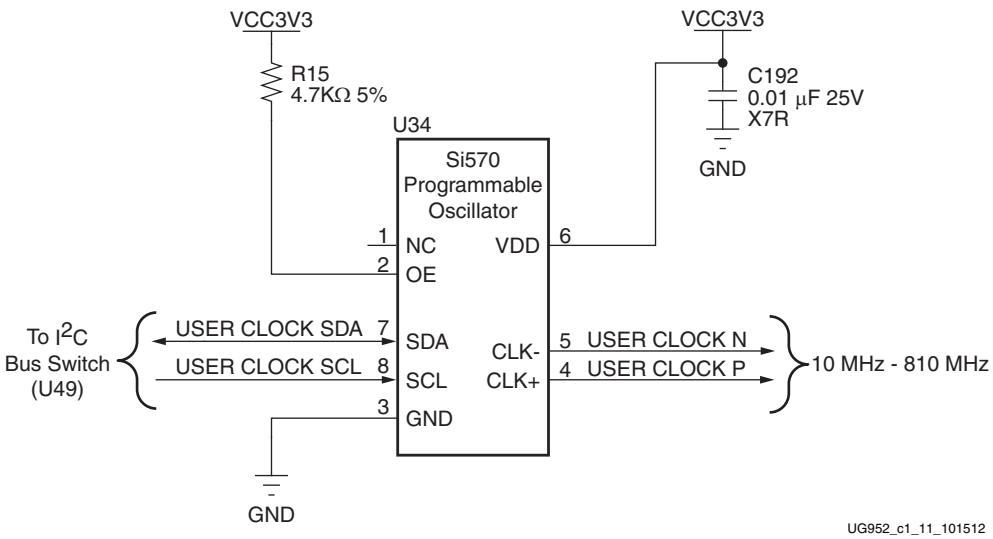


Figure 1-12: **User Clock Source**

The Silicon Labs Si570 data sheet is available from their website [Ref 21].

User SMA Clock Input

[Figure 1-2, callout 8]

An external high-precision clock signal can be provided to the FPGA bank 15 by connecting differential clock signals through the onboard 50Ω SMA connectors J31 (P) and J32 (N). The differential clock signal names are USER_SMA_CLOCK_P and USER_SMA_CLOCK_N, which are connected to FPGA U1 pins J23 and H23 respectively. The user-provided differential clock circuit is shown in Figure 1-13.

Note: This user clock is input to FPGA bank 15 which is powered by VCCO_VADJ. The VCCO_VADJ rail is typically 2.5V, but can be reprogrammed to be either 1.8V or 3.3V. The USER_SMA_CLOCK_P/N signals should not exceed the VCCO_VADJ voltage (1.8V, 2.5V or 3.3V) in use.

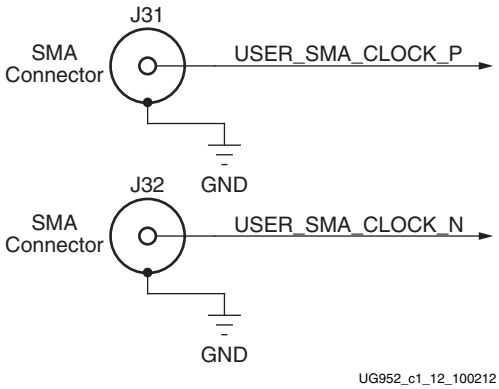


Figure 1-13: **User SMA Clock Source**

GTP Transceiver Clock Multiplexer

[Figure 1-2, callout 35]

The AC701 board provides flexible GTP Quad 213 MGTREFCLK options through the use of external multiplexer (MUX) components U3 and U4 to service the GTP Quad 213 SFP, FMC, and SMA MGT interfaces.

FPGA U1 MGT Bank 213 has two clock inputs, MGTREFCLK0 and MGTREFCLK1. Each clock input is driven by a series capacitor coupled clock sourced from a SY89544UMG 4-to-1 multiplexer.

Each multiplexer has a clock source at three of its four inputs; the fourth input is not connected.

The diagram for the GTP Quad 213 clock multiplexer circuit is shown in Figure 1-14.

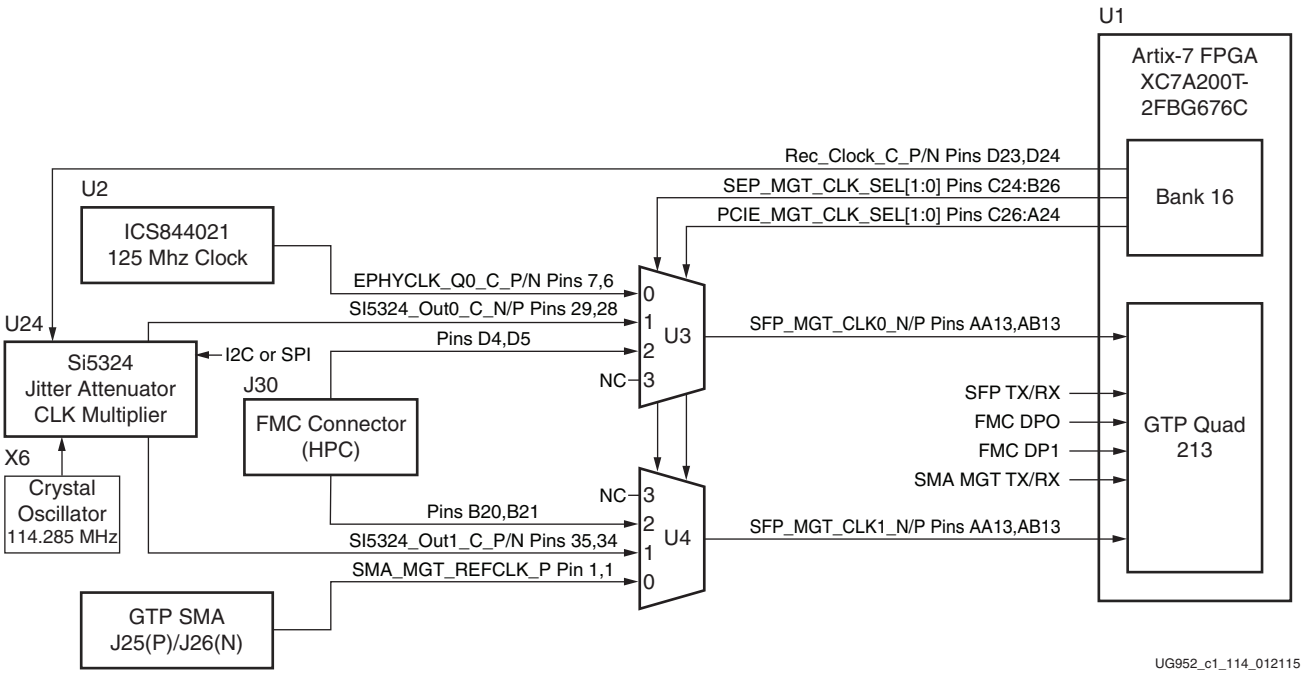


Figure 1-14: **AC701 Board GTP 213 U3 and U4 MUX Inputs**

Table 1-9 lists the MGT sources for U3 and U4. See Table 1-10 and Table 1-11 for details.

Table 1-9: **MGT Clock Multiplexer U3 and U4 Clock Sources**

Clock Name	Reference	Description
125 MHz clock generator	U2	ICS844021 Crystal-to-LVDS Clock Generator (ICS). See U3 IN0: 125 MHz Clock Generator.
Jitter attenuated clock	U24	Si5324C LVDS precision clock multiplier/jitter attenuator (Silicon Labs). See U3/U4 IN1: Jitter Attenuated Clock.
FMC HPC GBT CLK0 and CLK1	J30	FMC_HPC_GBTCLK0_M2C_C_P/N at U3; FMC_HPC_GBTCLK1_M2C_C_P/N at U4; See U3/U4 IN2: FMC HPC GBT Clocks.
GTP SMA REFCLK (differential pair)	J25	SMA_MGT_REFCLK_P (net name). See U4 IN0: GTP Transceiver SMA Clock Input.
	J26	SMA_MGT_REFCLK_N (net name). See U4 IN0: GTP Transceiver SMA Clock Input.

Clock Multiplexer U3 SY89544UMG drives Bank 213 MGTREFCLK0 pins AA13 (P) and AB13 (N).

See Table 1-10 for clock MUX U3 connections.

Table 1-10: **Multiplexer U3 SY89544UMG MGT Clock Inputs**

Clock Source			Schematic Net Name	SY89544UMG U3				Schematic Net Name (1)	FPGA U1 Bank 213	
Device	Ref	Pin		Input	SEL [1:0](2)	Pin	Output		Pin	Pin Name
ICS84402I	U2	7	EPHYCLK_Q0_P	IN0	00	4	10(Q) 11(QB)	SFP_MGT_CLK0_P SFP_MGT_CLK0_N	AA13 AB13	MGTREFCLK0P MGTREFCLK0N
		6	EPHYCLK_Q0_N			2				
SI5324C-GM	U24	29	SI5324_OUT0_C_N	IN1	01	32				
		28	SI5324_OUT0_C_P			30				
FMC HPC	J30	D4	FMC1_HPC_ GBTCLK0_M2C_P	IN2	10	27				
		D5	FMC1_HPC_ GBTCLK0_M2C_N			25				
Not connected				IN3	11	23				
						21				

Notes:
1. U3 output clock nets SFP_MGT_CLK0_P/N implement a series 0.1µF capacitor
2. SEL[1:0] nets SFP_MGT_CLK_SEL1 FPGA U1 pin C24 and SFP_MGT_CLK_SEL0 FPGA U1 pin B26. The I/O standard is LVCMOS25 (IOSTANDARD assumes a default V_{ADJ} of 2.5V)

The multiplexer U3 clock input channel select nets are SFP_MGT_CLK_SEL[1:0].

Net SFP_MGT_CLK_SEL1 is wired to FPGA U1 pin C24 and net SFP_MGT_CLK_SEL0 is wired to FPGA U1 pin B26 on FPGA U1 Bank 16.

The U3 multiplexer circuit is shown in Figure 1-15.

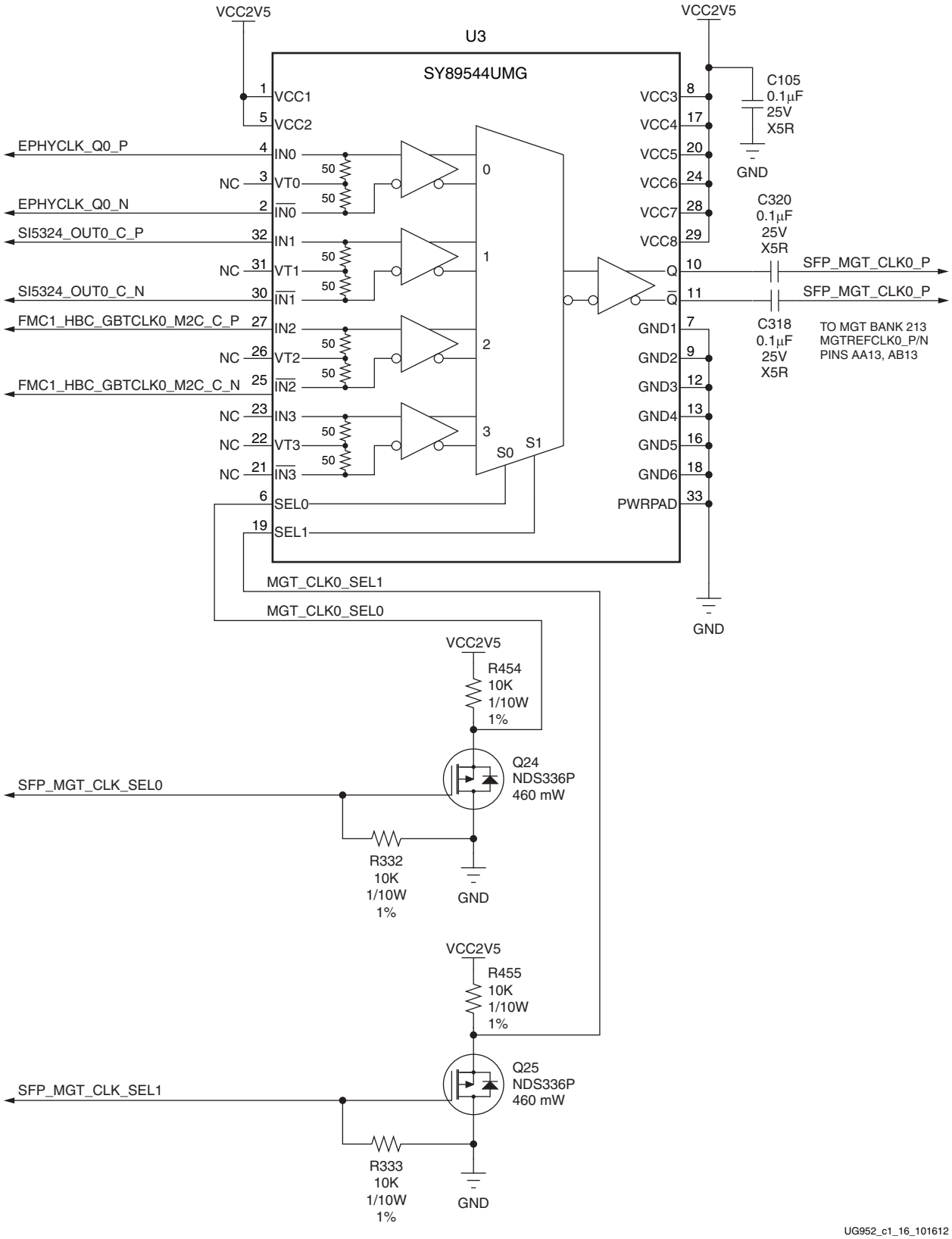


Figure 1-15: **MGT Clock Multiplexer U3 Circuit**

Clock Multiplexer U4 SY89544UMG drives Bank 213 MGTREFCLK1 pins AA11 (P) and AB11(N). See Table 1-11 for clock Multiplexer U4 connections.

Table 1-11: **Multiplexer U4 SY89544UMG MGT Clock Inputs**

Clock Source			Schematic Net Name	SY89544UMG (U4)				Schematic Net Name (1)	FPGA U1 Bank 213	
Device	Ref	Pin		Input	SEL [1:0]	Pin	Output		Pin	Pin Name
SMA	J25	1	SMA_MGT_REFCLK_P	IN0	00	4	10(Q) 11(QB)	SFP_MGT_CLK1_P SFP_MGT_CLK1_N	AA11 AB11	MGTREFCLK1P MGTREFCLK1N
SMA	J26	1	SMA_MGT_REFCLK_N			2				
SI5324C-GM	U24	35	SI5324_OUT1_C_N	IN1	01	32				
		34	SI5324_OUT1_C_P			30				
FMC HPC	J30	B20	FMC1_HPC_ GBTCLK1_M2C_P	IN2	10	27				
		B21	FMC1_HPC_ GBTCLK1_M2C_N			25				
Not connected				IN3	11	23				
						21				

Notes:
1. U4 output clock nets SFP_MGT_CLK0_P/N implement a series 0.1 µF capacitor.
2. SEL[1:0] nets PCIE_MGT_CLK_SEL1 FPGA U1 pin C26 and PCIE_MGT_CLK_SEL0 FPGA U1 pin A24 I/O standard = LVCMOS25 (IOSTANDARD assumes default V_{ADJ} of 2.5V)

The Multiplexer U4 clock input channel select nets are PCIE_MGT_CLK_SEL[1:0].

Net PCIE_MGT_CLK_SEL1 is wired to FPGA U1 pin C26 and net PCIE_MGT_CLK_SEL0 is wired to FPGA U1 pin A24 on FPGA U1 Bank 16.

The U4 Multiplexer circuit is shown in Figure 1-16.

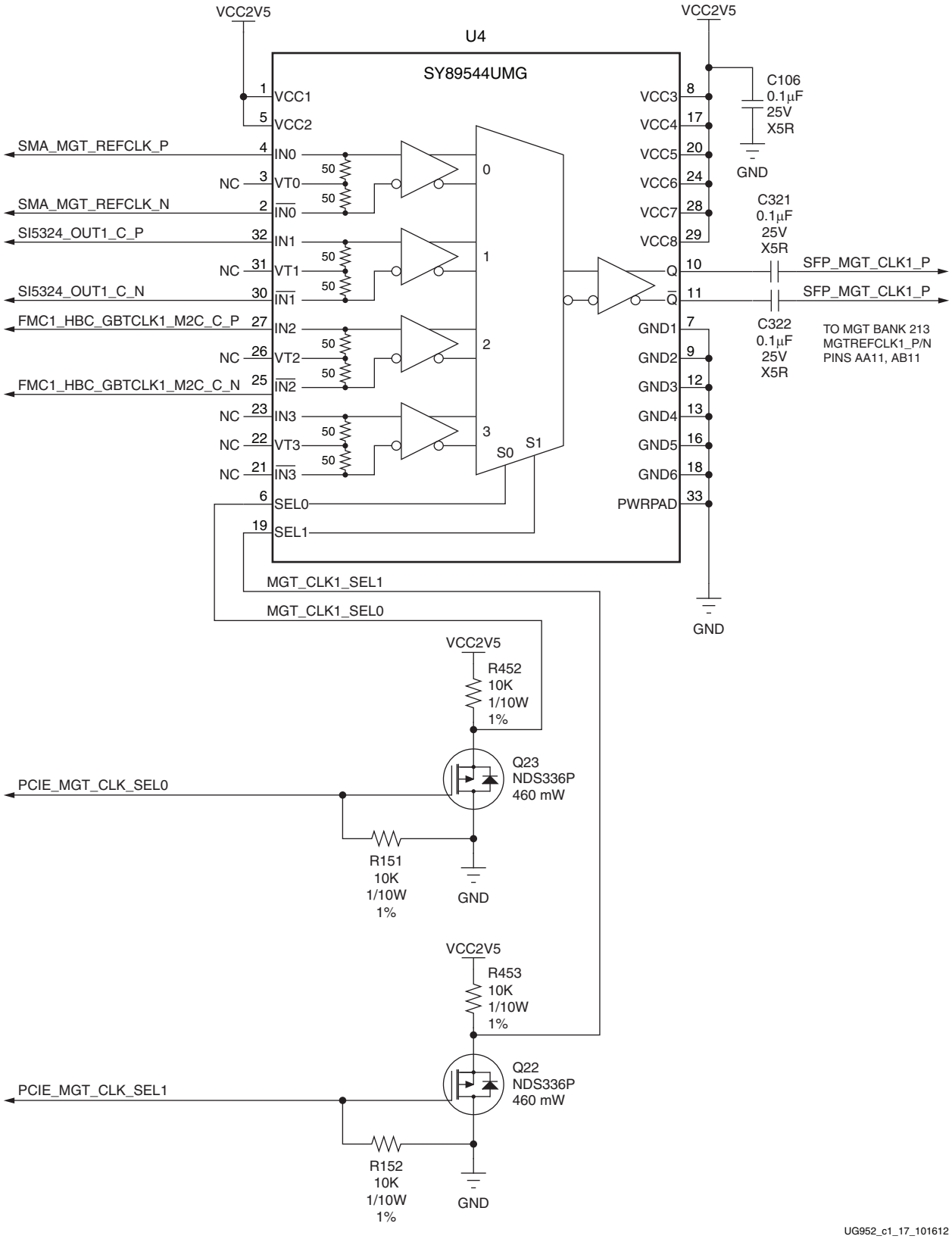


Figure 1-16: **MGT Clock Multiplexer U4 Circuit**

GTP Transceiver Clock Multiplexer Input Clock Sources

This section describes the GTP 213 Multiplexer U3 and U4 input clock circuits as listed in Table 1-11.

U3 IN0: 125 MHz Clock Generator

[Figure 1-2, callout 15]

Clock Multiplexer U3 IN 0 (pin 4 P, pin 2 N) is driven by U2 ICS84402I Crystal-to-LVDS clock generator. This device uses 25 MHz crystal X3 as its base input frequency and, using an internal VCO, multiplies this by five to produce a 0.45 ps (typical) RMS phase jitter, 125 MHz LVDS output. The circuit for the 125 MHz clock is shown in Figure 1-17.

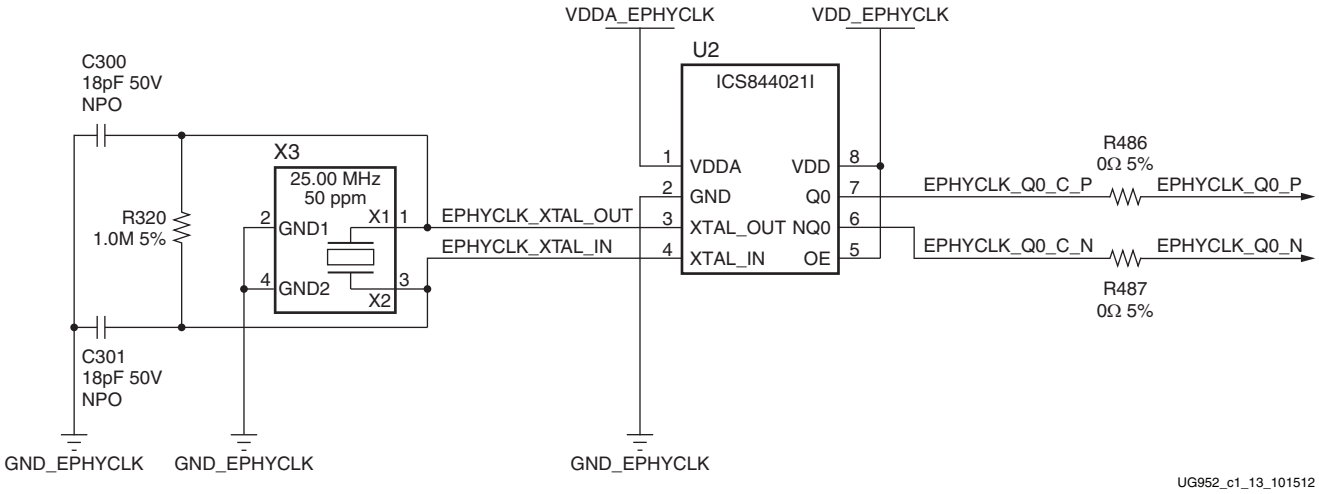


Figure 1-17: **AC701 Board 125 MHz U3 MUX IN0 Source Circuit**

U3/U4 IN1: Jitter Attenuated Clock

[Figure 1-2, callout 10]

The AC701 board includes a Silicon Labs Si5324 jitter attenuator U24 on the back side of the board. FPGA user logic can implement a clock recovery circuit and then output this clock to a differential I/O pair on I/O bank 16 (REC_CLOCK_C_P, FPGA U1 pin D23 and REC_CLOCK_C_N, FPGA U1 pin D24) for jitter attenuation. Duplicate capacitively coupled jitter attenuated clocks are routed to a pair of GTP clock MUX components U3 and U4. See Table 1-9.

The primary purpose of this clock is to support CPRI/OBSAI applications that perform clock recovery from a user-supplied SFP/SFP+ module and use the jitter attenuated recovered clock to drive the reference clock inputs of a GTP transceiver. The jitter attenuated clock circuit is shown in Figure 1-18.

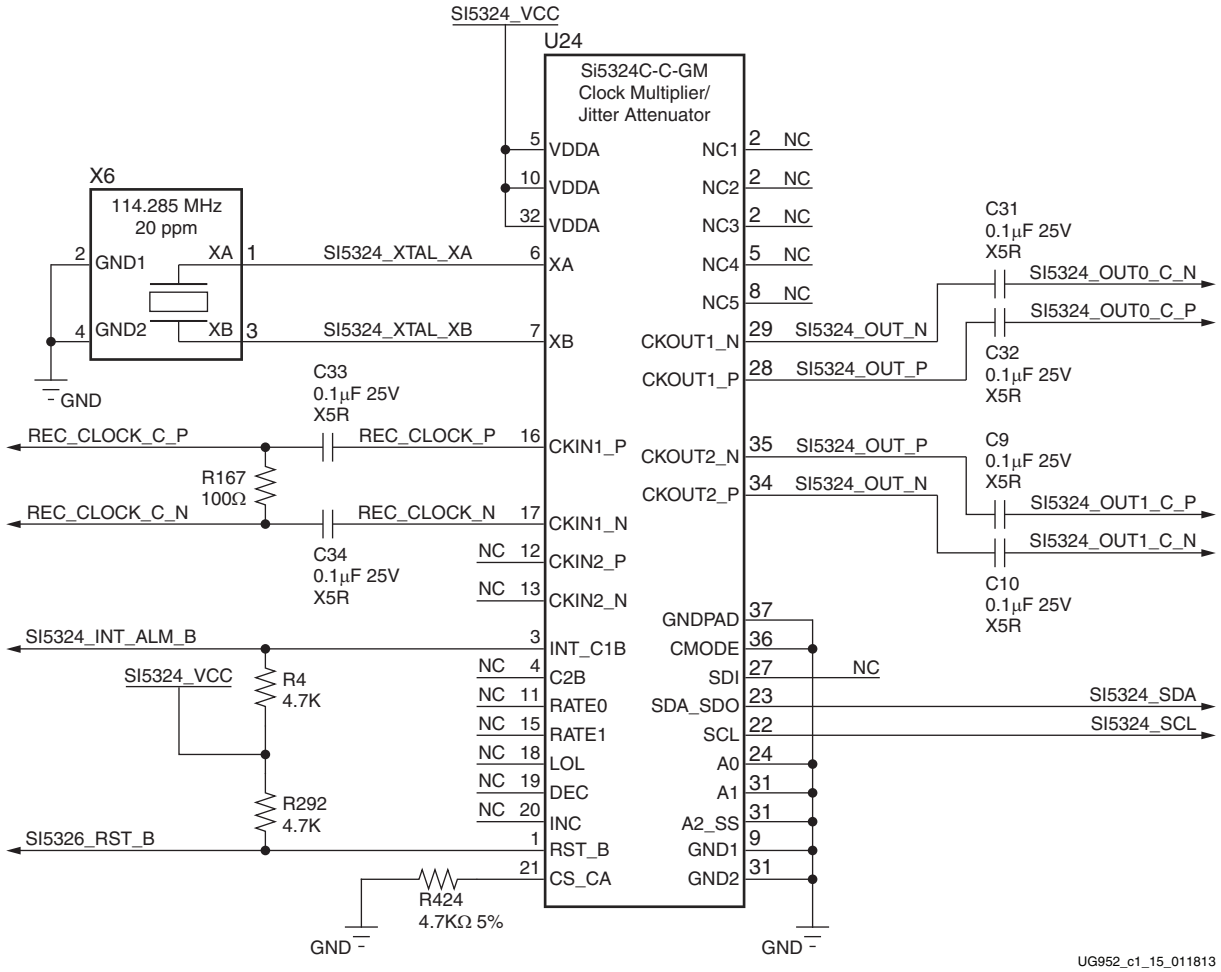


Figure 1-18: **Jitter Attenuated Clock**

See the Silicon Labs Si5324 data sheet for more information on this device [Ref 21]. The SI5324 U24 connections to FPGA U1 are shown in Table 1-10.

U4 IN0: GTP Transceiver SMA Clock Input

[Figure 1-2, callout 9]

The AC701 board includes a pair of SMA connectors for a GTP transceiver clock that are wired to GTP quad bank 213 through clock MUX U4. This differential clock has signal names SMA_MGT_REFCLK_P and SMA_REFCLK_N, which are connected to MGT clock MUX U4 input 0 pins 4 and 2 respectively. The clock MUX output pins 10 (P-side) and 11 (N-side) are capacitively coupled to FPGA U1 GTP Quad 213 MGTREFCLK1 pin AA11 and AB11 respectively. Figure 1-19 shows this direct-coupled SMA clock input circuit.

- External user-provided GTP reference clock on SMA input connectors
- Differential input

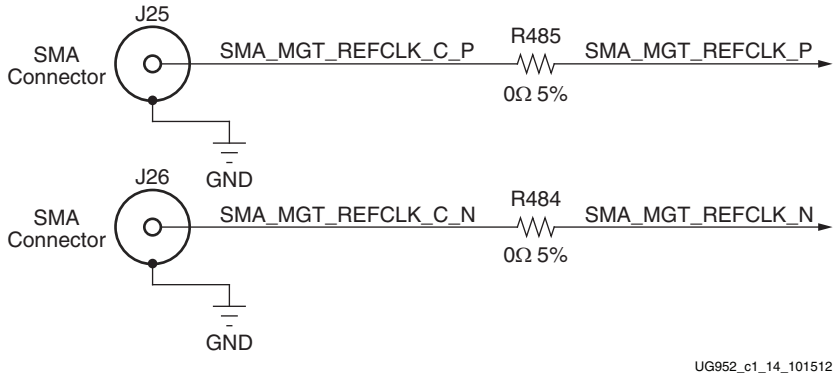


Figure 1-19: **GTP SMA Clock Source**

U3/U4 IN2: FMC HPC GBT Clocks

[Figure 1-2, callout 29]

The FMC HPC connector J30 sources two MGT clocks. FMC1_HPC_GBTCLK0_M2C_P/N from FMC connector section D (J30.D4(P), J30.D5(N)) is wired to SY89544UMG U3 IN2, pins 27(P) and 25(N). FMC1_HPC_GBTCLK1_M2C_P/N from connector section B (J30.B20(P), J30.B21(N)) is wired to SY89544UMG U4 IN2, pins 27(P) and 25(N).

GTP Transceivers

[Figure 1-2, callout 11]

The AC701 board provides access to eight GTP transceivers:

- Four of the GTP transceivers are wired to the PCI Express x4 endpoint edge connector (P1) fingers
- Two of the GTP transceivers are wired to the FMC HPC connector (J30)
- One GTP transceiver is wired to SMA connectors (RX: J46, J47 TX: J44, J45)
- One GTP transceiver is wired to the SFP/SFP+ Module connector (P3)

The GTP transceivers in 7 series FPGAs are grouped into four channels described as Quads. The reference clock for a Quad can be sourced from the Quad above or Quad below the GTP Quad of interest. There are two GTP transceiver Quads on the AC701 board with connectivity as shown here:

- Quad 213
  - Contains four GTP transceivers:
    - GTP0 SFP
    - GTP1 FMC HPC DP0
    - GTP2 FMC HPC DP1
    - GTP3 SMA transmit/receive connector pairs
  - MGTREFCLK0 Clock MUX U3 output
  - MGTREFCLK1 Clock MUX U4 output
- Quad 216
  - Contains four GTP transceivers for PCIe lanes 0–3
  - MGTREFCLK0 PCIe edge connector clock
  - MGTREFCLK1 NC

Table 1-12 lists the GTP transceiver interface connections to the FPGA (U1).

Table 1-12: **GTP Transceiver Interface Connections for FPGA U1**

Transceiver Bank	Placement	Pin Number	Pin Name	Schematic Net Name	Connected Pin	Connected Device
GTP_BANK_213	GTPE2_CHANNEL_X0Y0	AC10	MGTPTXP0_213	SFP_TX_P	P3.18	SFP+ Conn. P3
		AD10	MGTPTXN0_213	SFP_TX_N	P3.19	SFP+ Conn. P3
		AC12	MGTPRXP0_213	SFP_RX_P	P3.13	SFP+ Conn. P3
		AD12	MGTPRXN0_213	SFP_RX_N	P3.12	SFP+ Conn. P3
	GTPE2_CHANNEL_X0Y1	AE9	MGTPTXP1_213	FMC1_HPC_DP0_C2M_P	J30.C2	FMC HPC J30
		AF9	MGTPTXN1_213	FMC1_HPC_DP0_C2M_N	J30.C3	FMC HPC J30
		AE13	MGTPRXP1_213	FMC1_HPC_DP0_M2C_P	J30.C6	FMC HPC J30
		AF13	MGTPRXN1_213	FMC1_HPC_DP0_M2C_N	J30.C7	FMC HPC J30
	GTPE2_CHANNEL_X0Y2	AC8	MGTPTXP2_213	FMC1_HPC_DP1_C2M_P	J30.A22	FMC HPC J30
		AD8	MGTPTXN2_213	FMC1_HPC_DP1_C2M_N	J30.A23	FMC HPC J30
		AC14	MGTPRXP2_213	FMC1_HPC_DP1_M2C_P	J30.A2	FMC HPC J30
		AD14	MGTPRXN2_213	FMC1_HPC_DP1_M2C_N	J30.A3	FMC HPC J30
	GTPE2_CHANNEL_X0Y3	AE7	MGTPTXP3_213	SMA_MGT_TX_P	J44.1	Clock input SMA
		AF7	MGTPTXN3_213	SMA_MGT_TX_N	J45.1	Clock input SMA
		AE11	MGTPRXP3_213	SMA_MGT_RX_P	J46.1	Clock input SMA
		AF11	MGTPRXN3_213	SMA_MGT_RX_N	J47.1	Clock input SMA
	GTPE2_CHANNEL_X0Y0	AA13	MGTREFCLK0P_213	SFP_MGT_CLK0_C_P	U3.10(1)	Clock MUX U3
		AB13	MGTREFCLK0N_213	SFP_MGT_CLK0_C_N	U3.11(1)	Clock MUX U3
		AA11	MGTREFCLK1P_213	SFP_MGT_CLK1_C_P	U4.10(1)	Clock MUX U4
		AB11	MGTREFCLK1N_213	SFP_MGT_CLK1_C_N	U4.11(1)	Clock MUX U4

Table 1-12: **GTP Transceiver Interface Connections for FPGA U1 *(Cont'd)***

Transceiver Bank	Placement	Pin Number	Pin Name	Schematic Net Name	Connected Pin	Connected Device
GTP_BANK_216	GTPE2_CHANNEL_X0Y4	B7	MGTPTXP0_216	PCIE_TX3_P	P1.A29(2)	PCIe edge conn. P1
		A7	MGTPTXN0_216	PCIE_TX3_N	P1.A30(2)	PCIe edge conn. P1
		B11	MGTPRXP0_216	PCIE_RX3_P	P1.B27	PCIe edge conn. P1
		A11	MGTPRXN0_216	PCIE_RX3_N	P1.B28	PCIe edge conn. P1
	GTPE2_CHANNEL_X0Y5	D8	MGTPTXP1_216	PCIE_TX2_P	P1.A25(2)	PCIe edge conn. P1
		C8	MGTPTXN1_216	PCIE_TX2_N	P1.A26(2)	PCIe edge conn. P1
		D14	MGTPRXP1_216	PCIE_RX2_P	P1.B23	PCIe edge conn. P1
		C14	MGTPRXN1_216	PCIE_RX2_N	P1.B24	PCIe edge conn. P1
	GTPE2_CHANNEL_X0Y6	B9	MGTPTXP2_216	PCIE_TX1_P	P1.A21(2)	PCIe edge conn. P1
		A9	MGTPTXN2_216	PCIE_TX1_N	P1.A22(2)	PCIe edge conn. P1
		B13	MGTPRXP2_216	PCIE_RX1_P	P1.B19	PCIe edge conn. P1
		A13	MGTPRXN2_216	PCIE_RX1_N	P1.B20	PCIe edge conn. P1
	GTPE2_CHANNEL_X0Y7	D10	MGTPTXP3_216	PCIE_TX0_P	P1.A16(2)	PCIe edge conn. P1
		C10	MGTPTXN3_216	PCIE_TX0_N	P1.A17(2)	PCIe edge conn. P1
		D12	MGTPRXP3_216	PCIE_RX0_P	P1.B14	PCIe edge conn. P1
		C12	MGTPRXN3_216	PCIE_RX0_N	P1.B15	PCIe edge conn. P1
	GTPE2_CHANNEL_X0Y1	F11	MGTREFCLK0P_216	PCIE_CLK_QO_P	P1.A13(2)	PCIe edge conn. P1
		E11	MGTREFCLK0N_216	PCIE_CLK_QO_N	P1.A14(2)	PCIe edge conn. P1
		F13	MGTREFCLK1P_216	NC	NA	NA
		E13	MGTREFCLK1N_216	NC	NA	NA

Notes:

1. Clock MUX U3 and U4 output nets are capacitively coupled to the GTP REFCLK input pins.
2. PCIE_TXn_P/N and PCIE_CLK_Q0_P/N are capacitively coupled to the PCIe edge connector P1.

For more information on the GTP transceivers see *7 Series FPGAs GTX/GTH Transceivers User Guide* (UG476) [Ref 8].

PCI Express Edge Connector

[Figure 1-2, callout 12]

The 4-lane PCI Express edge connector performs data transfers at the rate of 2.5 GT/s for a Gen1 application and 5.0 GT/s for a Gen2 application. The PCIe transmit and receive signal datapaths have a characteristic impedance of 85Ω ±10%. The PCIe clock is routed as a 100Ω differential pair. The 7 series FPGAs GTP transceivers are used for multi-gigabit per second serial interfaces.

The XC7A200T-2FBG676C FPGA (-2 speed grade) included with the AC701 board supports up to Gen2 x4.

The PCIe clock is input from the edge connector. It is AC coupled to the FPGA through the MGTREFCLK0 pins of Quad 216. PCIE_CLK_Q0_P is connected to FPGA U1 pin F11, and the _N net is connected to pin E11. The PCI Express clock circuit is shown in Figure 1-20.

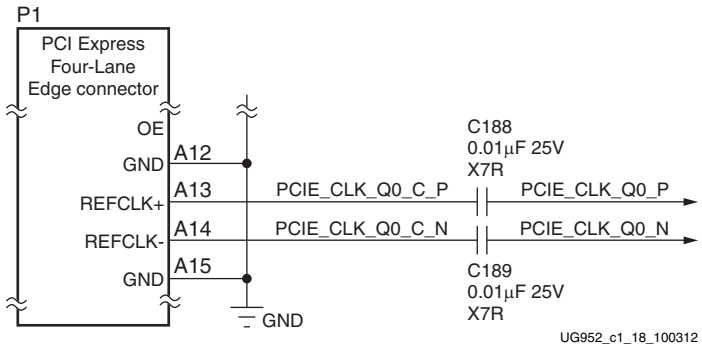


Figure 1-20: **PCI Express Clock**

PCIe lane width/size is selected using jumper J12 (Figure 1-21). The default lane size selection is 4-lane (J12 pins 3 and 4) jumpered).

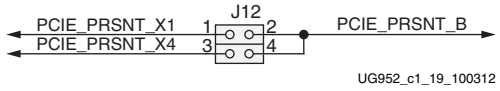


Figure 1-21: **PCI Express Lane Size Select Jumper J12**

Table 1-12 lists the PCIe edge connector connections.

For more information, see the *7 Series FPGAs Integrated Block for PCI Express v3.0 Product Guide* (PG054) [Ref 9].

SFP/SFP+ Connector

[Figure 1-2, callout 13]

The AC701 board contains a small form-factor pluggable (SFP+) connector and cage assembly (P3) that accepts SFP or SFP+ modules. Figure 1-22 shows the SFP+ module connector circuitry.

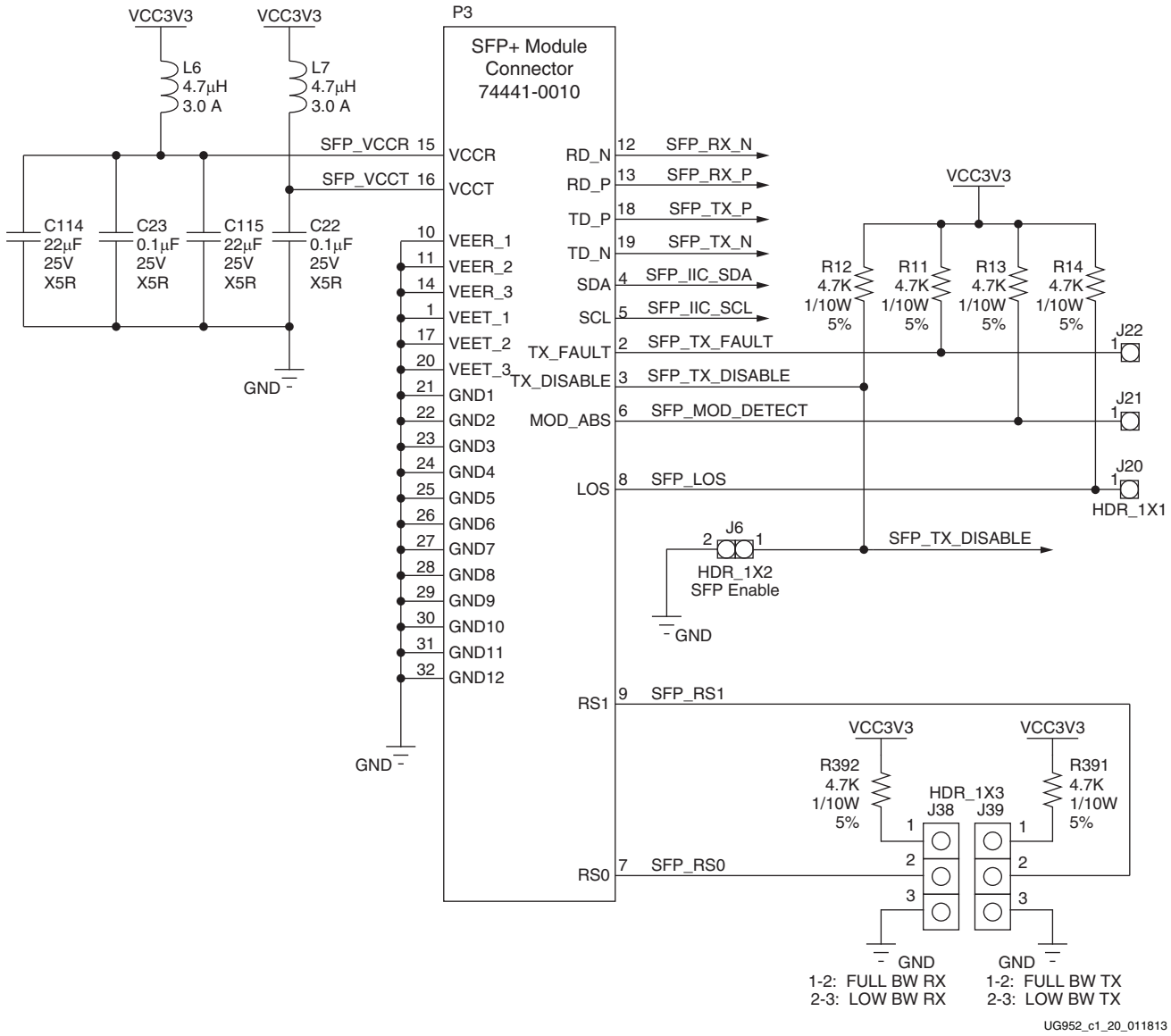


Figure 1-22: **SFP+ Module Connector**

Table 1-13 lists the SFP+ module receive and transmit connections to the FPGA.

Table 1-13: **FPGA U1 to SFP+ Module Connections**

FPGA Pin (U1)	Schematic Net Name	SFP+ Pin (P5)	SFP+ Pin Name (P5)
AD12	SFP_RX_N	12	RD_N
AC12	SFP_RX_P	13	RD_P
AD10	SFP_TX_N	19	TD_N
AC10	SFP_TX_P	18	TD_P
R18	SFP_TX_DISABLE(1)	3	TX_DISABLE
R23	SFP_LOS(1)	8	LOS

Notes:

1. For SFP_TX_DISABLE and SFP_LOS, the I/O standard = LVCMOS33.

Table 1-14 lists the SFP+ module control and status connections.

Table 1-14: **SFP+ Module Control and Status**

SFP Control/Status Signal	Board Connection
SFP_TX_FAULT	Test point J22
	High = fault
	Low = normal operation
SFP_TX_DISABLE	Jumper J6 (and FPGA pin R18)
	Off = SFP disabled
	On = SFP enabled
SFP_MOD_DETECT	Test point J21
	High = module not present
	Low = module present
SFP_RS0	Jumper J38
	Jumper pins 1-2 = full receiver bandwidth
	Jumper pins 2-3 = reduced receiver bandwidth
SFP_RS1	Jumper J39
	Jumper pins 1-2 = full transmitter bandwidth
	Jumper pins 2-3 = reduced transmitter bandwidth
SFP_LOS	Test point J20
	High = loss of receiver signal
	Low = normal operation

10/100/1000 Mb/s Tri-Speed Ethernet PHY

[Figure 1-2, callout 14]

The AC701 board uses the Marvell Alaska PHY device (88E1116R) at U12 for Ethernet communications at 10 Mb/s, 100 Mb/s, or 1,000 Mb/s. The board supports RGMII mode only. The PHY connection to a user-provided ethernet cable is through a Halo HFJ11-1G01E RJ-45 connector (P4) with built-in magnetics.

On power-up, or on reset, the PHY is configured to operate in RGMII mode with PHY address `0b00111` using the settings shown in Table 1-15. These settings can be overwritten by commands passed over the MDIO interface.

Table 1-15: **Ethernet PHY U12 Configuration Pin Settings**

U12 Pin Name (No.)	Setting	Configuration	
CONFIG0 (64)	VCCO1V8	PHYAD[1]=1	PHYAD[0]=1
CONFIG1 (1)	PHY_LED0	PHYAD[3]=0	PHYAD[2]=1
CONFIG2 (2)	GND	ENA_XC=0	PHYAD[4]=0
	PHY_LED0	ENA_XC=0	PHYAD[4]=1
	VCC1V8	ENA_XC=1	PHYAD[4]=1
CONFIG3 (3)	GND	RGMII_TX=0	RGMII_RX=0
	PHY_LED0	RGMII_TX=0	RGMII_RX=1
	PHY_LED1	RGMII_TX=1	RGMII_RX=0
	VCC1V8	RGMII_TX=1	RGMII_RX=1

The Ethernet connections from the XC7A200T at U1 to the 88E1116R PHY device at U12 are listed in Table 1-16 Ethernet PHY Connections to FPGA U1.

Table 1-16: **Ethernet PHY U12 Connections to FPGA U1**

FPGA Pin (U1)	Schematic Net Name	I/O Standard	M88E1116R (U12)	
			Pin	Pin Name
T14	PHY_MDIO	LVCMOS18	45	MDIO
W18	PHY_MDC	LVCMOS18	48	MDC
U22	PHY_TX_CLK	LVCMOS18	60	TX_CLK
T15	PHY_TX_CTRL	HSTL	63	TX_CTRL
U16	PHY_TXD0	HSTL	58	TXD0
U15	PHY_TXD1	HSTL	59	TXD1
T18	PHY_TXD2	HSTL	61	TXD2
T17	PHY_TXD3	HSTL	62	TXD3
U21	PHY_RX_CLK	LVCMOS18	53	RX_CLK
U14	PHY_RX_CTRL	HSTL	49	RX_CTRL
U17	PHY_RXD0	HSTL	50	RXD0
V17	PHY_RXD1	HSTL	51	RXD1
V16	PHY_RXD2	HSTL	54	RXD2
V14	PHY_RXD3	HSTL	55	RXD3
V18	PHY_RESET_B	LVCMOS18	10	RESET_B

Ethernet PHY Clock Source

A 25.00 MHz, 50 ppm crystal at X1 is the clock source for the 88E1116R PHY at U12. Figure 1-23 shows the clock source.

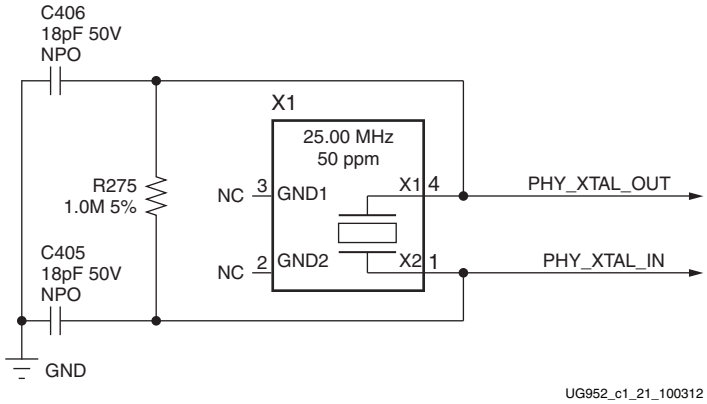


Figure 1-23: **Ethernet PHY Clock Source**

Ethernet PHY User LEDs

[Figure 1-2, callout 20]

The three Ethernet PHY user LEDs shown in Figure 1-24 are located near the RJ45 Ethernet jack P4. The ON/OFF state for each LED is software dependent and has no specific meaning at Ethernet PHY power-on.

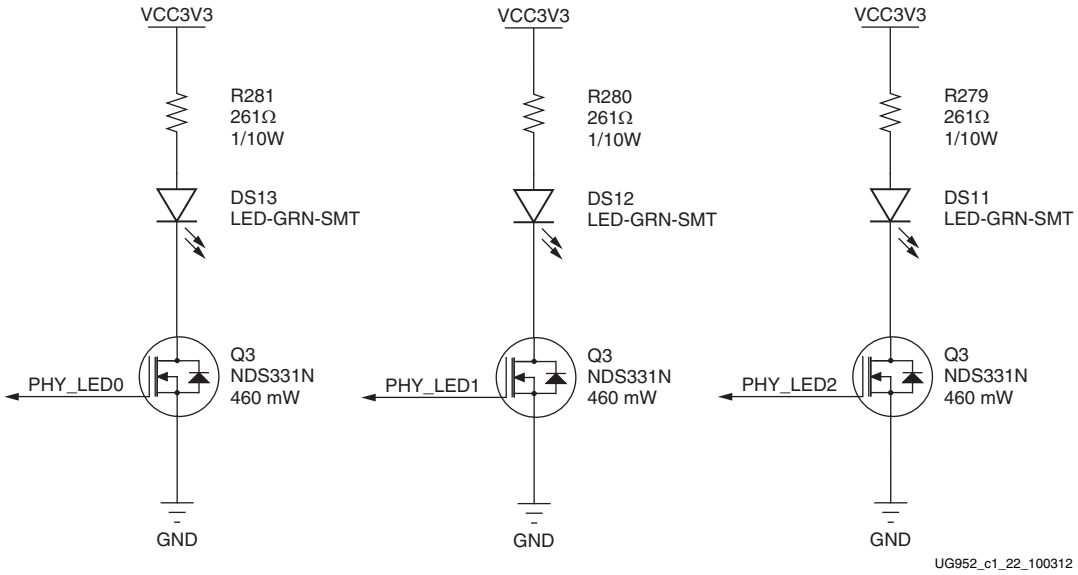


Figure 1-24: **Ethernet PHY User LEDs**

See the Marvell 88E1116R Alaska Gigabit Ethernet transceiver data sheet for details concerning the use of the Ethernet PHY user LEDs. They are referred to in the data sheet as LED0, LED1, and LED2. The product brief and other product information for the Marvell 88E1116R Alaska Gigabit ethernet transceiver is available at [Ref 18].

The Marvell 88E1116R PHY data sheet can be obtained under NDA with Marvell [Ref 18].

USB-to-UART Bridge

[Figure 1-2, callout 16]

The AC701 board contains a Silicon Labs CP2103GM USB-to-UART bridge device (U44) which allows a connection to a host computer with a USB port. The USB cable is supplied in the evaluation kit (standard-A plug to host computer, mini-B plug to AC701 board connector J17). The CP2103GM is powered by the USB 5V provided by the host PC when the USB cable is plugged into the USB port on the AC701 board.

Xilinx UART IP is expected to be implemented in the FPGA logic. The FPGA supports the USB-to-UART bridge using four signal pins: Transmit (TX), Receive (RX), Request to Send (RTS), and Clear to Send (CTS).

Silicon Labs provides royalty-free Virtual COM Port (VCP) drivers for the host computer. These drivers permit the CP2103GM USB-to-UART bridge to appear as a COM port to communications application software (for example, Tera Term or HyperTerm) that runs on the host computer. The VCP device drivers must be installed on the host PC prior to establishing communications with the AC701 board.

Table 1-17 shows the USB signal definitions at J17.

Table 1-17: **USB J17 Mini-B Receptacle Pin Assignments and Signal Definitions**

USB Receptacle Pins (J17)	Receptacle Pin Name	Schematic Net Name	Description	U44 Pin (CP2103GM)	U44 Pin Name (CP2103GM)
1	VBUS	USB_UART_VBUS	+5V from host system - U12 CP2103 power	7, 8	REGIN, VBUS
2	D_N	USB_D_N	Bidirectional differential serial data (N-side)	4	D–
3	D_P	USB_D_P	Bidirectional differential serial data (P-side)	3	D+
4	GND	USB_UART_GND	Signal ground	2, 29	GND, GND

Table 1-18 shows the USB connections between the FPGA and the UART.

Table 1-18: **FPGA to UART Connections**

FPGA (U1)				Schematic Net Name	CP2103GM Device (U44)		
Pin	Function	Direction	IOSTANDARD		Pin	Function	Direction
W19	Request to send	Output	LVCMOS18	USB_UART_CTS	22	Clear to send	Input
V19	Clear to send	Input	LVCMOS18	USB_UART_RTS	23	Request to send	Output
U19	Transmit	Data out	LVCMOS18	USB_UART_RX	24	Receive data	Data in
T19	Receive	Data in	LVCMOS18	USB_UART_TX	25	Transmit data	Data out

See the Silicon Labs website for technical information on the CP2103GM and the VCP drivers [Ref 21].

HDMI Video Output

[Figure 1-2, callout 17]

The AC701 board provides a HDMI video output using the Analog Devices ADV7511KSTZ-P HDMI transmitter (U48). The HDMI output is provided on a Molex 500254-1927 HDMI type-A connector (P2). The ADV7511 is wired to support 1080P 60 Hz, YCbCr 4:4:4 encoding using 24-bit input data mapping.

The AC701 board supports the following HDMI device interfaces:

- 24 data lines
- Independent VSYNC, HSYNC
- Single-ended input CLK
- Interrupt Out Pin to FPGA
- I2C
- SPDIF

Figure 1-25 shows the HDMI codec circuit.

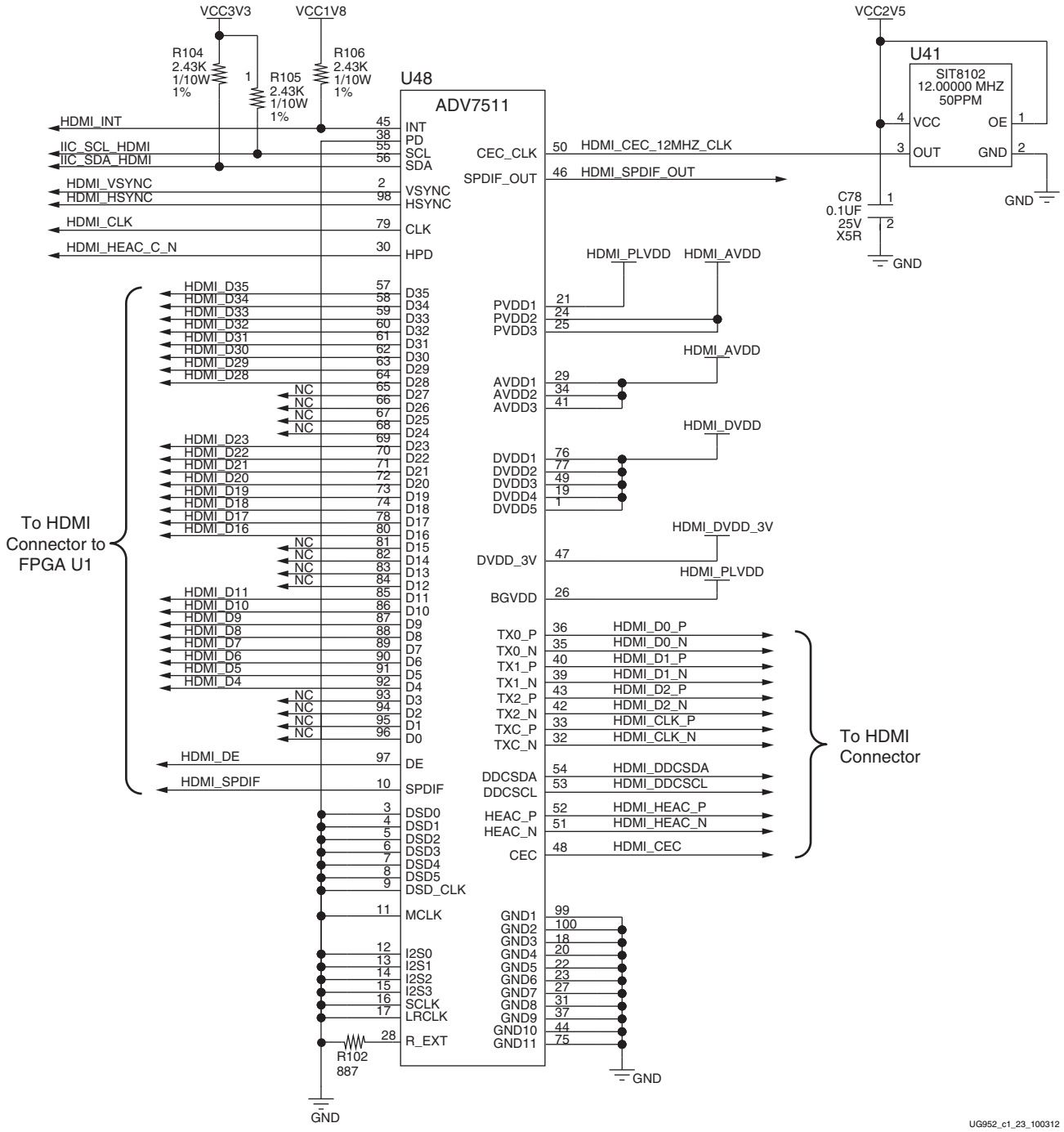


Figure 1-25: **HDMI Codec Circuit**

Table 1-19 lists the connections between the codec and the FPGA.

Table 1-19: **FPGA to HDMI Codec Connections (ADV7511)**

FPGA Pin (U1)	Schematic Net Name	I/O Standard	ADV7511 (U48)	
			Pin	Pin Name
AA24	HDMI_R_D4	LVCMOS18	92	D4
Y25	HDMI_R_D5	LVCMOS18	91	D5
Y26	HDMI_R_D6	LVCMOS18	90	D6
V26	HDMI_R_D7	LVCMOS18	89	D7
W26	HDMI_R_D8	LVCMOS18	88	D8
W25	HDMI_R_D9	LVCMOS18	87	D9
W24	HDMI_R_D10	LVCMOS18	86	D10
U26	HDMI_R_D11	LVCMOS18	85	D11
U25	HDMI_R_D16	LVCMOS18	80	D16
V24	HDMI_R_D17	LVCMOS18	78	D17
U20	HDMI_R_D18	LVCMOS18	74	D18
W23	HDMI_R_D19	LVCMOS18	73	D19
W20	HDMI_R_D20	LVCMOS18	72	D20
U24	HDMI_R_D21	LVCMOS18	71	D21
Y20	HDMI_R_D22	LVCMOS18	70	D22
V23	HDMI_R_D23	LVCMOS18	69	D23
AA23	HDMI_R_D28	LVCMOS18	64	D28
AA25	HDMI_R_D29	LVCMOS18	63	D29
AB25	HDMI_R_D30	LVCMOS18	62	D30
AC24	HDMI_R_D31	LVCMOS18	61	D31
AB24	HDMI_R_D32	LVCMOS18	60	D32
Y22	HDMI_R_D33	LVCMOS18	59	D33
Y23	HDMI_R_D34	LVCMOS18	58	D34
V22	HDMI_R_D35	LVCMOS18	57	D35
AB26	HDMI_R_DE	LVCMOS18	97	DE
Y21	HDMI_R_SPDIF	LVCMOS18	10	SPDIF
V21	HDMI_R_CLK	LVCMOS18	79	CLK
AC26	HDMI_R_VSYNC	LVCMOS18	2	VSYNC
AA22	HDMI_R_HSYNC	LVCMOS18	98	HSYNC
W21	HDMI_INT	LVCMOS18	45	INT
T20	HDMI_SPDIF_OUT_LS	LVCMOS18	46	SPDIF_OUT

Table 1-20 lists the connections between the codec and the HDMI connector P2.

Table 1-20: **ADV7511 Connections to HDMI Connector**

ADV7511 (U48)	Schematic Net Name	HDMI Connector P2 Pin
36	HDMI_D0_P	7
35	HDMI_D0_N	9
40	HDMI_D1_P	4
39	HDMI_D1_N	6
43	HDMI_D2_P	1
42	HDMI_D2_N	3
33	HDMI_CLK_P	10
32	HDMI_CLK_N	12
54	HDMI_DDCSDA	16
53	HDMI_DDCSCL	15
52	HDMI_HEAC_P	14
51	HDMI_HEAC_N	19
48	HDMI_CRC	13

Information about the ADV7511 is available on the Analog Devices website [Ref 16].

LCD Character Display

[Figure 1-2, callout 18]

A 2-line by 16-character display is provided on the AC701 board (Figure 1-26).

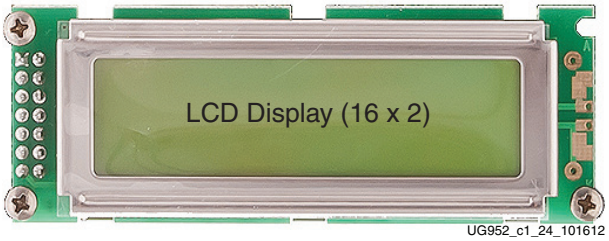


Figure 1-26: **LCD Display**

The character display runs at 5.0V and is connected to the FPGA 3.3V HP bank 14 through a TI TXS0108E 8-bit bidirectional voltage level translator (U45). Figure 1-27 shows the LCD interface circuit.

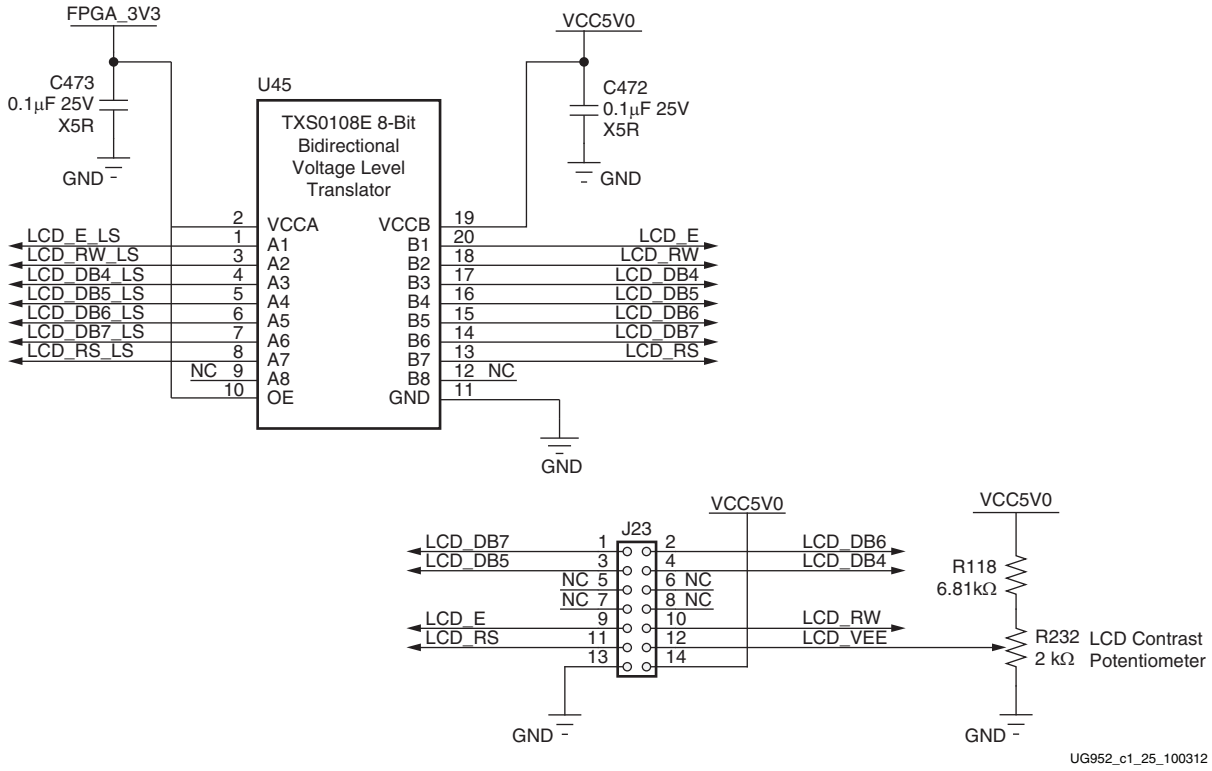


Figure 1-27: **LCD Interface Circuit**

The AC701 board base board uses a male Samtec MTLW-107-07-G-D-265 2x7 header (J23) with 0.025 inch square posts on 0.100 inch centers for connecting to a Samtec SLW-107-01-L-D female socket on the LCD display panel assembly. The LCD header shown in Figure 1-28.

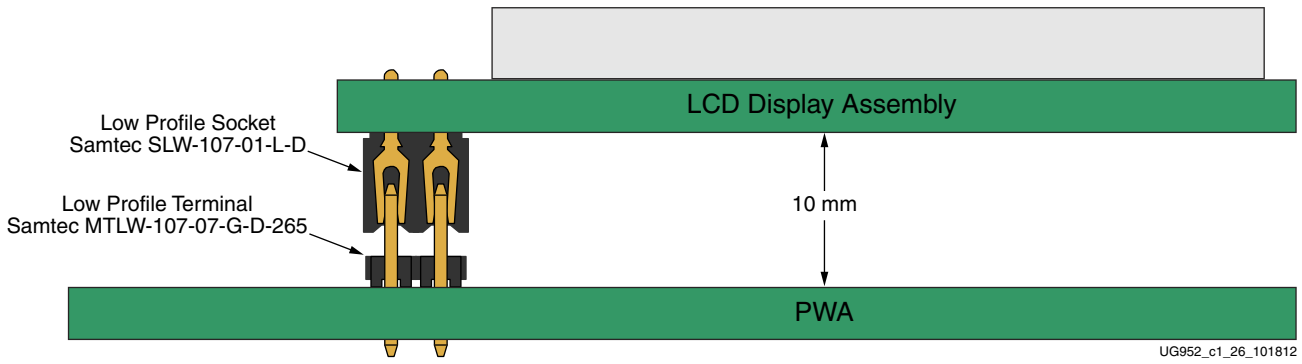


Figure 1-28: **LCD Header Details**

Table 1-21 lists the connections between the FPGA and the LCD header. If the LCD is not installed, the J23 pins listed in Table 1-21 can be used for GPIO.

Table 1-21: **FPGA to LCD Header Connections**

FPGA Pin (U1)	Schematic Net Name	I/O Standard	LCD Header Pin (J23)
L25	LCD_DB4_LS	LVCMOS33	4
M24	LCD_DB5_LS	LVCMOS33	3
M25	LCD_DB6_LS	LVCMOS33	2
L22	LCD_DB7_LS	LVCMOS33	1
L24	LCD_RW_LS	LVCMOS33	10
L23	LCD_RS_LS	LVCMOS33	11
L20	LCD_E_LS	LVCMOS33	9

For the Displaytech S162DBABC LCD data sheet, see [Ref 23].

I2C Bus Switch

[Figure 1-2, callout 19]

The AC701 board implements a single I2C port on FPGA Bank 14 (IIC_SDA_MAIN, FPGA pin K25 and IIC_SCL_MAIN, FPGA pin N18), which is routed through a Texas Instruments PCA9548 1-to-8 channel I2C switch (U52). The I2C switch can operate at speeds up to 400 kHz. The U52 bus switch at I2C address `0x74/0b01110100` must be addressed and configured to select the desired target downstream device.

The AC701 board I2C bus topology is shown in Figure 1-29.

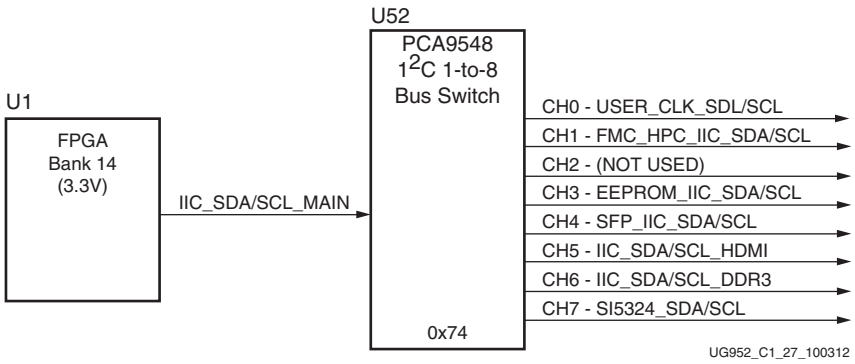


Figure 1-29: **I2C Bus Topology**

User applications that communicate with devices on one of the downstream I2C buses must first set up a path to the desired bus through the U52 bus switch at I2C address `0x74/0b01110100`.

Table 1-22 lists the address for each bus.

Table 1-22: **I2C Bus Addresses**

I2C Device	I2C Switch Position	I2C Address
PCA9548 bus switch	NA	0b1110100
Si570 clock	0	0b1011101
FMC HPC	1	0bXXXXX00
NOT USED	2	Not used
I2C EEPROM	3	0b1010100
SFP module	4	0b1010000
ADV7511 HDMI	5	0b0111001
DDR3 SODIMM	6	0b1010000, 0b0011000
Si5324 clock	7	0b1101000

Information about the PCA9548 is available on the TI Semiconductor website [Ref 22].

AC701 Board LEDs

Table 1-23 lists all LEDs on the AC701 board.

Table 1-23: **AC701 Board LEDs**

Reference Designator	Description	Notes	Schematic Page
DS1	INIT dual color red/green	Avago HSMF-C155	7
DS2	GPIO LED0	Lumex SML-LX0603GW	21
DS3	GPIO LED1	Lumex SML-LX0603GW	21
DS4	GPIO LED2	Lumex SML-LX0603GW	21
DS5	GPIO LED3	Lumex SML-LX0603GW	21
DS6	U8 TI controller #1 PWRGOOD	Lumex SML-LX0603GW	39
DS10	FPGA DONE	Lumex SML-LX0603GW	7
DS11	EPHY U12 status LED2	Lumex SML-LX0603GW	15
DS12	EPHY U12 status LED1	Lumex SML-LX0603GW	15
DS13	EPHY U12 status LED0	Lumex SML-LX0603GW	15
DS14	FMC PWRCTL1_VCC4B_PG	Lumex SML-LX0603GW	24
DS15	VCCINT ON	Lumex SML-LX0603GW	40
DS16	VCCAUX ON	Lumex SML-LX0603GW	41
DS17	VCCBRAM ON	Lumex SML-LX0603GW	42
DS18	FPGA_1V5 ON	Lumex SML-LX0603GW	43

Table 1-23: **AC701 Board LEDs *(Cont'd)***

Reference Designator	Description	Notes	Schematic Page
DS19	VCCO_VADJ ON	Lumex SML-LX0603GW	46
DS20	DDR3 SODIMM RTERM VTT ON	Lumex SML-LX0603GW	44
DS21	VCC3V3 ON	Lumex SML-LX0603GW	48
DS22	12V INPUT POWER ON	Lumex SML-LX0603GW	38
DS23	U9 TI Controller #2 PWRGOOD	Lumex SML-LX0603GW	45
DS24	MGTAVCC ON	Lumex SML-LX0603GW	49
DS25	MGTAVTT ON	Lumex SML-LX0603GW	50
DS26	FPGA_1V8 ON	Lumex SML-LX0603GW	47
DS27	DDR3 SODIMM VTT ON	Lumex SML-LX0603GW	44

Notes:

1. The Lumex SML-LX0603GW LED is green

User I/O

[Figure 1-2, callout 21–25]

The AC701 board provides the following user and general purpose I/O capabilities:

- Four user GPIO LEDs (callout 21)
  - GPIO_LED_[3-0]: DS5, DS4, DS3, DS2
- Five user pushbuttons and reset switch (callout 22)
  - GPIO_SW_[NESWC]: SW3, SW4, SW5, SW7, SW6
  - CPU_RESET: SW8
- 4-position user DIP switch (callout 23)
  - GPIO_DIP_SW[4-0]: SW2
- User rotary switch (callout 24, hidden beneath the LCD)
  - ROTARY_PUSH, ROTARY_INCA, ROTARY_INCB: SW10
- User SMA (callout 25)
  - USER_SMA_GPIO_P, USER_SMA_GPIO_N: J33, J34
- 2 line x 16 character LCD character display (callout 18)
  - If the display is unmounted, connector J23 pins are available as 7 independent GPIOs
- 6-pin in-line male 0.1 inch PMOD header
  - PMOD[3-0]: J48

User GPIO LEDs

[Figure 1-2, callout 21]

Figure 1-30 shows the user LED circuits.

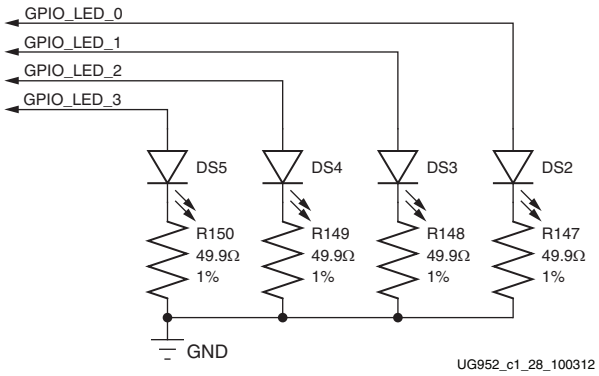


Figure 1-30: **User LEDs**

User Pushbuttons and Reset Switch

[Figure 1-2, callout 22]

Figure 1-31 shows the user pushbutton switch circuits.

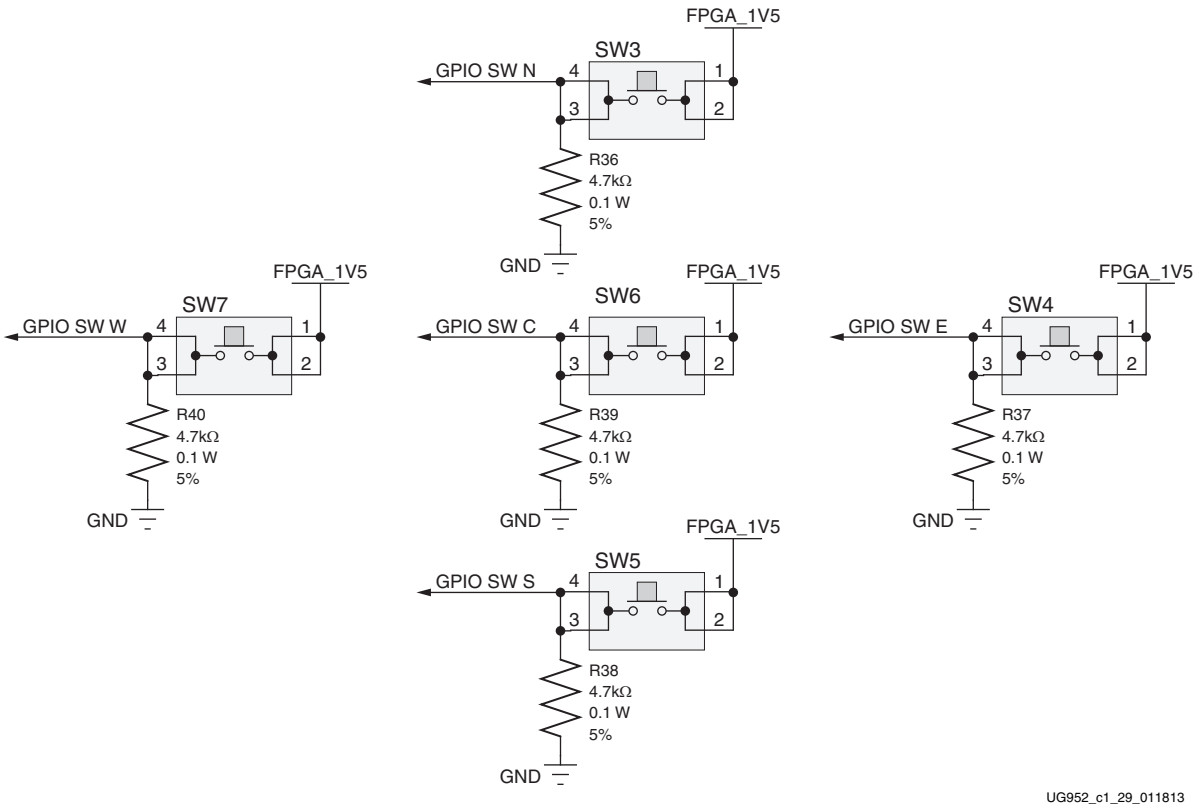


Figure 1-31: **User Pushbuttons**

Figure 1-32 shows the user CPU_RESET pushbutton switch circuit.

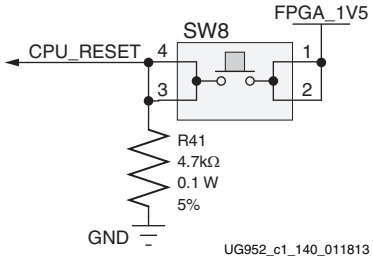


Figure 1-32: **CPU_RESET Pushbutton**

GPIO DIP Switch

[Figure 1-2, callout 23]

Figure 1-33 shows the GPIO DIP switch circuit.

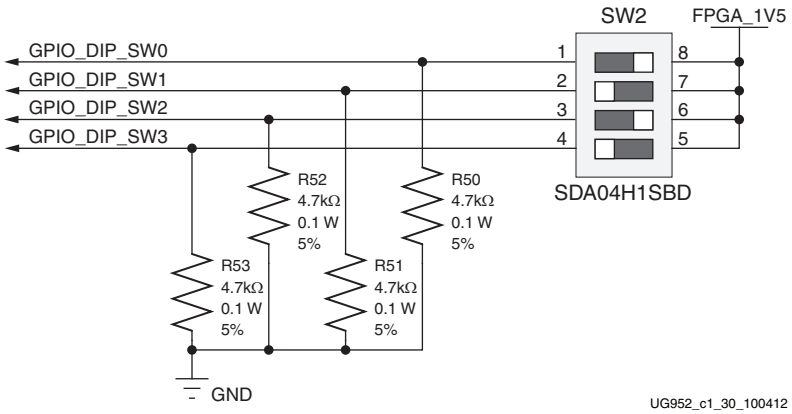


Figure 1-33: **GPIO DIP Switch**

User Rotary Switch

[Figure 1-2, callout 24]

Figure 1-34 shows the user rotary switch circuit.

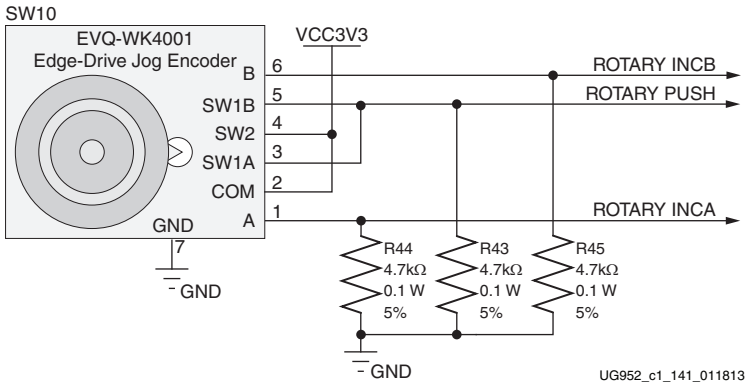


Figure 1-34: **User Rotary Switch Circuit**

User SMA Connectors

[Figure 1-2, callout 25]

Figure 1-35 shows the user SMA connector circuit.

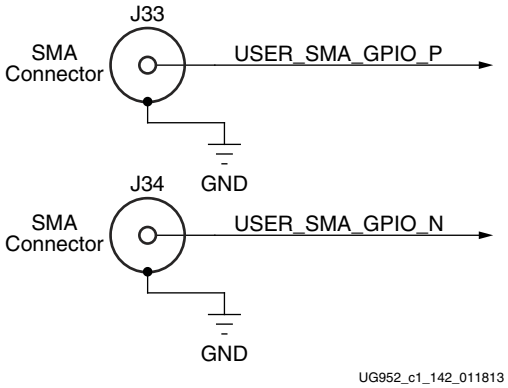


Figure 1-35: **User SMA Connector**

LCD Connector

Figure 1-36 shows the LCD J23 2x7 male pin header circuit.

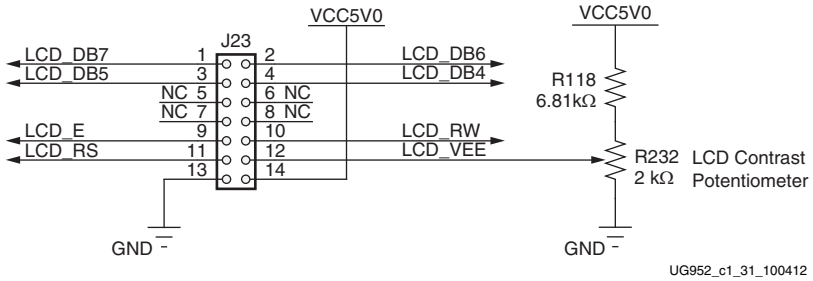


Figure 1-36: **LCD Header J23**

PMOD Connector

Figure 1-37 shows the J48 PMOD male pin header.

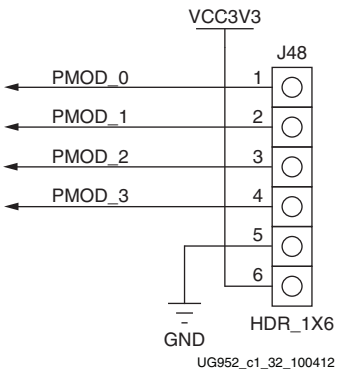


Figure 1-37: **PMOD Header J48**

Table 1-24 lists the GPIO Connections to FPGA U1.

Table 1-24: **GPIO Connections to FPGA U1**

FPGA Pin (U1)	Schematic Net Name	I/O Standard	GPIO Component Pin
User LEDs (Active High)			
M26	GPIO_LED_0	LVCMOS33	DS2.2
T24	GPIO_LED_1	LVCMOS33	DS3.2
T25	GPIO_LED_2	LVCMOS33	DS4.2
R26	GPIO_LED_3	LVCMOS33	DS5.2
User Directional Pushbutton Switches (Active High)			
P6	GPIO_SW_N	SSTL15	SW3.3
U5	GPIO_SW_E	SSTL15	SW4.3
T5	GPIO_SW_S	SSTL15	SW5.3
R5	GPIO_SW_W	SSTL15	SW7.3
U6	GPIO_SW_C	SSTL15	SW6.3
User CPU_RESET Pushbutton Switch (Active High)			
U4	CPU_RESET	SSTL15	SW8.3
User 4-Pole DIP Switch (Active High)			
R8	GPIO_DIP_SW0	SSTL15	SW2.1
P8	GPIO_DIP_SW1	SSTL15	SW2.2
R7	GPIO_DIP_SW2	SSTL15	SW2.3
R6	GPIO_DIP_SW3	SSTL15	SW2.4
User Rotary Encoder Switch (Active High)			
P20	ROTARY_INCB	LVCMOS33	SW10.6
N21	ROTARY_PUSH	LVCMOS33	SW10.5
N22	ROTARY_INCA	LVCMOS33	SW10.1
User SMA Connectors			
T8	USER_SMA_GPIO_P	SSTL15	J33.1
T7	USER_SMA_GPIO_N	SSTL15	J34.1
User GPIO PMOD Male Pin Header			
P26	PMOD_0	LVCMOS33	J48.1
T22	PMOD_1	LVCMOS33	J48.2
R22	PMOD_2	LVCMOS33	J48.3
T23	PMOD_3	LVCMOS33	J48.4

Switches

[Figure 1-2, callout 26–27]

The AC701 board includes a power and a configuration switch:

- Power on/off slide switch SW15 (callout 26)
- FPGA_PROGRAM_B SW14, active-Low (callout 27)

Power On/Off Slide Switch SW15

[Figure 1-2, callout 26]

The AC701 board power switch is SW15. Sliding the switch actuator from the Off to On position applies 12V power from J49, a 6-pin mini-fit connector. Green LED DS22 illuminates when the AC701 board power is on. See Power Management for details on the onboard power system.

> ***Caution!*** Do NOT plug a PC ATX power supply 6-pin connector into J49 on the AC701 board The ATX 6-pin connector has a different pinout than J49. Connecting an ATX 6-pin connector into J49 damages the AC701 board and voids the board warranty.

Figure 1-38 shows the simplified diagram of the power connector J49, power switch SW15 and indicator LED DS22.

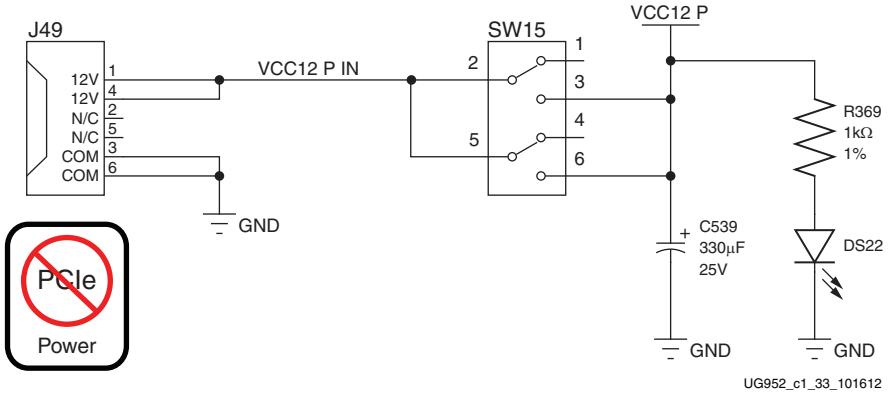


Figure 1-38: **Power On/Off Switch SW15**

The AC701 Evaluation Kit provides the adapter cable shown in Figure 1-39 for powering the AC701 board from the ATX power supply 4-pin peripheral connector. The Xilinx part number for this cable is 2600304, and is equivalent to Sourcegate Technologies part number AZCBL-WH-1109-RA4. For information on ordering this cable, see [Ref 24].

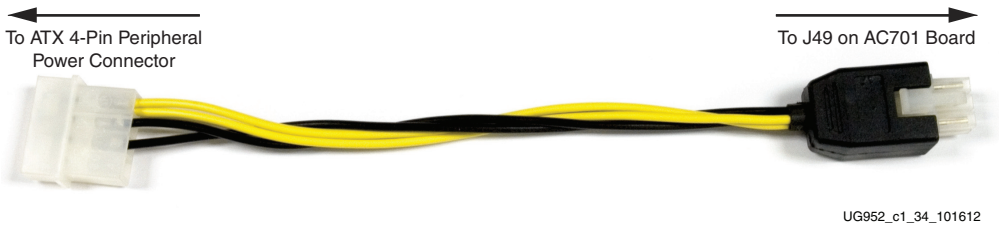


Figure 1-39: **ATX Power Supply Adapter Cable**

FPGA_PROG_B Pushbutton SW9 (Active-Low)

[Figure 1-2, callout 27]

Switch SW9 grounds the FPGA PROGRAM_B pin when pressed. This action initiates an FPGA reconfiguration. The FPGA_PROG_B signal is connected to FPGA U1 pin AE16.

See *7 Series FPGAs Configuration User Guide* (UG470) [Ref 6] for further details on configuring the 7 series FPGAs.

Figure 1-40 shows SW9.

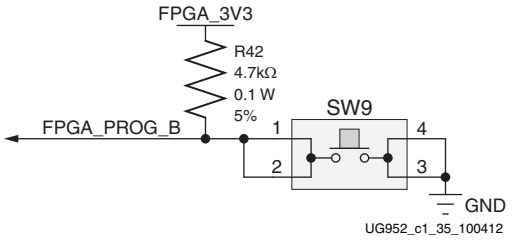


Figure 1-40: **FPGA_PROG_B Pushbutton SW9**

Configuration Mode Switch SW1

The AC701 board supports two of the five 7 series FPGA configuration modes:

- Master SPI flash memory using the onboard Quad SPI flash memory
- JTAG using a standard-A to micro-B USB cable for connecting the host PC to the AC701 board configuration port (on the Digilent module)

Each configuration interface corresponds to one or more configuration modes and bus widths as listed in Table 1-25. The mode switches M2, M1, and M0 are on SW1 positions 1, 2, and 3 respectively, as shown in Figure 1-41.

Note: On the AC701 board, SW1 switch position 2 is not used.

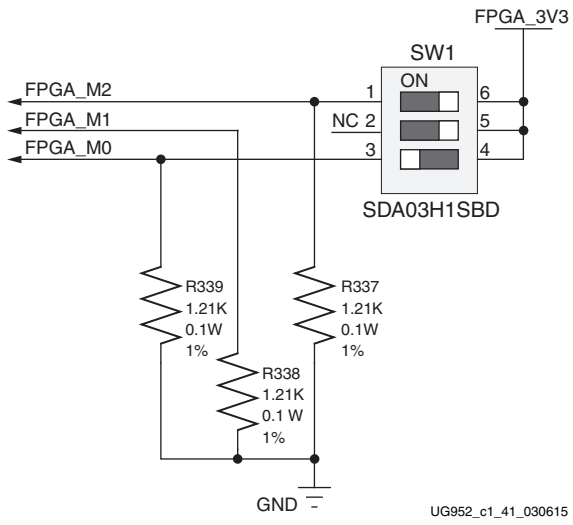


Figure 1-41: **Mode Switch SW1**

The default mode setting is M[2:0] = 001, which selects Master SPI flash memory at board power-on.

Table 1-25: **AC701 Board FPGA Configuration Modes**

Configuration Mode	SW13 DIP Switch Settings (M[2:0])	Bus Width	CCLK Direction
Master SPI flash memory	001	x1, x2, x4	Output
JTAG	101	x1	Not Applicable

See *7 Series FPGAs Configuration User Guide* (UG470) [Ref 6] for further details on configuring the 7 series FPGAs.

FPGA Mezzanine Card Interface

[Figure 1-2, callout 29]

The AC701 board supports the VITA 57.1 FPGA mezzanine card (FMC) specification by providing high pin count (HPC) connector J30. HPC J30 is keyed so that a the mezzanine card faces away from the AC701 board when connected.

Signaling speed ratings:

- Single-ended: 9 GHz (18 Gb/s)
- Differential optimal vertical: 9 GHz (18 Gb/s)
- Differential optimal horizontal: 16 GHz (32 Gb/s)
- High density vertical: 7 GHz (15 Gb/s)

The Samtec connector system is rated for signaling speeds up to 9 GHz (18 Gb/s) based on a –3 dB insertion loss point within a two-level signaling environment.

Connector type:

- Samtec SEAF series, 1.27 mm (0.050 in) pitch. Mates with SEAM series connector

For more information about SEAF series connectors, go to the Samtec website [Ref 19].

HPC Connector J30

[Figure 1-2, callout 29]

The 400-pin HPC connector defined by the FMC specification (Figure B-1) provides connectivity for up to:

- 160 single-ended or 80 differential user-defined signals
- 10 GTP transceivers
- 2 GTP transceiver clocks
- 4 differential clocks
- 159 ground and 15 power connections

The connections between the HPC connector at J30 and FPGA U1 (Table 1-26) implements a subset of this connectivity:

- 58 differential user defined pairs
  - 34 LA pairs (LA00-LA33)
  - 24 HA pairs (HA00-HA23)

- 4 GTP transceivers
- 2 GTP transceiver clocks
- 2 differential clocks
- 159 ground and 15 power connections

Note: The AC701 board VADJ voltage for HPC connector J30 is determined by the FMC VADJ power sequencing logic described in Power Management.

Table 1-26: **HPC Connections, J30 to FPGA U1**

J30 FMC1 HPC Pin	Schematic Net Name	I/O Standard	FPGA (U1) Pin	J30 FMC1 HPC Pin	Schematic Net Name	I/O Standard	FPGA (U1) Pin
A2	FMC1_HPC_DP1_M2C_P	(1)	AC14	B1	NC	NA	NA
A3	FMC1_HPC_DP1_M2C_N	(1)	AD14	B4	NC	NA	NA
A6	NC	NA	NA	B5	NC	NA	NA
A7	NC	NA	NA	B8	NC	NA	NA
A10	NC	NA	NA	B9	NC	NA	NA
A11	NC	NA	NA	B12	NC	NA	NA
A14	NC	NA	NA	B13	NC	NA	NA
A15	NC	NA	NA	B16	NC	NA	NA
A18	NC	NA	NA	B17	NC	NA	NA
A19	NC	NA	NA	B20	FMC1_HPC_GBTCLK1_M2C_P	NA	U4.27
A22	FMC1_HPC_DP1_C2M_P	(1)	AC8	B21	FMC1_HPC_GBTCLK1_M2C_N	NA	U4.25
A23	FMC1_HPC_DP1_C2M_N	(1)	AD8	B24	NC	NA	NA
A26	NC	NA	NA	B25	NC	NA	NA
A27	NC	NA	NA	B28	NC	NA	NA
A30	NC	NA	NA	B29	NC	NA	NA
A31	NC	NA	NA	B32	NC	NA	NA
A34	NC	NA	NA	B33	NC	NA	NA
A35	NC	NA	NA	B36	NC	NA	NA
A38	NC	NA	NA	B37	NC	NA	NA
A39	NC	NA	NA	B40	NC	NA	NA
C2	FMC1_HPC_DP0_C2M_P	(1)	AE9	D1	CTRL2_PWRGOOD	LVCMOS25	P15
C3	FMC1_HPC_DP0_C2M_N	(1)	AF9	D4	FMC1_HPC_GBTCLK0_M2C_P	NA	U3.27
C6	FMC1_HPC_DP0_M2C_P	(1)	AE13	D5	FMC1_HPC_GBTCLK0_M2C_N	NA	U3.25
C7	FMC1_HPC_DP0_M2C_N	(1)	AF13	D8	FMC1_HPC_LA01_CC_P	LVCMOS25	E17
C10	FMC1_HPC_LA06_P	LVCMOS25	G19	D9	FMC1_HPC_LA01_CC_N	LVCMOS25	E18
C11	FMC1_HPC_LA06_N	LVCMOS25	F20	D11	FMC1_HPC_LA05_P	LVCMOS25	G15
C14	FMC1_HPC_LA10_P	LVCMOS25	A17	D12	FMC1_HPC_LA05_N	LVCMOS25	F15
C15	FMC1_HPC_LA10_N	LVCMOS25	A18	D14	FMC1_HPC_LA09_P	LVCMOS25	E16
C18	FMC1_HPC_LA14_P	LVCMOS25	C21	D15	FMC1_HPC_LA09_N	LVCMOS25	D16
C19	FMC1_HPC_LA14_N	LVCMOS25	B21	D17	FMC1_HPC_LA13_P	LVCMOS25	B20

Table 1-26: **HPC Connections, J30 to FPGA U1 *(Cont'd)***

J30 FMC1 HPC Pin	Schematic Net Name	I/O Standard	FPGA (U1) Pin	J30 FMC1 HPC Pin	Schematic Net Name	I/O Standard	FPGA (U1) Pin
C22	FMC1_HPC_LA18_CC_P	LVCMOS25	G20	D18	FMC1_HPC_LA13_N	LVCMOS25	A20
C23	FMC1_HPC_LA18_CC_N	LVCMOS25	G21	D20	FMC1_HPC_LA17_CC_P	LVCMOS25	K21
C26	FMC1_HPC_LA27_P	LVCMOS25	F23	D21	FMC1_HPC_LA17_CC_N	LVCMOS25	J21
C27	FMC1_HPC_LA27_N	LVCMOS25	E23	D23	FMC1_HPC_LA23_P	LVCMOS25	K20
C30	FMC1_HPC_IIC_SCL	NA	U52.19	D24	FMC1_HPC_LA23_N	LVCMOS25	J20
C31	FMC1_HPC_IIC_SDA	NA	U52.20	D26	FMC1_HPC_LA26_P	LVCMOS25	J24
C34	GA0 = 0 = GND	NA	NA	D27	FMC1_HPC_LA26_N	LVCMOS25	H24
C35	VCC12_P	NA	NA	D29	FMC1_HPC_TCK_BUF	NA	U19.13
C37	VCC12_P	NA	NA	D30	FMC1_TDI_BUF	NA	U19.17
C39	VCC3V3	NA	NA	D31	FMC1_TDO_FPGA_TDI	NA	U19.2
				D32	VCC3V3	NA	NA
				D33	FMC1_HPC_TMS_BUF	NA	U19.15
				D34	NC	NA	NA
				D35	GA1 = 0 = GND	NA	NA
				D36	VCC3V3	NA	NA
				D38	VCC3V3	NA	NA
				D40	VCC3V3	NA	NA
E2	FMC1_HPC_HA01_CC_P	LVCMOS25	AB21	F1	FMC1_HPC_PG_M2C	LVCMOS25	N17
E3	FMC1_HPC_HA01_CC_N	LVCMOS25	AC21	F4	FMC1_HPC_HA00_CC_P	LVCMOS25	AA19
E6	FMC1_HPC_HA05_P	LVCMOS25	AD25	F5	FMC1_HPC_HA00_CC_N	LVCMOS25	AB19
E7	FMC1_HPC_HA05_N	LVCMOS25	AD26	F7	FMC1_HPC_HA04_P	LVCMOS25	AF24
E9	FMC1_HPC_HA09_P	LVCMOS25	AF19	F8	FMC1_HPC_HA04_N	LVCMOS25	AF25
E10	FMC1_HPC_HA09_N	LVCMOS25	AF20	F10	FMC1_HPC_HA08_P	LVCMOS25	AD21
E12	FMC1_HPC_HA13_P	LVCMOS25	AC18	F11	FMC1_HPC_HA08_N	LVCMOS25	AE21
E13	FMC1_HPC_HA13_N	LVCMOS25	AD18	F13	FMC1_HPC_HA12_P	LVCMOS25	AC19
E15	FMC1_HPC_HA16_P	LVCMOS25	AE17	F14	FMC1_HPC_HA12_N	LVCMOS25	AD19
E16	FMC1_HPC_HA16_N	LVCMOS25	AF17	F16	FMC1_HPC_HA15_P	LVCMOS25	Y18
E18	FMC1_HPC_HA20_P	LVCMOS25	Y16	F17	FMC1_HPC_HA15_N	LVCMOS25	AA18
E19	FMC1_HPC_HA20_N	LVCMOS25	Y17	F19	FMC1_HPC_HA19_P	LVCMOS25	AC17
E21	NC	NA	NA	F20	FMC1_HPC_HA19_N	LVCMOS25	AD17
E22	NC	NA	NA	F22	NC	NA	NA
E24	NC	NA	NA	F23	NC	NA	NA
E25	NC	NA	NA	F25	NC	NA	NA
E27	NC	NA	NA	F26	NC	NA	NA
E28	NC	NA	NA	F28	NC	NA	NA

Table 1-26: **HPC Connections, J30 to FPGA U1 *(Cont'd)***

J30 FMC1 HPC Pin	Schematic Net Name	I/O Standard	FPGA (U1) Pin	J30 FMC1 HPC Pin	Schematic Net Name	I/O Standard	FPGA (U1) Pin
E30	NC	NA	NA	F29	NC	NA	NA
E31	NC	NA	NA	F31	NC	NA	NA
E33	NC	NA	NA	F32	NC	NA	NA
E34	NC	NA	NA	F34	NC	NA	NA
E36	NC	NA	NA	F35	NC	NA	NA
E37	NC	NA	NA	F37	NC	NA	NA
E39	VCCO_VADJ	NA	NA	F38	NC	NA	NA
				F40	VCCO_VADJ	NA	NA
G2	FMC1_HPC_CLK1_M2C_P	LVCMOS25	H21	H1	NC	NA	NA
G3	FMC1_HPC_CLK1_M2C_N	LVCMOS25	H22	H2	FMC1_HPC_PRSNT_M2C_B	LVCMOS25	N16
G6	FMC1_HPC_LA00_CC_P	LVCMOS25	D18	H4	FMC1_HPC_CLK0_M2C_P	LVCMOS25	D19
G7	FMC1_HPC_LA00_CC_N	LVCMOS25	C18	H5	FMC1_HPC_CLK0_M2C_N	LVCMOS25	C19
G9	FMC1_HPC_LA03_P	LVCMOS25	G17	H7	FMC1_HPC_LA02_P	LVCMOS25	H14
G10	FMC1_HPC_LA03_N	LVCMOS25	F17	H8	FMC1_HPC_LA02_N	LVCMOS25	H15
G12	FMC1_HPC_LA08_P	LVCMOS25	C17	H10	FMC1_HPC_LA04_P	LVCMOS25	F18
G13	FMC1_HPC_LA08_N	LVCMOS25	B17	H11	FMC1_HPC_LA04_N	LVCMOS25	F19
G15	FMC1_HPC_LA12_P	LVCMOS25	E20	H13	FMC1_HPC_LA07_P	LVCMOS25	H16
G16	FMC1_HPC_LA12_N	LVCMOS25	D20	H14	FMC1_HPC_LA07_N	LVCMOS25	G16
G18	FMC1_HPC_LA16_P	LVCMOS25	E21	H16	FMC1_HPC_LA11_P	LVCMOS25	B19
G19	FMC1_HPC_LA16_N	LVCMOS25	D21	H17	FMC1_HPC_LA11_N	LVCMOS25	A19
G21	FMC1_HPC_LA20_P	LVCMOS25	M16	H19	FMC1_HPC_LA15_P	LVCMOS25	B22
G22	FMC1_HPC_LA20_N	LVCMOS25	M17	H20	FMC1_HPC_LA15_N	LVCMOS25	A22
G24	FMC1_HPC_LA22_P	LVCMOS25	L17	H22	FMC1_HPC_LA19_P	LVCMOS25	M14
G25	FMC1_HPC_LA22_N	LVCMOS25	L18	H23	FMC1_HPC_LA19_N	LVCMOS25	L14
G27	FMC1_HPC_LA25_P	LVCMOS25	G22	H25	FMC1_HPC_LA21_P	LVCMOS25	J19
G28	FMC1_HPC_LA25_N	LVCMOS25	F22	H26	FMC1_HPC_LA21_N	LVCMOS25	H19
G30	FMC1_HPC_LA29_P	LVCMOS25	G24	H28	FMC1_HPC_LA24_P	LVCMOS25	J18
G31	FMC1_HPC_LA29_N	LVCMOS25	F24	H29	FMC1_HPC_LA24_N	LVCMOS25	H18
G33	FMC1_HPC_LA31_P	LVCMOS25	E26	H31	FMC1_HPC_LA28_P	LVCMOS25	K22
G34	FMC1_HPC_LA31_N	LVCMOS25	D26	H32	FMC1_HPC_LA28_N	LVCMOS25	K23
G36	FMC1_HPC_LA33_P	LVCMOS25	G25	H34	FMC1_HPC_LA30_P	LVCMOS25	E25
G37	FMC1_HPC_LA33_N	LVCMOS25	F25	H35	FMC1_HPC_LA30_N	LVCMOS25	D25
G39	VCCO_VADJ	NA	NA	H37	FMC1_HPC_LA32_P	LVCMOS25	H26
				H38	FMC1_HPC_LA32_N	LVCMOS25	G26
				H40	VCCO_VADJ	NA	NA

Table 1-26: **HPC Connections, J30 to FPGA U1 *(Cont'd)***

J30 FMC1 HPC Pin	Schematic Net Name	I/O Standard	FPGA (U1) Pin	J30 FMC1 HPC Pin	Schematic Net Name	I/O Standard	FPGA (U1) Pin
J2	NC	NA	NA	K1	NC	NA	NA
J3	NC	NA	NA	K4	NC	NA	NA
J6	FMC1_HPC_HA03_P	LVCMOS25	AC22	K5	NC	NA	NA
J7	FMC1_HPC_HA03_N	LVCMOS25	AC23	K7	FMC1_HPC_HA02_P	LVCMOS25	AE25
J9	FMC1_HPC_HA07_P	LVCMOS25	AD23	K8	FMC1_HPC_HA02_N	LVCMOS25	AE26
J10	FMC1_HPC_HA07_N	LVCMOS25	AD24	K10	FMC1_HPC_HA06_P	LVCMOS25	AE23
J12	FMC1_HPC_HA11_P	LVCMOS25	AD20	K11	FMC1_HPC_HA06_N	LVCMOS25	AF23
J13	FMC1_HPC_HA11_N	LVCMOS25	AE20	K13	FMC1_HPC_HA10_P	LVCMOS25	AE22
J15	FMC1_HPC_HA14_P	LVCMOS25	AE18	K14	FMC1_HPC_HA10_N	LVCMOS25	AF22
J16	FMC1_HPC_HA14_N	LVCMOS25	AF18	K16	FMC1_HPC_HA17_CC_P	LVCMOS25	AA20
J18	FMC1_HPC_HA18_P	LVCMOS25	AA17	K17	FMC1_HPC_HA17_CC_N	LVCMOS25	AB20
J19	FMC1_HPC_HA18_N	LVCMOS25	AB17	K19	FMC1_HPC_HA21_P	LVCMOS25	AB16
J21	FMC1_HPC_HA22_P	LVCMOS25	Y15	K20	FMC1_HPC_HA21_N	LVCMOS25	AC16
J22	FMC1_HPC_HA22_N	LVCMOS25	AA15	K22	FMC1_HPC_HA23_P	LVCMOS25	W14
J24	NC	NA	NA	K23	FMC1_HPC_HA23_N	LVCMOS25	W15
J25	NC	NA	NA	K25	NC	NA	NA
J27	NC	NA	NA	K26	NC	NA	NA
J28	NC	NA	NA	K28	NC	NA	NA
J30	NC	NA	NA	K29	NC	NA	NA
J31	NC	NA	NA	K31	NC	NA	NA
J33	NC	NA	NA	K32	NC	NA	NA
J34	NC	NA	NA	K34	NC	NA	NA
J36	NC	NA	NA	K35	NC	NA	NA
J37	NC	NA	NA	K37	NC	NA	NA
J39	NC	NA	NA	K38	NC	NA	NA
				K40	NC	NA	NA

Notes:

1. No I/O standards are associated with MGT connections.

Power Management

[Figure 1-2, callout 30]

The AC701 board uses power regulators and PMBus compliant system controllers from Texas Instruments to supply core and auxiliary voltages. The Texas Instruments Fusion Digital Power GUI is used to monitor the voltage and current levels of the board power modules.

The AC701 board power distribution diagram is shown in Figure 1-42.

The pcb layout and power system design meets the recommended criteria described in the *7 Series FPGAs PCB Design and Pin Planning Guide* (UG483) [Ref 11].

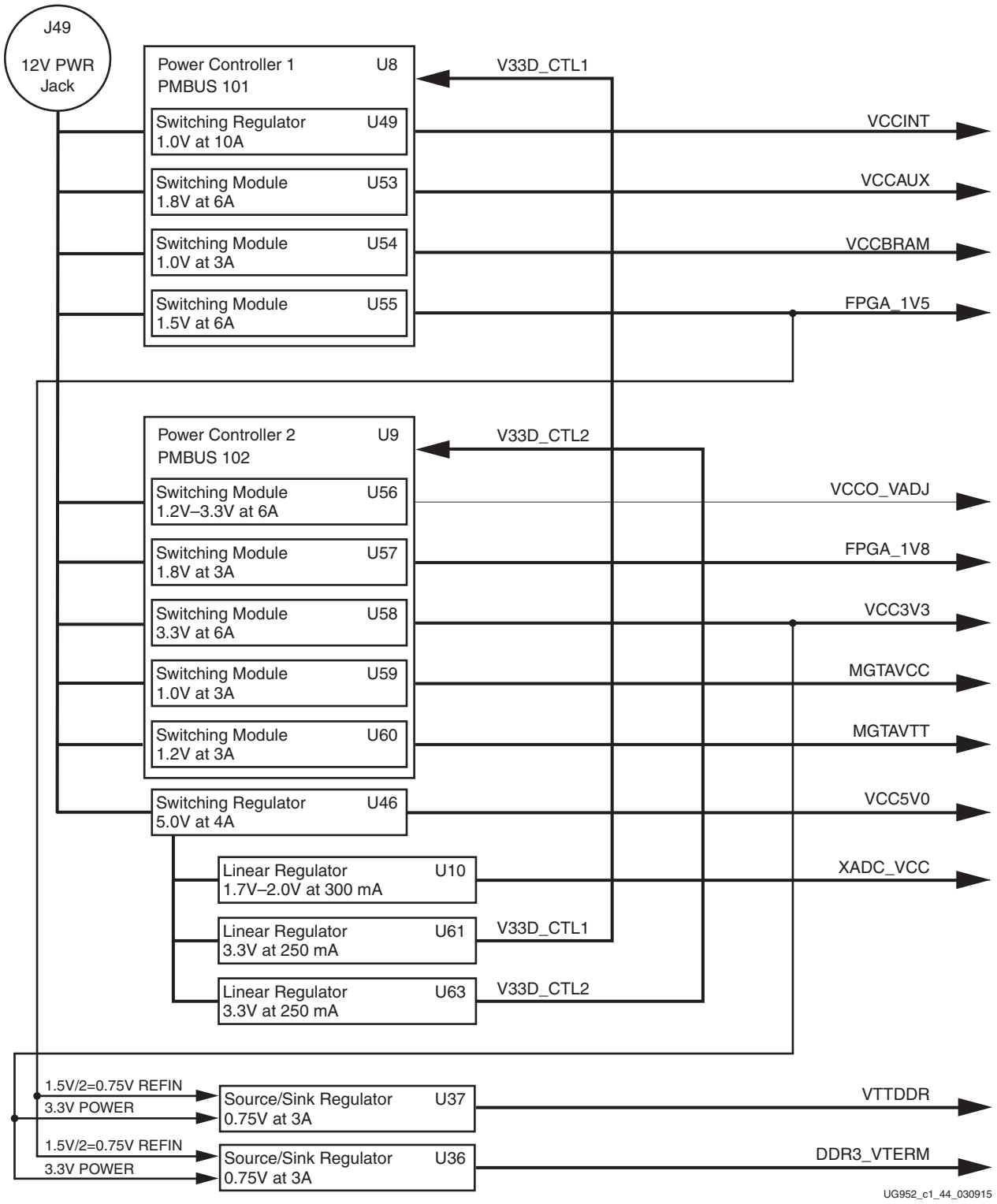


Figure 1-42: **AC701 Board Onboard Power Regulators**

The AC701 board core and auxiliary voltages are listed in Table 1-27.

Table 1-27: **AC701 Board Onboard Power System Devices**

Device Type	Reference Designator	Description	Power Rail Net Name	Power Rail Voltage	Schematic Page
UCD90120A[1] (4 Rails)	U8	PMBus controller - PMBus Addr = 101			39
LMZ31710RVQ[2]	U49	10A 0.6V–5.5V adjustable switching regulator	VCCINT	1.00V	40
LMZ31506RUQ[5]	U53	6A 0.6V–5.5V adjustable switching regulator	VCCAUX	1.80V	41
LMZ31503RUQ[6]	U54	3A 0.6V–5.5V adjustable switching regulator	VCCBRAM	1.00V	42
LMZ31506RUQ[5]	U55	6A 0.6V–5.5V adjustable switching regulator	FPGA_1V5	1.50V	43
UCD90120A[3] (5 Rails)	U9	PMBus controller - PMBus Addr = 102			45
LMZ31506RUQ[5]	U56	6A 0.6V–5.5V adjustable switching regulator	VCCO_VADJ	2.50V	46
LMZ31503RUQ[6]	U57	3A 0.6V–5.5V adjustable switching regulator	VCC1V8/ FPGA_1V8	1.80V	47
LMZ31506RUQ[5]	U58	6A 0.6V–5.5V adjustable switching regulator	VCC3V3/ FPGA_3V3	3.30V	48
LMZ31503RUQ[6]	U59	3A 0.6V–5.5V adjustable switching regulator	MGTAVCC	1.00V	49
LMZ31503RUQ[6]	U60	3A 0.6V–5.5V adjustable switching regulator	MGTAVTT	1.20V	50
LMZ31704RVQ[4]	U46	4A 0.6V–5.5V adjustable linear regulator	VCC5V0	5.00V	34
TL1963ADCQR	U62	1.5A 1.21V–5V adjustable LDO linear regulator	VCC2V5	2.50V	48
TPS51200DR	U37	3A source-sink DDR termination regulator	VTTDDR	0.75V	44
TPS51200DR	U36	3A source-sink DDR termination regulator	DDR3_VTERM_ R_0V75	0.75V	44
TPS79433DCQ	U61	0.25A 1.2V–5.5V adjustable LDO linear regulator	V33D_CTL1	3.30V	39
TPS79433DCQ	U63	0.25A 1.2V–5.5V adjustable LDO linear regulator	V33D_CTL2	3.30V	45
ADP123	U10	0.3A 0.8V–5V adjustable linear regulator	XADC_VCC	1.85V	29
REF3012	U35	50 uA fixed 1.25V voltage reference	XADC_VREF	1.25V	29

Notes:

1. See Table 1-28.
2. LMZ22010TZ U49 10A 0.8V–6V adjustable switching regulator on AC701 boards. previous to rev. 2.0. Previous board revisions are identified by an assembly number label affixed to each pre-rev 2.0 PCB, 0431747-xx.
3. See Table 1-29.
4. LMZ12002TZ U46 2A 0.8V–6V adjustable linear regulator on AC701 boards previous to rev. 2.0. Previous board revisions are identified by an assembly number label affixed to each pre-rev 2.0 PCB, 0431747-xx.
5. TPS84621RUQ adjustable linear regulator was on AC701 boards previous to board Rev. 2.0. Previous board revisions are identified by an assembly number label affixed to each pre-rev 2.0 PCB, 0431747-xx.
6. TPS84620RUQ adjustable linear regulator was on AC701 boards previous to board Rev. 2.0. Previous board revisions are identified by an assembly number label affixed to each pre-rev 2.0 PCB, 0431747-xx.

Monitoring Voltage and Current

Voltage and current monitoring and voltage control are available for the TI controlled power rails through the Texas Instruments Fusion Digital Power Designer GUI. The two onboard TI UCD90120A power controllers (U8 at PMBus address 101 and U9 at address 102) are wired to the same PMBus. The PMBus connector, J2, is provided for use with the TI USB Interface Adapter PMBus pod (TI part number EVM USB-TO-GPIO) and associated TI Fusion Digital Power Designer GUI. This is the simplest and most convenient way to monitor the voltage and current values for the power rail listed in Table 1-28 and Table 1-29. For more information, see Answer Record 54022.

In Table 1-28 and Table 1-29 (one per controller), the Power Good (PG) On Threshold is the set-point at or above which the particular rail is deemed good. The PG Off Threshold is the set-point at or below which the particular rail is no longer deemed good. The controller internally ORs these PG conditions together and drives an output PG pin High only if all active rail PG states are good. The on and off delay parameter values are relative to when the board power on-off slide switch SW15 is turned on and off.

Table 1-28 defines the voltage and current values for each power rail controlled by the UCD90120A U8 controller at PMBus Address 101.

Table 1-28: **Power Rail Specifications for UCD90120A PMBus Controller U8 at Address 101**

Rail		Nominal Voltage	Power Good On		Power Good Off		Turn On Delay (ms)	Turn Off Delay (ms)	Fault Shutdown Slaves	Rail Turn-on Dependencies	
										Rail	GPI
1	VINT_1V0	1.000	0.900	–10.0%	0.850	–15.0%	0.0	15.0	Rail #2,3,4	None	None
2	VAUX_1V8	1.800	1.620	–10.0%	1.530	–15.0%	10.0	5.0	Rail #1,3,4	Rail #3	None
3	VBRAM_1V0	1.000	0.900	–10.0%	0.850	–15.0%	5.0	10.0	Rail #1,2,4	Rail #1	None
4	FPGA_1V5	1.500	1.350	–10.0%	1.275	–15.0%	15.0	0.0	Rail #1,2,3	Rail #2	None

Table 1-29 defines the voltage and current values for each power rail controlled by the UCD90120A U9 controller at PMBus Address 102.

Table 1-29: **Power Rail Specifications for UCD90120A PMBus Controller U9 at Address 102**

Rail		Nominal Voltage	Power Good On		Power Good Off		Turn On Delay (ms)	Turn Off Delay (ms)	Fault Shutdown Slaves	Rail Turn-on Dependencies	
										Rail	GPI
1	VADJ_2V5	2.500	2.250	–10.0%	2.125	–15.0%	5.0	15.0	Rail #2,3,4,5	Rail #3	FMC_VADJ_ON_B
2	FPGA_1V8	1.800	1.620	–10.0%	1.530	–15.0%	10.0	10.0	Rail #1,3,4,5	None	None
3	FPGA_3V3	3.300	2.970	–10.0%	2.805	–15.0%	0.0	20.0	Rail #1,2,4,5	None	None
4	MGTVC_1V0	1.000	0.900	–10.0%	0.850	–15.0%	5.0	5.0	Rail #1,2,3,5	Rail #2	None
5	MGTVT_1V2	1.200	1.080	–10.0%	1.020	–15.0%	10.0	0.0	Rail #1,2,3,4	Rail #4	None

VCCO_VADJ Voltage Control

The FMC VCCO_VADJ rail is set to 2.5V. When the AC701 board is powered on, the state of the FMC_VADJ_ON_B signal wired to header J8 is sampled by the TI UCD90120A controller U9. If a jumper is installed on J8, signal FMC_VADJ_ON_B is held low, and TI controller U9 energizes the FMC VCCO_VADJ rail at power on.

Removing the jumper at J8 after the board is powered up does not affect the 2.5V power delivered to the VCCO_VADJ rail and it remains on.

A jumper installed at J8 is the default setting. If a jumper is not installed on J8 at power on, the signal FMC_VADJ_ON_B is High and the AC701 board does not energize the VCCO_VADJ 2.5V power.

Installing a jumper at J8 after the AC701 board powers up in this mode turns on the VCCO_VADJ rail.

In this VCCO_VADJ off mode, you can control when to turn on VCCO_VADJ and to what voltage level (1.8V, 2.5V or 3.3V).

With VCCO_VADJ off, the FPGA still configures and has access to the TI controller PMBus and the VADJ_ON_B signal which are wired to FPGA U1 Bank 14. The combination of these features allows you to develop code to command the VCCO_VADJ rail to be set to 1.8V or 3.3V instead of the default setting of 2.5V.

See AC701 board schematic page 46 for a brief discussion concerning selectable VCCO_VADJ voltages. The important controller-to-regulator circuit signals are VCCO_VADJ_EN and FMC_ADJ_SEL[1:0]. In the VCCO_VADJ off mode, controller U9 does not toggle the regulator turn-on signal VCCO_VADJ_EN High, so the U56 regulator stays off. You must re-program the controller U9 VCCO_VADJ rail settings to the desired VCCO_VADJ voltage so that the controller expects the new voltage to appear on its MON1 remote sense pin. The FMC_ADJ_SEL[1:0] controller GPIO16 and GPIO17 pins must be set to the correct logic levels to force the VCCO_VADJ regulator Reset MUX U64 to select the appropriate RT_CLK and VADJ resistors for the desired voltage as shown in Table 1-30.

Table 1-30: **VCCO_VADJ Voltage Selection**

FMC_ADJ_SEL[10]		VCCO_ADJ (V)
BIT 1	**BIT 0**	
0	0	2.5V
0	1	1.8V
1	0	3.3V
1	1	NOT USED

When the new VCCO_VADJ rail settings and Reset MUX logic levels are programmed into controller U9, the FMC_VADJ_ON_B signal can be driven Low by user FPGA logic and the controller toggles the VCCO_VADJ_EN signal High to allow the rail to come up at the new VCCO_VADJ voltage level.

Documentation describing PMBus programming for the UCD90120A controller is available at Texas Instruments [Ref 22].

Cooling Fan Control

Cooling fan RPM is controlled and monitored by user-created IP in the FPGA using the fan control circuit is shown in Figure 1-43.

FPGA U1 can be cooled by a user-supplied 12V DC fan connected to J61. $12V_{DC}$ is provided to the fan through J61 pin 2. The fan GND return is provided through J61 pin 1 and transistor Q17. Fan speed is controlled by a pulse-width-modulated signal from FPGA U1 pin J26 (on Bank 15) driving the gate of Q17. The default unprogrammed FPGA fan operation mode is ON. The fan speed tachometer signal on J61 pin 3 can be monitored on FPGA U1 pin J25 (on Bank 15).

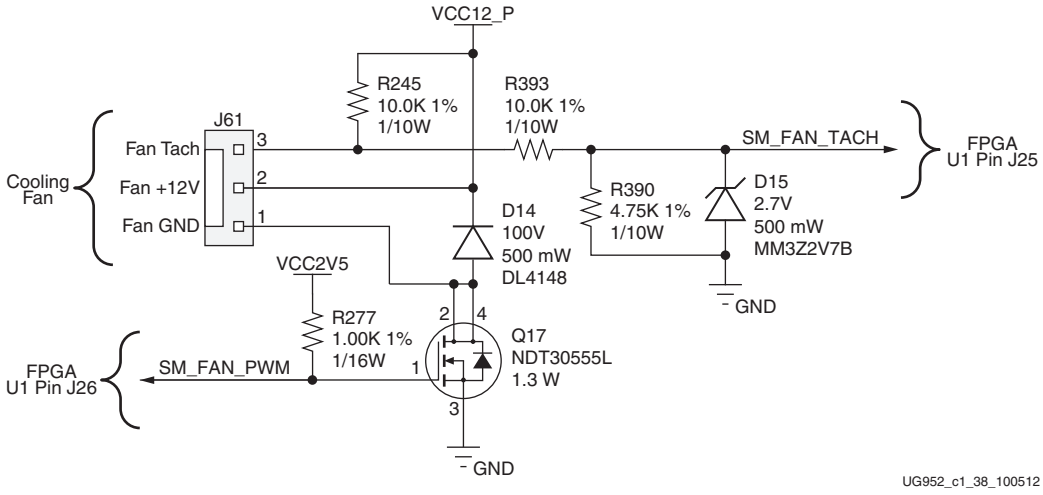


Figure 1-43: **FPGA Cooling Fan Circuit**

AC701 Board Power System

The AC701 board hosts a power system based on the Texas Instruments (TI) UCD90120A power supply sequencer and monitor, and the LMZ31500 and LMZ31700 family voltage regulators.

UCD90120A Description

The UCD90120A is a 12-rail PMBus/I2C addressable power-supply sequencer and monitor. The device integrates a 12-bit ADC for monitoring up to 12 power supply voltage inputs. Twenty-six GPIO pins can be used for power supply enables, power-on reset signals, external interrupts, cascading, or other system functions. 12 of these pins offer PWM functionality. Using these pins, the UCD90120A device offers support for margining and general-purpose PWM functions.

The UCD90120A device is configured by using the PC-based TI Fusion Digital Power Designer software. This software provides a graphical user interface (GUI) for configuring, storing, and monitoring power system operating parameters.

LMZ31500 Family Regulator Description

The LMZ31506RUQ (6A) and LMZ31503RUQ (3A) regulators are integrated synchronous buck switching regulators that combines a DC/DC converter with power MOSFETs, an inductor, and passives into low profile, BQFN packages. The LMZ3150x devices accept an input voltage rail between 4.5V and 14.5V and deliver an adjustable output voltage in the 0.6V to 5.5V range. This type of power solution allows as few as three external components and eliminates the loop compensation and magnetic parts selection process.

LMZ31700 Family Regulator Description

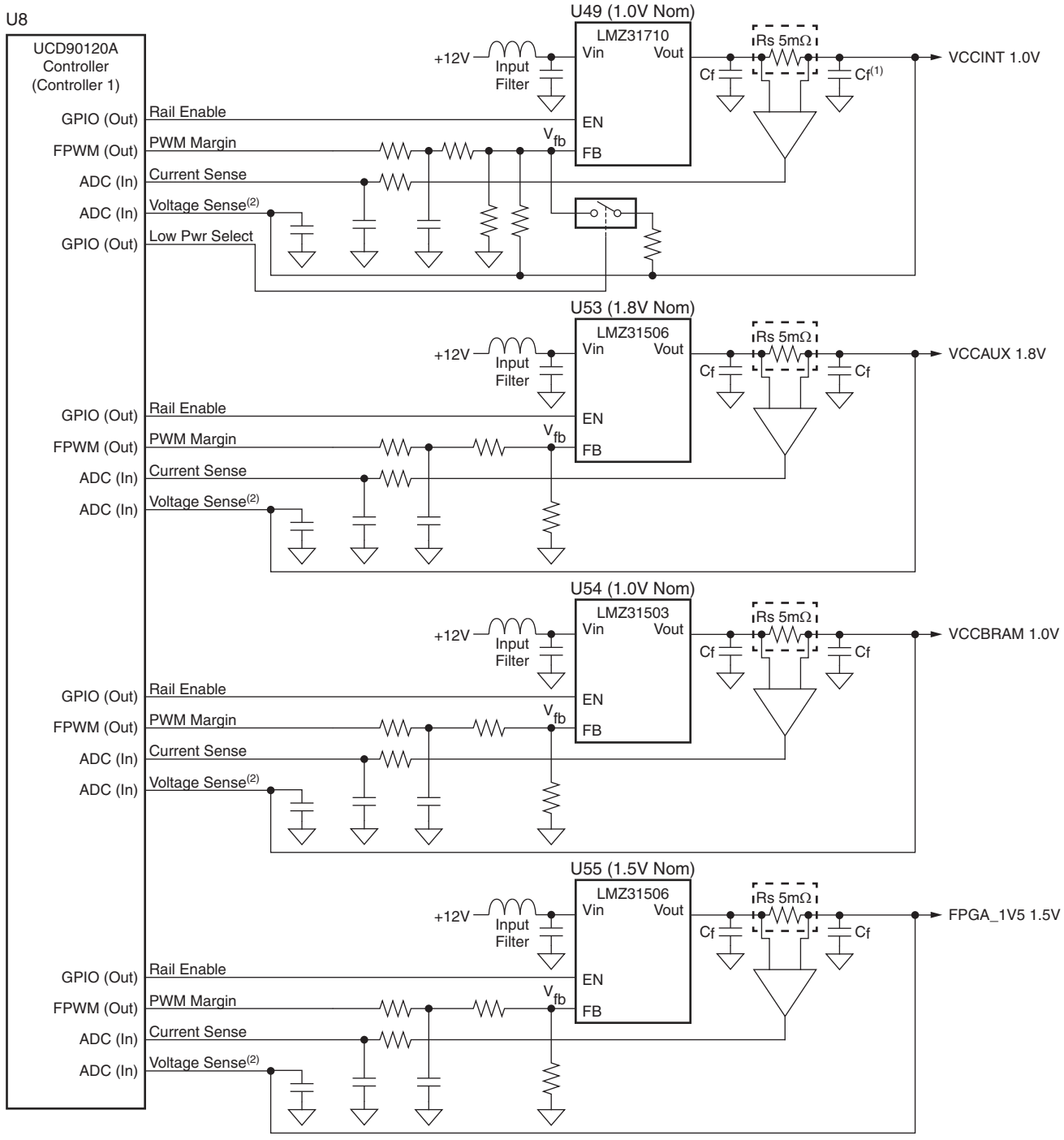
The LMZ31710 power module is a step-down DC-DC switching regulator capable of driving up to 10A load. The LMZ31710 can accept an input voltage rail between 4.5V and 17V, and deliver an adjustable and highly accurate output voltage as low as 0.6V. The LMZ31710 requires two external resistors and external capacitors to complete the design. The LMZ31710 is a reliable and robust design with these protection features: thermal shutdown, programmable input under-voltage lockout, output over-voltage protection, short-circuits protection, output current limit, and allows start -up into a pre-biased output. The sync input allows synchronization over the 200 kHz to 1200 kHz switching frequency range and up to six modules can be connected in parallel for higher load currents.

Table 1-31 shows the AC701 board power system configuration for controller U8.

Table 1-31: **Controller U8 Power System Configuration**

Sequencer	Schematic			Regulator Type	Voltage	Current
	Page	Contents	Net Name			
#1 U8 PMBus Addr 101, 4 Rails	39	UCD90120A #1				
	40	Addr 101, Rail 1	VCCINT	LMZ31710 (U49)	1.0V	10A
	41	Addr 101, Rail 2	VCCAUX	LMZ31506 (U53)	1.8V	6A
	42	Addr 101, Rail 3	VCCBRAM	LMZ31503 (U54)	1.0V	3A
	43	Addr 101, Rail 4	FPGA_1V5	LMZ31506 (U55)	1.5V	6A

Figure 1-44 shows the power system for UCD90120A U8 controller #1



Notes:

1. Capacitors labled Cf are bulk filter capacitors.
2. Voltage Sense is connected at point of load.

UG952_c1_41_030915

Figure 1-44: **U8 Controller #1 UCD90120A Power System**

Table 1-32 shows the AC701 TI power system configuration for controller U9.

Table 1-32: **Controller U9 Power System Configuration**

Sequencer	Schematic			Regulator Type	Voltage	Current
	Page	Page Contents	Net Name			
#2 U9 PMBus Addr 102, 5 rails	45	UCD90120A #2				
	46	Addr 102, Rail 1	VCCO_VADJ	LMZ31506 (U56)	2.5V	6A
	47	Addr 102, Rail 2	FPGA_1V8	LMZ31503 (U57)	1.8V	3A
	48	Addr 102, Rail 3	FPGA_3V3	LMZ31506 (U58)	3.3V	6A
	49	Addr 102, Rail 4	MGTAVCC	LMZ31503 (U59)	1.0V	3A
	50	Addr 102, Rail 5	MGTAVTT	LMZ31503 (U60)	1.2V	3A

Figure 1-45 shows the power system for UCD90120A U9 controller #2 rails 1 through 5.

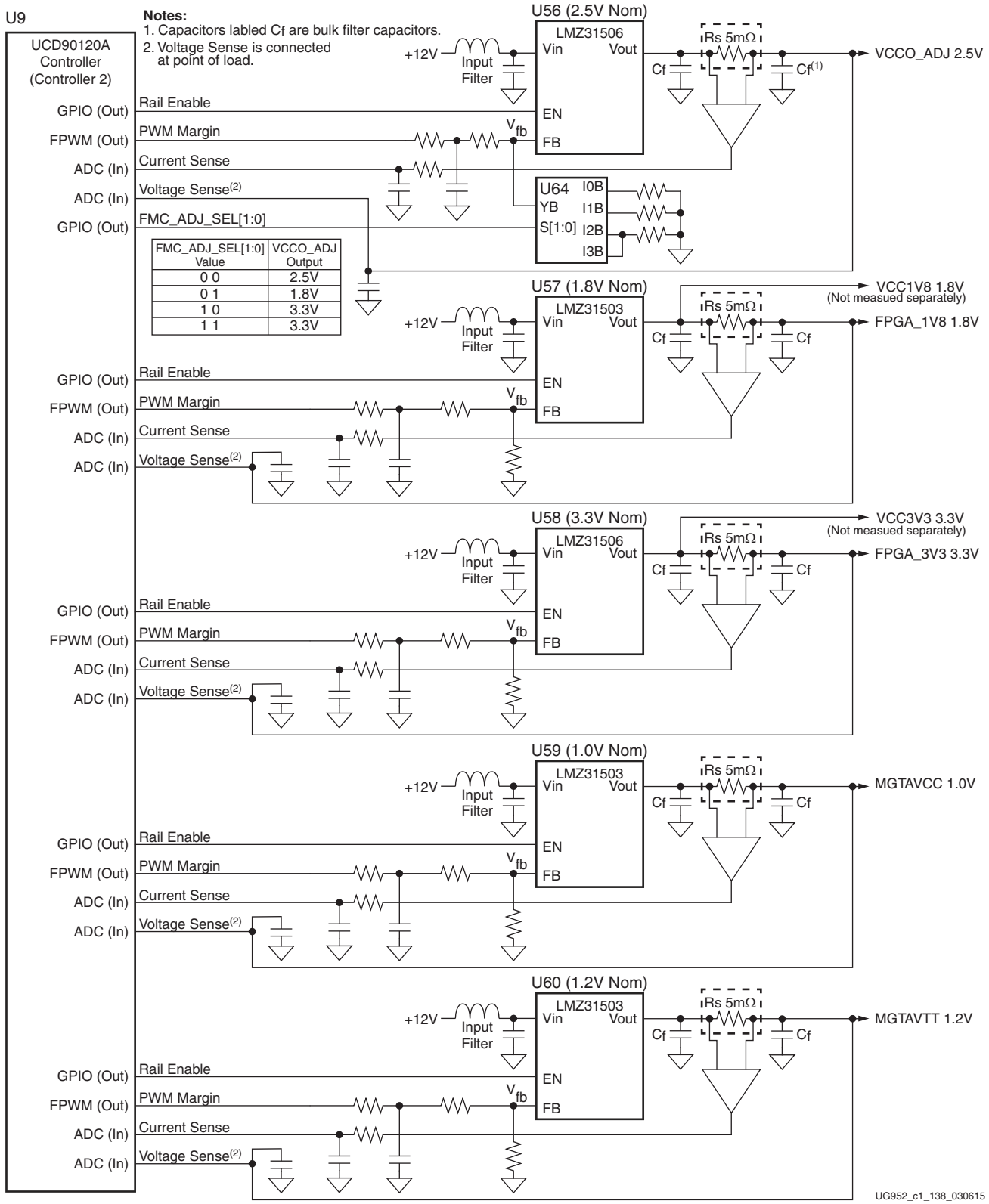


Figure 1-45: **U9 Controller #2 UCD90120A Power System**

The LMZ31503 and LMZ31700 family adjustable voltage regulators have their output voltage set by an external resistor. The regulator topology on the AC701 board permits the UCD90120A to monitor rail voltage and current. Voltage margining at +5% and -5% is also implemented.

Each voltage regulator external V_{OUT} setting resistor is calculated and implemented as if the regulator is standalone. The UCD90120A has two ADC inputs allocated per voltage rail, one input for the remote voltage sense connection, the other for the current sense resistor op amp output voltage connection. The UCD90120A ADC full scale input is 2.5V. The remote voltage feedback is scaled to approximately 2V if it exceeds 2V—that is, the VCCO_VADJ rail for the 2.5V and 3.3V modes, and the FPGA_3V3 rail also at 3.3V are resistor attenuated to scale the remotely sensed voltage at 0.606 to give approximately 2V at the ADC input pin for a 3.3V remote sense value. Rails below 2V are not scaled.

Each rail current sense op amp has its gain set to provide approximately 2V maximum at the TI UCD90120A ADC input pin when the rail current is at its expected maximum current level, as shown in Figure 1-44 (U8 controller #1) and Figure 1-45 (U9 controller #2).

The UCD90120A has an assignable group of GPIO pins with PWM capability. Each controller channel has a PWM GPIO pin connected to the associated voltage regulator V_{ADJ} pin. The external V_{OUT} setting resistor is also wired to this pin. The PWM GPIO pin is configured in 3-state mode. This pin is not driven unless a Margin command is executed. The Margin command is available within the TI Fusion Digital Power Designer software.

During the margin high or low operation, the PWM GPIO pin drives a voltage into the voltage regulator V_{ADJ} pin, which causes a slight voltage change resulting in the regulator V_{OUT} moving to the margin +5% or -5% voltage commanded.

XADC Power System Measurement

The AC701 board XADC interface includes power system voltage and current measuring capability. The V_{CCINT}, V_{CCAUX} and V_{CCBRAM} rail voltages are measured through the XADC internal voltage measurement capability. Other rails are measured through two external Analog Devices ADG707BRU multiplexers U14 and U13. Each rail has a TI INA333 op amp strapped across its series current sense resistor Kelvin terminals. This op amp has its gain adjusted to give approximately 1V at the expected full scale current value for the rail.

Figure 1-46 shows the XADC external multiplexer block diagram.

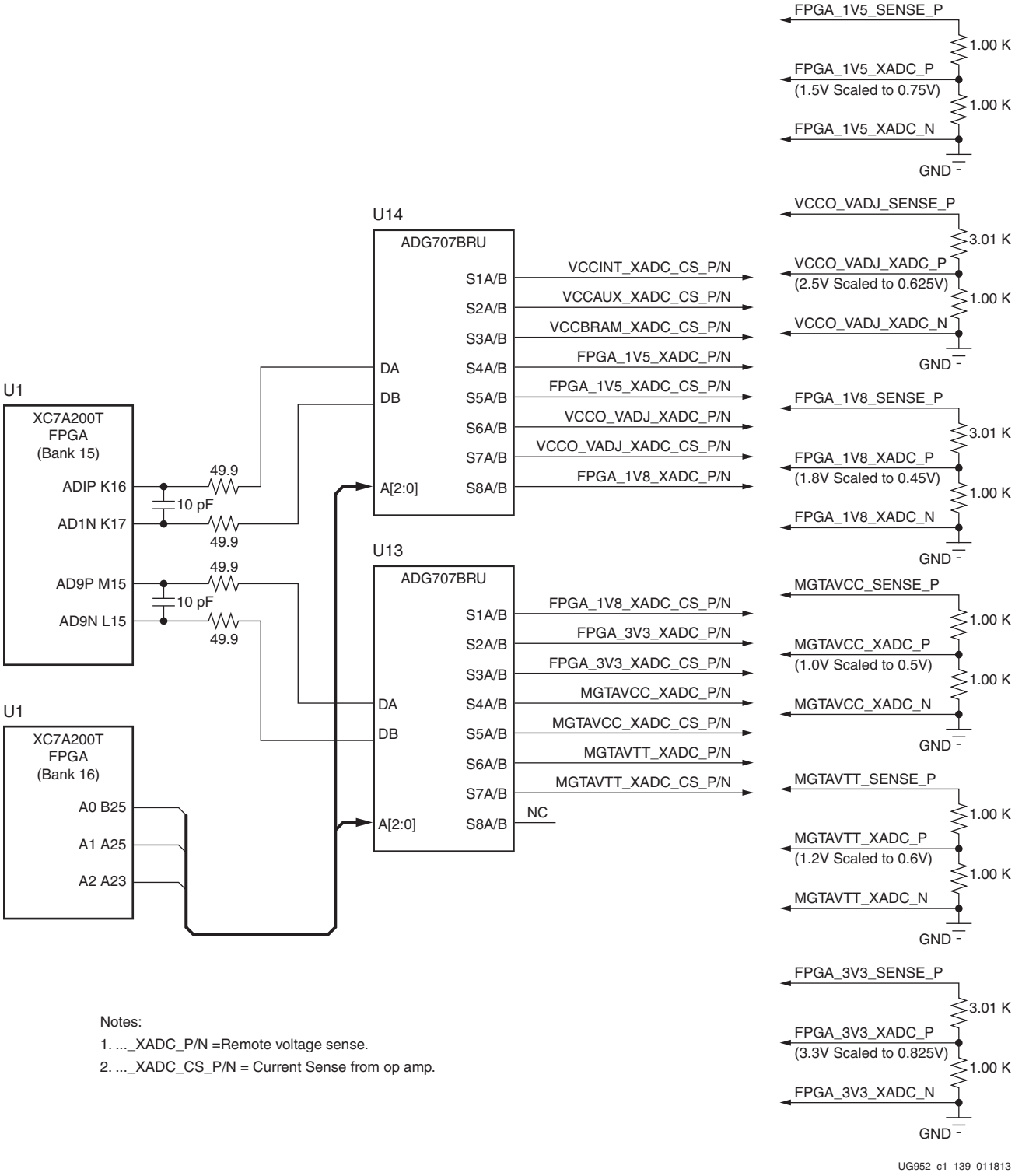


Figure 1-46: **XADC External Multiplexer Block Diagram**

Table 1-33 and Table 1-34 list the AC701 board XADC power system voltage and current measurement details for the external MUXes U14 and U13.

Table 1-33: **XADC Measurements through Mux U14**

Measurement Type	Rail Name	Current Range	I_{sense} Op Amp			Schematic Net Name	8-to-1 Multiplexer U14		MUX A[2:0]
			Reference Designator	Gain	V_o Range		Pin Number	Pin Name	
V	VCCINT	NA	NA	NA	NA	XADC INTERNAL	NA	NA	NA
I	VCCINT CS	0A-4A	U16	50	0V-0.996V	VCCINT_XADC_CS_P	19	S1A	000
						VCCINT_XADC_CS_N	11	S1B	
V	VCCAUX	NA	NA	NA	NA	XADC INTERNAL	NA	NA	NA
I	VCCAUX CS	0A-6A	U17	30	0V-0.913V	VCCAUX_XADC_CS_P	20	S2A	001
						VCCAUX_XADC_CS_N	10	S2B	
V	VCCBRAM	NA	NA	NA	NA	XADC INTERNAL	NA	NA	NA
I	VCCBRAM CS	0A-1.8A	U20	100	0V-0.909V	VCCBRAM_XADC_CS_P	21	S3A	010
						VCCBRAM_XADC_CS_N	9	S3B	
V	FPGA_1V5	NA	FPGA_1V5 remote sense divided to deliver 0.75V on FPGA_1V5_XADC_P			FPGA_1V5_XADC_P	22	S4A	011
						FPGA_1V5_SENSE_N	8	S4B	
I	FPGA_1V5 CS	0A-6A	U18	20	0V-0.604V	FPGA_1V5_XADC_CS_P	23	S5A	100
						FPGA_1V5_XADC_CS_N	7	S5B	
V	VCCO_VADJ	NA	VCCO_VADJ 2.5V remote sense divided to deliver 0.625V on FPGA_1V5_XADC_P			VCCO_VADJ_XADC_P	24	S6A	101
						VCCO_VADJ_SENSE_N	6	S6B	
I	VCCO_VADJ CS	0A-3.2A	U22	50	0V-0.796V	VCCO_VADJ_XADC_CS_P	25	S7A	110
						VCC0VADJ_XADC_CS_N	5	S7B	
V	FPGA_1V8	NA	FPGA_1V8 remote sense divided to deliver 0.45V on FPGA_1V8_XADC_P			FPGA_1V8_XADC_P	26	S8A	111
						FPGA_1V8_SENSE_N	4	S8B	

Table 1-34: **XADC Measurements through Mux U13**

Measurement Type	Rail Name	Current Range	I_{sense} Op Amp			Schematic Net Name	8-to-1 Multiplexer U14		MUX A[2:0]
			Reference Designator	Gain	V_o Range		Pin Number	Pin Name	
I	FPGA_1V8 CS	0A-3A	U21	50	0V-0.747V	FPGA_1V8_XADC_CS_P	19	S1A	000
						FPGA_1V8_XADC_CS_N	11	S1B	
V	FPGA_3V3 SENSE	NA	FPGA_3V3 remote sense divided to deliver 0.825V on FPGA_3V3_XADC_P			FPGA_3V3_XADC_P	20	S2A	001
						FPGA_3V3_SENSE_N	10	S2B	
I	FPGA_3V3 CS	0A-3.2A	U15	50	0V-0.796V	FPGA_3V3_XADC_CS_P	21	S3A	010
						FPGA_3V3_XADC_CS_N	9	S3B	
V	MGTAVCC SENSE	NA	MGTAVCC remote sense divided to deliver 0.5V on MGTAVCC_XADC_P			MGTAVCC_XADC_P	22	S4A	011
						MGTAVCC_SENSE_N	8	S4B	
I	MGTAVCC CS	0A-3A	U25	50	0V-0.747V	MGTAVCC_XADC_CS_P	23	S5A	100
						MGTAVCC_XADC_CS_N	7	S5B	
V	MGTAVTT SENSE	NA	MGTAVTT remote sense divided to deliver 0.6V on MGTAVTT_XADC_P			MGTAVTT_XADC_P	24	S6A	101
						MGTAVTT_SENSE_N	6	S6B	

Table 1-34: **XADC Measurements through Mux U13 *(Cont'd)***

Measurement Type	Rail Name	Current Range	I_{sense} Op Amp			Schematic Net Name	8-to-1 Multiplexer U14		MUX A[2:0]
			Reference Designator	Gain	V_o Range		Pin Number	Pin Name	
I	MGTAVTT CS	0A-1.5A	U23	100	0V-0.756V	MGTAVTT_XADC_CS_P	25	S7A	110
						MGTAVTT_XADC_CS_N	5	S7B	
Not used, not connected						Not connected	26	S8A	111
						Not connected	4	S8B	

XADC Header

[Figure 1-2, callout 31]

7 series FPGAs provide an Analog Front End (XADC) block. The XADC block includes a dual 12-bit, 1 MSPS Analog-to-Digital Convertor (ADC) and on-chip sensors. See *7 Series FPGAs XADC Dual 12-Bit 1MSPS Analog-to-Digital Converter User Guide* (UG480) [Ref 10] for details on the capabilities of the analog front end. Figure 1-47 shows the AC701 board XADC support features.

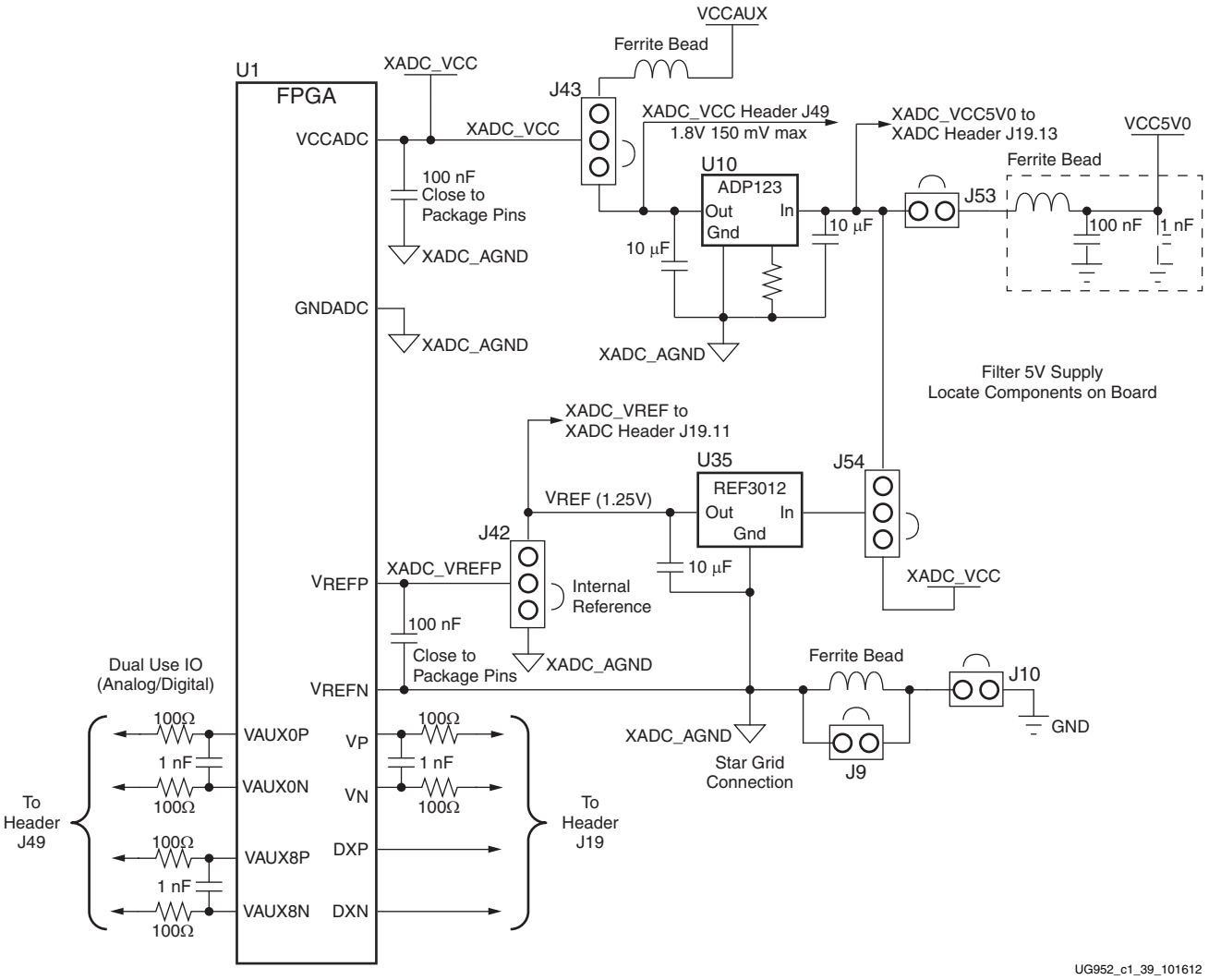


Figure 1-47: **Header XADC_VREF Voltage Source Options**

The AC701 board supports both the internal FPGA sensor measurements and the external measurement capabilities of the XADC. Internal measurements of the die temperature, V_{CCINT}, V_{CCAUX}, and V_{CCBRAM} are available. The AC701 board V_{CCINT} and V_{CCBRAM} are provided by a common 1.0V supply.

Jumper J42 can be used to select either an external differential voltage reference (XADC_VREF) or on-chip voltage reference (jumper J42 2–3) for the analog-to-digital converter.

For external measurements, an XADC header (J19) is provided. This header can be used to provide analog inputs to the FPGA dedicated VP/VN channel, and to the VAUXP[0]/VAUXN[0], VAUXP[8]/VAUXN[8] auxiliary analog input channels. Simultaneous sampling of Channel 0 and Channel 8 is supported.

A user-provided analog signal multiplexer card can be used to sample additional external analog inputs using the four GPIO pins available on the XADC header as multiplexer address lines. Figure 1-48 shows the XADC header J19 connections.

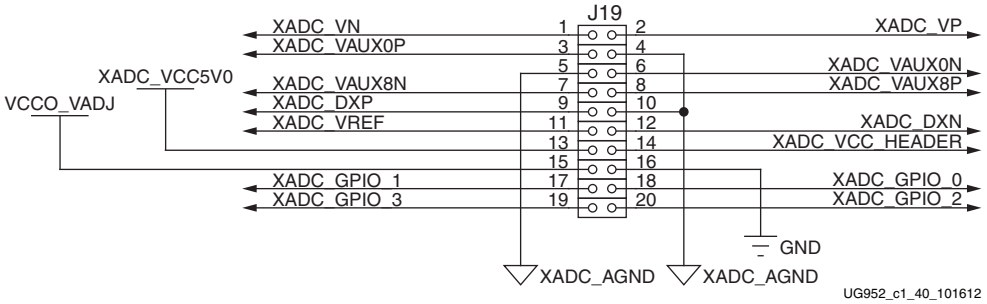


Figure 1-48: **XADC header (J19)**

Table 1-35 describes the XADC header J19 pin functions.

Table 1-35: **XADC Header J19 Pinout**

Net Name	J19 Pin Number	Description
XADC_VN, _VP	1, 2	Dedicated analog input channel for the XADC.
XADC_VAUX0P, N	3, 6	Auxiliary analog input channel 0. Also supports use as I/O inputs when anti alias capacitor is not present.
XADC_VAUX8N, P	7, 8	Auxiliary analog input channel 8. Also supports use as I/O inputs when anti alias capacitor is not present.
DXP, DXN	9, 12	Access to thermal diode.
XADC_AGND	4, 5, 10	Analog ground reference.
XADC_VREF	11	1.25V reference from the board.
XADC_VCC5V0	13	Filtered 5V supply from board.
XADC_VCC_HEADER	14	Analog 1.8V supply for XADC.
VCCO_VADJ	15	V_{CCO} supply for bank which is the source of DIO pins.
GND	16	Digital ground (board) reference
XADC_GPIO_3, 2, 1, 0	19, 20, 17, 18	Digital I/O. These pins come from FPGA U1 banks 15 and 16 (V_{CCO} = VCCO_VADJ). The XDC constraints file I/O standard is default LVCMOS25, assuming VCCO_VADJ = 2.5V. If VCCO_VADJ is changed from 2.5V to 1.8V or 3.3V, the ADC file I/O standard for these nets needs to be changed to match.

Configuration Options

The FPGA on the AC701 board can be configured using these methods:

- Master SPI flash memory (uses the Quad SPI flash memory U7).
- JTAG (uses the U26 Digilent USB-to-JTAG bridge or J4 download cable connector).

See USB JTAG Module for more information.

See *7 Series FPGAs XADC Dual 12-Bit 1MSPS Analog-to-Digital Converter User Guide* (UG480) [Ref 10] for further details on configuration modes.

The method used to configure the FPGA is controlled by the mode pins (M2, M1, M0) setting selected through DIP switch SW1. Table 1-36 lists the supported mode switch settings.

Table 1-36: **Mode Switch SW1 Settings**

Configuration Mode	Mode Pins (M[2:0])	Bus Width	CCLK Direction
Master SPI flash memory	001	x1, x2, x4	Output
JTAG	101	x1	Not applicable

Figure 1-49 shows mode switch SW1.

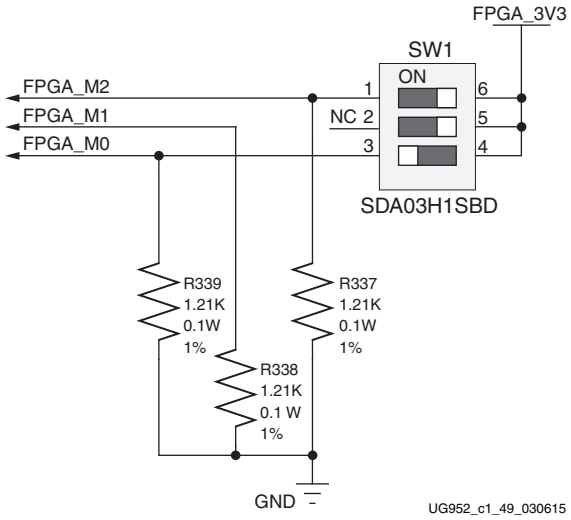


Figure 1-49: **Mode Switch**

Figure 1-50 shows the Quad SPI flash memory U7 configuration circuit.

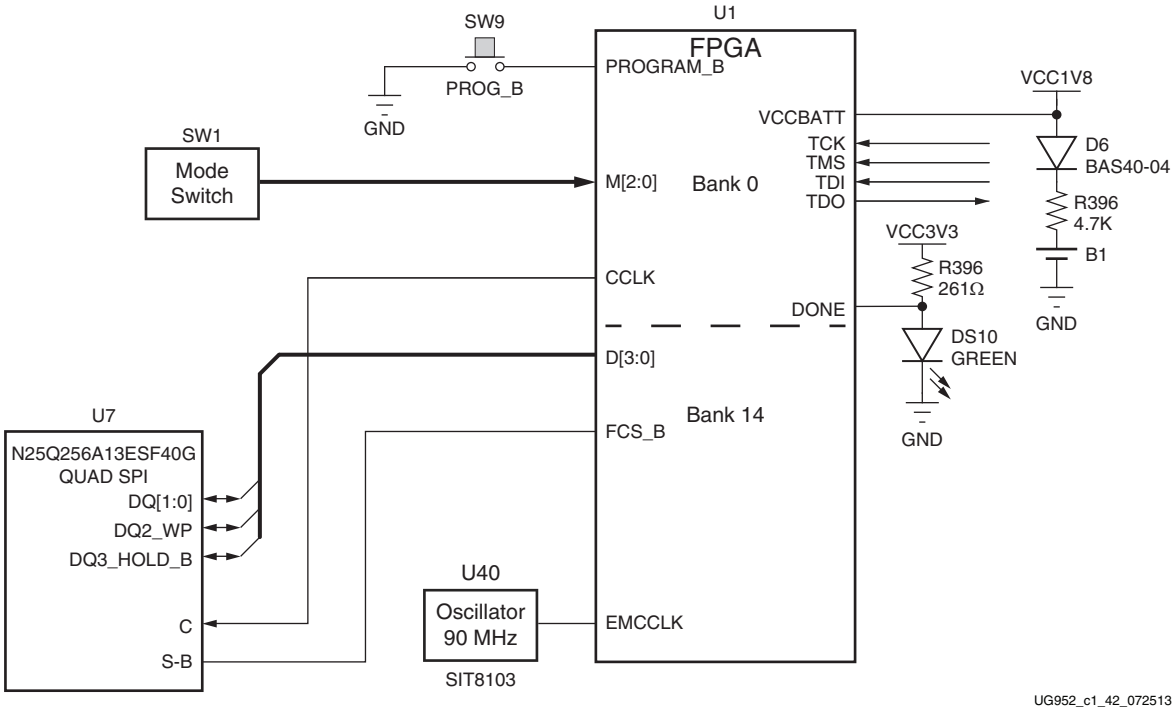


Figure 1-50: **AC701 Board Quad SPI Flash Memory Configuration Circuit**

Appendix A

Default Switch and Jumper Settings

User GPIO DIP Switch SW2

See Figure 1-2 callout 23 for location of SW2. Default settings are shown in Figure A-1 and details are listed in Table A-1.

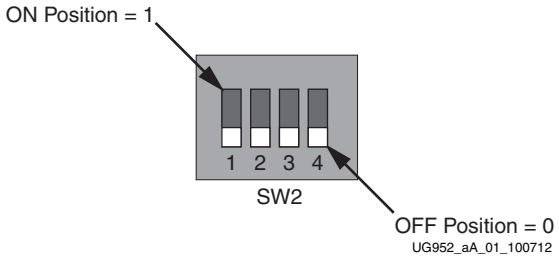


Figure A-1: **SW2 Default Settings**

Table A-1: **SW2 Default Switch Settings**

Position	Function	Default
1	GPIO_DIP_SW0	OFF
2	GPIO_DIP_SW1	OFF
3	GPIO_DIP_SW2	OFF
4	GPIO_DIP_SW3	OFF

Configuration DIP Switch SW1

See Figure 1-2 callout 28 for location of SW1. Default settings are shown in Figure A-2 and details are listed in Table A-2.

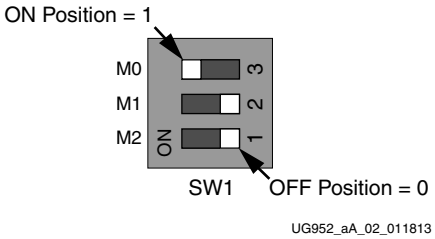


Figure A-2: **SW1 Default Settings**

The default mode setting M[2:0] = `001` selects Master SPI flash memory configuration at board power-on.

Table A-2: **SW1 Default Switch Settings**

Position	Function		Default
1	FPGA_M2	M2	OFF
2	FPGA_M1	M1	OFF
3	FPGA_M0	M0	ON

Default Jumper Settings

The AC701 board default jumper configurations are listed in Table A-3. The AC701 board jumper header locations are shown in Figure A-3.

Table A-3: **AC701 Default Jumper Settings**

Callout	Header Ref Des	Jumper Position	Description	Schematic 0381502 Page
2-pin				
1	J3	None	SPI SELECT = onboard SPI flash memory device	4
2	J5	1-2	EPHY U12.2 CONFIG2 = LOW	15
3	J6	1-2	P3 SFP+ TX enabled	20
4	J8	1-2	VCCO_VADJ (FMC) voltage = ON	45
5	J9	1-2	U35 REF3012 XADC_AGND L3 bypassed	29
6	J10	1-2	U35 REF3012 XADC_AGND = GND	29
7	J11	1-2	XADC V_{CCINT} 4A range	34
8	J52	None	J52.1 INIT_B, J51.2 DONE test header, not a jumper	7
9	J53	1-2	XADC_VCC5V0 = 5V	29
10	J63	None	Voltage regulators enabled	38
3-pin				
11	J35	1-2	EPHY U12.3 CONFIG3 = HI	15
12	J36	None	EPHY U12.2 CONFIG2 option header	15
13	J37	None	EPHY U12.3 CONFIG3 option header	15
14	J38	1-2	SFP RX BW = FULL	20
15	J39	1-2	SFP TX BW = FULL	20
16	J42	1-2	XADC_VREFP = REF3012 XADC_VREF	29
17	J43	2-3	XADC_VCC = ADP123 1.85V	29
18	J54	2-3	REF3012 V_{IN} = XADC_VCC	29
2x2				
19	J12	3-4	PCIE lane width = 4	28

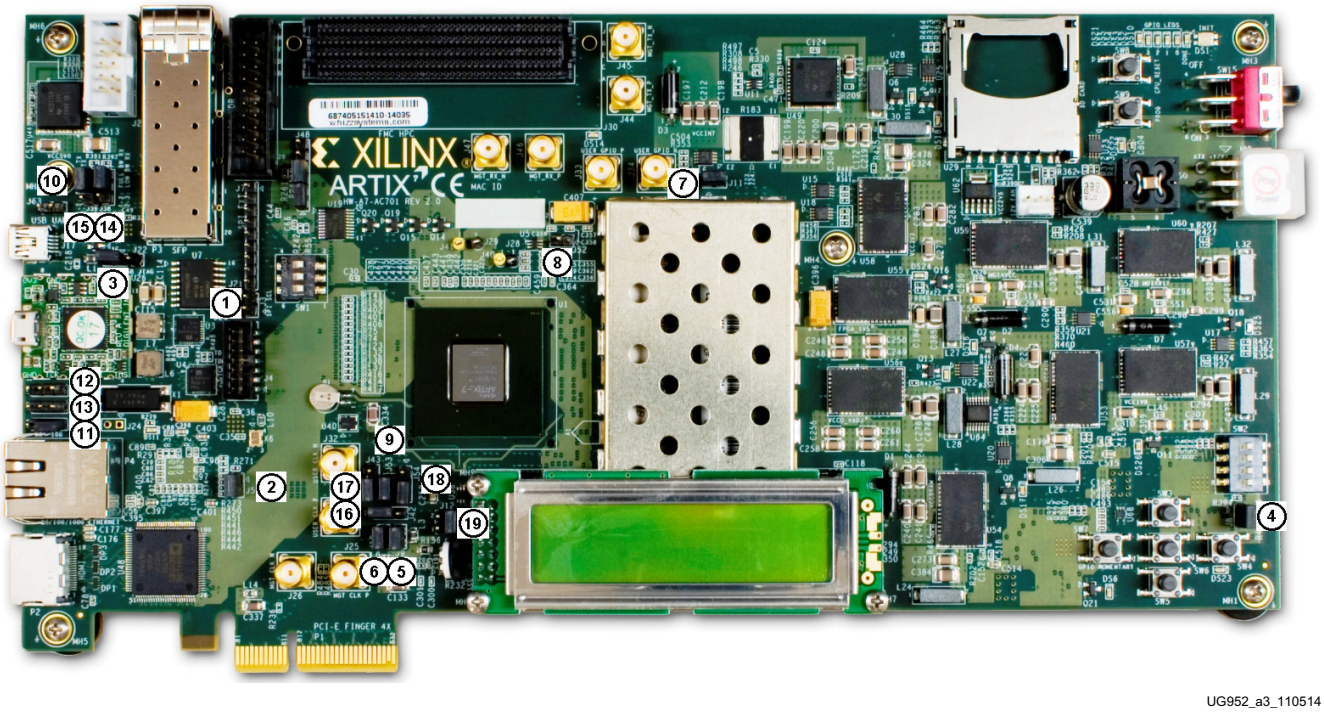


Figure A-3: **AC701 Board Components (Rev. 2.0)**

VITA 57.1 FMC Connector Pinouts

Figure B-1 shows the pinout of the FPGA mezzanine card (FMC) high pin count (HPC) connector defined by the VITA 57.1 FMC specification. For a description of how the AC701 board implements the FMC specification, see FPGA Mezzanine Card Interface and HPC Connector J30.

	K	J	H	G	F	E	D	C	B	A
1	VREF_B_M2C	GND	VREF_A_M2C	GND	PG_M2C	GND	PG_C2M	GND	RES1	GND
2	GND	CLK3_M2C_P	PRSNT_M2C_L	CLK1_M2C_P	GND	HA01_P_CC	GND	DP0_C2M_P	GND	DP1_M2C_P
3	GND	CLK3_M2C_N	GND	CLK1_M2C_N	GND	HA01_N_CC	GND	DP0_C2M_N	GND	DP1_M2C_N
4	CLK2_M2C_P	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	GBTCLK0_M2C_P	GND	DP9_M2C_P	GND
5	CLK2_M2C_N	GND	CLK0_M2C_N	GND	HA00_N_CC	GND	GBTCLK0_M2C_N	GND	DP9_M2C_N	GND
6	GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	DP0_M2C_P	GND	DP2_M2C_P
7	HA02_P	HA03_N	LA02_P	LA00_N_CC	HA04_P	HA05_N	GND	DP0_M2C_N	GND	DP2_M2C_N
8	HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_P_CC	GND	DP8_M2C_P	GND
9	GND	HA07_P	GND	LA03_P	GND	HA09_P	LA01_N_CC	GND	DP8_M2C_N	GND
10	HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA06_P	GND	DP3_M2C_P
11	HA06_N	GND	LA04_N	GND	HA08_N	GND	LA05_P	LA06_N	GND	DP3_M2C_N
12	GND	HA11_P	GND	LA08_P	GND	HA13_P	LA05_N	GND	DP7_M2C_P	GND
13	HA10_P	HA11_N	LA07_P	LA08_N	HA12_P	HA13_N	GND	GND	DP7_M2C_N	GND
14	HA10_N	GND	LA07_N	GND	HA12_N	GND	LA09_P	LA10_P	GND	DP4_M2C_P
15	GND	HA14_P	GND	LA12_P	GND	HA16_P	LA09_N	LA10_N	GND	DP4_M2C_N
16	HA17_P_CC	HA14_N	LA11_P	LA12_N	HA15_P	HA16_N	GND	GND	DP6_M2C_P	GND
17	HA17_N_CC	GND	LA11_N	GND	HA15_N	GND	LA13_P	GND	DP6_M2C_N	GND
18	GND	HA18_P	GND	LA16_P	GND	HA20_P	LA13_N	LA14_P	GND	DP5_M2C_P
19	HA21_P	HA18_N	LA15_P	LA16_N	HA19_P	HA20_N	GND	LA14_N	GND	DP5_M2C_N
20	HA21_N	GND	LA15_N	GND	HA19_N	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND
21	GND	HA22_P	GND	LA20_P	GND	HB03_P	LA17_N_CC	GND	GBTCLK1_M2C_N	GND
22	HA23_P	HA22_N	LA19_P	LA20_N	HB02_P	HB03_N	GND	LA18_P_CC	GND	DP1_C2M_P
23	HA23_N	GND	LA19_N	GND	HB02_N	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N
24	GND	HB01_P	GND	LA22_P	GND	HB05_P	LA23_N	GND	DP9_C2M_P	GND
25	HB00_P_CC	HB01_N	LA21_P	LA22_N	HB04_P	HB05_N	GND	GND	DP9_C2M_N	GND
26	HB00_N_CC	GND	LA21_N	GND	HB04_N	GND	LA26_P	LA27_P	GND	DP2_C2M_P
27	GND	HB07_P	GND	LA25_P	GND	HB09_P	LA26_N	LA27_N	GND	DP2_C2M_N
28	HB06_P_CC	HB07_N	LA24_P	LA25_N	HB08_P	HB09_N	GND	GND	DP8_C2M_P	GND
29	HB06_N_CC	GND	LA24_N	GND	HB08_N	GND	TCK	GND	DP8_C2M_N	GND
30	GND	HB11_P	GND	LA29_P	GND	HB13_P	TDI	SCL	GND	DP3_C2M_P
31	HB10_P	HB11_N	LA28_P	LA29_N	HB12_P	HB13_N	TDO	SDA	GND	DP3_C2M_N
32	HB10_N	GND	LA28_N	GND	HB12_N	GND	3P3VAUX	GND	DP7_C2M_P	GND
33	GND	HB15_P	GND	LA31_P	GND	HB19_P	TMS	GND	DP7_C2M_N	GND
34	HB14_P	HB15_N	LA30_P	LA31_N	HB16_P	HB19_N	TRST_L	GA0	GND	DP4_C2M_P
35	HB14_N	GND	LA30_N	GND	HB16_N	GND	GA1	12P0V	GND	DP4_C2M_N
36	GND	HB18_P	GND	LA33_P	GND	HB21_P	3P3V	GND	DP6_C2M_P	GND
37	HB17_P_CC	HB18_N	LA32_P	LA33_N	HB20_P	HB21_N	GND	12P0V	DP6_C2M_N	GND
38	HB17_N_CC	GND	LA32_N	GND	HB20_N	GND	3P3V	GND	GND	DP5_C2M_P
39	GND	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N
40	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	RES0	GND

UG952_aB_01_101612

Figure B-1: **FMC HPC Connector Pinout**

Appendix C

Xilinx Design Constraints

The AC701 board Xilinx Design Constraints (XDC) file template provides for designs targeting the AC701 board. Net names in the constraints correlate with net names on the AC701 board schematic. You must identify the appropriate pins and replace the net names in this list with net names in the user RTL. For more information, see *Vivado Design Suite User Guide, Using Constraints* (UG903) [Ref 12].

The FMC HPC connector J30 is connected to a 2.5V V_{CCO} bank. Because each user FMC card implements customer-specific circuitry, the FMC bank I/O standards must be uniquely defined by each customer.

Refer to the Board Files area under the Documentation tab on the Virtex-7 FPGA AC701 Evaluation Kit product page for the latest constraints file.

Board Setup

Installing the AC701 Board in a PC Chassis

Installation of the AC701 board inside a computer chassis is required when developing or testing PCI Express® functionality.

When the AC701 board is used inside a computer chassis (that is, plugged in to the PCIe® slot), power is provided from the ATX power supply 4-pin peripheral connector through the ATX adapter cable shown in Figure D-1 to J49 on the AC701 board. The Xilinx part number for this cable is 2600304.

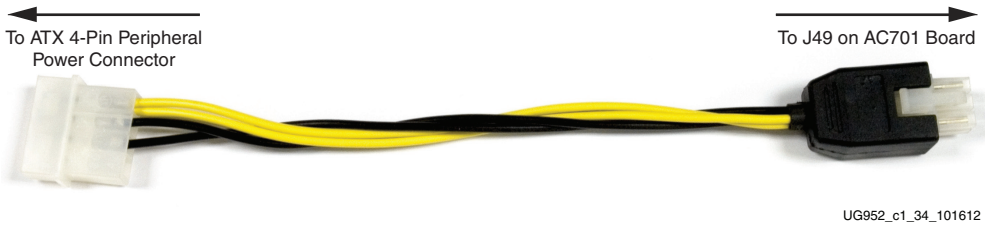


Figure D-1: **ATX Power Supply Adapter Cable**

To install the AC701 board in a PC chassis:

1. On the AC701 board, remove all six rubber feet, the standoffs, and the PCIe bracket. The standoffs and feet are affixed to the board by screws on the top side of the board. Remove all six screws. Reinstall the PCIe bracket using two of the screws.
2. Power down the host computer and remove the power cord from the PC.
3. Open the PC chassis following the instructions provided with the PC.
4. Select a vacant PCIe expansion slot and remove the expansion cover (at the back of the chassis) by removing the screws on the top and bottom of the cover.
5. Plug the AC701 board into the PCIe connector at this slot.
6. Install the top mounting bracket screw into the PC expansion cover retainer bracket to secure the AC701 board in its slot.

   Note: The AC701 board is taller than standard PCIe cards. Ensure that the height of the card is free of obstructions.
7. Connect the ATX power supply to the AC701 board using the ATX power supply adapter cable as shown in Figure D-1:
   a. Plug the 6-pin 2 x 3 Molex connector on the adapter cable into J49 on the AC701 board.
   b. Plug the 4-pin 1 x 4 peripheral power connector from the ATX power supply into the 4-pin adapter cable connector.

8. Slide the AC701 board power switch SW15 to the ON position. The PC can now be powered on.

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Appendix E

Board Specifications

Dimensions

Height 5.5 in. (14.0 cm)

Length 10.5 in. (26.7 cm)

Note: The AC701 board height exceeds the standard 4.376 in. (11.15 cm) height of a PCI Express card.

Environmental

Temperature

Operating: 0°C to +45°C

Storage: –25°C to +60°C

Humidity

10% to 90% non-condensing

Operating Voltage

+12 V_{DC}

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Appendix F

Regulatory and Compliance Information

Overview

This product is designed and tested to conform to the European Union directives and standards described in this section.

Refer to the Artix-7 FPGA AC701 Evaluation Kit Master Answer Record concerning the CE requirements for the PC test environment.

The Artix-7 FPGA AC701 Declaration of Conformity is online.

CE Directives

2006/95/EC, *Low Voltage Directive (LVD)*

2004/108/EC, *Electromagnetic Compatibility (EMC) Directive*

CE Standards

EN standards are maintained by the European Committee for Electrotechnical Standardization (CENELEC). IEC standards are maintained by the International Electrotechnical Commission (IEC).

Electromagnetic Compatibility

EN 55022:2010, *Information Technology Equipment Radio Disturbance Characteristics – Limits and Methods of Measurement*

EN 55024:2010, *Information Technology Equipment Immunity Characteristics – Limits and Methods of Measurement*

Note: This is a Class A product and can cause radio interference. In a domestic environment, the user might be required to take adequate corrective measures.

Safety

IEC 60950-1:2005, *Information technology equipment – Safety, Part 1: General requirements*

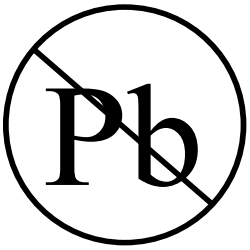
EN 60950-1:2006, *Information technology equipment – Safety, Part 1: General requirements*

Markings

In August of 2005, the European Union (EU) implemented the EU WEEE Directive 2002/96/EC and later the WEEE Recast Directive 2012/19/EU requiring Producers of electronic and electrical equipment (EEE) to manage and finance the collection, reuse, recycling and to appropriately treat WEEE that the Producer places on the EU market after August 13, 2005. The goal of this directive is to minimize the volume of electrical and electronic waste disposal and to encourage re-use and recycling at the end of life.

Xilinx has met its national obligations to the EU WEEE Directive by registering in those countries to which Xilinx is an importer. Xilinx has also elected to join WEEE Compliance Schemes in some countries to help manage customer returns at end-of-life.

If you have purchased Xilinx-branded electrical or electronic products in the EU and are intending to discard these products at the end of their useful life, please do not dispose of them with your other household or municipal waste. Xilinx has labeled its branded electronic products with the WEEE Symbol to alert our customers that products bearing this label should not be disposed of in a landfill or with municipal or household waste in the EU.



This product complies with Directive 2002/95/EC on the restriction of hazardous substances (RoHS) in electrical and electronic equipment.

This product complies with CE Directives 2006/95/EC, *Low Voltage Directive (LVD)* and 2004/108/EC, *Electromagnetic Compatibility (EMC) Directive.*

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Appendix G

Additional Resources

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see the Xilinx Support website.

To create a Xilinx user account and sign up to receive automatic email notification whenever this document is updated, go to myAlerts.

Solution Centers

See the Xilinx Solution Centers for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

References

The most up to date information related to the AC701 board and its documentation is available on the following websites.

Artix-7 FPGA AC701 Evaluation Kit

Artix-7 AC701 Evaluation Kit - Master Answer Record 51900

These Xilinx documents provide supplemental material useful with this guide:

1. *LogiCORE IP Tri-Mode Ethernet MAC User Guide* (UG138)
2. *7 Series FPGAs Overview* (DS180)
3. *Artix-7 FPGAs Data Sheet: DC and AC Switching Characteristics* (DS181)
4. *Zynq-7000 SoC and 7 Series Devices Memory Interface Solutions User Guide* (UG586)
5. *7 Series FPGAs Memory Resources User Guide* (UG473)
6. *7 Series FPGAs Configuration User Guide* (UG470)
7. *7 Series FPGAs Packaging and Pinout Product Specification* (UG475)
8. *7 Series FPGAs GTX/GTH Transceivers User Guide* (UG476)
9. *7 Series FPGAs Integrated Block for PCI Express LogiCORE IP Product Guide* (PG054)
10. *7 Series FPGAs and Zynq-7000 SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide* (UG480)
11. *7 Series FPGAs PCB Design Guide* (UG483)
12. *Vivado Design Suite User Guide: Using Constraints* (UG903)
13. *AC701 Si570 Programming Tutorial* (XTP230)
14. *AC701 Si570 Fixed Frequencies Tutorial* (XTP229)

Documents associated with other devices used by the AC701 board are available at these vendor websites:

15. Micron Technology: www.micron.com
    (N25Q256A13ESF40G, MT8JTF12864HZ-1G6G1)
16. Analog Devices: www.analog.com/en/index
    (ADV7511KSTZ-P)
17. Integrated Device Technology: www.idt.com
    (ICS844021I)
18. Marvell Semiconductor: www.marvell.com/transceivers/alaska-gbe/
    (88E1116R)
19. Samtec: www.samtec.com
    (SEAF series connectors)
20. Si Time: www.sitime.com
    (SiT9102)
21. Silicon Labs: www.silabs.com
    (Si570, Si5324C)
22. Texas Instruments: www.ti.com
    (UCD90120A, TPS84621RUQ, TPS84320RUQ, LMZ31710, LMZ31704, TL1963ADC, ADP123, TPS51200DR, TPS79433DCQ, TLV111733CDCY, PCA9548)

    Documentation describing PMBus programming for the UCD90120A controller: www.ti.com/fusiondocs.
23. Displaytech S162DBABC LCD can be found at: www.displaytech-us.com/products/charactermodules.php.

    Choose the S162D model full spec download arrow.
24. Sourcegate Technologies: www.sourcegate.net.
    To order the custom ATX cable, contact Sourcegate at, +65 6483 2878 for price and availability.

    Note: The Xilinx ATX cable part number 2600304 is manufactured by Sourcegate Technologies and is equivalent to the Sourcegate Technologies part number AZCBL-WH-11009. Sourcegate only manufactures the latest revision, which is currently A4. This is a custom cable and cannot be ordered from the Sourcegate website.