Kintex UltraScale FPGA KCU1250 Characterization Kit IBERT

Getting Started Guide

Vivado Design Suite

UG1061 (v2017.4) December 20, 2017

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
12/20/2017	2017.4	Updated for Vivado® Design Suite 2017.4. Design file changed to `rdf0352-kcu1250-ibert-2017-4.zip`.
10/09/2017	2017.3	Updated for Vivado® Design Suite 2017.3. Design file changed to `rdf0352-kcu1250-ibert-2017-3.zip`.
06/20/2017	2017.2	Updated for Vivado Design Suite 2017.2. Design file changed to `rdf0352-kcu1250-ibert-2017-2.zip`.
04/19/2017	2017.1	Updated text and graphics for Vivado Design Suite 2017.1. Design file changed to `rdf0352-kcu1250-ibert-2017-1.zip`.
12/15/2016	2016.4	Updated for Vivado Design Suite 2016.4. Design file changed to `rdf0352-kcu1250-ibert-2016-4.zip`.
10/12/2016	2016.3	Updated for Vivado Design Suite 2016.3. Design file changed to `rdf0352-kcu1250-ibert-2016-3.zip`. Updated Figure 1-14, Figure 2-1, Figure 2-2, and Figure 2-4.
06/08/2016	2016.2	Updated for Vivado Design Suite 2016.2. Design file changed to `rdf0352-kcu1250-ibert-2016-2.zip`. Updated Figure 2-11, Figure 2-12, and Figure 2-13.
04/13/2016	2016.1	Updated for Vivado Design Suite 2016.1. Design file `rdf0352-kcu1250-ibert-2015-4.zip` changed to `rdf0352-kcu1250-ibert-2016-1.zip`. Updated Figure 1-2 and Figure 1-19.
11/24/2015	2015.4	Updated for Vivado Design Suite 2015.4. Design file `rdf0352-kcu1250-ibert-2015-3.zip` changed to `rdf0352-kcu1250-ibert-2015-4.zip`.
10/07/2015	2015.3	Updated for Vivado Design Suite 2015.3. Design file `rdf0352-kcu1250-ibert-2015-2.zip` changed to `rdf0352-kcu1250-ibert-2015-3.zip`. A step 11 was added to Starting the SuperClock-2 Module. Updated Figure 1-12, Figure 2-2, and Figure 2-5 through Figure 2-8.
06/30/2015	2015.2	Updated for Vivado Design Suite 2015.2. Design file `rdf0352-kcu1250-ibert-2015-1.zip` changed to `rdf0352-kcu1250-ibert-2015-2.zip`. Board power on was added to step 3, page 13. Updated Figure 2-2, Figure 2-4, and Figure 2-8.
04/27/2015	2015.1	Initial Xilinx release.

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Chapter 1

KCU1250 IBERT Getting Started Guide

Overview

This document describes setting up the Kintex® UltraScale™ FPGA KCU1250 GTH Transceiver Characterization Board and running the Integrated Bit Error Ratio Test (IBERT) demonstration using the Vivado® Design Suite. The designs required to run the IBERT demonstration are stored in a Secure Digital (SD) memory card provided with the KCU1250 board. The demonstration shows the capabilities of the Kintex UltraScale XCKU040-FFVA1156 FPGA GTH transceiver.

The KCU1250 board is described in detail in the *KCU1250 Board User Guide* (UG1057) [Ref 1].

The IBERT demonstration operates one GTH Quad. The procedure consists of:

1. Setting Up the KCU1250 Board
2. Extracting the Project Files
3. Connecting the GTH Transceivers and Reference Clocks
4. Starting the SuperClock-2 Module
5. Configuring the FPGA
6. Setting Up the Vivado Design Suite
7. Viewing GTH Transceiver Operation
8. Closing the IBERT Demonstration

Requirements

The following hardware and software is required to run and rebuild the GTH IBERT demonstrations:

- Kintex UltraScale FPGA KCU1250 GTH Transceiver Characterization Board, including:
  - One SD card containing the IBERT demonstration designs
  - One Samtec Bulls Eye® cable
  - Eight SMA female-to-female (F-F) adapters
  - Six 50-Ω SMA terminators
  - UltraScale transceiver power supply module (installed)
  - SuperClock-2 module, Rev 1.0 (installed)
  - Active BGA heat sink (installed)
  - 12V DC power adapter
  - Two USB cables, standard-A plug to micro-B plug
- Host PC with:
  - SD card reader
  - USB ports
- Xilinx® Vivado Design Suite 2017.4

The hardware and software required to rebuild the IBERT demonstration designs are:

- Xilinx Vivado Design Suite 2017.4
- PC with a version of Windows supported by Xilinx Vivado Design Suite

Setting Up the KCU1250 Board

This section describes how to set up the KCU1250 board.

CAUTION! The KCU1250 board can be damaged by electrostatic discharge (ESD). Follow standard ESD prevention measures when handling the board, such as using a grounding strap and static dissipative mat.

When shipped, the KCU1250 board is configured to support the GTH IBERT demonstrations described in this document. If the board has been re-configured, it must be returned to the default setup before running the IBERT demonstrations by following these steps:

1. Move all jumpers and switches to their default positions. The default jumper and switch positions are listed in the *KCU1250 Board User Guide* (UG1057) [Ref 1].
2. Confirm that the UltraScale transceiver power module is plugged into connectors J124 and J46.
3. Confirm that the SuperClock-2 module is installed. See *HW-CLK-101-SCLK2 SuperClock-2 Module User Guide* (UG770) [Ref 2]:
   a. Align the three metal standoffs on the bottom side of the module with the three mounting holes in the SUPERCLOCK-2 MODULE interface of the KCU1250 board.
   b. Using three 4-40 x 0.25 inch screws, firmly screw down the module from the bottom of the KCU1250 board.
   c. On the SuperClock-2 module, place a jumper across pins 2–3 (2V5) of the CONTROL VOLTAGE header, J18, and place another jumper across Si570 INH header J11.
   d. Screw down a 50Ω SMA terminator onto each of the six unused Si5368 clock output SMA connectors: J7, J8, J12, J15, J16 and J17.

Extracting the Project Files

The Vivado Design Suite BIT files required to run the IBERT demonstrations are located in `rdf0352-kcu1250-ibert-2017-4.zip` on the SD card provided with the KCU1250 board. The BIT files are also available online at Kintex UltraScale FPGA KCU1250 Characterization Kit documentation.

The ZIP file contains these BIT files:

- `kcu1250_ibert_q224_125.bit`
- `kcu1250_ibert_q225_125.bit`
- `kcu1250_ibert_q226_125.bit`
- `kcu1250_ibert_q227_125.bit`
- `kcu1250_ibert_q228_125.bit`

To copy the files from the SD card:

1. Connect the SD card to the host computer.
2. Locate the file `rdf0352-kcu1250-ibert-2017-4.zip` on the SD card.
3. Unzip the files to a working directory on the host computer.

Running the GTH IBERT Demonstration

The GTH IBERT demonstration operates one GTH Quad at a time. This section describes how to test GTH Quad 224. The remaining GTH Quads can be tested by following a similar series of steps.

Connecting the GTH Transceivers and Reference Clocks

Figure 1-1 shows the locations for GTH transceiver Quads 224, 225, 226, 227, and 228 on the KCU1250 board.

Note: Figure 1-1 is for reference only and might not reflect the current revision of the board.

Note: Quad 131 and Quad 132 are not available on the XCKU040 device.

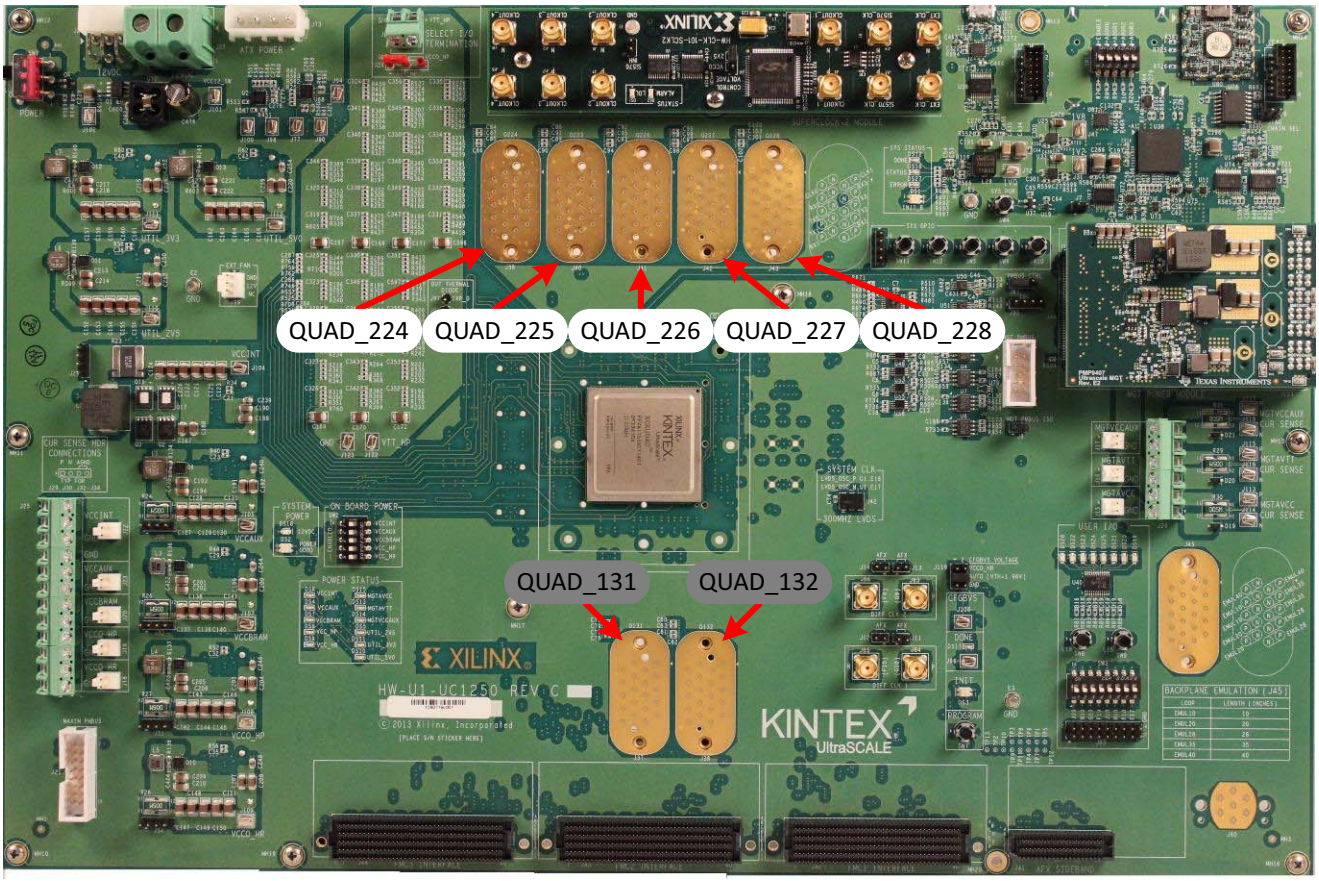

Figure 1-1: **GTH Quad Locations**

All GTH transceiver pins and reference clock pins are routed from the FPGA to a connector pad that interfaces with Samtec Bulls Eye connectors. Figure 1-2 **A** shows the connector pad. Figure 1-2 **B** shows the connector pinout.

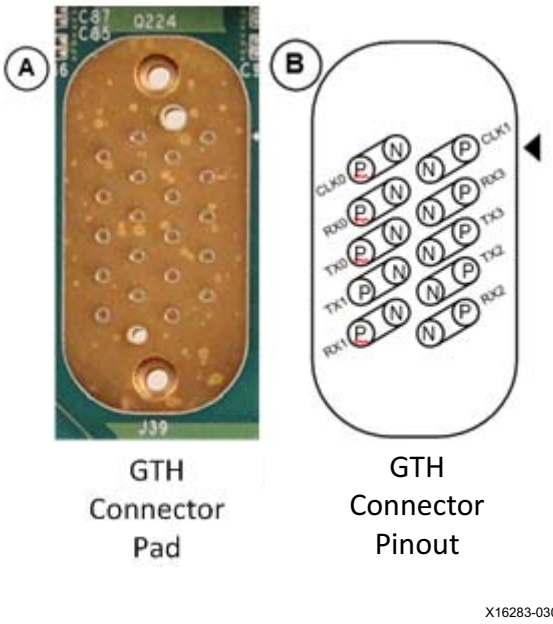

Figure 1-2: **A – GTH Connector Pad. B – GTH Connector Pinout**

The SuperClock-2 module provides LVDS clock outputs for the GTH reference clocks in the IBERT demonstrations. Figure 1-3 shows the locations of the differential clock SMA connectors on the clock module which can be connected to the reference clock cables.

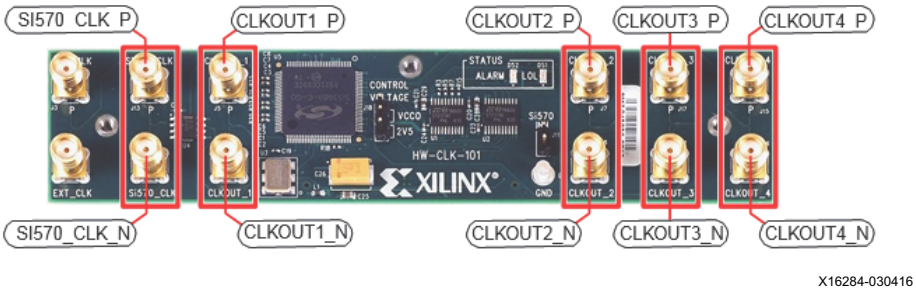

Figure 1-3: **SuperClock-2 Module Output Clock SMA Locations**

The four SMA pairs labeled CLKOUT provide LVDS clock outputs from the Si5368 clock multiplier/jitter attenuator device on the clock module. The SMA pair labeled Si570_CLK provides LVDS clock output from the Si570 programmable oscillator on the clock module.

Note: The Si570 oscillator does not support LVDS output on the Rev B and earlier revisions of the SuperClock-2 module.

For more information on the SuperClock-2 module, see the *HW-CLK-101-SCLK2 SuperClock-2 Module User Guide* (UG770) [Ref 2].

Attaching the GTH Quad Connector

1. Before connecting the Bulls Eye cable assembly to the board, firmly secure the blue elastomer seal provided with the cable assembly to the bottom of the connector housing if it is not already inserted (see Figure 1-4).

   Note: Figure 1-4 is for reference only and might not reflect the current version of the connector.

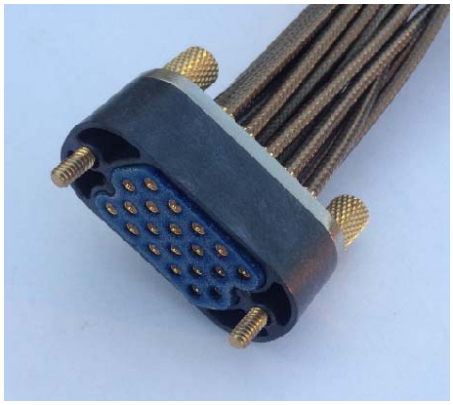

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Figure 1-4: **Bulls Eye Connector with Elastomer Seal**

2. Attach the Samtec Bulls Eye connector to GTH Quad 224 (Figure 1-5), aligning the two indexing pins on the bottom of the connector with the guide holes on the board. Hold the connector flush with the board and fasten it by tightening the two captive screws.

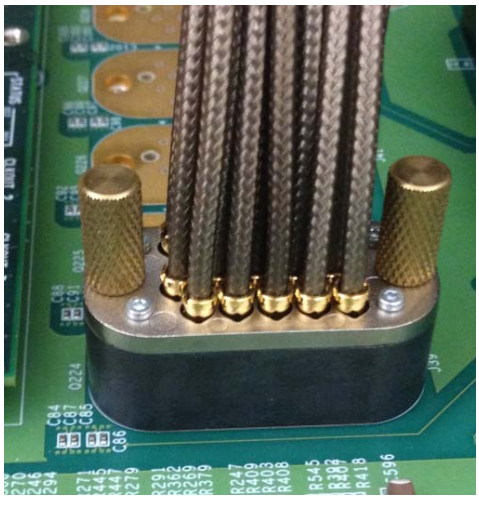

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Figure 1-5: **Bulls Eye Connector Attached to Quad 224**

GTH Transceiver Clock Connections

1. See Figure 1-2 to identify the P and N coax cables that are connected to the CLK0 reference clock inputs.
2. Connect these cables to the SuperClock-2 module as follows:
   - CLK0_P coax cable → SMA connector J7 (CLKOUT1_P) on the SuperClock-2 module
   - CLK0_N coax cable → SMA connector J8 (CLKOUT1_N) on the SuperClock-2 module

   Note: Any one of the five differential outputs from the SuperClock-2 module can be used to source the GTH reference clock. CLKOUT1_P and CLKOUT1_N are used here as an example.

GTH TX/RX Loopback Connections

1. See Figure 1-2 to identify the P and N coax cables that are connected to the four receivers (RX0, RX1, RX2, and RX3) and the four transmitters (TX0, TX1, TX2, and TX3).
2. Use eight SMA female-to-female (F-F) adapters (Figure 1-6) to connect the transmit and receive cables as shown in Figure 1-7:
   - TX0_P → SMA F-F Adapter → RX0_P
   - TX0_N → SMA F-F Adapter → RX0_N
   - TX1_P → SMA F-F Adapter → RX1_P
   - TX1_N → SMA F-F Adapter → RX1_N
   - TX2_P → SMA F-F Adapter → RX2_P
   - TX2_N → SMA F-F Adapter → RX2_N
   - TX3_P → SMA F-F Adapter → RX3_P
   - TX3_N → SMA F-F Adapter → RX3_N

RECOMMENDED: *To ensure good connectivity, it is recommended that the adapters be secured with a wrench; however, do not over-tighten the SMAs.*

Figure 1-6: **SMA F-F Adapter**

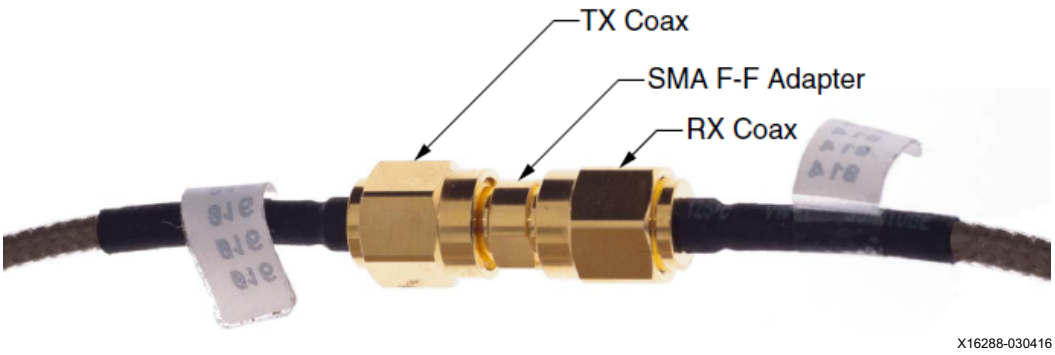

Figure 1-7: **TX-to-RX Loopback Connection Example**

Figure 1-8 shows the KCU1250 board with the cable connections required for the Quad 224 GTH IBERT demonstration.

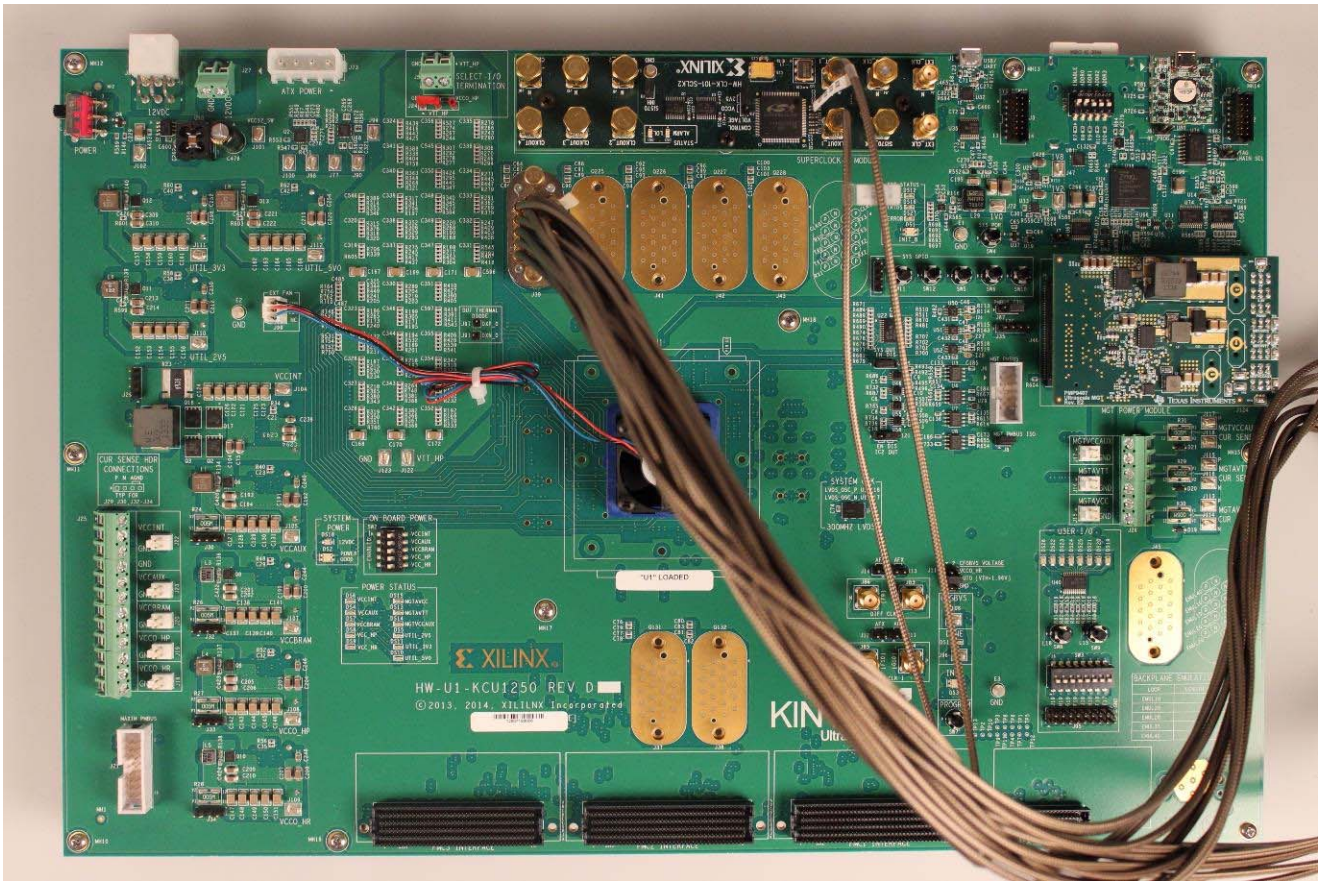

Figure 1-8: **Cable Connections for Quad 224 GTH IBERT Demonstration**

Starting the SuperClock-2 Module

The SuperClock-2 module features two clock-source components:

- Always-on Si570 crystal oscillator
- Si5368 jitter-attenuating clock multiplier

Outputs from either source can be used to drive the transceiver reference clocks.

To start the SuperClock-2 module:

1. Configure the SuperClock-2 module using the Xilinx XC7Z010CLG225 Zynq-7000 AP SoC System Controller command line, which can be accessed through a serial communication terminal connection using the enhanced communication port of the Silicon Labs USB to Dual UART Bridge (Figure 1-9). Additional information about the Silicon Labs USB-to-UART is available in *Silicon Labs CP210x USB-to-UART Installation Guide* (UG1033) [Ref 3].

   Review the *KCU1250 Board User Guide* (UG1057) [Ref 1] for additional information about the System Controller.

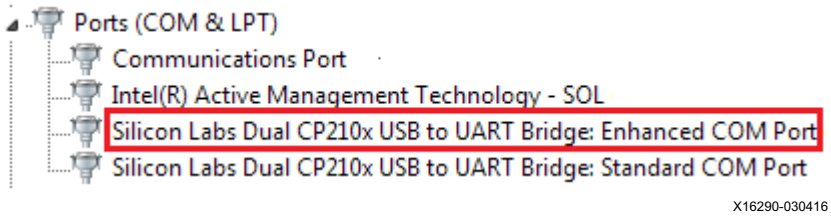

Figure 1-9: **Silicon Labs Enhanced COM PORT**

2. Set the System Controller configuration DIP switches (SW13) to the OFF position (Figure 1-10). This disables configuration of the FPGA at power reset.

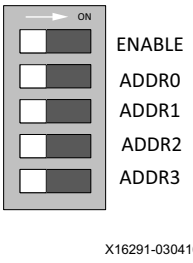

Figure 1-10: **Configuration DIP Switch (SW13)**

3. Connect J1 connector (USB/UART) on the KCU1250 board to the host computer using one of the standard-A plug to micro-B plug USB cables provided (Figure 1-11).
4. Power up the board by placing SW1 in the ON position.

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Figure 1-11: **USB-UART Connector**

5. Open a serial communication terminal application on the host computer, for example "Hyper Terminal".
6. Connect to the port number associated with the **enhanced COM port** of the Silicon Lab USB-UART Bridge.

7. Set up a new connection as shown in Figure 1-12, and click **OK**.
8. Open the connection and press the **Enter** key to view the **System Controller** options menu.

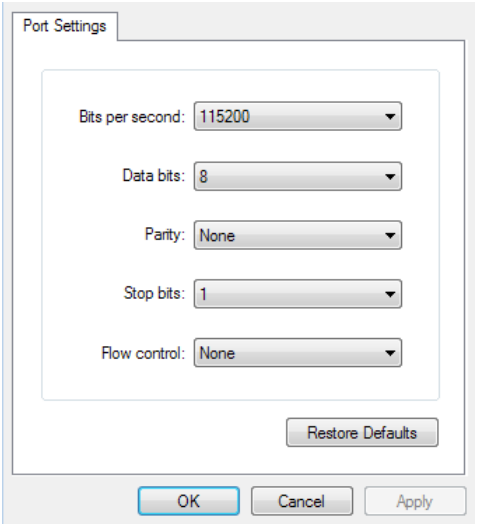

Figure 1-12: **Terminal Setting**

9. From the main **System Controller** menu, select option 1 **Set Programmable Clocks** to access the SuperClock-2 options.
10. Use the Programmable Clocks menu option 2 **Set Si5368 Frequency** to set the output clock frequencies of the Si5368 clocks to 125 MHz.
11. Select option 2 **Free-Run using XA-XB crystal** operating mode when prompted.

Configuring the FPGA

The Xilinx Zynq-7000 AP SoC XC7Z010CLG225 System Controller includes a System Integrated Configuration Engine (System ICE) option. The System ICE can be used to configure the FPGA, in 8-bit SMAP configuration mode, using one of the `*.bit` files provided on the SD card.

The FPGA can also be configured through the Vivado Design Suite using the `*.bit` files available on the SD card or online (as collection `rdf0352-kcu1250-ibert-2017-4.zip`) at Kintex UltraScale FPGA KCU1250 Characterization Kit documentation.

Review *UltraScale Architecture Configuration User Guide* (UG570) [Ref 4] for additional information about UltraScale device configuration.

1. Insert the SD card provided with the KCU1250 board into the SD card reader slot located on the bottom-side (upper-right corner) of the KCU1250 board.
2. From the main **System Controller** menu, select option 7 **Configure UltraScale FPGA** to access the SuperClock-2 options.

3. Select option 1 **Configure UltraScale FPGA from SD Card** to configure the FPGA from the SD card:

   The IBERT design demonstrations included with the SD cards can be selected using one of the bitstream numbers listed in Table 1-1.

Table 1-1: **IBERT Examples Bitstream Number**

IBERT Demonstration Design	Bitstream Number
QUAD_224	0
QUAD_225	1
QUAD_226	2
QUAD_227	3
QUAD_228	4

4. Select option (0) to configure the FPGA with the Quad 224 IBERT example design. Press **Enter** and review the terminal for configuration progress:

```
Enter a Bitstream number (0-15):

0

Info: xilinx.sys opened

Info: Opening rev_1/set0/config.def

Info: Configuration definition file "rev_1/set0/config.def"
opened

Info: Clock divider is set to 2

Info: Configuration clock frequency is 25MHz

Info: Bitfile "rev_1/set0/ibert224.bit" opened

...10%...20%...30%...40%...50%...60%...70%...80%...90%...100%

Configuration completed successfully
```

Setting Up the Vivado Design Suite

1. Connect the host computer to the KCU1250 board using the second standard-A plug to micro-B plug USB cable. The standard-A plug connects to a USB port on the host computer and the micro-B plug connects to U80 (the Digilent USB JTAG configuration port on the KCU1250 board (Figure 1-13)).

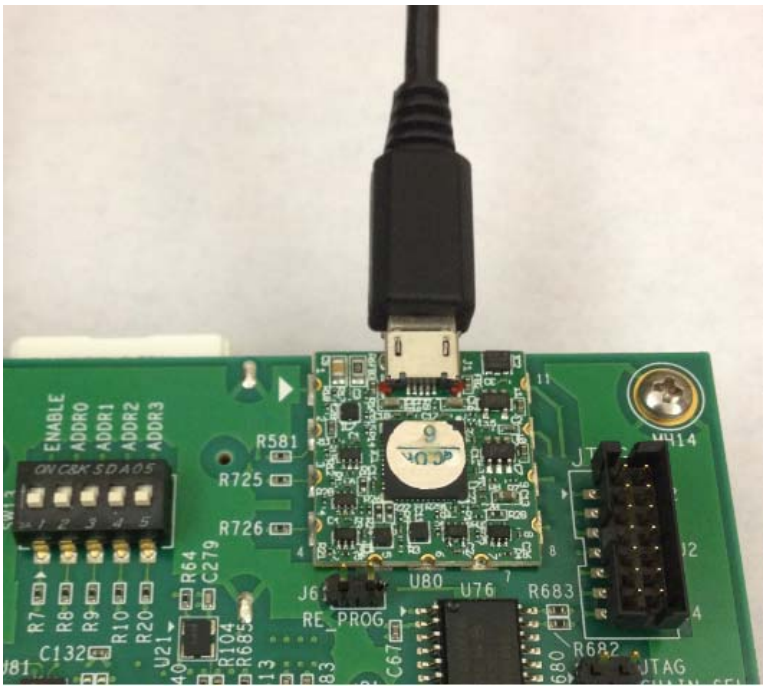

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Figure 1-13: **USB-UART Connector**

2. Start the Vivado Design Suite on the host computer and click **Flow > Open Hardware Manager** (highlighted in Figure 1-14).

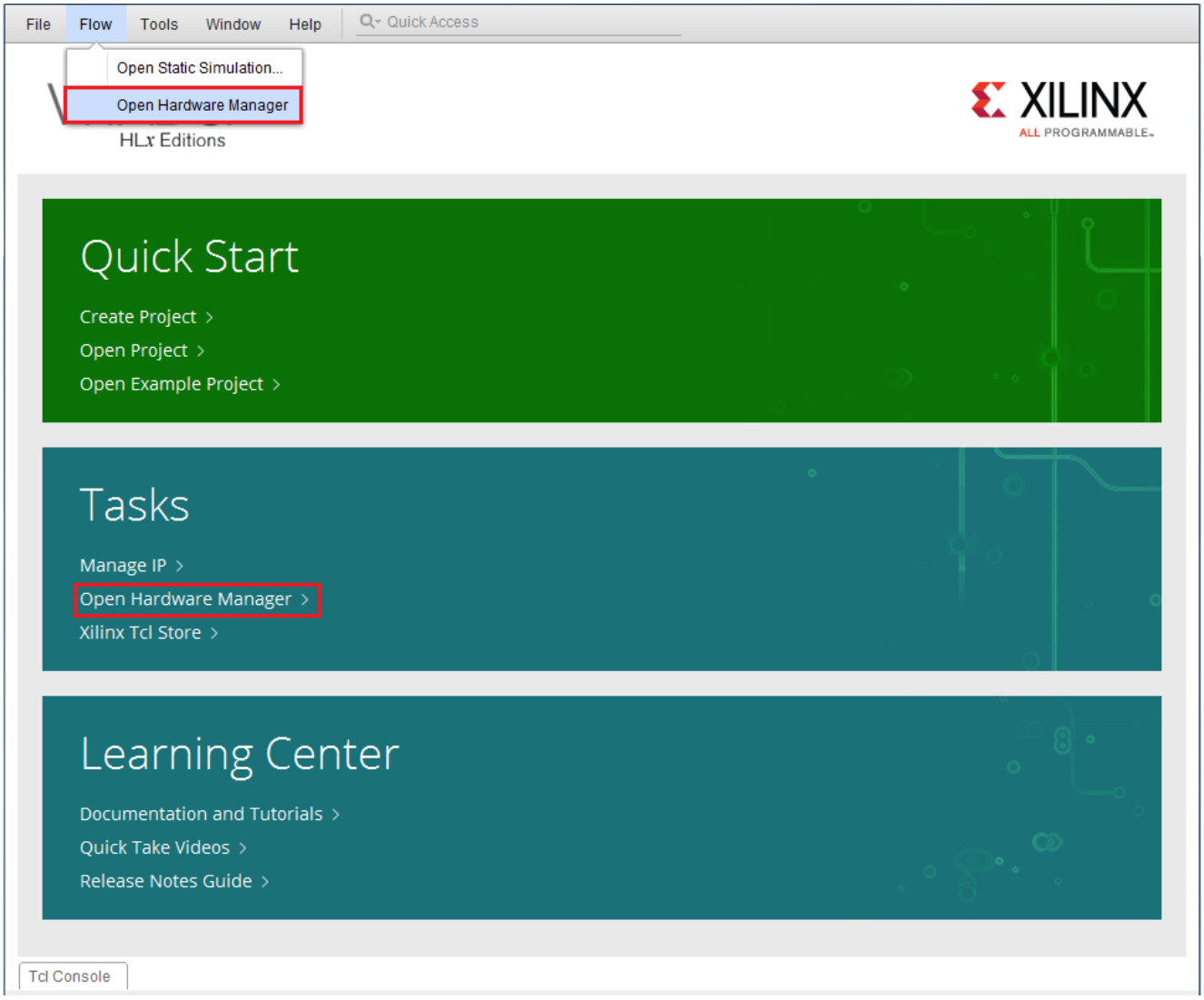

Figure 1-14: **Vivado Design Suite, Open Hardware Manager**

3. In the **Hardware Manager** window (Figure 1-15), click **Open New Target**.

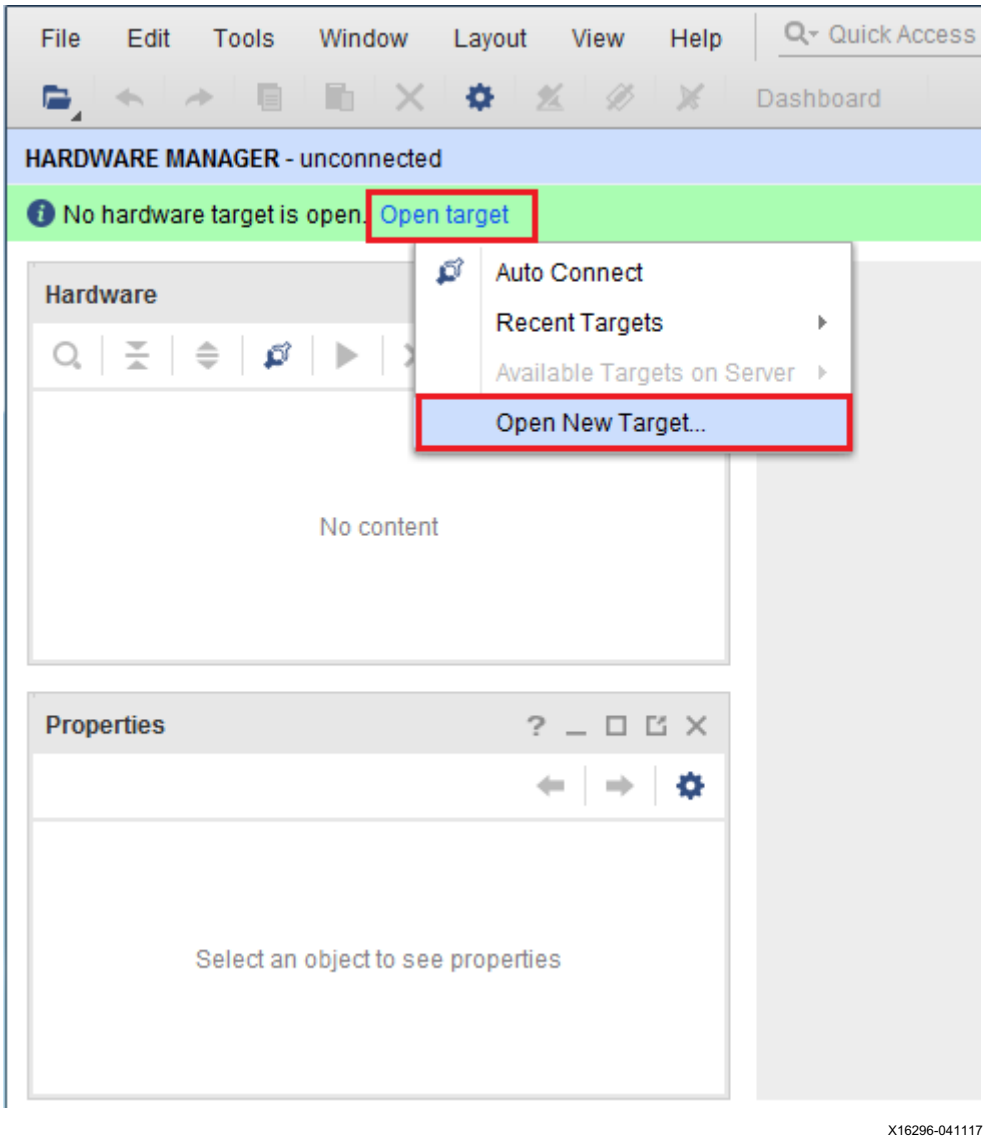

Figure 1-15: **Open a New Hardware Manager**

4. In the **Hardware Server Settings** window, select **Local server (target is on local machine)**. Click **Next**.

5. In the **Select Hardware Target** window, the **xilinx_tcf** cable appears under **Hardware Targets**, and the JTAG chain contents of the selected cable appear under **Hardware Devices** (Figure 1-16). Select the **xilinx_tcf_Digilent** target and keep the JTAG Clock Frequency at the default value (**15 MHz**). Click **Next**.

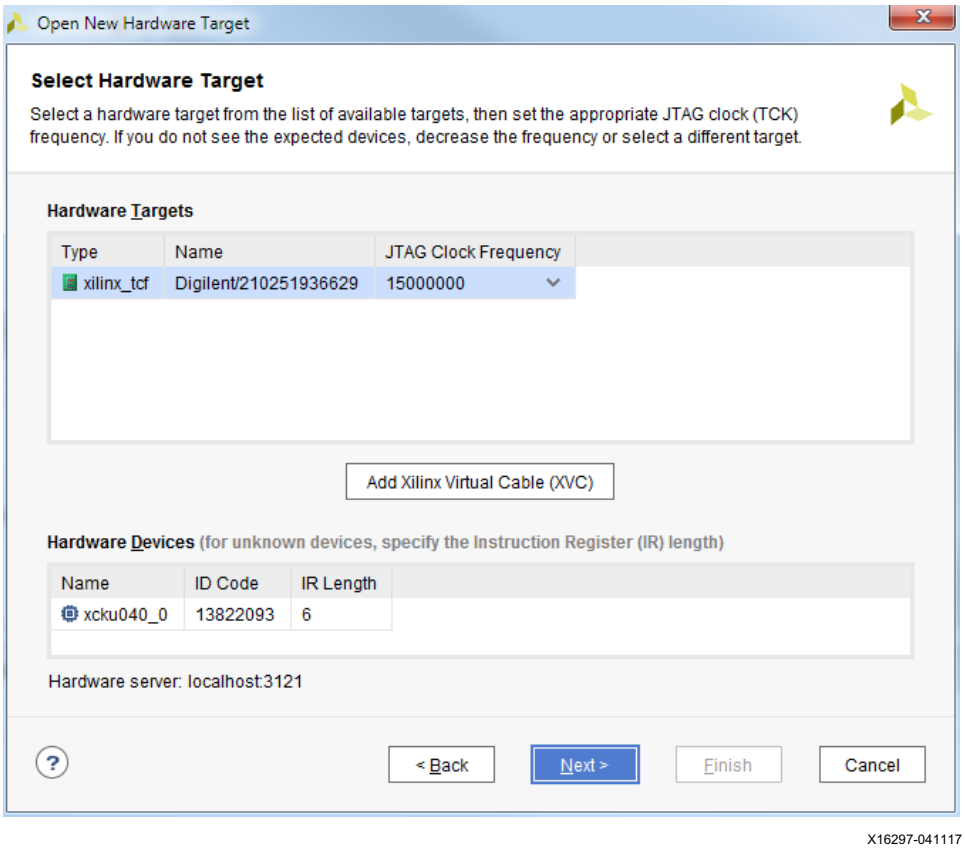

Figure 1-16: **Select Hardware Target**

6. In the **Open Hardware Target Summary** window, click **Finish**. The wizard closes and the Vivado Design Suite opens the hardware target.

   To view the GTH transceiver operation, click **Layout > Serial I/O Analyzer**. From the top of the **Hardware Manager** window, select **Auto-Detect Links** to display all available links automatically. Links can also be created manually in the **Links** window by right-clicking and selecting **Create Links** or by clicking the **Create Links** button (Figure 1-17).

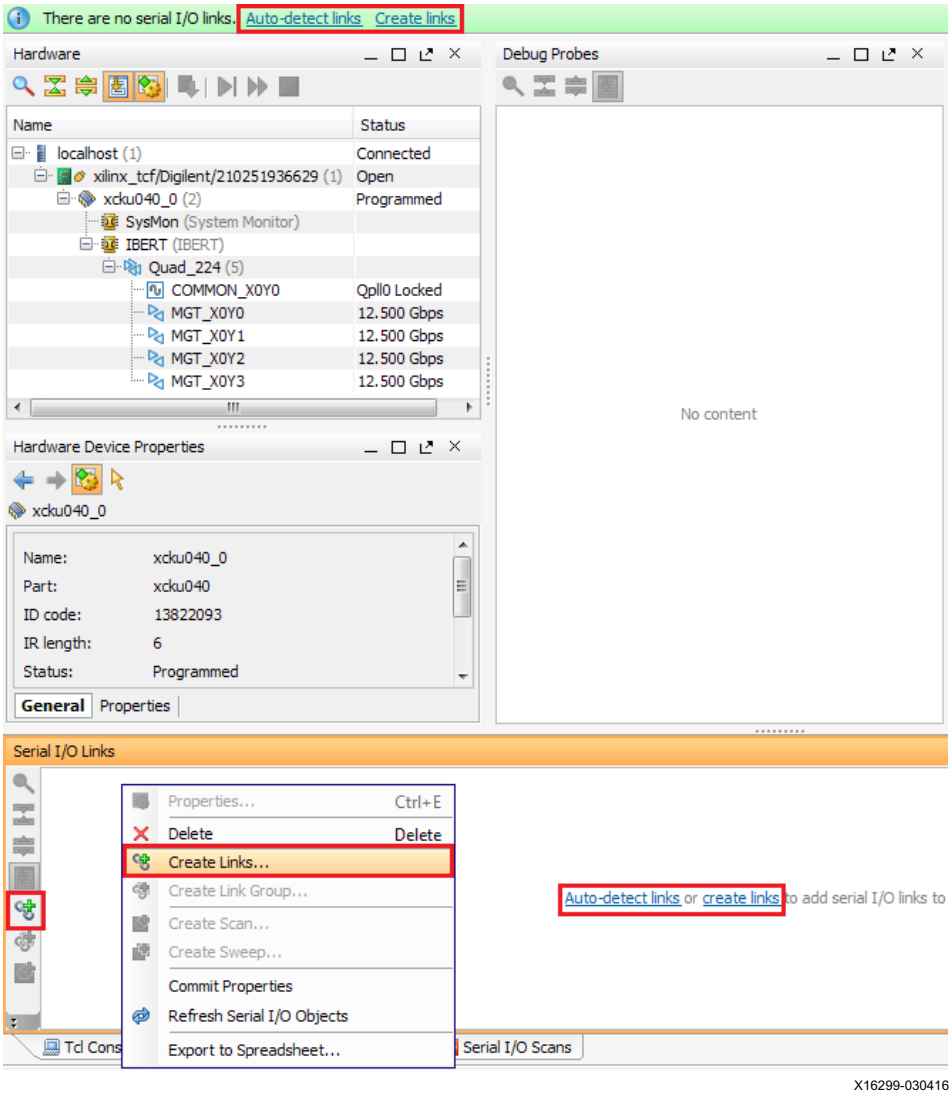

Figure 1-17: **Serial I/O Analyzer – Create Links**

If links are created manually, the **Create Links** window is displayed. The options in this window are used to link any TX GT to any RX GT. To create links, select the TX GT and RX GT from the two lists, then click the **Add (+)** button. For this project, connect the following links (Figure 1-18):

- MGT_X0Y0/TX (xcku040_0/Quad_224) to MGT_X0Y0/RX (xcku040_0/Quad_224)
- MGT_X0Y1/TX (xcku040_0/Quad_224) to MGT_X0Y1/RX (xcku040_0/Quad_224)
- MGT_X0Y2 /TX (xcku040_0/Quad_224) to MGT_X0Y2/RX (xcku040_0/Quad_224)
- MGT_X0Y3/TX (xcku040_0/Quad_224) to MGT_X0Y3/RX (xcku040_0/Quad_224)

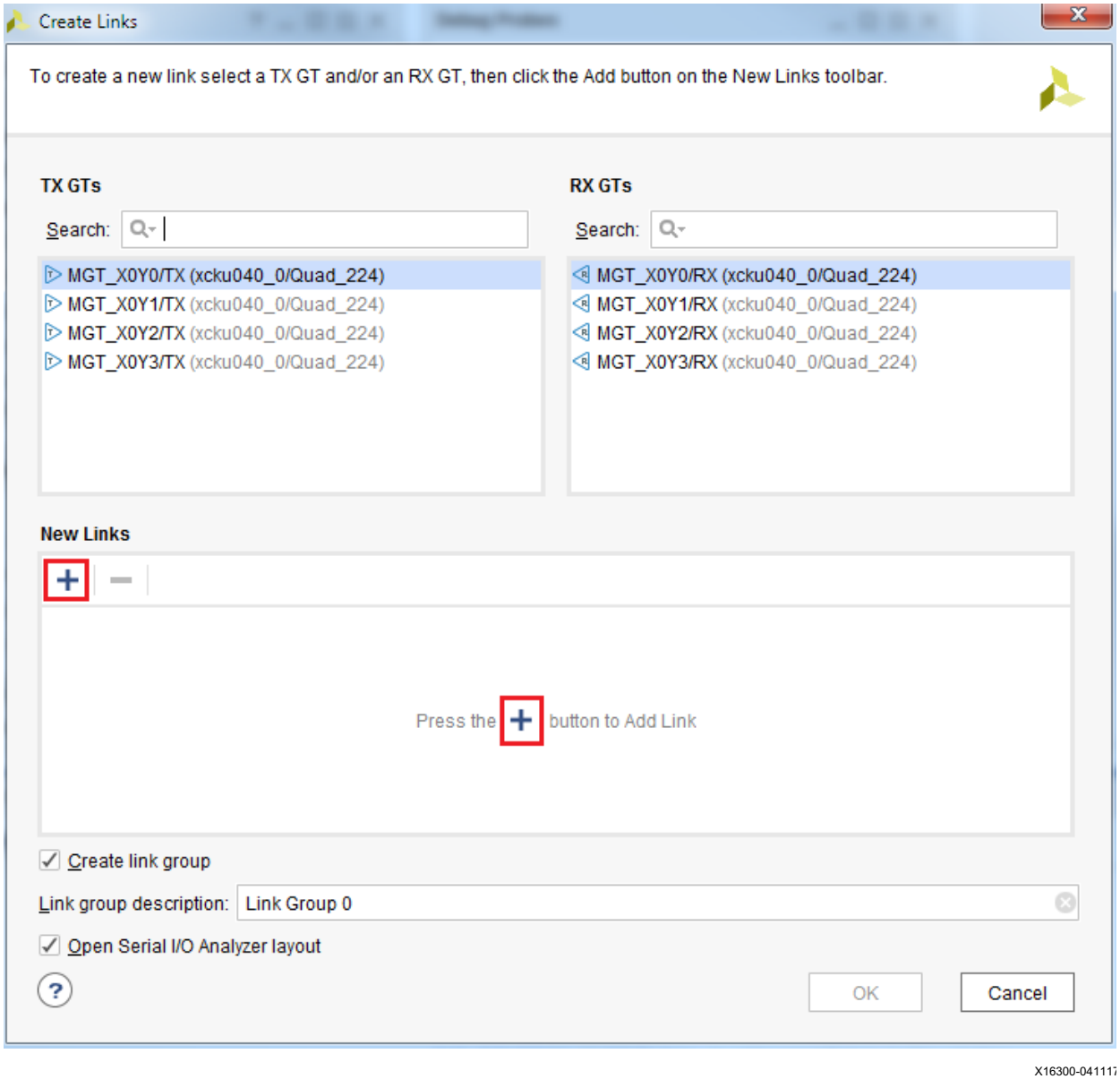

Figure 1-18: **Create Links Window**

Viewing GTH Transceiver Operation

After completing Setting Up the Vivado Design Suite, the IBERT demonstration is configured and running. The status and test settings are displayed on the serial I/O link tab in the Links window shown in Figure 1-19.

Review the line rate and RX bit error count. The line rate for all four GTH transceivers is 12.5 Gb/s (see Status in Figure 1-19). Verify that the there are no bit errors.

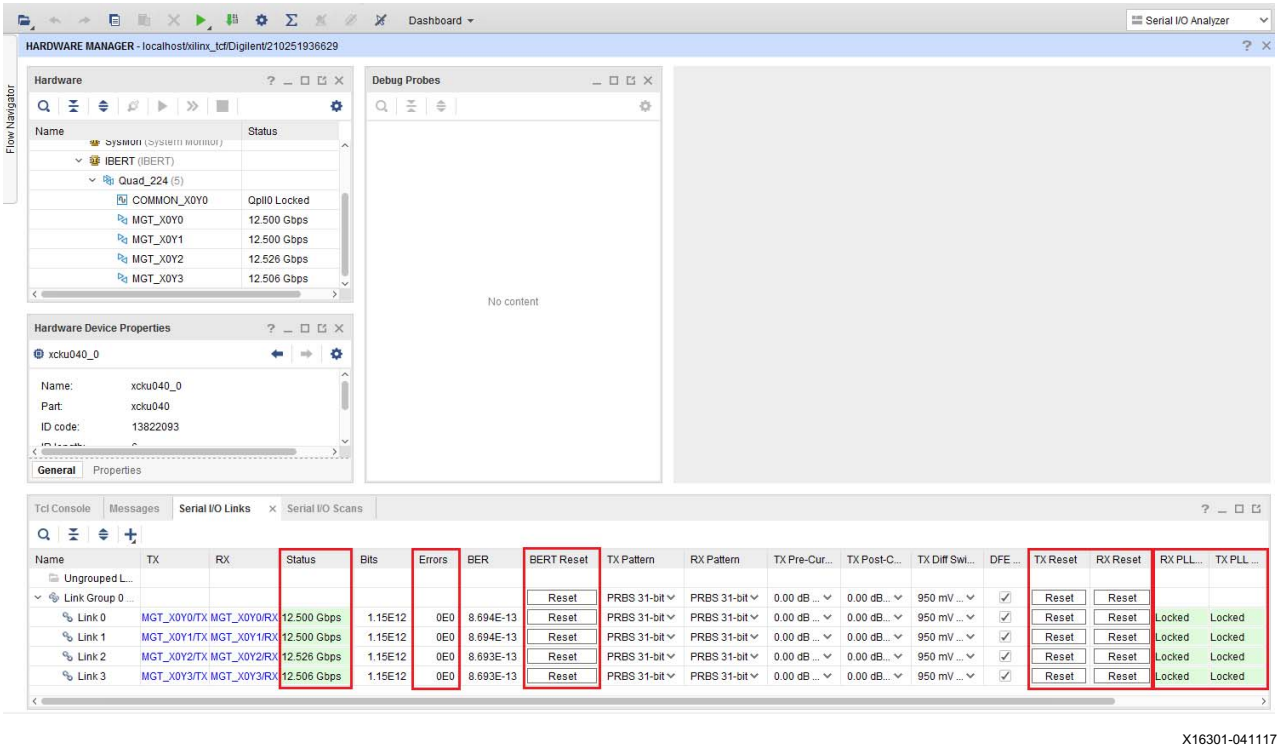

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Figure 1-19: **Serial I/O Analyzer Links**

In Case of RX Bit Errors

If there are initial bit errors after linking, or as a result of changing the TX or RX pattern, click the respective **BERT Reset** button to zero the count.

If the **Status** column shows `No Link` for one or more transceivers:

- Make sure the blue elastomer seal is connected to the bottom of the Bulls Eye cable (refer to Figure 1-4) and the cable is firmly connected and flush on the board.
- Increase the TX differential swing of the transceiver (to compensate for any loss due to PCB process variation).
- Click the respective **TX Reset** button followed by **BERT Reset**.

Additional information on the Vivado Design Suite and IBERT core can be found in *Vivado Design Suite User Guide: Programming and Debugging* (UG908) [Ref 5].

Closing the IBERT Demonstration

To close the IBERT demonstration:

1. Close the Vivado Design Suite by selecting **File > Exit**.
2. Place the main power switch SW1 in the OFF position.

Creating the GTH IBERT Core

Note: Vivado® Design Suite 2017.4 is required to rebuild the designs shown here.

This section provides a procedure to create a single Quad GTH IBERT core. The procedure assumes Quad 224 at 12.5 Gb/s line rate, but cores for any of the GTH Quads with any supported line rate can be created following the same series of steps.

For more details on generating IBERT cores, see the *Vivado Design Suite User Guide: Programming and Debugging* (UG908) [Ref 5].

1. Start the Vivado Design Suite.
2. In the Vivado Design Suite window, click **Manage IP** (highlighted in Figure 2-1) and select **New IP Location**.

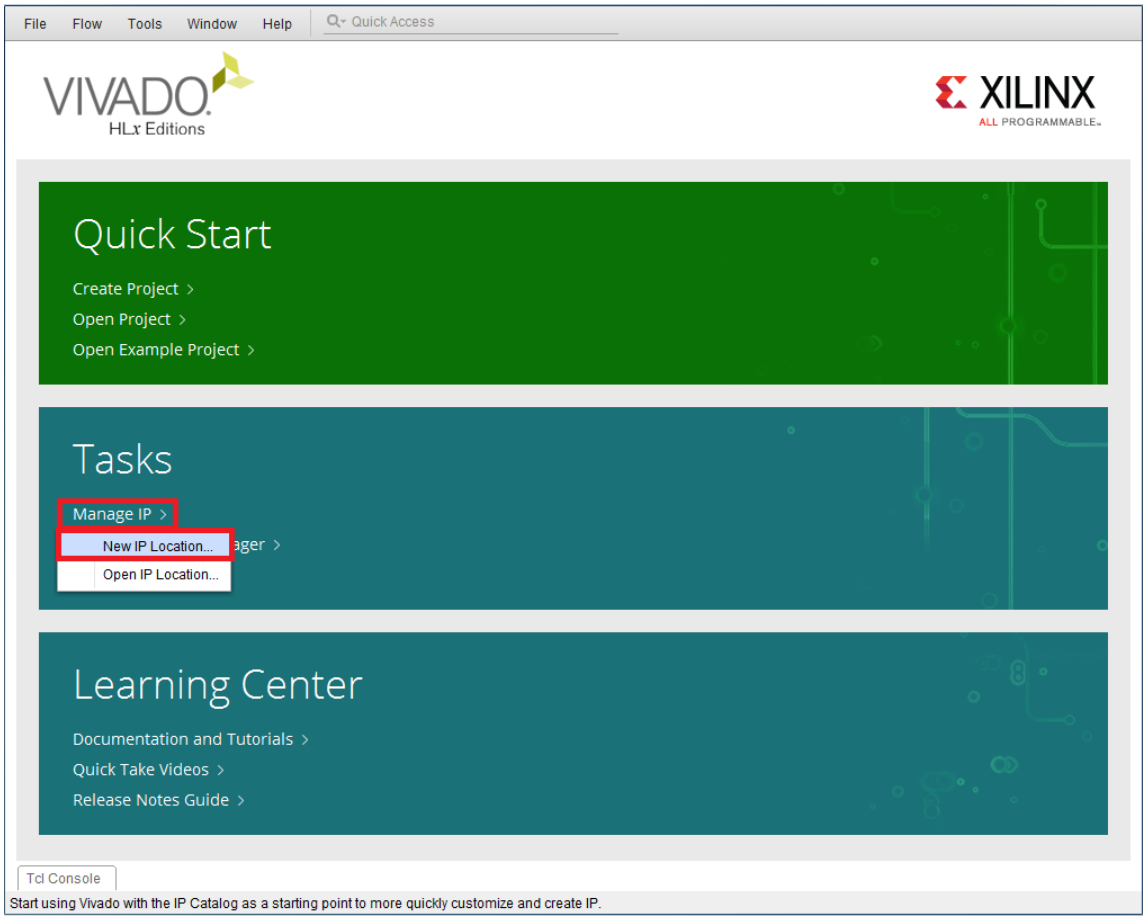

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Figure 2-1: **Vivado Design Suite Initial Window**

3. In the **Manage IP Settings** window, click the **(...)** button next to the Part field to select the target part. Use the drop-down menu items to filter the devices. Select the **xcku040-ffva1156-3-e** device (see Figure 2-2). Click **OK**.

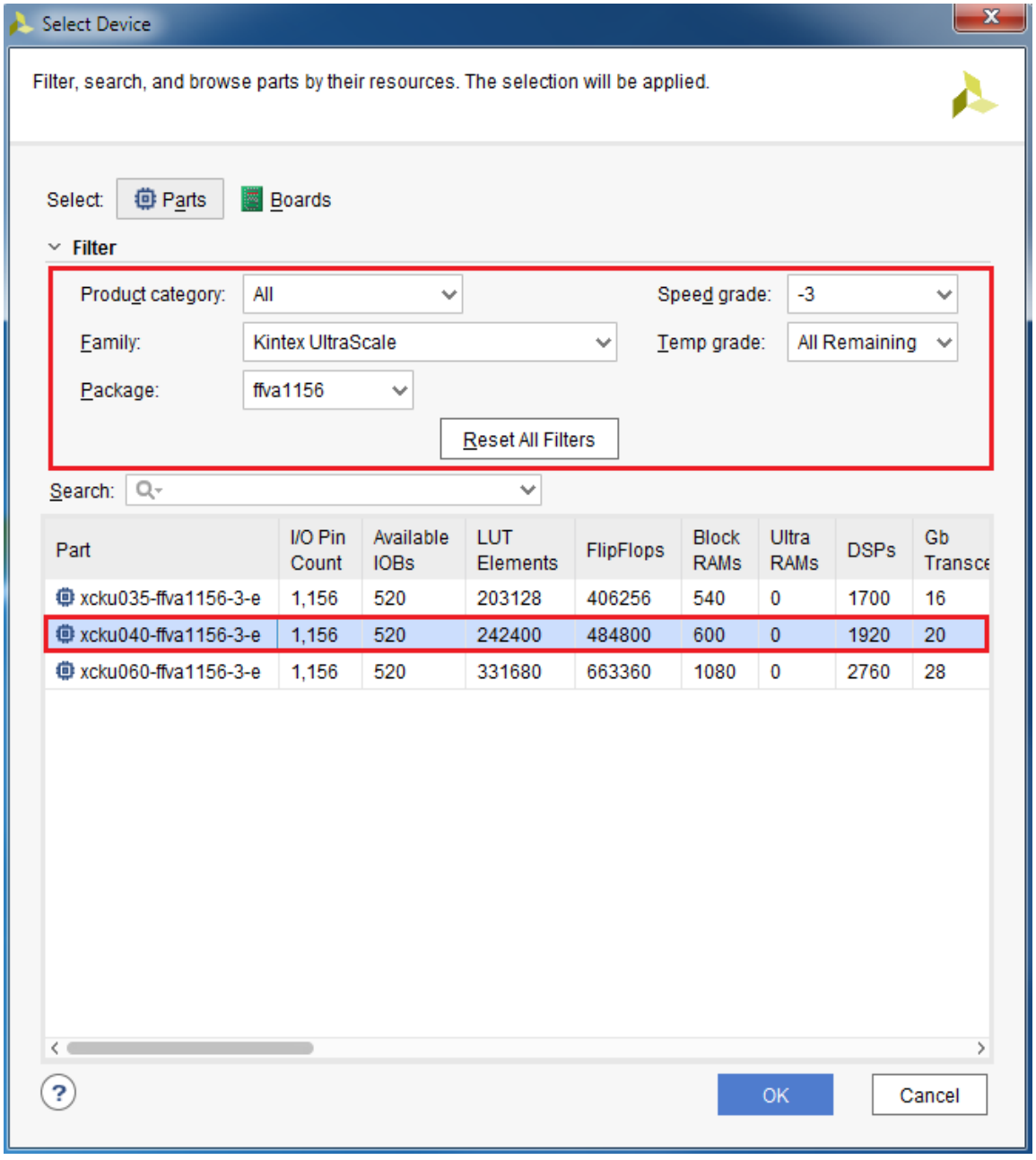

Figure 2-2: **Select Device**

4. Back on the **Manage IP** window, select **Verilog** for Target language, **Vivado Simulator** for Target simulator, **Mixed** for Simulator language, and a directory to save the customized IP (Figure 2-3). Click **Finish**.

   Note: Make sure the directory name does not include spaces.

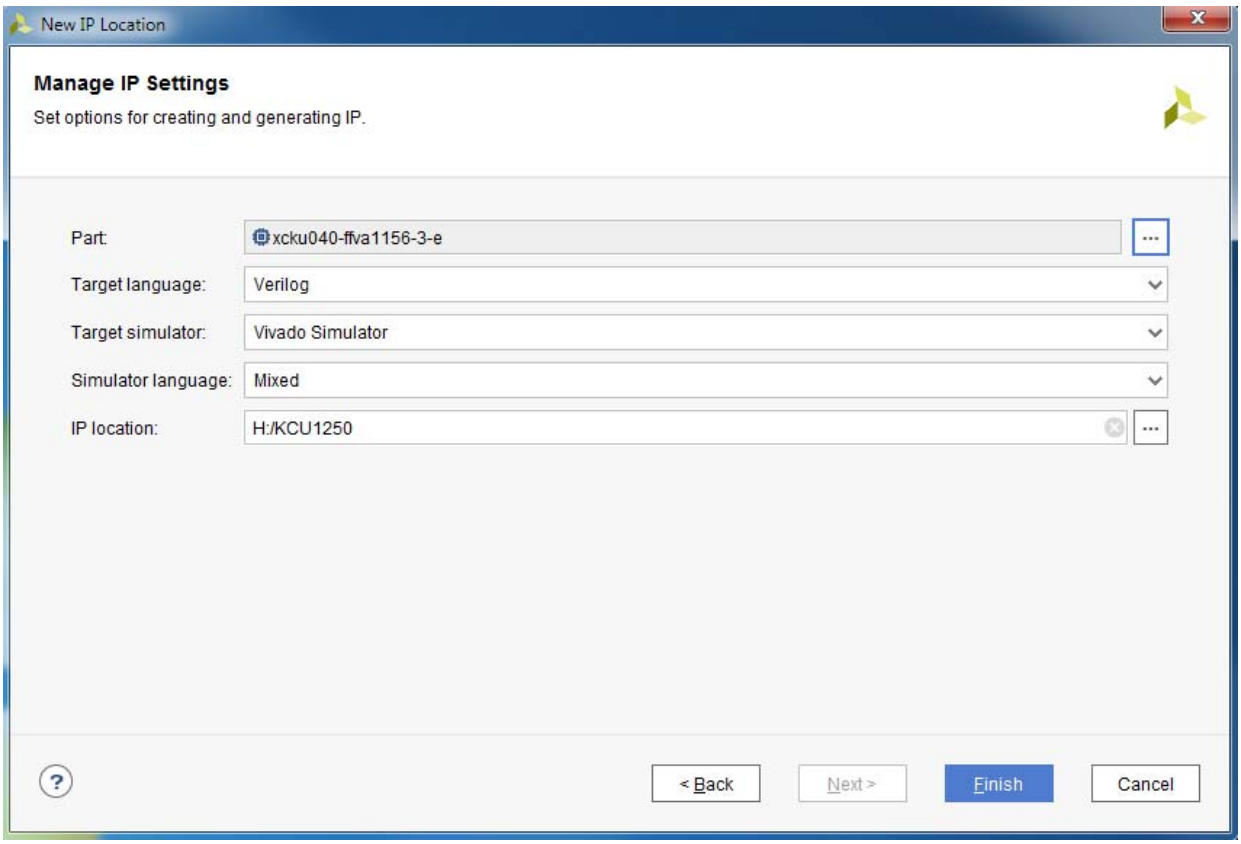

Figure 2-3: **Manage IP Settings**

5. In the **IP Catalog** window, expand the **Debug & Verification** folder, expand the **Debug** folder, and double-click **IBERT UltraScale GTH** (Figure 2-4).

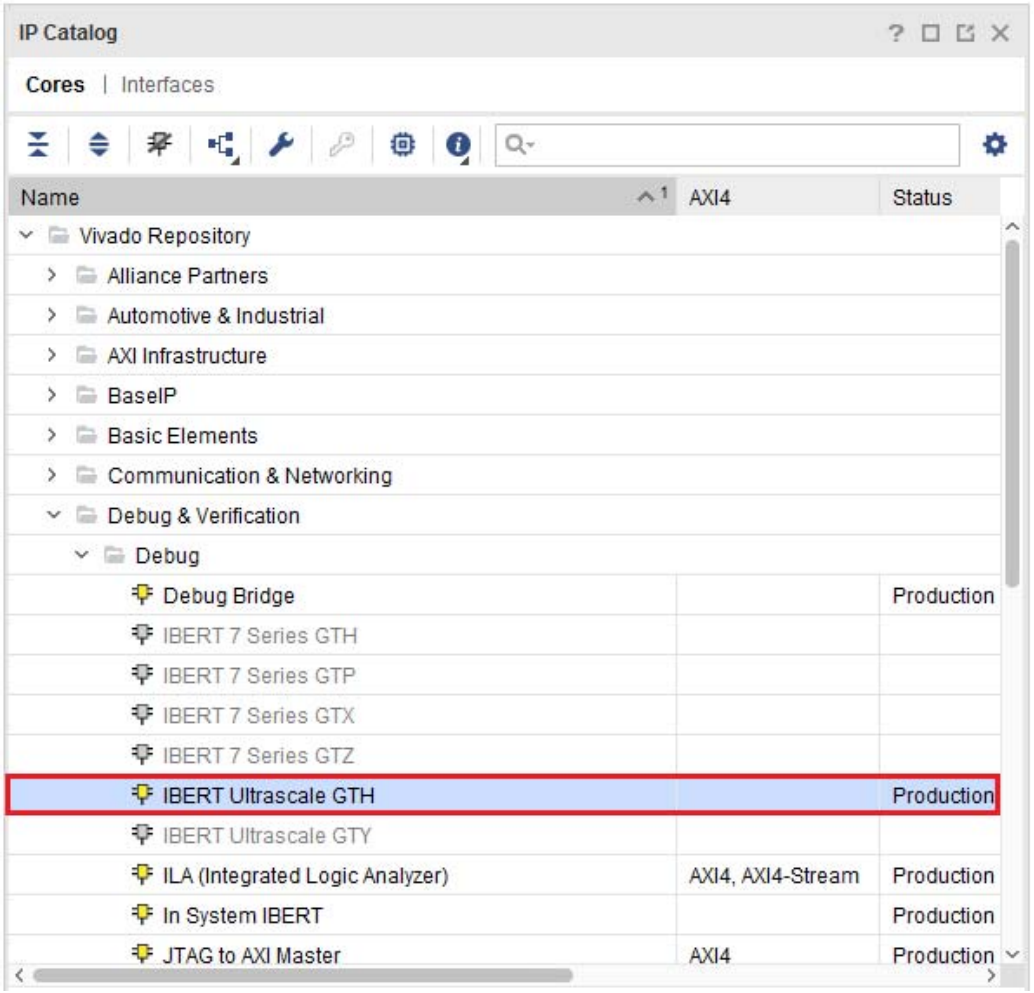

Figure 2-4: **IP Catalog**

6. A **Customize IP** window opens. In the Protocol Definition tab, set the **LineRate (Gb/s)** to **12.5 Gbps**. Change **Refclk (MHz)** to **125**. Keep defaults for other fields (Figure 2-5).

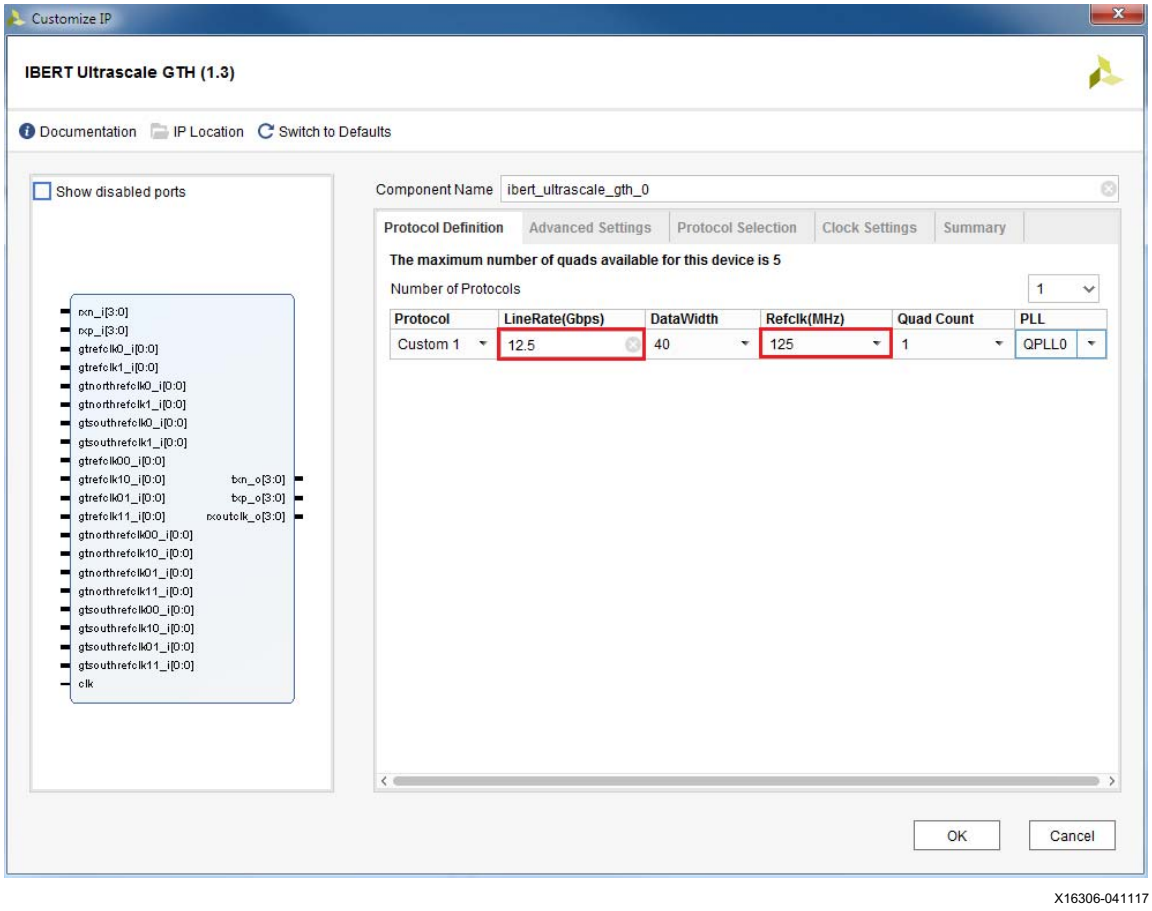

Figure 2-5: **Customize IP – Protocol Definition**

7. In the **Protocol Selection** tab, use the **Protocol Selected** drop-down menu next to QUAD_224 to select **Custom 1/12.5 Gb/s** and select **MGTREFCLK0 224** from the REFCLK Selection menu (Figure 2-6).

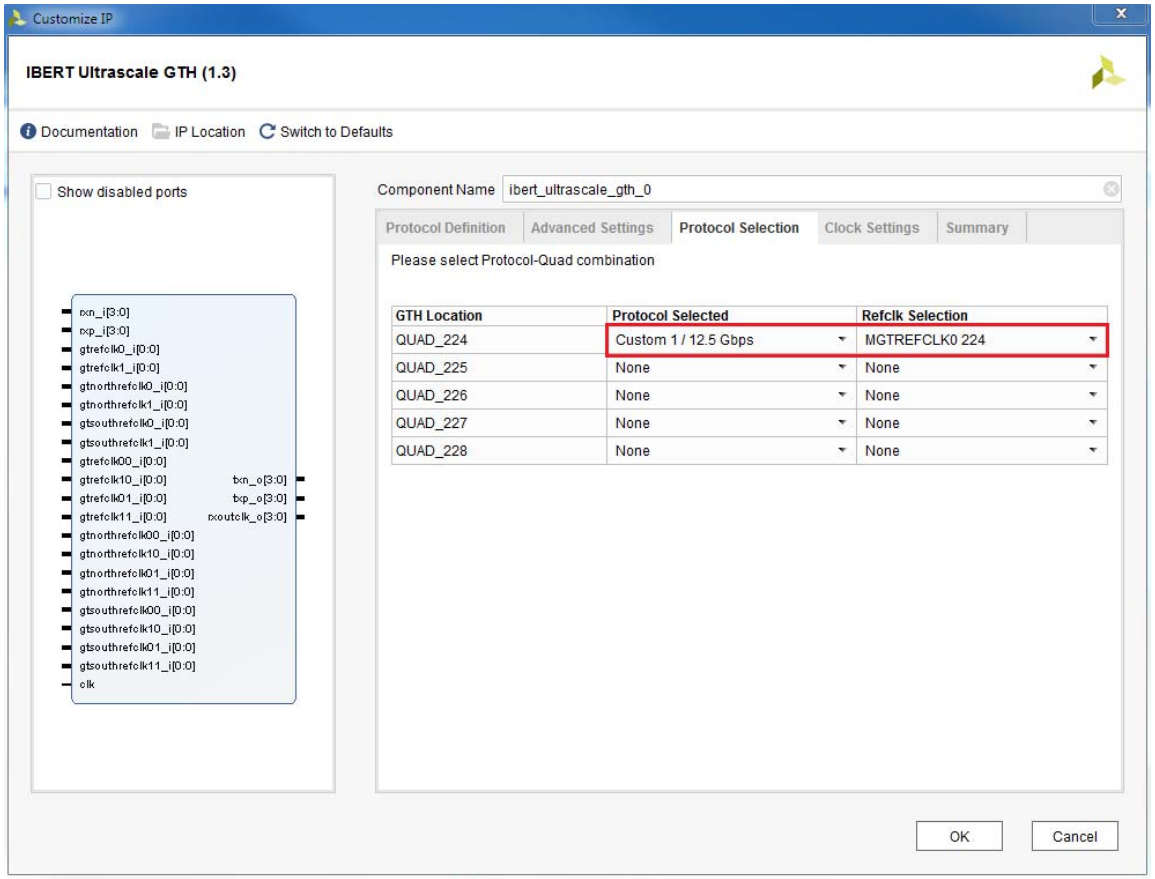

Figure 2-6: **Customize IP – Protocol Selection**

8. In the **Clock Settings** tab, select **DIFF SSTL15** for the I/O Standard, enter **E18** for the P Package Pin (the FPGA pins to which the system clock is connected), and make sure the **Frequency (MHz)** is set to **300** (Figure 2-7). Click **OK**.

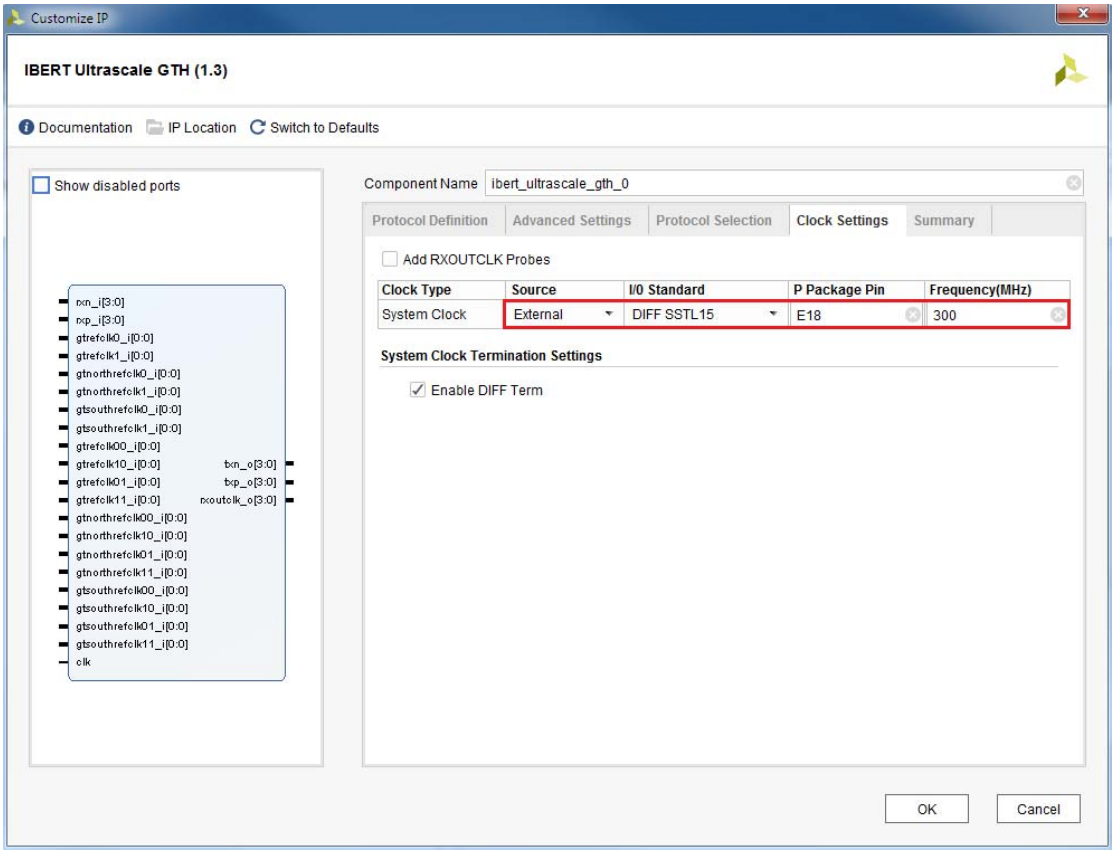

Figure 2-7: **Customize IP - Clock Settings**

9. From the **Project Manager** window, in the **Sources** window, right-click the **IBERT IP** and select **Open IP Example Design** (Figure 2-8). Specify a location to save the design, click **OK**, and the example design launches in a new Vivado Design Suite window.

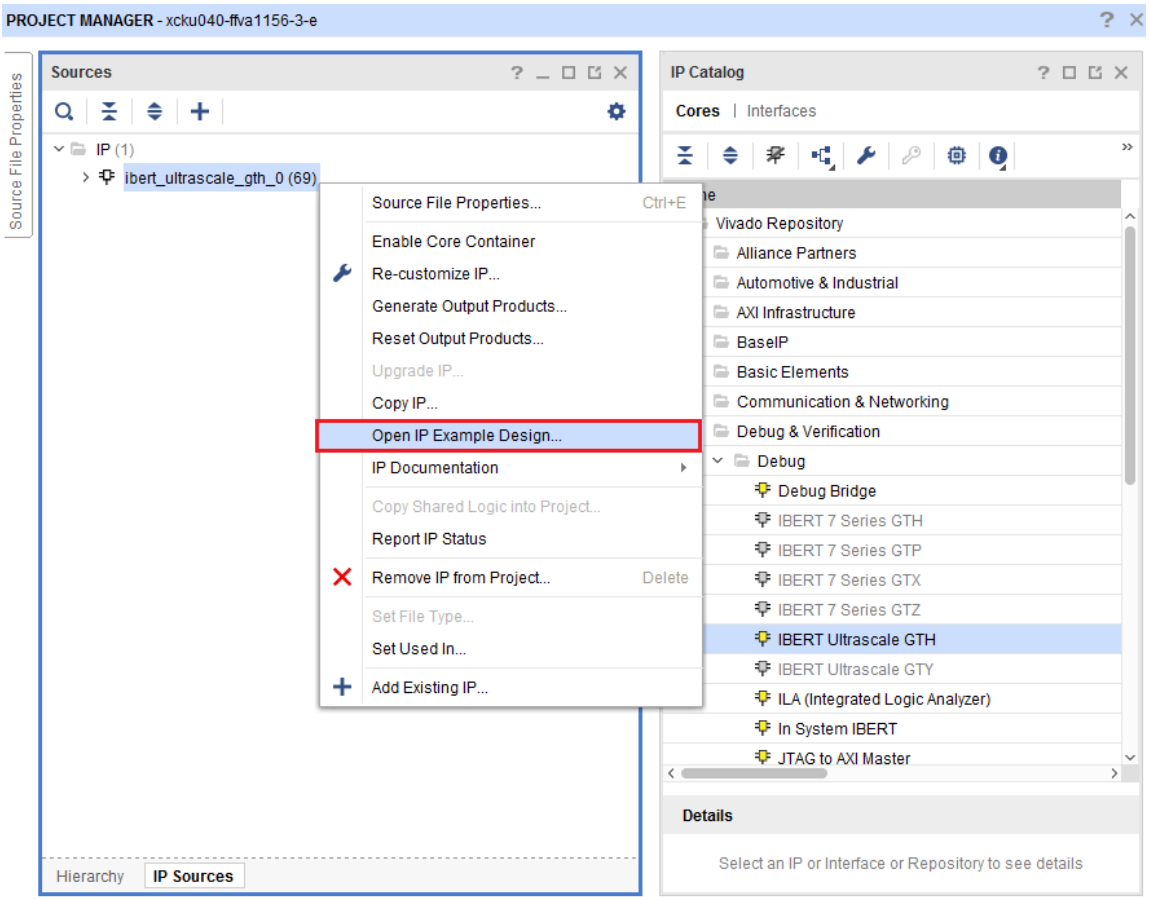

Figure 2-8: **Open IP Example Design**

10. In the **Sources** window, Design Sources should now show the IBERT design example (Figure 2-9).

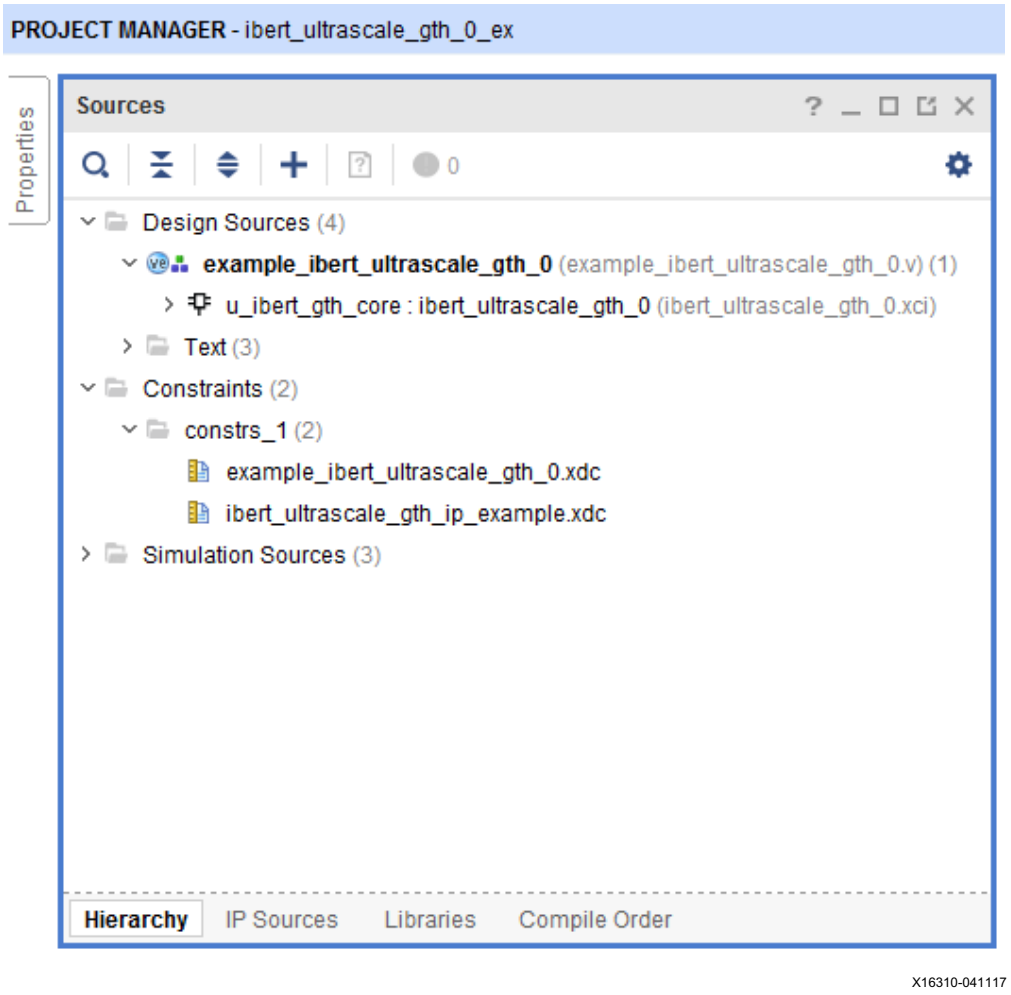

Figure 2-9: **Design Sources File Hierarchy**

11. Click **Run Synthesis** from the **Flow Navigator** to synthesize the design (Figure 2-10).

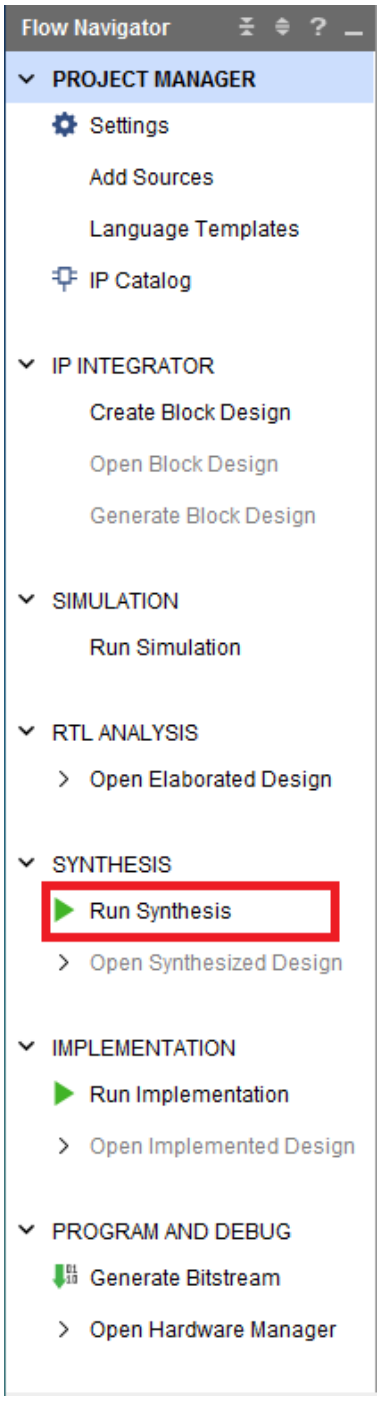

Figure 2-10: **Run Synthesis**

12. When the synthesis is done, a **Synthesis Completed** window opens. Select **Run Implementation** and click **OK** (Figure 2-11).

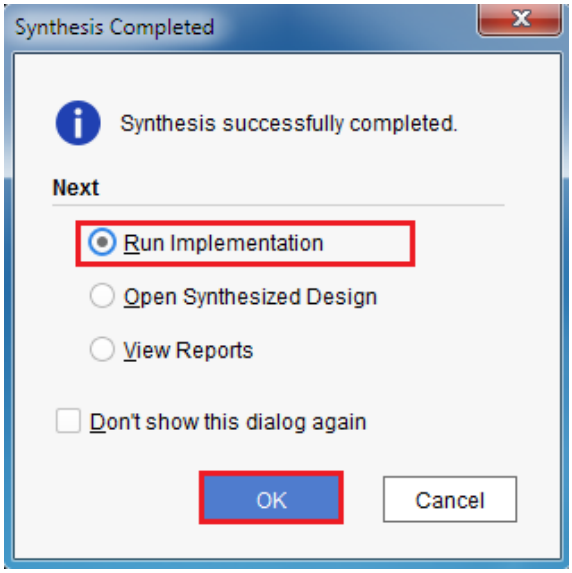

Figure 2-11: **Synthesis Completed**

13. When the implementation is done, an **Implementation Completed** window opens. **Select Generate Bitstream** and click **OK** (Figure 2-12).

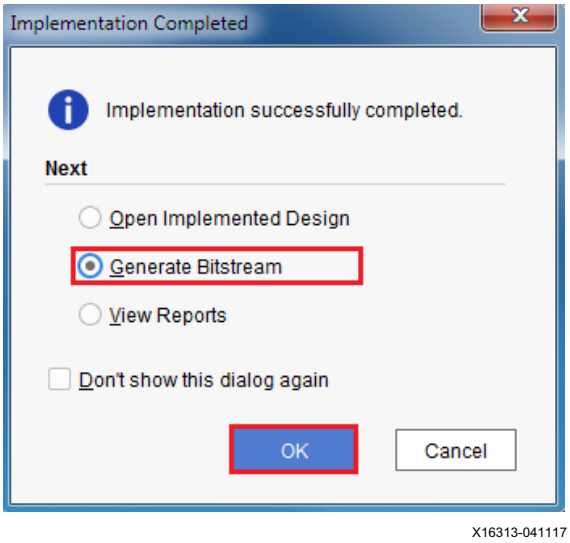

Figure 2-12: **Implementation Completed**

14. When the **Bitstream Generation Completed** dialog window appears, click **Cancel** (Figure 2-13).

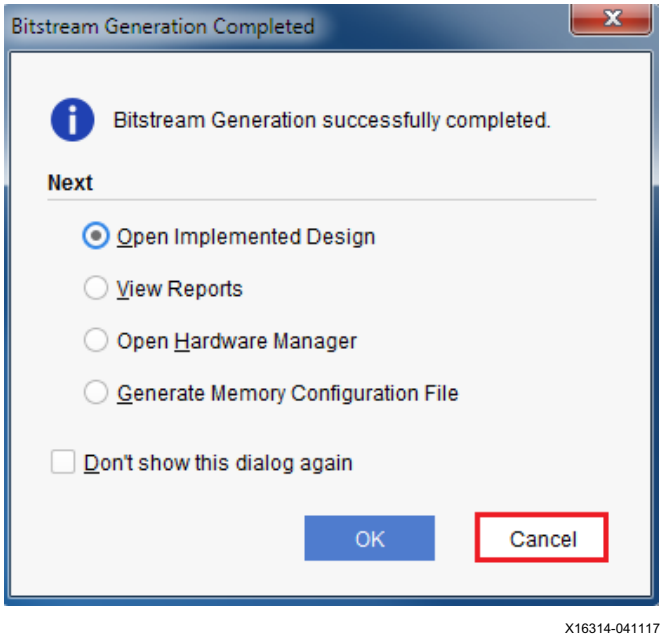

Figure 2-13: **Bitstream Generation Complete**

15. Navigate to the `...\ibert_ultrascale_gth_0_example\ibert_ultrascale_gth_0_example.runs\impl_1` directory to locate the generated bitstream.

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- On the Xilinx website, see the Design Hubs page.

Note: For more information on Documentation Navigator, see the Documentation Navigator page on the Xilinx website.

References

The most up to date information related to the KCU1250 kit and its documentation is available on these websites.

Kintex UltraScale FPGA KCU1250 Characterization Kit

Kintex UltraScale FPGA KCU1250 Characterization Kit documentation

Kintex UltraScale FPGA KCU1250 Characterization Kit Master Answer Record (AR 63058)

These Xilinx documents provide supplemental material useful with this guide:

1. *KCU1250 Board User Guide* (UG1057)
2. *HW-CLK-101-SCLK2 SuperClock-2 Module User Guide* (UG770)
3. *Silicon Labs CP210x USB-to-UART Installation Guide* (UG1033)
4. *UltraScale Architecture Configuration User Guide* (UG570)
5. *Vivado Design Suite User Guide: Programming and Debugging (*UG908)
6. *Kintex UltraScale FPGAs Data Sheet: DC and AC Switching Characteristics* (DS892)
7. *Zynq-7000 All Programmable SoC Overview* (DS190)
8. *UltraScale Architecture GTH Transceivers User Guide* (UG576)
9. *Vivado Design Suite User Guide: Getting Started* (UG910)
10. *Tera Term Terminal Emulator Installation Guide* (UG1036)
11. *UltraScale FPGAs Transceivers Wizard LogiCORE IP Product Guide* (PG182)

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