SmartLynq+ Module User Guide

UG1514 (v1.0) March 8, 2021

Revision History

The following table shows the revision history for this document.

Section	Revision Summary
03/08/2021 Version 1.0	
Initial release.	N/A

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Overview

The Xilinx® SmartLynq+ Module is a high-speed debug and trace module, primarily targeting the Versal™ adaptive compute acceleration platform (ACAP). It drastically improves configuration and trace speed. For trace capture, the SmartLynq+ module is capable of speeds up to 10 Gb/s by means of its high-speed debug port (HSDP), which is 100 times faster than standard JTAG. Faster iterations and repetitive downloads increase development productivity and reduce the design cycle.

Features

The SmartLynq+ Module provides the following features:

- Super-fast download speed, maximize development productivity for faster iterations
- High-speed trace with enhanced visibility, up to 14 GB of trace memory for execution history
- Full visibility for heterogeneous architectures, in-depth debug for Hard IP and Engines in Versal ACAP
- Cohesive and time-related debug of all subsystems
- Flexible and smart debug platform with features such as smart filtering and a software-programmable built-in debugger
- Sharable debug platform with unified view for remote, multi-user environment

***Note*:** The SmartLynq+ Module is not supported by Xilinx ISE® tools.

Description

The SmartLynq+ Module offers high-bandwidth connectivity to allow heterogenous system debug and trace of Versal ACAP-based applications. It provides all of the desired connections for programming, debug and trace. JTAG can be a direct connection with PC4 connector, MICTOR-38 connector, or via USB-C when used along with HSDP.

The contents of the SmartLynq+ Module kit are shown in the following figure.

Figure 1: **SmartLynq+ Module Kit Contents**

Physical Description

The SmartLynq+ module circuitry is housed in a plastic enclosure with an OLED display, as shown in the following figure. The enclosure and heat sink assembly attenuates internally generated emissions and protects against susceptibility to radiated emissions.

Figure 2: **SmartLynq+ Module**

CAUTION! *The SmartLynq+ module is designed to operate in the temperature range of 10°C to 26°C (50°F to 80°F). Operating outside of this range might cause malfunction or permanent damage to the device.*

Connectors

Connectors on the SmartLynq+ Module are located as follows.

Host Side

The DC power, USB 3.0, and Ethernet connectors are located on the left side of the SmartLynq+ Module, as shown in the following figure.

Figure 3: **Host-Side Connections**

Power to the SmartLynq+ Module is supplied by a 12V / 2A DC module connected to the Power connector. Note that when the DC module is connected to the power connector, the SmartLynq+ Module turns on. The Ethernet connector is always active when the cable is powered. When an ethernet cable is connected to the SmartLynq+ module, the cable initializes the ethernet port and a host can communicate with it by using the IP address shown on the display screen. The USB 3.0 is an alternate host interface that can be used for host communication. The USB 3.0 interface is also active upon power up and initializes on connection to an active USB connection.

Target Side

The GPIO, JTAG, HSDP, and MICTOR connectors are on the right side of the SmartLynq+ Module, as shown in the following figure.

Figure 4: **Target-Side Connections**

For standard HSDP communication use the HSDP connector. Typically, this is the only connection required to a target board such as the Versal ACAP VCK190 evaluation board. For target boards without the HSDP connector use the 14 pin JTAG connector using a ribbon cable or flying leads. The GPIO cable provides additional low-speed signals for controlling the target or other instruments used alongside the board under test.

Front View

The reset pin, mode selector switch, and micro-SD card slot are located on the front of the SmartLynq+ Module, as shown in the following figure.

Figure 5: **Front View Connections**

The SmartLynq+ Module MODE switch setting determines the source from which the module boots. When the mode is set towards MICRO SD, the module boots using the SD card image. When the MODE switch is set away from MICRO SD, the module boots from the EMMC image. Note that you must have written an image to the eMMC for the system to boot properly.

Installing the SmartLynq+ Module

Prior to using the SmartLynq+ Module you need to download the latest SD card image and the SmartLynq+ application software. Go to the SmartLynq+ Module wiki page to access the download links and installation instructions:

USB 3.0 Host Connection

The SmartLynq+ Module can be accessed by a host system using the USB 3.0 connection. When accessing the module through the USB 3.0 interface, the host establishes a network interface used by applications such as Vivado® Design Suite to communicate with the module. Vivado Design Suite version 2020.2 or later is required to support the SmartLynq+ Module for USB3.0 and HSDP.

Note: The SmartLynq+ Module is not powered by the USB 3.0 interface and must have the power cable plugged in and supplying power prior to use.

Minimum Host System Requirements

These are the supported operating systems on x86 and x86-64 processor architectures:

- Microsoft Windows Professional/Enterprise 10.0 1809 Update; 10.0 1903 Update; 10.0 1909 Update; 10.0 2004 Update
- Red Hat Enterprise Workstation/Server 7.4 - 7.8, and 8.2 (64-bit), English/Japanese
- CentOS 7.4 - 7.8, and 8.2 (64-bit), English/Japanese
- Ubuntu Linux 16.04.5 LTS;16.04.6 LTS; 18.04.1 LTS; 18.04.2 LTS, 18.04.3 LTS; 18.04.4 LTS; and 20.04 LTS (64-bit), English/Japanese

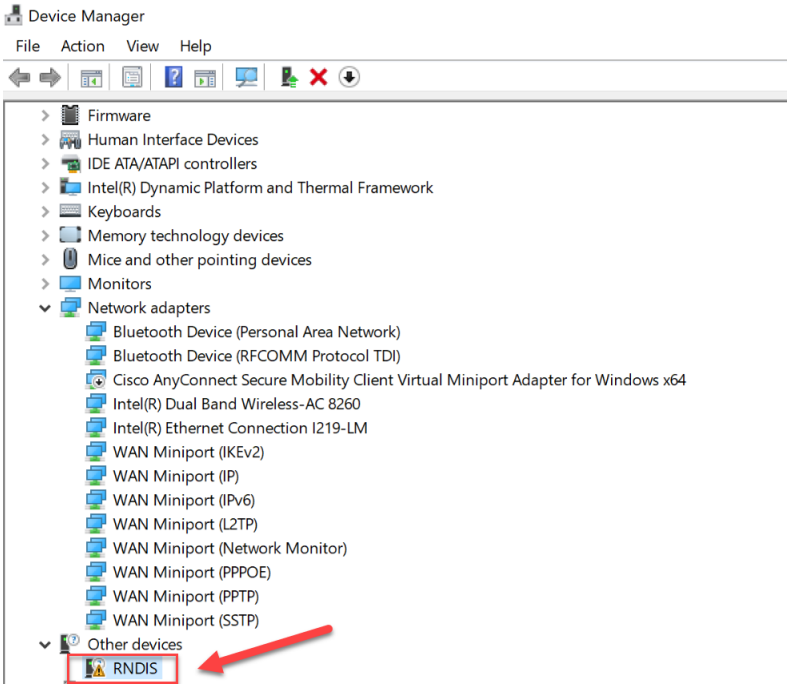
Default USB 3.0 IP Setting

The default factory image setting for the SmartLynq+ Module USB 3.0 interface is 10.0.0.2. Ensure that 10.0.0.2 IP on the host machine can be used to form a local network for the SmartLynq+ Module. If necessary, you can change this setting but you still need to have the host initially access 10.0.0.2 to be able to change the USB 3.0 IP factory setting.

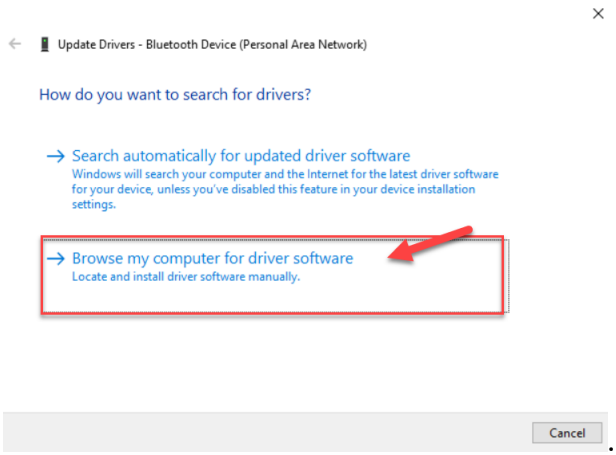
Windows USB 3.0 Driver Setup

The Windows 10 included RNDIS driver needs to be associated with the SmartLynq+ Module. These are the steps to associate the cable to the driver. You might need to repeat these steps if you connect the SmartLynq+ Module to a different port on the Windows PC.

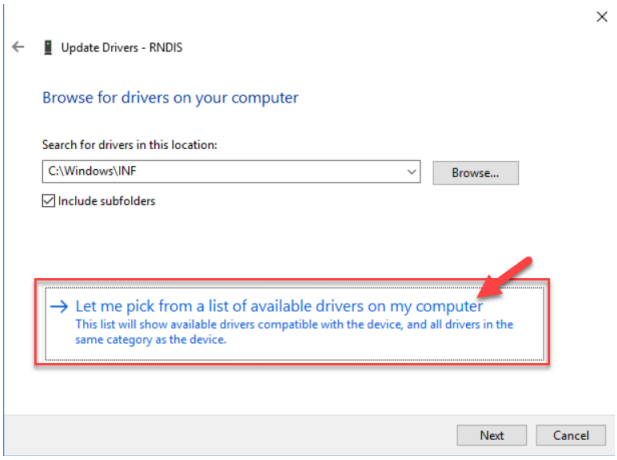
1. Connect the SmartLynq+ Module to a Windows PC using the USB-B cable.
2. Open Device Manager. You should see a device named RNDIS.



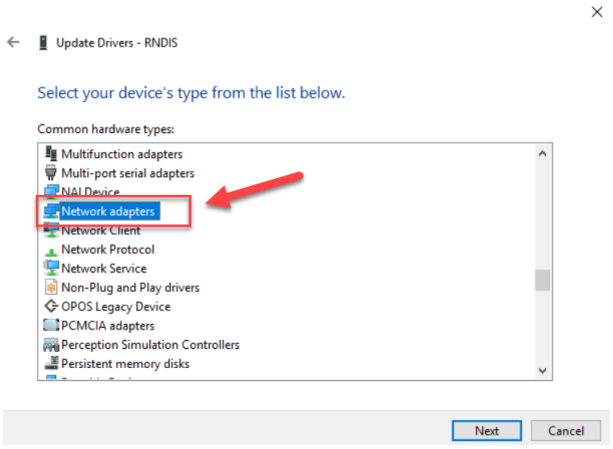
3. Right-click the RNDIS device and click **Update Driver**.
4. A new window pops up. Click **Browse my computer for driver software**.



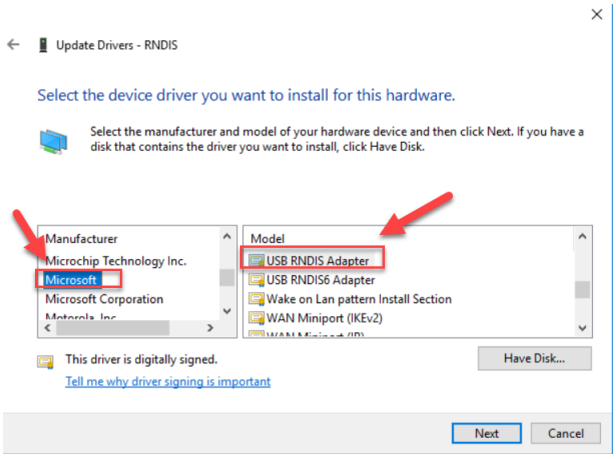
5. Click **Let me pick from a list of available drivers of my computer**.



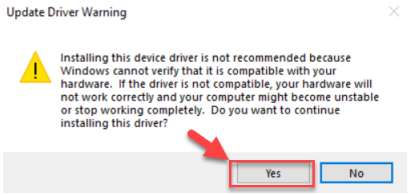
6. Select *Network adapters* from the list and click **Next**.



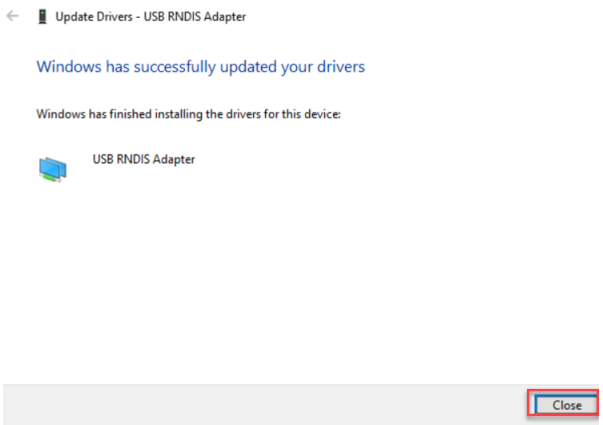
7. Select *Microsoft* from the Manufacturer list and select *USB RNDIS Adapter* from the Model list. Click **Next**.



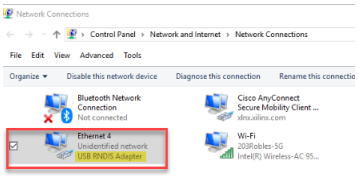
8. You will now see an *Update Driver Warning*. Click **Yes** to proceed.



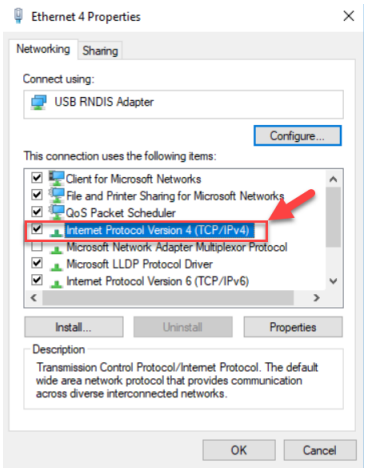
9. You should now see the driver successfully installed.



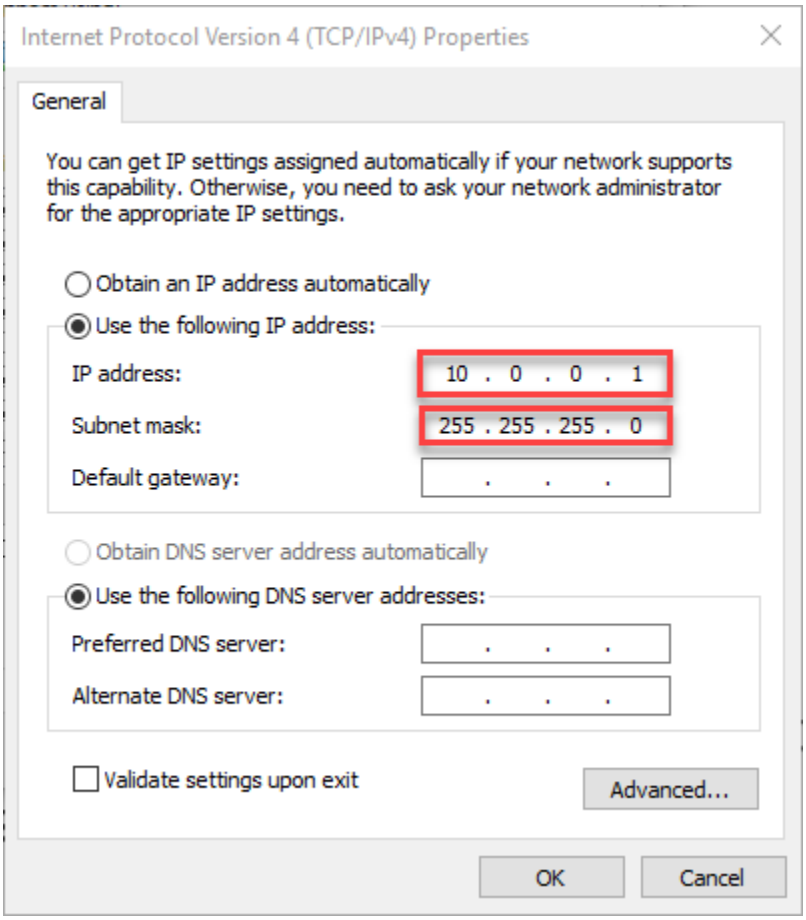
10. Open the Windows network connections panel.
11. You should see a device with the description *USB RNDIS Adapter*.



12. Right-click this adapter and click **Properties**.
13. Select *Internet Protocol Version 4 (TCP/IPv4)* from the list and click **Properties**.



14. A new window pops up. Configure the network interface as follows and click **OK**.



15. You should now be able to access the SmartLynq+ Module at 10.0.0.2

Linux USB 3.0 Setup

Run the `ifconfig` command to configure the network interface on the IP address Linux assigned to the SmartLynq+ Module. Linux assigns the IP address as 10.0.0.2. Run `ifconfig` to view the currently active network interfaces on this system. For example:

```
eth0      Link encap:Ethernet HWaddr D7:45:89:22:88:97
          inet addr:172.19.3.148 Bcast:172.19.3.255 Mask:255.255.252.0 UP
BROADCAST
RUNNING MULTICAST MTU:1500 Metric:1
          RX packets:2278375690 errors:0 dropped:307 overruns:0 frame:0 TX
packets:2305014867 errors:0 dropped:22 overruns:0 carrier:0 collisions:0
txqueuelen:1000
          RX bytes:1026403610964 (955.9 GiB) TX bytes:1048839754879 (976.8
GiB)
          Interrupt:17

lo        Link encap:Local Loopback
```

```
        inet addr:127.0.0.1 Mask:255.0.0.0
        UP LOOPBACK RUNNING MTU:16436 Metric:1
        RX packets:41586323 errors:0 dropped:0 overruns:0 frame:0 TX
packets:41586323
errors:0 dropped:0 overruns:0 carrier:0 collisions:0 txqueuelen:0
        RX bytes:107897957583 (100.4 GiB) TX bytes:107897957583 (100.4 GiB)
```

If none of the interface names have an internet address that is part of the protocol address family that covers the assigned SmartLynq+ Module address, use `ifconfig` to configure a new interface.

In the preceding example, the Linux system has two interfaces defined: `eth0` and `lo`. Neither interface has an internet address format of 10.0.x.x that includes the address 10.0.0.2 assigned to SmartLynq+ Module. Set up the interface by running `ifconfig` with the following arguments:

```
sudo ifconfig eth1 10.0.0.1 netmask 255.255.0.0
```

Running `ifconfig` again shows the new interface:

```
eth0      Link encap:Ethernet HWaddr D7:45:89:22:88:97
        inet addr:172.19.3.148 Bcast:172.19.3.255 Mask:255.255.252.0 UP
BROADCAST
RUNNING MULTICAST MTU:1500 Metric:1
        RX packets:2278375690 errors:0 dropped:307 overruns:0 frame:0 TX
packets:2305014867 errors:0 dropped:22 overruns:0 carrier:0 collisions:0
txqueuelen:1000
        RX bytes:1026403610964 (955.9 GiB) TX bytes:1048839754879 (976.8
GiB)
        Interrupt:17

eth1      Link encap:Ethernet HWaddr 00:5D:03:00:00:01
        inet addr:10.0.0.1 Bcast:10.0.255.255 Mask:255.255.0.0 UP BROADCAST
RUNNING MULTICAST MTU:1500 Metric:1
        RX packets:10 errors:0 dropped:0 overruns:0 frame:0 TX
packets:2 errors:0 dropped:0 overruns:0 carrier:0 collisions:0
txqueuelen:1000
        RX bytes:2396 (2.3 KiB) TX bytes:345 (345.0 b)

lo        Link encap:Local Loopback
        inet addr:127.0.0.1 Mask:255.0.0.0
        UP LOOPBACK RUNNING MTU:16436 Metric:1
        RX packets:41586323 errors:0 dropped:0 overruns:0 frame:0 TX
packets:41586323
errors:0 dropped:0 overruns:0 carrier:0
        collisions:0 txqueuelen:0
        RX bytes:107897957583 (100.4 GiB) TX bytes:107897957583 (100.4 GiB
```

Changing the USB 3.0 IP Setting

To change the default USB 3.0 IP address setting on the SmartLynq+ Module you first need to set up the host to communicate using the 10.0.0.2 IP default address. To change the IP address, connect the host to the module using ssh on the host machine and passing in the IP address 10.0.0.2. When prompted for a user name and password, enter in the default user name *xilinx* with the password *xilinx*.

After logging into the SmartLynq+ Module, run the following command to edit the USB network settings:

```
sudoedit /etc/systemd/network/20-usb-gadget.network
```

This command brings up a linux nano editor where you can adjust the settings as needed. The following are the default settings:

```
[Match]
Name=usb0
[Network]
Address=10.0.0.2/24
Gateway=10.0.0.1
```

Reset the SmartLynq+ Module to update the USB interface.

Ethernet Connection

By default, the SmartLynq+ Module's Ethernet connection is configured to use DHCP to obtain the cable's IP address. When you connect the cable to a network with a DHCP server, the module obtains an IP address and shows the value on the display. This value can be used to connect to the module. If you need to reserve a MAC address for the module you can inspect the label on the bottom of the module for the unique MAC address value.

Changing the Ethernet IP Settings

To change the default factory Ethernet IP settings you need to first ssh to the SmartLynq+ Module. You can use the USB 3.0 interface to make the Ethernet changes. When prompted for a user name and password, enter in the default user name *xilinx* with the password *xilinx*.

After logging into the SmartLynq+ Module, run the following command to edit the usb network settings:

```
sudoedit /etc/systemd/network/20-eth0.network
```

This command brings up a Linux nano editor where you can adjust the settings as needed. The following are the default settings:

```
[Match]
Name=eth0

[Network]
DHCP=ipv4
#Address=10.101.0.101/24
#Gateway=10.101.0.1
```

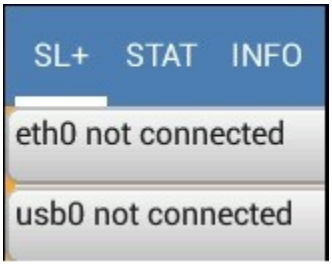
To set a static address, remove the # on Address and Gateway lines and set them as needed while adding a # at the beginning of the DHCP line. After the edits are complete, save the file.

To update the Ethernet interface, reset the SmartLynq+ Module or run the following command:

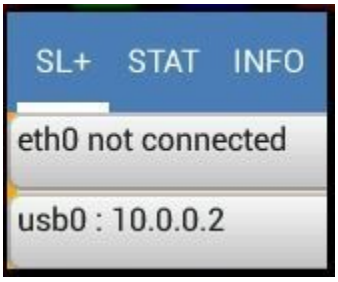
```
sudo systemctl restart systemd-networkd
```

SmartLynq+ Module Display

The SmartLynq+ Module display provides general information about the module and allows some tasks to be performed. The following SL+ menu is the default menu displayed at power up when no connections are active:



The SL+ tab displays the IP address when a connection is active:



Use the up and down arrow keys to select different tabs. These keys transition from the SL+ (SmartLynq+) tab to the STAT (status) tab and to the INFO (information) tab. The drop-down menu in the STAT tab allows drilling down into various sub menus by pressing the select button on the STAT tab. The INFO tab shows software build information.

JTAG Target Interface

The JTAG target interface uses a standard 14-pin connector. Xilinx recommends using the provided 6-inch ribbon cable or 6-inch flying leads to connect the SmartLynq+ Module to the JTAG interface on the target board, as shown in the following figure.

Figure 6: **SmartLynq+Module JTAG Connection to the JTAG Interface on a Target Board**

To take advantage of the ribbon cable, a mating connector must be incorporated into the target board, as is implemented on Xilinx evaluation boards. This connector is normally installed only during prototype development. When the production hardware is functional and the JTAG devices can be configured from alternate sources, the connector can be eliminated from the board cost. Maintaining the footprint for this connector is recommended if space permits.

The connector has a 2-mm shrouded, keyed header. (See the *Header Manufacturers* table in Chapter 8: GPIO Target Interface for Vendor part numbers.) Mating connectors for attaching the high-performance ribbon cable to the JTAG port on a target board are available in both through-hole and surface-mount configurations.

Shrouded and keyed versions should always be used to guarantee proper orientation when inserting the cable. The connector requires 105 mm2 of board space. The target board voltage applied to pin 2 of the JTAG connector is used as a power source for the output buffers that drive the output pins. Target interface connector details including dimensions, signal assignments, pin descriptions, vendor part numbers, DC electrical and switching characteristics, and timing are provided in the following tables and figures.

Figure 7: **Dimensions and Signal Assignments**

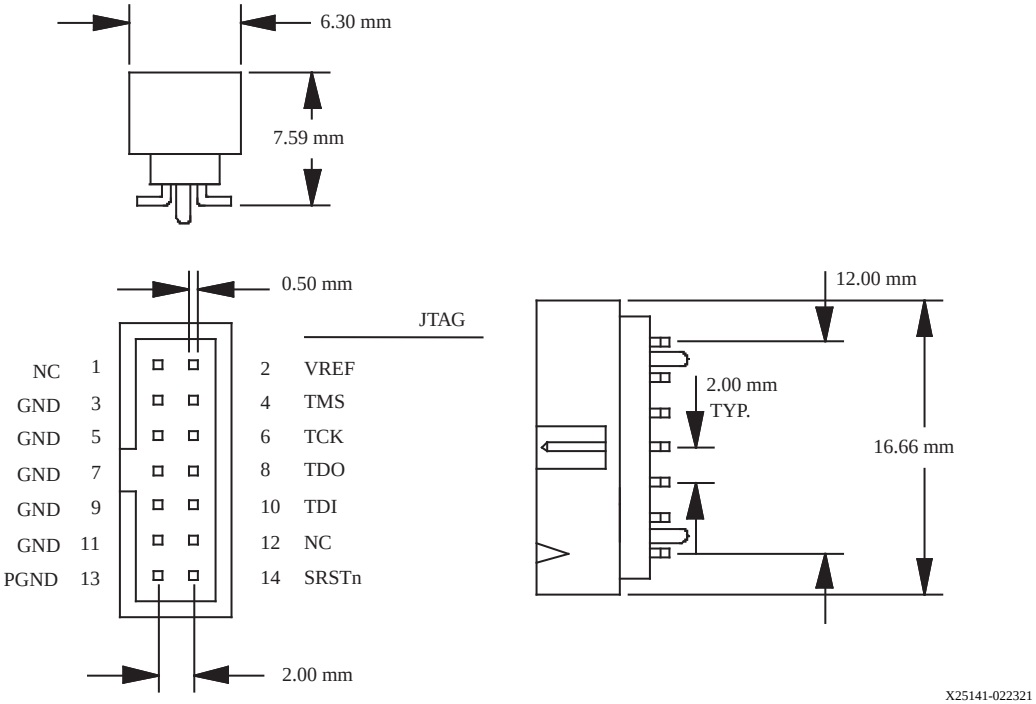


Table 1: **Interface Pin Descriptions**

Pin Number	Pin Name	Direction	Description
2	V_{REF}	In	**Target Reference Voltage.** Connected to a voltage bus on the target board that serves the JTAG interface.
4	TMS	Out	**JTAG Test Mode Select.** JTAG mode signal establishing appropriate TAP state transitions on all target JTAG devices.
6	TCK	Out	**JTAG Test Clock.** Clock signal for JTAG operations connected to the TCK pin on all target JTAG devices sharing the same data stream.
8	TDO	In	**JTAG Test Data Out.** Serial data stream received from the TDO pin on the last device in a JTAG chain.

Table 1: **Interface Pin Descriptions** *(cont'd)*

Pin Number	Pin Name	Direction	Description
10	TDI	Out	**JTAG Test Data In.** Outputs the serial data stream transmitted to the TDI pin on the first device in a JTAG chain.
13	PGND	Out	**JTAG Pseudo Ground.** Use of this pin is optional, if unused it can be left with no connection. PGND is LOW during JTAG operation.
14	SRST	Out	**System Reset.** Use of this pin is optional, if unused it can be left with no connection. Host applications can customize the behavior of this signal.

Table 2: **Mating Connectors for 2 mm pitch, 14-Conductor Ribbon Cable**

Manufacturer	SMT, Vertical	Through-Hole, Vertical	Through-Hole, Right Angle	Website
Molex	87832-1420	87831-1420	87833-1420	www.molex.com

Table 3: **DC Electrical Characteristics**

Symbol	Description	Conditions	Min.	Max.	Unit
V_{OH}	High-level output voltage	V_{REF} = 1.65V, I_{OH} = –8 mA	1.2	-	V
		V_{REF} = 2.3V, I_{OH} = –9 mA	1.7		
		V_{REF} = 3V, I_{OH} = –12 mA	2.3		
V_{OL}	Low-level output voltage	I_{OL} = 8 mA	-	0.4	V
		I_{OL} = 9 mA		0.5	
		I_{OL} = 12 mA		0.7	
V_{IH}	High-level input voltage	V_{REF} = 1.2V to 1.35V	0.78	-	V
		V_{REF} = 1.35V to 1.65V	0.88		
		V_{REF} = 1.65V to 1.95V	1.1		
		V_{REF} = 1.95V to 2.7V	1.6		
		V_{REF} = 2.7V to 3.3V	2		
V_{IL}	Low-level input voltage	V_{REF} = 1.2V to 1.95V	-	0.4	V
		V_{REF} = 1.95V to 2.7V		0.7	
		V_{REF} = 2.7V to 3.3V		0.8	
I_{CC}	Dynamic current	-	-	110	mA

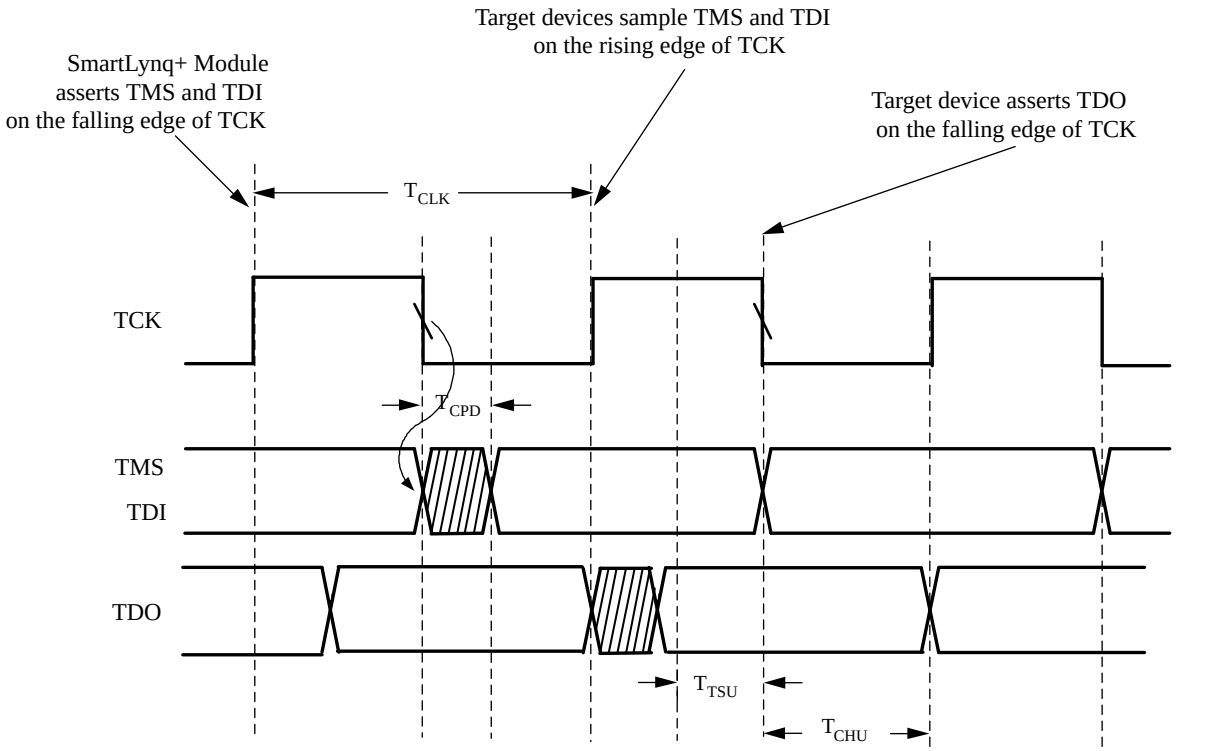
Table 4: **Switching Characteristics**

Symbol	Description	Conditions	Min.	Max.	Unit
T_{CLK}	Clock period with 50% duty cycle	50 kHz to 100 MHz	10	8,000	ns
T_{CPD}	Cable Propagation Delay Time (TDI or TMS relative to the negative edge of TCK)	V_{REF} = 1.2V to 3.3V	-	1	ns
T_{TSU}	Cable Setup Time (TDO relative to the negative edge of TCK)	V_{REF} = 1.2V to 3.3V	1	-	ns

Table 4: **Switching Characteristics** *(cont'd)*

Symbol	Description	Conditions	Min.	Max.	Unit
T_{CHU}	Cable Hold Time (TDO relative to the negative edge of TCK)	V_{REF} = 1.2V to 3.3V	1	-	ns

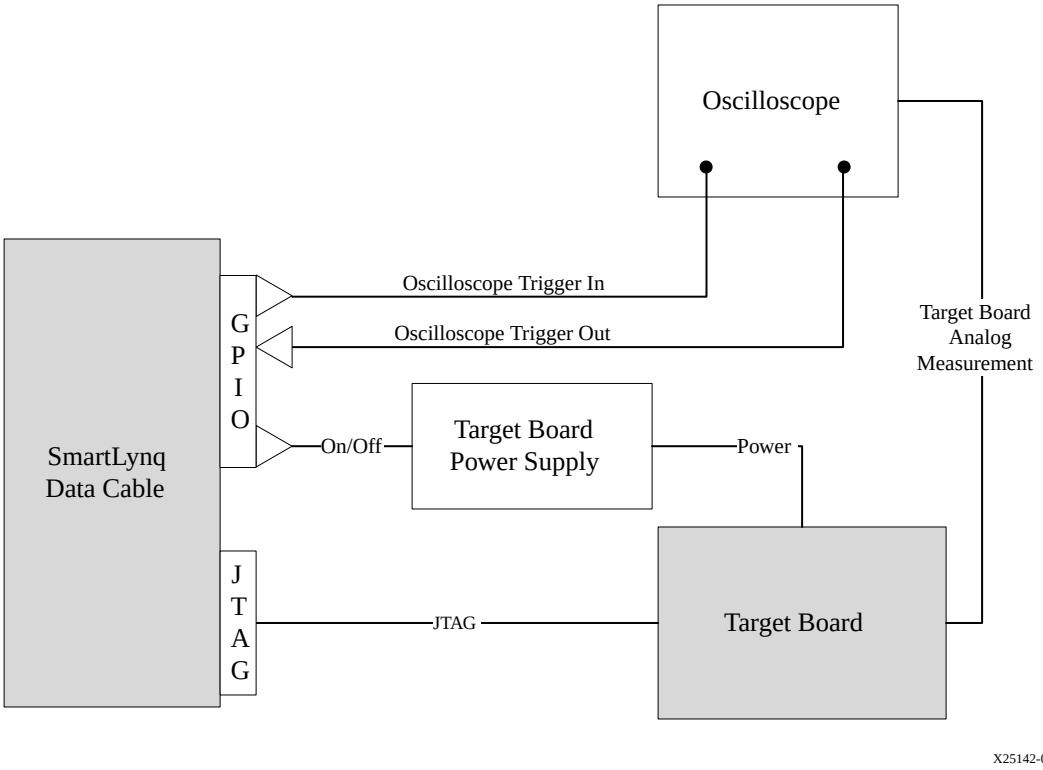
Figure 8: **SmartLynq+ Module Timing Diagram**



GPIO Target Interface

The SmartLynq+ Module GPIO can be used for a variety of basic input/output operations on the target board. The following figure shows a sample setup where the SmartLynq+ Module is connected to an oscilloscope, power supply, and a target board.

Figure 9: **Sample Setup: SmartLynq+ Module to an Oscilloscope**



In this setup, the SmartLynq+ Module uses an output from the GPIO pins to drive a trigger input to the oscilloscope. The oscilloscope drives an input to module to allow monitoring a trigger event from the oscilloscope. With this arrangement, it is possible to take analog measurements with the oscilloscope and synchronize trigger events with the SmartLynq+ Module. The figure also shows how a power supply or relay could be controlled through the GPIO port so as to power on/off the target board. Thus, through the GPIO ports, it is possible to simplify the driving and sensing of additional instruments connected to the target system. Note that the latency of such a trigger is unpredictable because these are software-driven triggers.

The GPIO 2x6 connector, shown in the following figure, is available for 8-bit static read/write operations. The 8-bit GPIO interface does not turn on until the GPIO_VREF pin 11 on the GPIO 2x6 interface is powered by 3.3V. You can attach flying leads to any of the standard 0.1-inch headers listed in the following table to connect to the GPIO interface.

Figure 10: **GPIO Connector**

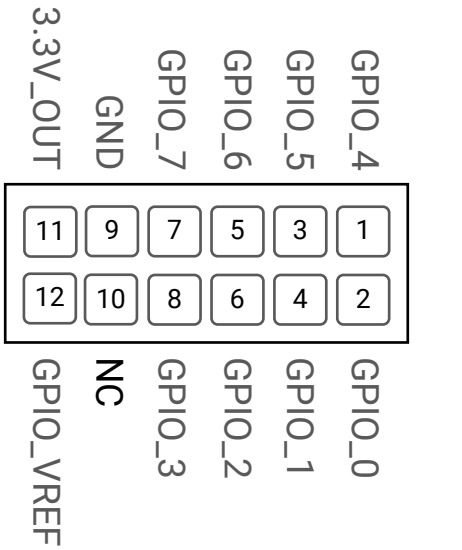


Table 5: **Header Manufacturers**

Manufacturer	Part Number
Samtec	TSW-106-23-S-D
Amphenol FCI	67997-212HLF
3M	929836-01-06-RK
Hirose	A1-12PA-2.54DSA(71)
Sullins	PBC06DAAN

The 8-bit general purpose read/write interface is controlled by the update_hw_gpio shell command. The GPIO interface defaults to read mode on power-on-reset. The format of this command is as follows:

```
update_hw_gpio <direction> <value>
```

The <direction> is an 8-bit hexadecimal value. Bits set to 1 in the <direction> field are set as outputs. Otherwise the pin is used as an input. The second optional *value* argument is used for specifying how to drive the pins that are set as outputs. Note that setting the direction to 0xff makes all pins outputs. The following is an example of how to use this command when logged in over ssh:

```
sudo /opt/xilinx/bin/update_hw_gpio 0x3f 0xe7
```

This does the following:

- <direction> 0x3f sets pin 0 to 5 as outputs; 6 and 7 as inputs
- <value> 0xef sets the output values: pin 0 = 1, pin 1 = 1, pin 2 = 1, pin 3 = 0, pin 4 = 0, pin 5 = 1

HSDP Target Interface

HSDP support can be added to a board by adding a USB-C connector and connecting up the high speed lines to Versal ACAP dedicated HSDP GT ports, as shown in the following figure. By making use of the custom protocol support allowed by the USB-C/USB 3.0 specification, a board can readily have basic HSDP support with just the addition of the HSDP connector. However, because it is necessary to first initialize a Versal ACAP with an initial image, a target must have the JTAG interface connected to the SmartLynq+ Module. When performing the initial bring up of a Versal ACAP it is also helpful to make use of a UART to gain further observability of the system. For this reason it is very useful to integrate all these debug capabilities through a single connector. As a result the HSDP debug connector has a superset option that fully enables you to gain essential observability with a minimum connector footprint with an added benefit of scalable debug support.

Figure 11: **SmartLynq+ to HSDP on a Target Board**

The following table and figures show two options for the HSDP interface. Note that each option has tradeoffs that must be considered by the end user. For the greatest observability use option 1. For reduced observability use option 2. The table provides a quick summary with the pros/cons of the various options.

Table 6: **HSDP Interface Options**

Option	Description	Pro	Con
1	HSDP with FTDI JTAG	One connector integrates all essential debug observability	Extra cost incurred by by FTDI and related support parts/power
2	HSDP with PC4 JTAG	Lower cost and reduced real estate	No integrated UART support

Figure 12: **Option 1: HSDP with FTDI JTAG**

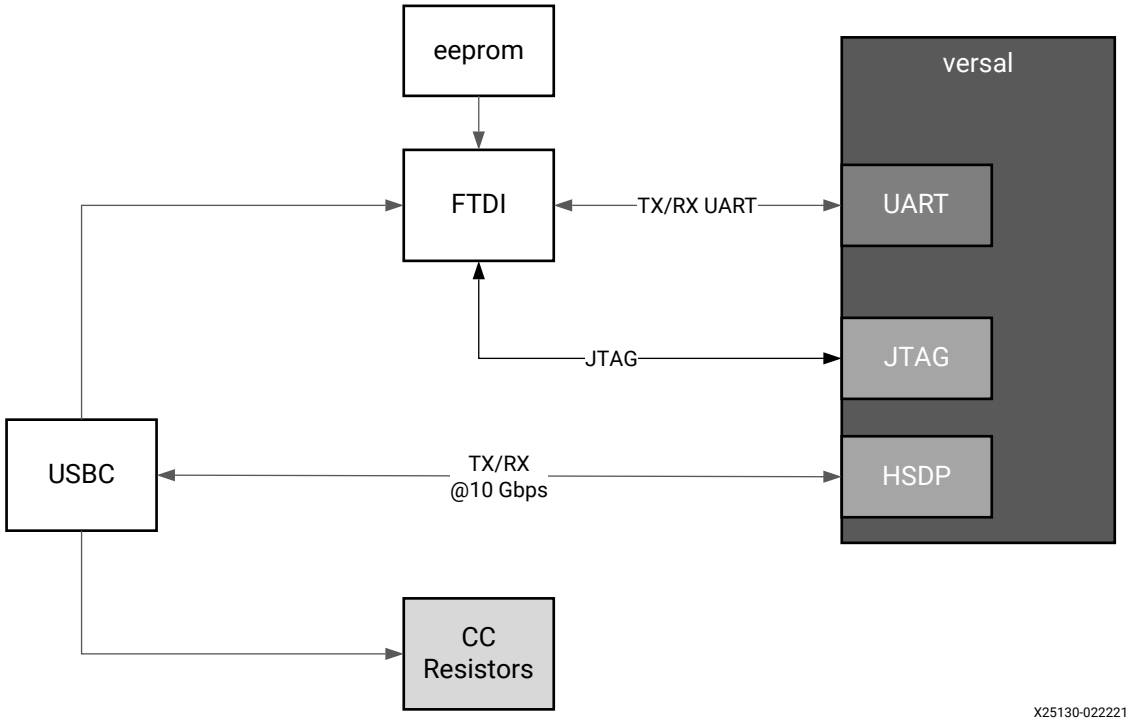
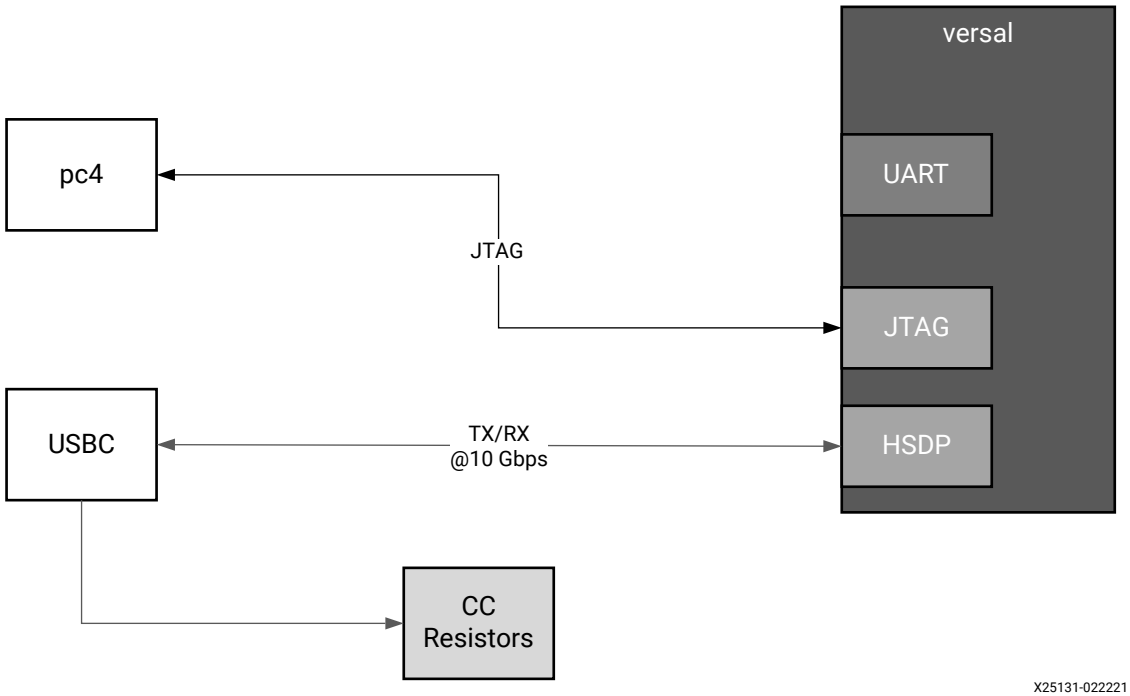


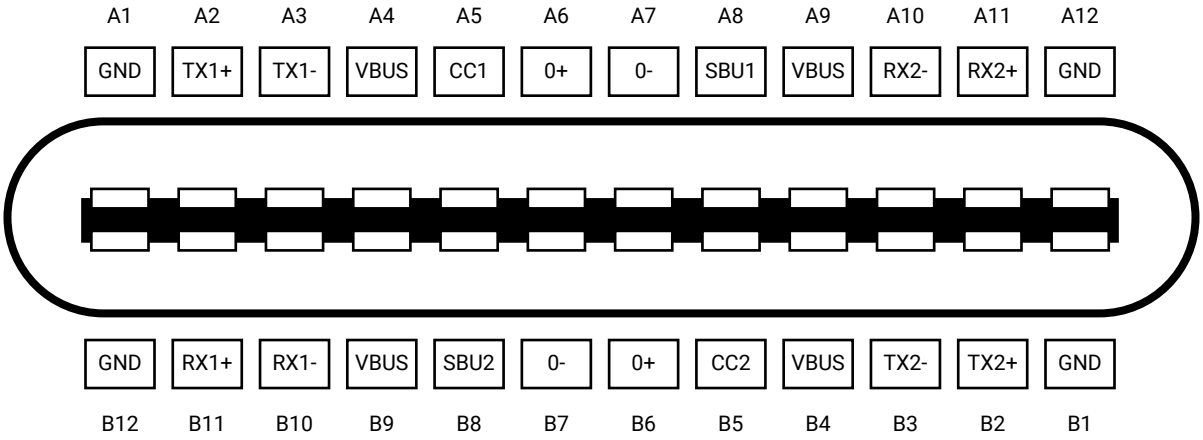
Figure 13: **Option 2: HSDP with PC4 JTAG**



HSDP Connector

The HSDP target implements a UFP (upstream facing port) peripheral interface through a USB-C receptacle connector. The receptacle features four power and four ground pins, two differential pairs for high-speed USB data (though they are connected together on devices), four shielded differential pairs for Enhanced SuperSpeed data (two transmit and two receive pairs), two Sideband Use (SBU) pins, and two Configuration Channel (CC) pins.

Figure 14: **HSDP Connector**



***Note*:** The SmartLynq+ Module high-speed serial interface does not support USB-C compliant devices; however, USB-C compliant devices will not be damaged if they are accidentally plugged into this interface.

Pin assignments are identified in the following table.

Table 7: **HSDP to USB-C Connector Pin Assignments**

Pin	USB Name	HSDP Name	Description	Pin	USB Name	HSDP Name	Description
A1	GND	GND	Ground return	B12	GND	GND	Ground return
A2	SSTXp1	HSDP-TXp	HSDP diff pair, TX, positive	B11	SSRXp1	HSDP-RXp	HSDP diff pair, RX
A3	SSTXn1	HSDP-TXn	HSDP diff pair, TX, negative	B10	SSRXn1	HSDP-RXn	HSDP diff pair, RX
A4	Vbus	Vbus	Bus power (from host)	B9	Vbus	Vbus	Bus power (from host)
A5	CC1	CC1	Configuration channel	B8	SBU2	SBU2	Sideband use (SBU)
A6	Dp1	Dp1	USB 2.0 differential pair, position 1, positive	B7	Dn2	Dn2	USB 2.0 differential pair
A7	Dn1	Dn1	USB 2.0 differential pair, position 1, negative	B6	Dp2	Dp2	USB 2.0 differential pair
A8	SBU1	SBU1	Sideband use (SBU)	B5	CC2	CC2	Configuration channel

Table 7: **HSDP to USB-C Connector Pin Assignments** *(cont'd)*

Pin	USB Name	HSDP Name	Description	Pin	USB Name	HSDP Name	Description
A9	Vbus	Vbus	Bus power (from host)	B4	Vbus	Vbus	Bus power (from host). Note: This power is supplied from the SmartLynq + Module when the target is detected. The power is used to enable powering the FTDI part. Note that only minimal USB2.0 power is supplied.
A10	SSTXn2	-	No connection	B3	SSRXn2	-	No connection
A11	SSTXp2	-	No connection	B2	SSRXn2	-	No connection
A12	GND	GND	Ground return	B1	GND	-	Ground return

High Speed Differential Pairs

The SmartLynq+ HSDP interface supports standard USB 3.0 cables. As such, high-speed differential pairs (HSDP-TXp/HSDP-TXn and HSDP-RXp/HSDP-RXn) must comply with the electrical requirements specified in Section 5.6.1 of the *Universal Serial Bus 3.0 Specification*. The key electrical requirements are identified in the following table.

Table 8: **High Speed Differential Pair Electrical Requirements**

Parameter	Value
Characteristic impedance	90Ω ± 7Ω
Intra-pair (P-to-N) skew	Less than 15 pS per meter
Differential insertion loss	30 AWG: 1.4 dB/m @ 625 MHz, 2.0 dB/m @ 1.25 GHz, 3.00 dB/m @ 2.50 GHz
	28 AWG: 1.2 dB/m @ 625 MHz, 1.8 dB/m @ 1.25 GHz, 2.65 dB/m @ 2.50 GHz

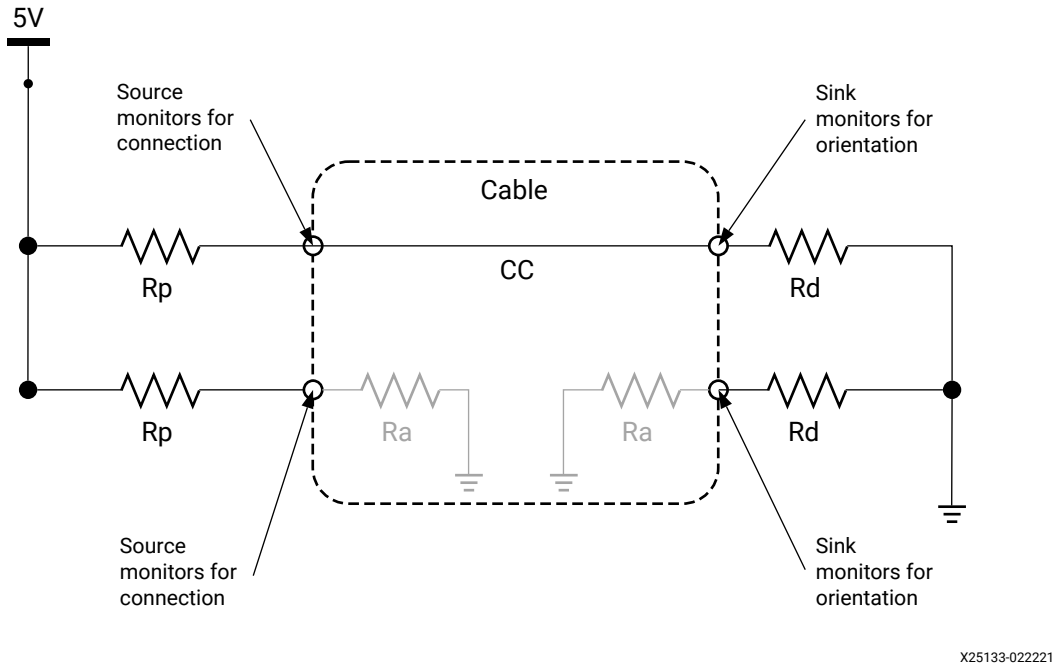
Configuration Channel (CC) Connections

The CC lines are used to determine orientation and power sense. HSDP targets do NOT use the power from the host, therefore the power sense is ignored. This is how the cable orientation is detected from the host:

1. If CC1 is pulled down, the cable is not flipped.
2. If CC2 is pulled down, the cable is flipped.

The CC connections are shown in the following figure.

Figure 15: **CC Connections**



The CC lines should be connected as follows in order to have the host detect the device as a USB 2.0 peripheral. The SmartLynq+ Module supports USB-C in a single orientation currently for HSDP capability. The following LED status can be used to check if the USB-C cable is connected in the expected orientation:

- Green: USB-C is properly connected
- Amber: Either the cable is not connected or needs to be flipped
  - Pressing the "SL+" tab select key on the display shows the root cause for the amber LED.

Table 9: **CC Connections**

HSDP Name	Connection	Desciption
CC1	Rd = 5.1 KΩ	The UFP Rd value is fixed at 5.1 kΩ.
CC2	Rd = 5.1 KΩ	The UFP Rd value is fixed at 5.1 kΩ.

Versal ACAP Connectivity

- See the *VCK190 Schematics* (XTP610) for a sample board connectivity.
- For the HSDP connector, follow the recommended USBC guidelines to run at 10 Gb/s. The preceding table contains some of the highlights of these requirements.
- When connecting the GTs from the Versal ACAP to the HSDP connector, keep the differential lengths matched and close to the connector.

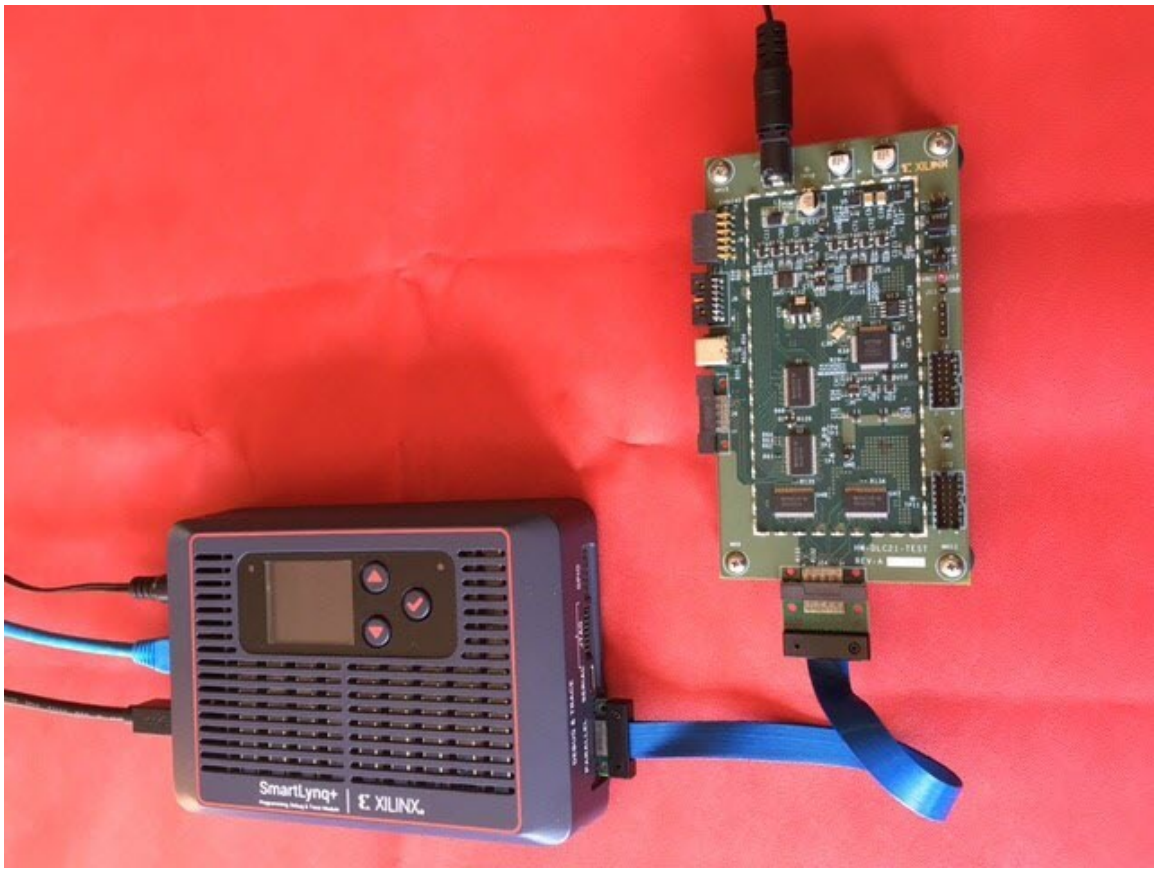
- For more information on adding HSDP to Versal ACAP designs, seethe *Versal ACAP Design Guide* (UG1273).

Parallel Debug Interface

***Note*:** The 38-pin MICTOR interface is currently not supported. See the SmartLynq+ Module wiki page for the latest information.

The SmartLynq+ Module provides a MICTOR interface for high-speed trace capture. The interface supports 16-bit wide parallel trace and includes status and sync signals. The interface is implemented with a 38-pin, 0.64 mm pitch connector (TE P/N 5767044-1). The following figure shows the SmartLynq+ Module connected to the MICTOR interface on a target board.

Figure 16: **SmartLynq+ Connected to MICTOR Interface on a Target Board**



The following figure shows the MICTOR connector pinout. The signals are described in the table that follows.

Figure 17: **MICTOR Connector Pinout**

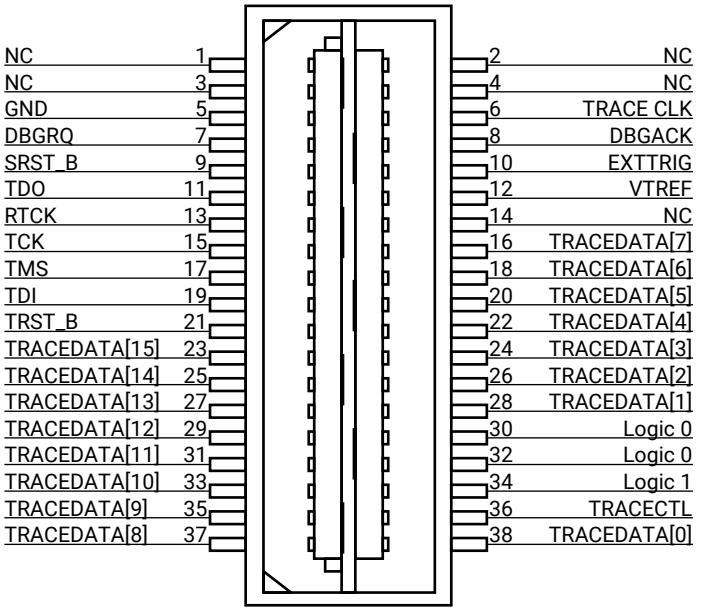


Table 10: **Signal Descriptions**

Pin	Name	Direction	Description
1, 2, 3, 4	-	-	No connection
5	GND	Power	Ground return
6	TRACE_CLK	Input	Trace clock
7	DBGRQ	Output	Debug request. Pulled to GND through 4.7 KΩ resistor
8	DBGACK	Input	Debug acknowledge. Pulled to GND through 4.7 KΩ resistor
9	SRST_B	Output	System reset. Pulled up to VTREF through 4.7 KΩ resistor
10	EXTTRIG	Input	External trigger
11	TDO	Input	JTAG Test Data Out. Pulled up to VTREF through 4.7 KΩ resistor
12	VTREF	Input	Voltage target reference. Used to set the interface I/O levels. Supports voltages in the range of 1.2V to 3.6V.
13	RTCK	Input	Return test clock. Pulled up to VTREF through 4.7 KΩ resistor
14	-	-	No connection
15	TCK	Output	JTAG Test Clock. Pulled up to VTREF through 4.7 KΩ resistor
16	TRACEDATA7	Input	Trace data 7
17	TMS	Output	JTAG Test Mode Select. Pulled up to VTREF through 4.7 KΩ resistor
18	TRACEDATA6	Input	Trace data 6
19	TDI	Output	JTAG Test Data In. Pulled up to VTREF through 4.7 KΩ resistor
20	TRACEDATA5	Input	Trace data 5
21	TRST_B	Output	JTAG Test Reset. Pulled up to VTREF through 4.7 KΩ resistor
22	TRACEDATA4	Input	Trace data 4

Table 10: **Signal Descriptions** *(cont'd)*

Pin	Name	Direction	Description
23	TRACEDATA15	Input	Trace data 15
24	TRACEDATA3	Input	Trace data 3
25	TRACEDATA14	Input	Trace data 14
26	TRACEDATA2	Input	Trace data 2
27	TRACEDATA13	Input	Trace data 13
28	TRACEDATA1	Input	Trace data1
29	TRACEDATA12	Input	Trace data12
30	LOGIC0	Output	Logic bit 0. Pulled to GND through 4.7 KΩ resistor
31	TRACEDATA11	Input	Trace data 11
32	LOGIC1	Output	Logic bit 1 Pulled to GND through 4.7 KΩ resistor
33	TRACEDATA10	Input	Trace data 10
34	LOGIC2	Output	Logic bit 2. Pulled up to VTREF through 4.7 KΩ resistor
35	TRACEDATA9	Input	Trace data 9
36	TRACECTL	Input	Trace control
37	TRACEDATA8	Input	Trace data 8
38	TRACEDATA0	Input	Trace data 0

Appendix A

Regulatory and Compliance Information

See the SmartLynq+ Module Declaration of Conformity for regulatory and compliance information.

XILINX

Appendix B

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

Documentation Navigator and Design Hubs

Xilinx® Documentation Navigator (DocNav) provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open DocNav:

- From the Vivado® IDE, select **Help → Documentation and Tutorials**.
- On Windows, select **Start → All Programs → Xilinx Design Tools → DocNav**.
- At the Linux command prompt, enter `docnav`.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In DocNav, click the **Design Hubs View** tab.
- On the Xilinx website, see the Design Hubs page.

Note: For more information on DocNav, see the Documentation Navigator page on the Xilinx website.

References

These documents provide supplemental material useful with this guide:

1. *Vivado Design Suite User Guide: Programming and Debugging* (UG908)
2. *Control, Interface and Processing System LogiCORE IP Product Guide* (PG352)
3. *Versal ACAP Design Guide* (UG1273)
4. *VCK190 Evaluation Board User Guide* (UG1366)
5. *VMK180 Evaluation Board User Guide* (UG1411)
6. *Universal Serial Bus 3.0 Specification*

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