

VCU1525 Reconfigurable Acceleration Platform

User Guide

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/22/2019	1.5	Removed references to PCIe Gen4. Updated graphics to remove schematic detail. Updated QSFP28 Module Connectors . Updated and moved <i>Appendix A Board Installation</i> into Chapter 3, Board and Deployment Software Installation . Updated Markings in Appendix A, Regulatory and Compliance Information .
09/27/2018	1.4	Added the Electrostatic Discharge Caution section. Renamed heading QSFP28 Module Connectors and updated the section (28 Gb/s QSFP+ became QSFP28 throughout). Updated banks in Figure 3-1 . Renamed Figure 3-1 . Updated DDR4 DIMM Memory . Note: Figure numbers are accurate as of version 1.4.
08/07/2018	1.3	Revised Step 4: Program the Base Platform. Note: This citation was accurate as of version 1.3.
07/09/2018	1.2	Revised Board Features , Board Specifications , Table 2-1 , VCU1525 Board Installation , and Figure 3-1 . Removed Xilinx constraints file information. Added Board and Deployment Software Installation . Note: Table and figure numbers are accurate as of version 1.2.
04/02/2018	1.1	Revised Board Specifications and VCU1525 Board Installation . Updated Table 2-1 , Table 2-2 , and Table 3-2 . Revised paragraph after Table 3-1 . Added Figure 3-2 . Updated Figure 3-3 , Figure 3-4 , and Figure 3-1 . Revised Appendix A, Regulatory and Compliance Information . Note: Table and figure numbers are accurate as of version 1.1.
11/13/2017	1.0	Initial Xilinx release.

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Introduction

Overview

The VCU1525 Reconfigurable Acceleration Platform is a peripheral component interconnect express (PCIe[®]) Gen3 x16 compliant board featuring the Xilinx[®] Virtex[®] UltraScale+[™] XCVU9P-L2FSGD2104E FPGA. This Xilinx FPGA-based PCIe accelerator board is designed to accelerate compute-intensive applications like machine learning, data analytics, and video processing.

The VCU1525 board is available in both active and passive cooling configurations and designed to be used in cloud data center servers.

[Figure 1-1](#) shows the VCU1525 active cooling configuration (PC applications).



X20017-110217

Figure 1-1: VCU1525 Reconfigurable Acceleration Platform (Active Cooling)

Figure 1-2 shows the VCU1525 passive cooling configuration (data center server applications).



X20018-110217

Figure 1-2: VCU1525 Reconfigurable Acceleration Platform (Passive Cooling)

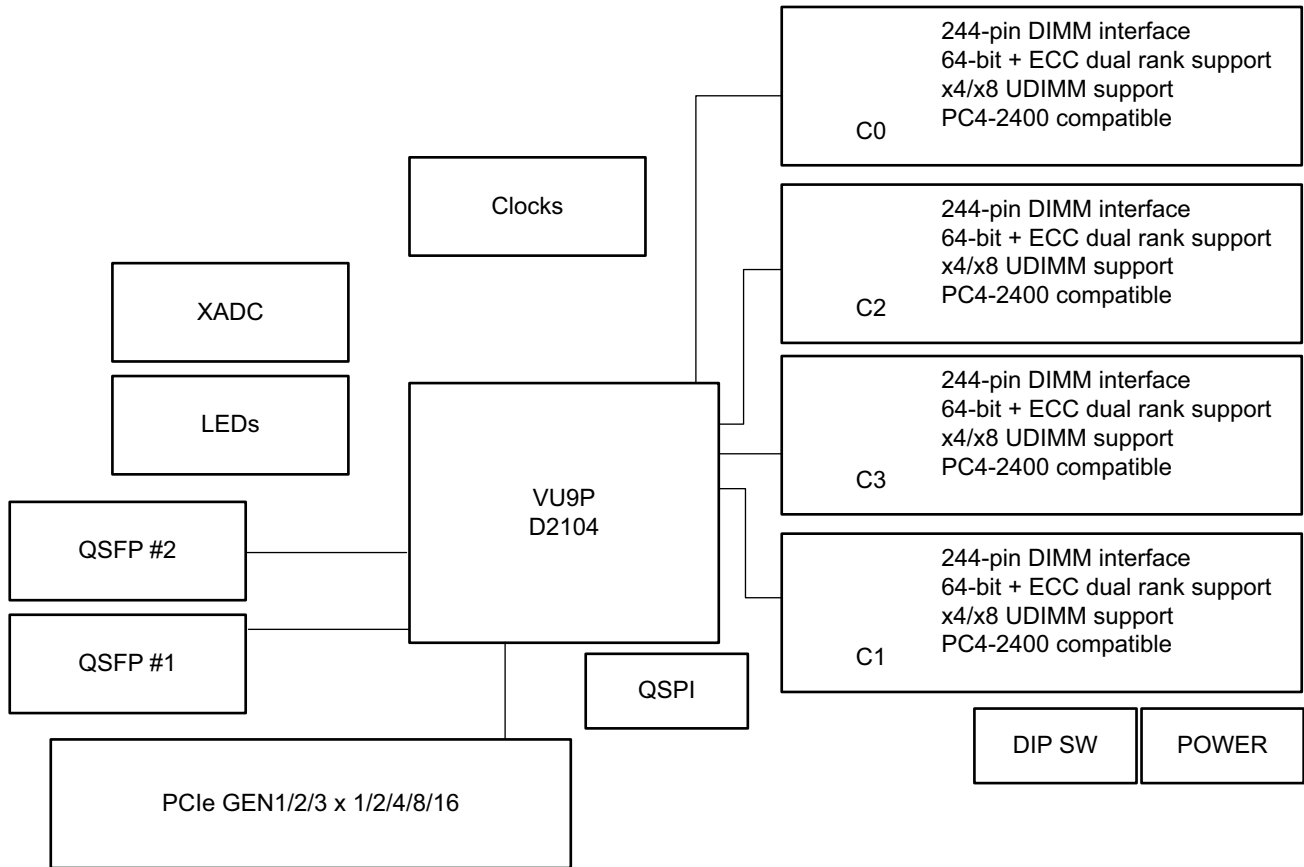


CAUTION! The VCU1525 board with passive cooling is designed to be installed into a data center server, where controlled air flow provides direct cooling. The VCU1525 board with active cooling is designed to be installed into a PC environment where the air flow is uncontrolled, hence this configuration has the heat sink and fan enclosure cover installed to provide appropriate cooling. In either cooling configuration, the board enclosure makes the board top-side components inaccessible (except the triple-LED module DS3 which protrudes through the left front end PCIe bracket). Board details revealed in this user guide are provided to aid understanding of board features. If the cooling enclosure is removed from either configuration of the board and it is powered-up, external fan cooling airflow **MUST** be applied to prevent over-temperature shut-down and possible damage to the board electronics.

See [Appendix B, Additional Resources and Legal Notices](#) for references to documents, files, and resources relevant to the VCU1525 board.

Block Diagram

A block diagram of the VCU1525 board is shown in Figure 1-3.



X19964-022419

Figure 1-3: VCU1525 Board Block Diagram

Board Features

The VCU1525 board features are listed in this section. Detailed information for each feature is provided in [Feature Descriptions](#) in [Chapter 2](#).

- Virtex UltraScale+ XCVU9P-L2FSGD2104E FPGA
- Memory (four independent dual-rank DDR4 interfaces)
 - 64 gigabyte (GB) DDR4 memory
 - 4x DDR4 16 GB, 2400 mega-transfers per second (MT/s), 64-bit with error correcting code (ECC) DIMM
 - x4/x8 unregistered dual inline memory module (RDIMM) support
- Configuration options
 - 1 gigabit (Gb) Quad Serial Peripheral Interface (SPI) flash memory
 - Micro-AB universal serial bus (USB) JTAG configuration port
- 16-lane PCI Express
- Two QSFP28 100G interfaces
- USB-to-UART FT4232HQ bridge with Micro-AB USB connector
- Integrated Endpoint block for PCI Express connectivity
 - Gen1, 2 or 3 x1/x2/x4/x8/x16
- I2C bus
- Status LEDs
- Power management with system management bus (SMBus) voltage, current, and temperature monitoring
- Dynamic power sourcing based on external power supplied
- 75W PCIe slot functional with 35 A max V_{CCINT} current PCIe slot power only
- 150 W PCIe slot functional with 110 A max V_{CCINT} current PCIe slot power and 6-pin PCIe Aux power cable connected
- 225 W PCIe slot functional with 160 A max V_{CCINT} current PCIe slot power and 8-pin PCIe Aux power cable connected
- Two QSFP28 100G interfaces
- Onboard reprogrammable flash configuration memory
- Front panel JTAG and universal asynchronous receiver-transmitter (UART) access through the USB port

- FPGA configurable over USB/JTAG and Quad SPI configuration flash memory
 - Thermal management with variable rate fan for minimal fan noise (active version)
-

Board Specifications

Dimensions

- Height: 4.2 inch (10.67 cm)
- PCB thickness ($\pm 5\%$): 0.062 inch (0.157 cm)
- Board length, passive heat sink: 9.2 inch (23.4 cm)
- Board length, active heat sink: 11.4 inch (29 cm)
- Board thickness with heat sink enclosure installed:
 - Active: 1.52 inch (3.86 cm)
 - Passive: 1.44 inch (3.66 cm)
- Dual slot PCIe full-length, full height form-factor compliant

Note: A 3D model of this board is not available.

Environmental

Temperature

- Operating: 0°C to +45°C
- Storage: -25°C to +60°C

Humidity

- 10% to 90% non-condensing

Operating Voltage

- PCIe slot +12 V_{DC}, +3.3 V_{DC}, +3.3 V_{AUXDC}, External +12 V_{DC}

FPGA Configuration

The VCU1525 board supports two UltraScale+ FPGA configuration modes:

- Quad SPI flash memory
- JTAG using USB JTAG configuration port lower connector in the PCIe bracket

The FPGA bank 0 mode pins are hardwired to M[2:0] = 001 Master SPI mode with pull-up/down resistors.

At power up, the FPGA is configured by the Quad SPI NOR Flash device (Micron MT25QU01GBBA8E12-0SIT) with the FPGA_CCLK operating at clock rate of 105 MHz (EMCCLK) using the Master Serial Configuration mode.

The Quad SPI flash memory NOR device has a capacity of 1 Gb.

While the FPGA default mode selects Quad SPI configuration, JTAG mode overrides it if invoked. JTAG mode is always available independent of the Mode pin settings.

For complete details on configuring the FPGA, see *UltraScale Architecture Configuration User Guide* (UG570) [\[Ref 1\]](#).

Table 1-1: Configuration Modes

Configuration Mode	M[2:0]	Bus Width	CCLKL Direction
Master SPI	001	x1, x2, x4	FPGA output
JTAG	Not applicable - JTAG overrides	x1	Not applicable

Board Component Descriptions

Overview

This chapter provides a detailed functional description of board components and features.

Feature Descriptions

Virtex UltraScale+ XCVU9P-L2FSGD2104E FPGA

The VCU1525 board is populated with the Virtex® UltraScale+™ XCVU9P-L2FSGD2104E FPGA.

For more information on Virtex UltraScale+ FPGAs, see *Virtex UltraScale+ FPGA Data Sheet: DC and AC Switching Characteristics (DS923)* [Ref 2].

DDR4 DIMM Memory

Four independent dual-rank DDR4 DIMM interfaces are available on the VCU1525 board. The VCU1525 board is populated with four socketed single-rank DDR4 RDIMM modules.

- Manufacturer: Micron
- Part Number: MTA18ASF2G72PZ-2G3B1
- Description:
 - 16GB DDR4 RDIMM, 288-pin
 - Configuration: 2Gb x 72
 - Single rank
 - Supports ECC error detection and correction
 - Supports 2400 MT/s

The VCU1525 XCVU9P FPGA DDR4 interface performance is documented in the *Virtex UltraScale+ FPGA Data Sheet: DC and AC Switching Characteristics (DS923)* [Ref 2].

For more details about the Micron DDR4 DIMM, see the Micron MTA18ASF2G72PZ-2G3B1IG data sheet at the Micron website [\[Ref 13\]](#).

Quad SPI Flash Memory

The VCU1525 board provides Quad Serial Peripheral Interface (SPI) flash memory for FPGA bitstream storage. The Quad SPI device provides 1 Gb of nonvolatile storage.

- Part number: MT25QU01GBB8E12-0SIT (Micron)
- Supply voltage: 1.8V
- Datapath width: 4 bits
- Data rate: variable

For more flash memory details, see the Micron MT25QU01GBB8E12-0SIT data sheet at the Micron website [\[Ref 13\]](#).

For configuration details, see *UltraScale Architecture Configuration User Guide* (UG570) [\[Ref 1\]](#).

USB JTAG Interface

The VCU125 board provides access to the FPGA via the Joint Test Action Group (JTAG) interface.

FPGA configuration is available through the Xilinx® Vivado® tool hardware device programmer which accesses the onboard USB-to-JTAG FT4232HQ bridge device. The Micro-AB USB connector available on the VCU1525 PCIe panel/bracket provides external device programming access.

Note: JTAG configuration is allowed at any time regardless of the FPGA mode pin settings consistent with *UltraScale Architecture Configuration User Guide* (UG570) [\[Ref 1\]](#).

For more details about the FT4232HQ device, see the FTDI website [\[Ref 14\]](#).

FT4232HQ USB-UART Interface

The FT4232HQ Quad USB-UART on the VCU1525 board provides a UART connection through the Micro-AB USB connector accessible through the PCIe panel/bracket. The FPGA UART TX/RX (2-wire) connection is made via the FT4232HQ BD port.

Channel BD implements a 2-wire level-shifted TX/RX UART connection to the XVU9P FPGA.

The FTDI FT4232HQ data sheet is available on the FTDI website [\[Ref 14\]](#).

PCI Express Endpoint

The VCU1525 board implements a 16-lane PCI Express edge connector which performs data transfers at the rate of 2.5 GigaTransfers per second (GT/s) for Gen1, 5.0 GT/s for Gen2, and 8.0 GT/s for Gen3 applications.

QSFP28 Module Connectors

The VCU1525 board hosts two 4-lane QSFP28 small form-factor pluggable (QSFP) connectors which accept an array of optical modules. Each connector is housed within a single QSFP cage assembly.

The QSFP28 connectors are accessible via the I2C interface on the VCU1525 board.

Each QSFP module's sideband signals are accessible directly from the FPGA. The MODSELL, RESETL, MODPRSL, INTL, and LPMODE sideband signals are defined in the specifications noted below.

The components visible through the VCU1525 PCIE panel/bracket, top to bottom, are:

- Triple-stack status LEDs
- QSFP0
- QSFP1
- USB

Each QSFP has its own clock generator.

- QSFP0 clock
 - Clock generator: Silicon Labs SI5335A-B06201-GM

Two outputs of the QSFP0 SI5335A are used:

- Output CLK0A/B: 300 MHz SYSClk_300_P/N
- Output CLK1A/1B: The QSFP0_CLOCK_P/N clock is an AC-coupled LVDS 156.25-MHz clock wired to the QSFP0 GTY interface.
- Output CLK2A/2B: Not used.
- Output CLK3A/3B: Not used.

The SI5335A QSFP0 CLK1A/1B output frequency is set via the SI5335A FS0 and FS1 pin setting options, shown in [Table 2-1](#).

- QSFP1 clock
 - Clock generator: Silicon Labs SI5335A-B06201-GM

One output of the QSFP1 SI5335A are used:

- Output CLK0A/B: Not used.
- Output CLK1A/1B: The QSFP1_CLOCK_P/N clock is an AC-coupled LVDS 156.25-MHz clock wired to the QSFP1 GTY interface.
- Output CLK2A/2B: Not used.
- Output CLK3A/3B: Not used.

The SI5335A QSFP1 CLK1A/1B output frequency is set via the SI5335A FS0 and FS1 pin setting options, shown in [Table 2-1](#).

Table 2-1: QSFP0/1 SI5335A CLK1A/1B Frequency Select

QSFP0/1 SI5335A	
Pin Name	Pin Number
FS0	12
FS1	19
FS[1:0] Input	CLK1A/1B Fout
01	156.250 MHz
1X	161.1328 MHz

For additional information about the quad small form-factor pluggable (28 Gb/s QSFP+) module, see the SFF-8663 and SFF-8679 specifications at the SNIA Technology Affiliates website [\[Ref 15\]](#).

I2C Bus

The VCU1525 board implements an I2C bus network (device tree details can be found in the Board Support Package (BSP)).

Status LEDs

The VCU1525 board is designed to operate with the heat sink and fan enclosure cover installed so the DS1 and DS2 LEDs are not visible. Status light emitting diode (LED) DS3 is a triple-stack LED which is visible through a cut-out in the PCIe end bracket. The DS3 LEDs are controlled by the FPGA (see the BSP).

Table 2-2 defines VCU1525 board status LEDs.

Table 2-2: VCU1525 Board Status LEDs

Reference Designator	Description
DS1	RED: POWER_GOOD
DS2	BLUE: DONE_0
DS3	RED: STATUS_LED0
DS3	YELLOW: STATUS_LED1
DS3	GREEN: STATUS_LED2

VCU1525 Board Power System

Limited power system telemetry is available on I2C (see the BSP).

Board and Deployment Software Installation

Introduction

This appendix provides the hardware and software installation procedures for the Xilinx[®] VCU1525 board, using SDx™ development environment version 2018.3.

Both RedHat/CentOS and Ubuntu operating systems are supported. All software installations use standard Linux RPM and Linux DEB packages and can be found on the [Set Up the VCU1525 Accelerator Card website](#).

Safety and Antistatic Precautions

Electrostatic Discharge Caution



CAUTION! ESD can damage electronic components when they are improperly handled, and can result in total or intermittent failures. Always follow ESD-prevention procedures when removing and replacing components.

To prevent ESD damage:

- Use an ESD wrist or ankle strap and ensure that it makes skin contact. Connect the equipment end of the strap to an unpainted metal surface on the chassis.
- Avoid touching the adapter against your clothing. The wrist strap protects components from ESD on the body only.
- Handle the adapter by its bracket or edges only. Avoid touching the printed circuit board or the connectors.
- Put the adapter down only on an antistatic surface such as the bag supplied in your kit.
- If you are returning the adapter to Xilinx Product Support, place it back in its antistatic bag immediately.



CAUTION! Always wear an electrostatic discharge (ESD) strap when handling hardware. Follow the guidelines in [Electrostatic Discharge Caution](#).

Follow these additional safety guidelines:

- Keep your work area and the computer/system clean and clear of debris.
- Before opening a computer or system cover, unplug the power cord.



CAUTION! The active configuration of the VCU1525 board has hazardous moving parts. Keep away from fan blades.

Step 1: Board Installation

1. Make sure the host computer is completely turned off.
2. Unplug the computer.
3. Install the FPGA board in an open PCIe® slot on the host computer.
4. Plug the computer in.
5. Turn on the host computer.

Note: Follow the host computer manufacturer recommendations to ensure proper mounting and adequate cooling.

To verify that the device has been installed correctly, enter the following Linux command in a terminal:

```
$ sudo lspci -vd 10ee:
```

If the card is successfully installed and found by the operating system, a message similar to the one below displays:

```
65:00.0 Processing accelerators: Xilinx Corporation Device 6a8f
  Subsystem: Xilinx Corporation Device 4353
  Flags: bus master, fast devsel, latency 0
  Memory at 38bff2000000 (64-bit, prefetchable) [size=32M]
  Memory at 38bff4000000 (64-bit, prefetchable) [size=128K]
  Capabilities: [40] Power Management version 3
  Capabilities: [60] MSI-X: Enable- Count=33 Masked-
  Capabilities: [70] Express Endpoint, MSI 00
  Capabilities: [100] Advanced Error Reporting
  Capabilities: [1c0] #19
  Capabilities: [400] Access Control Services
  Capabilities: [410] #15
```

Step 2: Deployment Software Installation

The deployment software installation requires installing the following software packages:

- Xilinx® Runtime (XRT).

XRT provides the libraries and drivers for an application to run on VCU1525 boards.

- Deployment shell

The deployment shell provides the base firmware needed to run pre-compiled applications but cannot be used to compile or create a new application. See [Step 4: Installing the Development Software](#) for development software installation.

Your operating system might require additional dependencies before installing XRT and the deployment shell. See *SDAccel Development Environment Release Notes, Installation, and Licensing Guide, v2018.3* (UG1238) for a list of these packages [\[Ref 3\]](#).



IMPORTANT: *Root access is required for all software and firmware installations.*

XRT and Deployment Shell Installation Procedures on RedHat and CentOS

Use the following steps to download and install the RPM software package.

Many commands below use the `xbutil` utility. See *SDx Command and Utility Reference Guide, v2018.3* (UG1279) for additional details on this command [\[Ref 4\]](#).

Note: To successfully install XRT, you must have the `kernel-headers` and `kernel-devel` packages installed on your machine. On CentOS/RedHat, XRT supports Linux kernel up to 3.10.0-862.14.4.el7.x86_64.



IMPORTANT: *The installation packages referenced here are being updated regularly and the file names frequently change. If you copy and paste any commands from this user guide, be sure to update the placeholders in those commands to match the downloaded packages.*

1. Xilinx Runtime (XRT) installation requires Extra Packages for Enterprise Linux (EPEL) and a related repository. The initial setup depends on whether you are using RedHat or CentOS.

For RedHat:

Open a terminal window and enter the following command:

```
$ sudo yum-config-manager --enable rhel-7-server-optional-rpms
```

This enables an additional repository on your system.

Enter the following command to install EPEL:

```
$ sudo yum install -y  
https://dl.fedoraproject.org/pub/epel/epel-release-latest-7.noarch.rpm
```

For CentOS:

Enter the following command in a terminal window:

```
$ sudo yum install epel-release
```

This installs and enables the repository for Extra Packages for Enterprise Linux (EPEL).

2. Run the following commands to install the `kernel-headers` and `kernel-devel` packages. Ensure that `uname` is surrounded by backticks (```) and not single quotes (`'`):

```
$ sudo yum install kernel-headers-`uname -r`  
$ sudo yum install kernel-devel-`uname -r`
```

Note: If these yum commands fail because they cannot find packages matching your kernel version, set up a Vault repository as described in "Creating a Vault Repository for CentOS" in *Getting Started with Alveo Data Center Accelerator Cards* (UG1301) [Ref 5].

3. After the above command finishes running, reboot your machine.
4. Download both the XRT and deployment shell installation packages associated with your board from the [Set Up the VCU1525 Accelerator Card website](#).
5. Install the XRT installation package using the following command, where `<rpm-dir>` is the directory where the RPM packages were downloaded in the previous step and `<version>` is the latter part of the XRT file name.

```
$ sudo yum install ./<rpm-dir>/xrt_<version>.rpm
```

This installs the XRT and its necessary dependencies. Follow the instructions when prompted throughout the installation.

6. Install the deployment shell installation package you downloaded in a previous step by running the following command, where `<version>` is the latter part of the downloaded deployment shell package name.

```
$ sudo yum install ./<rpm-dir>/xilinx-<version>.rpm
```

The deployment software sources are now installed on the system. The installation of the drivers, runtime software, and utilities are located in the `/opt/xilinx/` directory and contains the `xrt` and `dsa` sub-directories. Note that the `dsa` folder contains the deployment shell installation.

7. After installing the deployment shell, the terminal output instructs you to flash the board by running a command. Do not run this command. You will manually generate the correct command in [step 9](#).

8. Cold boot your machine by fully powering it off, then on.



CAUTION! *Cold boot* means to remove power completely, i.e., turn off the supply or unplug the machine.

9. Follow instructions in [Generating the xbutil flash Command](#) to manually generate the correct `xbutil flash` command, which includes the `-d` option to specify the board in the system to be flashed, as shown below. The `-a` and `-t` options specify the deployment shell name and timestamp associated with the specific card ID.

```
sudo /opt/xilinx/xrt/bin/xbutil flash -a <shell_name> -t <timestamp> -d <card_ID>
```



CAUTION! *Not specifying the card ID within the xbutil flash command via the -d option can damage the card.*

10. Run the manually generated `xbutil flash` command.

If you have multiple cards installed on the system, you **MUST** run the `xbutil flash` command separately for each card.



TIP: *If you are flashing a board after the deployment shell is already installed, see [Troubleshooting](#).*

11. You will be asked to confirm the update, as shown below. Type **y** and **Enter**.

```
Probing board[0]: DSA on FPGA needs updating
DSA on below boards will be updated:
Card [0]
Are you sure you wish to proceed? [y/n]
```

Flashing will take up to 10 minutes. Successfully flashing a new board results in a message similar to the one shown below. If you do not see one, refer to [Troubleshooting](#).

```
INFO: ***Found 880 ELA Records
Idcode byte[0] ff
Idcode byte[1] 20
Idcode byte[2] bb
Idcode byte[3] 21
Idcode byte[4] 10
Enabled bitstream guard. Bitstream will not be loaded until flashing is finished.
Erasing flash.....
Programming flash.....
Cleared bitstream guard. Bitstream now active.
DSA image flashed successfully
Cold reboot machine to load the new image on FPGA
```

If you have previously updated the board, you will see the a message similar to the following, indicating that no update was needed:

```
Probing board[0]: DSA on FPGA is up-to-date
0 Card(s) flashed successfully.
```

12. Cold boot your machine to load the new image on the FPGA.



CAUTION! *Cold boot* means to remove power completely, i.e., turn off the supply or unplug the machine. The image will not boot from flash if the machine is only rebooted.

The installation for deployment is now complete. You can go directly to [Step 3: Board Bring-Up and Validation](#) to validate the installation.

XRT and Deployment Shell Installation Procedures on Ubuntu

Use the following steps to download and install the software using a DEB installation package.



IMPORTANT: *The installation packages referenced here are being updated regularly and the file names frequently change. If you copy and paste any commands from this user guide, be sure to update the placeholders in those commands to match the downloaded packages.*

1. Download both the XRT and deployment shell installation packages associated with your board from the [Set Up the VCU1525 Accelerator Card website](#).
2. Install the XRT installation package using the following command, where `<deb-dir>` is the directory where the DEB packages were downloaded in the previous step, and `<OS>` is either `16.04` or `18.04`, depending on the version of Ubuntu you are running:

```
$ sudo apt install ./<deb-dir>/xrt_<version>.deb
```

This will install the XRT and its necessary dependencies. Follow the instructions when prompted throughout the installation.

3. Install the deployment shell installation package you downloaded in a previous step by running the following command where `<version>` is the latter part of the downloaded deployment shell package name.

```
$ sudo apt install ./<deb-dir>/xilinx-<version>.deb
```

The deployment software sources are now installed and deployed on the system. The installation of the drivers, runtime software, and utilities are in the `/opt/xilinx/` directory and contains the `xrt` and `dsa` sub-directories. Note that the `dsa` folder contains the deployment shell installation.

4. After installing the deployment shell, the terminal output instructs you to flash the board by running a command. **Do not** run this command. You will manually generate the correct command in [step 6](#).
5. Cold boot your machine by fully powering it off, then on.

- Follow the instructions in [Generating the xbutil flash Command](#) to manually generate the correct `xbutil flash` command, which includes the `-d` option to specify the board in the system to be flashed, as shown below. The `-a` and `-t` options specify the deployment shell name and timestamp associated with the specific card ID.

```
sudo /opt/xilinx/xrt/bin/xbutil flash -a <shell_name> -t <timestamp> -d <card_ID>
```



CAUTION! *Not specifying the card ID within the `xbutil flash` command via the `-d` option can damage the card.*

- Run the manually generated `xbutil flash` command.

If you have multiple cards installed in the system, you **MUST** run the `xbutil flash` command separately for each card.



TIP: *If you are updating a board after the deployment shell is already installed, see [Troubleshooting](#).*

- You will be asked to confirm the update, as shown below. Type **y** and **Enter**.

```
Probing board[0]: DSA on FPGA needs updating
DSA on below boards will be updated:
Card [0]
Are you sure you wish to proceed? [y/n]
```

Flashing will take up to 10 minutes. Successfully flashing a new board results in a message similar to the one shown below. If you do not see one, refer to [Troubleshooting](#).

```
INFO: ***Found 880 ELA Records
Idcode byte[0] ff
Idcode byte[1] 20
Idcode byte[2] bb
Idcode byte[3] 21
Idcode byte[4] 10
Enabled bitstream guard. Bitstream will not be loaded until flashing is finished.
Erasing flash.....
Programming flash.....
Cleared bitstream guard. Bitstream now active.
DSA image flashed successfully
Cold reboot machine to load the new image on FPGA
```

If you have previously updated the board, you will see a message similar to the following, indicating that no update was needed:

```
Probing board[0]: DSA on FPGA is up-to-date
0 Card(s) flashed successfully.
```

- Cold boot your machine to load the new firmware image on the FPGA.



CAUTION! *Be sure to fully power off the machine and then power it on again. The image will not boot from flash if the machine is only rebooted.*

The installation for deployment is now complete.

Step 3: Board Bring-Up and Validation

After installing the XRT and deployment shell, `lspci` and the `xbutil` utility are used to validate a successful hardware and software setup.

The `xbutil` utility is included in the XRT package. It includes multiple commands to validate and identify the installed boards, along with additional board details related to DDR, PCIe, shell name, and system information. See *SDx Command and Utility Reference Guide* (UG1279) for a complete list of `xbutil` commands and definitions [Ref 4].

Set the environment to use the `xbutil` utility by running the following command. Note that the command is dependent on the shell you are using.

- Use the following command in `csh` shell:

```
$ source /opt/xilinx/xrt/setup.csh
```

- Use the following command in `bash` shell:

```
$ source /opt/xilinx/xrt/setup.sh
```

After installing the XRT and deployment shell, the VCU1525 board installation can be verified using the following commands:

- `lspci`
- `xbutil flash scan`
- `xbutil validate`

Running `lspci`

Enter the following command:

```
$ sudo lspci -vd 10ee:
```

If the card is successfully installed and found by the operating system, you will see a message similar to the one below. Note that for each card, there will be two different devices found: one for management and one for user.

```
65:00.0 Processing accelerators: Xilinx Corporation Device 6a8f
Subsystem: Xilinx Corporation Device 4353
Flags: bus master, fast devsel, latency 0
Memory at 38bff2000000 (64-bit, prefetchable) [size=32M]
Memory at 38bff4000000 (64-bit, prefetchable) [size=128K]
Capabilities: [40] Power Management version 3
Capabilities: [60] MSI-X: Enable- Count=33 Masked-
Capabilities: [70] Express Endpoint, MSI 00
```

```

Capabilities: [100] Advanced Error Reporting
Capabilities: [1c0] #19
Capabilities: [400] Access Control Services
Capabilities: [410] #15

65:00.1 Processing accelerators: Xilinx Corporation Device 6a90
Subsystem: Xilinx Corporation Device 4353
Flags: bus master, fast devsel, latency 0, IRQ 11
Memory at 38bff000000 (64-bit, prefetchable) [size=32M]
Memory at 38bff4020000 (64-bit, prefetchable) [size=64K]
Memory at 38bfe0000000 (64-bit, prefetchable) [size=256M]
Capabilities: [40] Power Management version 3
Capabilities: [60] MSI-X: Enable- Count=33 Masked-
Capabilities: [70] Express Endpoint, MSI 00
Capabilities: [100] Advanced Error Reporting
Capabilities: [400] Access Control Services
Capabilities: [410] #15
    
```

Running xbutil flash scan

Use the `xbutil flash scan` command to view and validate the board's current firmware version and to display the installed board details, including card ID, shell name, and timestamp. Enter the following command:

```
$ sudo /opt/xilinx/xrt/bin/xbutil flash scan
```

You will see an output similar to the one below related to the deployment shell name and the timestamp running on the FPGA and installed in the system. They should be identical. If not, see the [Troubleshooting](#) section.

```

Card [0]
Card BDF:                0000:65:00.0
Card type:               vcu1525
Flash type:              SPI
DSA running on FPGA:
  xilinx_vcu1525_xdma_201830_1, [TS=0x000000005bf05050]
DSA package installed in system:
  xilinx_vcu1525_xdma_201830_1, [TS=0x000000005bf05050]
    
```

Running xbutil validate

The `xbutil validate` command generates a high-level, easy to read summary of the installed board. It validates the correct installation by performing the following set of tests:

1. Validates the device found.
2. Checks PCIe link status.
3. Runs a verify kernel on the board.
4. Performs the following data bandwidth tests:
 - DMA test - Data transfer between host and FPGA DDR via PCIe
 - DDR test - Data transfer between kernels and FPGA DDR

To run the validate command, enter the following:

```
$ sudo /opt/xilinx/xrt/bin/xbutil validate
```

If the board was installed correctly, you will see a message similar to the following output. If the output is not similar to the one shown below, review [Troubleshooting](#).

```
INFO: Found 1 cards

INFO: Validating card[0]: xilinx_vcu1525_xdma_201830_1
INFO: Checking PCIE link status: PASSED
INFO: Starting verify kernel test:
INFO: verify kernel test PASSED
INFO: Starting DMA test
Host -> PCIe -> FPGA write bandwidth = 11346.1 MB/s
Host <- PCIe <- FPGA read bandwidth = 11333.6 MB/s
INFO: DMA test PASSED
INFO: Starting DDR bandwidth test: .....
Maximum throughput: 47515.703125 MB/s
INFO: DDR bandwidth test PASSED
INFO: Card[0] validated successfully.

INFO: All cards validated successfully.
```

Step 4: Installing the Development Software

The development shell provides added features to support the development and debug of applications to run on the VCU1525 board. See *SDAccel Development Environment Release Notes, Installation, and Licensing Guide, v2018.3* (UG1238) for complete instructions on installing the SDAccel development software and development shell for the VCU1525 board [\[Ref 3\]](#).

Note: The machine you are installing the development software on does not need to have a VCU1525 board installed.

Generating the xbutil flash Command

To flash the firmware to the VCU1525 board, use the xbutil flash command, which flashes the deployment shell installed in the system onto the VCU1525 board.

The format of the xbutil flash command is:

```
sudo /opt/xilinx/xrt/bin/xbutil flash -a <shell_name> -t <timestamp> -d <card_ID>
```

To obtain the necessary card ID (-d), shell name (-a), and timestamp (-t) command options, run the following `xbutiM1 flash scan` command. For more information, see [Running xbutil flash scan](#).

```
sudo /opt/xilinx/xrt/bin/xbutil flash scan
```

For each card in the server, you will see an output similar to the example below:

```
Card [0]
Card BDF:                0000:65:00.0
Card type:               vcu1525
Flash type:              SPI
DSA running on FPGA:
  xilinx_vcu1525_xdma_201830_1, [TS=0x000000005bf05050]
DSA package installed in system:
  xilinx_vcu1525_xdma_201830_1, [TS=0x000000005bf05050]
```

Both the shell name and timestamp values need to be taken from DSA package installed in system:. In this output, the `xbutil flash` command options are:

- Card ID (-d):

```
Card [0]
```

The card ID is 0. The card ID will change if any cards are installed or uninstalled. Do not assume that the card ID will remain static.

- Shell name (-a):

```
DSA package installed in system:
xilinx_vcu1525_xdma_201830_1, [TS=0x000000005bf05050]
```

The shell name is `xilinx_vcu1525_xdma_201830_1`.

- Timestamp (-t):

```
DSA package installed in system:
xilinx_vcu1525_xdma_201830_1, [TS=0x000000005bf05050]
```

The timestamp is `0x000000005bf05050`.

For the example output above, the `xbutil flash` command is:

```
sudo /opt/xilinx/xrt/bin/xbutil flash -a xilinx_vcu1525_xdma_201830_1 -t
0x000000005bf05050 -d 0
```

When the VCU1525 board is successfully flashed, the `xbutil flash scan` output will show the same package information for both DSA package installed in FPGA: and DSA package installed in system:.



IMPORTANT: Use a separate `xbutil flash` command to flash each board in the system.

Troubleshooting

Table 3-1 lists some possible problems you might encounter, identifies a possible cause, and suggests a solution.

For information about using SDx environment 2018.2, refer to [Virtex UltraScale+ FPGA VCU1525 Master Answer Record 69844](#).

Table 3-1: Board Troubleshooting

Issue	Potential Cause	Fix
Card not found	Card not correctly installed.	Reinstall the VCU1525 board. Check if the card shows up by typing the following Linux command: <code>lspci -vd 10ee</code>
	Maintenance USB cable attached.	Ensure maintenance USB cable is removed before booting system.
<code>lspci</code> no longer recognizes the card.	Card is overheating.	Ensure that operating ambient conditions do not exceed specifications
XRT or deployment shell installation incomplete or unsuccessful	Missing dependent packages.	Contact your Linux administrator.
<code>xbutil flash</code> returns the error: Specified DSA is not applicable	Correct deployment shell package not installed.	Install the correct deployment shell package.
Unable to install the packages.	Incorrect permissions for download directory.	Download the packages to a directory where root has read access (for example <code>/tmp</code>).
When running <code>xbutil</code> the following message is displayed: Failed to open device: 0000:3b:00.0 INFO: Found total 1 card(s); 0 are usable.	Driver has not loaded successfully or the card is not flashed successfully.	Perform a cold reboot.
XRT package fails to install in CentOS 7.4 or CentOS 7.5.	Kernel development headers are missing. The XRT package is missing a dependency on <code>kernel-devel</code> and <code>kernel-headers</code> .	Manually install <code>kernel-devel</code> and <code>kernel-header</code> with <code>yum</code> install: <code>\$ sudo yum install kernelheaders-`uname -r`</code> <code>\$ sudo yum install kernel-devel-`uname -r`</code> Note: Do not run <code>sudo yum upgrade</code> . This will update the kernel-headers to an incompatible version.

Table 3-1: Board Troubleshooting (Cont'd)

Issue	Potential Cause	Fix
Flashing the card does not complete after 20 minutes.	The flash operation has failed.	Perform a cold reboot and then re-flash the card.
Run time fails with following message: Error: Failed to find Xilinx platform	Failed to source the <code>setup.sh</code> script.	Source <code>/opt/xilinx/xrt/setup.sh</code>
When installing XRT, you see the following message: N: Can't drop privileges for downloading as file '/root/xrt_201802.2.1.79_16.04.deb' couldn't be accessed by user '_apt'. - pkgAcquire::Run (13: Permission denied)	This is caused by running <code>sudo apt install</code> as root.	The XRT will install correctly, despite the error. You can find more information about this error on AskUbuntu .

Regulatory and Compliance Information

Overview

This product is designed and tested to conform to the European Union directives and standards described in this section.

Refer to the VCU1525 board Master Answer Record concerning the CE requirements for the PC Test Environment: [Virtex UltraScale+ FPGA VCU1525 Master Answer Record 69844](#)

For Technical Support, open a [Support Service Request](#).

CE Directives

2006/95/EC, *Low Voltage Directive (LVD)*

2004/108/EC, *Electromagnetic Compatibility (EMC) Directive*

CE Standards

EN standards are maintained by the European Committee for Electrotechnical Standardization (CENELEC). IEC standards are maintained by the International Electrotechnical Commission (IEC).

Electromagnetic Compatibility

EN 55022:2010, *Information Technology Equipment Radio Disturbance Characteristics – Limits and Methods of Measurement*

EN 55024:2010, *Information Technology Equipment Immunity Characteristics – Limits and Methods of Measurement*



IMPORTANT: *This is a Class A product. In a domestic environment, this product can cause radio interference, in which case the user might be required to take adequate measures.*

Safety

IEC 60950-1:2005, *Information technology equipment – Safety, Part 1: General requirements*

EN 60950-1:2006, *Information technology equipment – Safety, Part 1: General requirements*

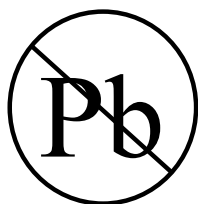
Markings



In August of 2005, the European Union (EU) implemented the EU WEEE Directive 2002/96/EC and later the WEEE Recast Directive 2012/19/EU requiring Producers of electrical and electronic equipment (EEE) to manage and finance the collection, reuse, recycling and to appropriately treat WEEE that the Producer places on the EU market after August 13, 2005. The goal of this directive is to minimize the volume of electrical and electronic waste disposal and to encourage re-use and recycling at the end of life.

Xilinx has met its national obligations to the EU WEEE Directive by registering in those countries to which Xilinx is an importer. Xilinx has also elected to join WEEE Compliance Schemes in some countries to help manage customer returns at end-of-life.

If you have purchased Xilinx-branded electrical or electronic products in the EU and are intending to discard these products at the end of their useful life, please do not dispose of them with your other household or municipal waste. Xilinx has labeled its branded electronic products with the WEEE Symbol to alert our customers that products bearing this label should not be disposed of in a landfill or with municipal or household waste in the EU.



This product complies with Directive 2002/95/EC on the restriction of hazardous substances (RoHS) in electrical and electronic equipment.



This product complies with CE Directives 2006/95/EC, *Low Voltage Directive (LVD)* and 2004/108/EC, *Electromagnetic Compatibility (EMC) Directive*.

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see [Xilinx Support](#).

Documentation Navigator and Design Hubs

Xilinx[®] Documentation Navigator provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open the Xilinx Documentation Navigator (DocNav):

- From the Vivado[®] IDE, select **Help > Documentation and Tutorials**.
- On Windows, select **Start > All Programs > Xilinx Design Tools > DocNav**.
- At the Linux command prompt, enter `docnav`.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In the Xilinx Documentation Navigator, click the **Design Hubs View** tab.
- On the Xilinx website, see the [Design Hubs](#) page.

Note: For more information on Documentation Navigator, see the [Documentation Navigator](#) page on the Xilinx website.

References

The most up to date information related to the VCU1525 board and its documentation is available on the following websites.

[VCU1525 Acceleration Development Kit \(Active\)](#)

[VCU1525 Acceleration Development Kit \(Passive\)](#)

[Set Up the VCU1525 Accelerator Card](#)

[Virtex UltraScale+ FPGA VCU1525 Master Answer Record 69844](#)

These websites and Xilinx documents provide supplemental material useful with this guide:

1. *UltraScale Architecture Configuration User Guide (UG570)*
2. *Virtex UltraScale+ FPGA Data Sheet: DC and AC Switching Characteristics (DS923)*
3. *SDAccel Development Environment Release Notes, Installation, and Licensing Guide, v2018.3 (UG1238)*
4. *SDx Command and Utility Reference Guide, v2018.3 (UG1279)*
5. *Getting Started with Alveo Data Center Accelerator Cards (UG1301)*
Note: The February 12, 2019 (v1.3) document supports SDx 2018.3.
6. *SDAccel Environment User Guide, v2018.3 (UG1023)*
7. *UltraScale Architecture PCB Design User Guide (UG583)*
8. *Vivado Design Suite User Guide: Using Constraints (UG903)*
9. *UltraScale Architecture-Based FPGAs Memory IP LogiCORE IP Product Guide (PG150)*
10. Xilinx, Inc: www.xilinx.com
(XCVU9P-L2FSGD2104E)

For additional documents associated with Xilinx devices, design tools, intellectual property, boards, and kits see the [Xilinx documentation website](#).

The following websites provide supplemental material useful with this guide:

11. Silicon Labs: www.silabs.com
(Si5335A, Si570)
12. PCI Express® standard: www.pcisig.com/specifications
13. Micron Technology: www.micron.com
(MTA18ASF2G72PZ-2G3B1IG, MT25QU01GBB8E12-0SIT)

14. Future Technology Devices International Ltd.: www.ftdichip.com
(FT4232HQ)
15. SFF-8663, SFF-8679 specification: [SNIA Technology Affiliates](#)

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