EX XILINX®

Radiation Tolerant Kintex UltraScale XQRKU060 FPGA Data Sheet

Product Specification

General Description

The radiation tolerant (RT) XQR UltraScale™ architecture-based devices extend the benefit of commercial silicon with unique ceramic column grid array package, tested to stringent qualification flows like Xilinx® class B, class Y test flows (QML compliant), full M-grade operating temperature range support, and radiation tested for single-event effects.

XQR Kintex® UltraScale FPGAs are high-performance monolithic FPGAs with a focus on performance. High DSP and block RAM-to-logic ratios and next-generation transceivers combined with space-grade packaging to handle vibration and handling requirements during launch and operation enable a new generation of high-density FPGAs for on-orbit reconfiguration, targeted for applications like on-board processing, digital payloads, remote sensing, and many more. The Xilinx Space Secure Site provides access to design guidelines and resources specific to space applications.

This data sheet is part of an overall set of documentation on the UltraScale architecture-based devices available on the Xilinx website at www.xilinx.com/documentation.

Summary of Radiation Characteristics for Kintex UltraScale XQRKU060 Devices

This product is intended for use in space environments and offered in Xilinx class Y, class B manufacturing and process flows. Xilinx 20 nm UltraScale device technology is developed with innovative configuration memory and block RAM design for single-event upset (SEU) mitigation, with optimized SEU design rules and strategic implementation of SEU enhanced cells. The Kintex UltraScale XQRKU060 device uses more than 40 proprietary, patented circuit design and layout techniques to reduce the SEU cross-section. Block RAM includes embedded error detection and correction (EDAC) for high-performance SEU mitigation.

Table 1: **Radiation Characteristics**

Symbol	Description	Min	Typ	Max	Units
TID	Total Ionizing Dose (GEO)	-	100	120	Krad (Si)
SEL	Single-Event Latch-Up Immunity[1]	-	80	-	MeV-cm^2/mg
SEU$_{CRAM}$	Single-Event Upset in Configuration RAM (GEO)[2][3]	-	9.5e-9	-	Upset/bit/day
SEU$_{BRAM}$	Single-Event Upset in Block RAM (GEO)[2][3]	-	2.3e-8	-	Upset/bit/day

Table 1: **Radiation Characteristics** *(Cont'd)*

Symbol	Description	Min	Typ	Max	Units
$SEFI_{CRAM}$	Single-Event Functional Interrupt Orbital Upset Frequency - Configuration RAM (GEO) [2][3]	-	4.5e-4	-	Upsets/device/day

Notes:

1. SEL immunity at maximum recommended operating voltage and junction temperature.
2. Error bar is ±40% at 90% confidence interval.
3. GEO estimate is based on CREME96 orbital models for worst-case conditions (solar minimum) and 100 mils of Al shielding.

Table 2: **Single Event Effect Type Descriptions**

Single Event Effect (SEE) Type	SEE Signature	Target/Comments
Single Event Upset (SEU)	Corruption of the information stored in a memory element	Memories, latches in logic devices. Composed of single bit upset (SBU) or multiple bit upset (MBU).
Single Event Transient (SET)	Impulse response of certain amplitude and duration	Analog and mixed-signal circuits. Can lead to SEU if latched in memory cell.
Single Event Latchup (SEL)	High-current conditions	CMOS devices. Might lead to hard failure.
Single Event Functional Interrupt (SEFI)	Corruption of a datapath leading to loss of normal operation	Complex devices with built-in state machine/control sections or systems.

Weibull Fit Parameters

Weibull curves were fitted to the measured test data. See the radiation test summary data in the radiation reports in the XQRKU060 area of the Xilinx Space Secure Site. A summary of the best fit Weibull parameters for the various components of the XQRKU060 FPGA is shown in Table 3.

Table 3: **Weibull Fit Parameters**

Parameter	LET_{th}	W	S	σ_{sat}
Configuration RAM	0.5	5	1.3	8.00E-10
Block RAM	0.9	2	0.98	9.60E-10
Shift Registers	1.16	12	0.92	1.00E-03
Counter	1.16	6	0.96	4.00E-04
DSP	1.16	6	0.93	7.00E-04
GTH	1.16	2	0.96	2.00E-05
IOB	0.9	5	0.97	5.00E-04
PLL	1	3	0.92	1.00E-05
MMCM	1	3	0.92	1.00E-05

Kintex UltraScale XQRKU060 FPGA Feature Summary

*Table 4:* **Kintex UltraScale XQRKU060 FPGA Feature Summary**

Feature	Quantity
System Logic Cells	725,550
CLB Flip-Flops	663,360
CLB LUTs	331,680
Maximum Distributed RAM (Mb)	9
Block RAM Blocks	1,080
Block RAM (Mb)	38
CMTs (1 MMCM, 2 PLLs)	12
I/O DLLs	48
Maximum HP I/Os[1]	516
Maximum HR I/Os[2]	104
DSP Slices	2,760
System Monitor	1
PCIe® Gen1/Gen2/Gen3 up to 8 lanes	3
GTH Transceivers (12.5 Gb/s)	32

Notes:

1. HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.
2. HR = High-range I/O with support for I/O voltage from 1.2V to 3.3V.

Device Layout

Programmable resources in the XQRKU60 device are arranged in a column-and-grid layout. Figure 1 shows a device-level view with resources grouped together. For simplicity, certain resources such as the integrated blocks for PCIe, configuration logic, and System Monitor are not shown.
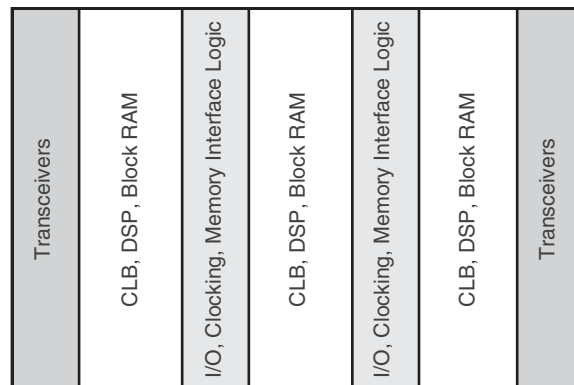
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Figure 1: **FPGA with Columnar Resources**

Resources within the device are divided into segmented clock regions. The height of a clock region is 60 CLBs. A bank of 52 I/Os, 24 DSP slices, 12 block RAMs, or 4 transceiver channels also matches the height of a clock region. The width of a clock region is essentially the same in all cases, regardless of the mix of resources in the region, enabling repeatable timing results. Each segmented clock region contains vertical and horizontal clock routing that span its full height and width. These horizontal and vertical clock routes can be segmented at the clock region boundary to provide a flexible, high-performance, low-power clock distribution architecture. Figure 2 is a representation of an FPGA divided into regions.
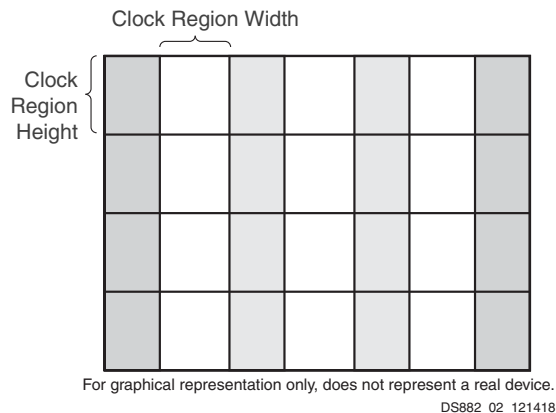

For graphical representation only, does not represent a real device.

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Figure 2: **Column-Based FPGA Divided into Clock Regions**

Input/Output

The XQRKU060 device has I/O pins for communicating to external components. Each I/O is configurable and can comply with a large number of I/O standards. The I/Os are classed as high-range (HR) or high-performance (HP). The HR I/Os offer the widest range of voltage support, from 1.2V to 3.3V. The HP I/Os are optimized for highest performance operation, from 1.0V to 1.8V.

All I/O pins are organized in banks, with typically 52 HP or HR pins per bank. Each bank has one common V_{CCO} output buffer power supply, which also powers certain input buffers. In addition, HR banks can be split into two half-banks, each with their own V_{CCO} supply. Some single-ended input buffers require an internally generated or an externally applied reference voltage (V_{REF}). V_{REF} pins can be driven directly from the PCB or internally generated using the internal V_{REF} generator circuitry present in each bank.

I/O Electrical Characteristics

Single-ended outputs use a conventional CMOS push/pull output structure driving High towards V_{CCO} or Low towards ground, and can be put into a high-Z state. The system designer can specify the slew rate and the output strength. The input is always active but is usually ignored while the output is active. Each pin can optionally have a weak pull-up or a weak pull-down resistor.

Most signal pin pairs can be configured as differential input pairs or output pairs. Differential input pin pairs can optionally be terminated with a 100Ω internal resistor. The XQRKU060 device supports differential standards beyond LVDS, including RSDS, BLVDS, differential SSTL, and differential HSTL. Each of the I/Os supports memory I/O standards, such as single-ended and differential HSTL as well as single-ended and differential SSTL.

3-State Digitally Controlled Impedance and Low Power I/O Features

The 3-state digitally controlled impedance (T_DCI) can control the output drive impedance (series termination) or can provide parallel termination of an input signal to V_{CCO} or split (Thevenin) termination to V_{CCO}/2. This allows users to eliminate off-chip termination for signals using T_DCI. In addition to board space savings, the termination automatically turns off when in output mode or when 3-stated, saving considerable power compared to off-chip termination. The I/Os also have low power modes for IBUF and IDELAY to provide further power savings, especially when used to implement memory interfaces.

I/O Logic

Input and Output Delay

All inputs and outputs can be configured as either combinatorial or registered. Double data rate (DDR) is supported by all inputs and outputs. Any input or output can be individually delayed by up to 1,250 ps of delay with a resolution of 5–15 ps. Such delays are implemented as IDELAY and ODELAY. The number of delay steps can be set by configuration and can also be incremented or decremented while in use. The IDELAY and ODELAY can be cascaded together to double the amount of delay in a single direction.

ISERDES and OSERDES

Many applications combine high-speed, bit-serial I/O with slower parallel operation inside the device. This requires a serializer and deserializer (SerDes) inside the I/O logic. Each I/O pin possesses an IOSERDES (ISERDES and OSERDES) capable of performing serial-to-parallel or parallel-to-serial conversions with programmable widths of 2, 4, or 8 bits. These I/O logic features enable high-performance interfaces, such as Gigabit Ethernet/1000BaseX/SGMII, to be moved from the transceivers to the SelectIO™ interface.

High-Speed Serial Transceivers

Serial data transmission between devices on the same PCB, over backplanes, and across even longer distances is becoming increasingly important. Specialized dedicated on-chip circuitry and differential I/O capable of coping with the signal integrity issues are required at these high data rates.

The XQRKU060 FPGA has GTH transceivers. All transceivers are arranged in groups of four, known as a transceiver Quad. Each serial transceiver is a combined transmitter and receiver.

GTH Transceivers

The serial transmitter and receiver are independent circuits that use an advanced phase-locked loop (PLL) architecture to multiply the reference frequency input by certain programmable numbers between 4 and 25 to become the bit-serial data clock. Each transceiver has a large number of user-definable features and parameters. All of these can be defined during device configuration, and many can also be modified during operation.

Transmitter

The transmitter is fundamentally a parallel-to-serial converter with a conversion ratio of 16, 20, 32, 40, 64, or 80. This allows the designer to trade off datapath width against timing margin in high-performance designs. These transmitter outputs drive the PC board with a single-channel differential output signal. TXOUTCLK is the appropriately divided serial data clock and can be used directly to register the parallel data coming from the internal logic. The incoming parallel data is fed through a FIFO and has additional hardware support for the 8B/10B, 64B/66B, or 64B/67B encoding schemes to provide a sufficient number of transitions. The bit-serial output signal drives two package pins with differential signals. This output signal pair has programmable signal swing as well as programmable pre- and post-emphasis to compensate for PC board losses and other interconnect characteristics. For shorter channels, the swing can be reduced to reduce power consumption.

Receiver

The receiver is fundamentally a serial-to-parallel converter, changing the incoming bit-serial differential signal into a parallel stream of words, each 16, 20, 32, 40, 64, or 80 bits. This allows the designer to trade off internal datapath width against logic timing margin. The receiver takes the incoming differential data stream, feeds it through programmable DC automatic gain control, linear and decision feedback equalizers (to compensate for PC board, cable, optical and other interconnect characteristics), and uses the reference clock input to initiate clock recognition. There is no need for a separate clock line. The data pattern uses non-return-to-zero (NRZ) encoding and optionally ensures sufficient data transitions by using the selected encoding scheme. Parallel data is then transferred into the device logic using the RXUSRCLK clock. For short channels, the transceivers offer a special low-power mode (LPM) to reduce power consumption by approximately 30%. The receiver DC automatic gain control and linear and decision feedback equalizers can optionally *auto-adapt* to automatically learn and compensate for different interconnect characteristics. This enables even more margin for 10G+ and 25G+ backplanes.

Out-of-Band Signaling

The transceivers provide out-of-band (OOB) signaling, often used to send low-speed signals from the transmitter to the receiver while high-speed serial data transmission is not active. This is typically done when the link is in a powered-down state or has not yet been initialized. This benefits PCIe and SATA/SAS and QPI applications.

Integrated Interface Blocks for PCI Express Designs

The integrated block for PCIe on the XQRKU060 device is compliant with the PCI Express Base Specification v3.1 and can operate with a lane width of up to x8 and a speed up to 8.0 GT/s (Gen3).

All integrated blocks for PCIe can be configured as Endpoint or Root Port. The Root Port can be used to build the basis for a compatible Root Complex, to allow custom chip-to-chip communication via the PCI Express protocol, and to attach ASSP Endpoint devices, such as Ethernet Controllers or Fibre Channel HBAs, to the FPGA.

The maximum lane widths and data rates per family are listed in Table 5.

Table 5: **PCIe Maximum Configurations**

Gen1 (2.5 GT/s)	x8
Gen2 (5 GT/s)	x8
Gen3 (8 GT/s)	x8

For high-performance applications, advanced buffering techniques of the block offer a flexible maximum payload size of up to 1,024 bytes. The integrated block interfaces to the integrated high-speed transceivers for serial connectivity and to block RAMs for data buffering. Combined, these elements implement the Physical Layer, Data Link Layer, and Transaction Layer of the PCI Express protocol.

Xilinx provides LogiCORE™ IP options to configure the integrated blocks for PCIe in the XQRKU060 device. This includes AXI-Stream interfaces at the PCIe packet level and more advanced IP such as AXI to PCIe Bridges and DMA engines. This IP gives the designer control over many configurable parameters such as link width and speed, maximum payload size, and reference clock frequency. For a complete list of features that can be configured for each of the IP, go to the specific Product Guide.

Clock Management

The clock generation and distribution components are located adjacent to the columns that contain the memory interface and input and output circuitry. This tight coupling of clocking and I/O provides low-latency clocking to the I/O for memory interfaces and other I/O protocols. Within every clock management tile (CMT) resides one mixed-mode clock manager (MMCM), two PLLs, clock distribution buffers and routing, and dedicated circuitry for implementing external memory interfaces.

MMCM

The MMCM can serve as a frequency synthesizer for a wide range of frequencies and as a jitter filter for incoming clocks. At the center of the MMCM is a voltage-controlled oscillator (VCO), which speeds up and slows down depending on the input voltage it receives from the phase frequency detector (PFD).

There are three sets of programmable frequency dividers (D, M, and O) that are programmable by configuration and during normal operation via the Dynamic Reconfiguration Port (DRP). The pre-divider D reduces the input frequency and feeds one input of the phase/frequency comparator. The feedback divider M acts as a multiplier because it divides the VCO output frequency before feeding the other input of the phase comparator. D and M must be chosen appropriately to keep the VCO within its specified frequency range. The VCO has eight equally-spaced output phases (0°, 45°, 90°, 135°, 180°, 225°, 270°, and 315°). Each phase can be selected to drive one of the output dividers, and each divider is programmable by configuration to divide by any integer from 1 to 128.

The MMCM has three input-jitter filter options: low bandwidth, high bandwidth, or optimized mode. Low-Bandwidth mode has the best jitter attenuation. High-Bandwidth mode has the best phase offset. Optimized mode allows the tools to find the best setting.

The MMCM can have a fractional counter in either the feedback path (acting as a multiplier) or in one output path. Fractional counters allow non-integer increments of 1/8 and can thus increase frequency

synthesis capabilities by a factor of 8. The MMCM can also provide fixed or dynamic phase shift in small increments that depend on the VCO frequency. At 1,600 MHz, the phase-shift timing increment is 11.2 ps.

PLL

With fewer features than the MMCM, the two PLLs in a clock management tile are primarily present to provide the necessary clocks to the dedicated memory interface circuitry. The circuit at the center of the PLLs is similar to the MMCM, with PFD feeding a VCO and programmable M, D, and O counters. There are two divided outputs to the device fabric per PLL as well as one clock plus one enable signal to the memory interface circuitry.

Clock Distribution

Clocks are distributed throughout the XQRKU060 device via buffers that drive a number of vertical and horizontal tracks. There are 24 horizontal clock routes per clock region and 24 vertical clock routes per clock region with 24 additional vertical clock routes adjacent to the MMCM and PLL. Within a clock region, clock signals are routed to the device logic (CLBs, etc.) via 16 gateable leaf clocks.

Several types of clock buffers are available. The BUFGCE and BUFCE_LEAF buffers provide clock gating at the global and leaf levels, respectively. BUFGCTRL provides glitchless clock muxing and gating capability. BUFGCE_DIV has clock gating capability and can divide a clock by 1 to 8. BUFG_GT performs clock division from 1 to 8 for the transceiver clocks.

Memory Interfaces

Memory interface data rates continue to increase, driving the need for dedicated circuitry that enables high performance, reliable interfacing to current and next-generation memory technologies. Every UltraScale device includes dedicated physical interfaces (PHY) blocks located between the CMT and I/O columns that support implementation of high-performance PHY blocks to external memories such as DDR4, DDR3, QDRII+, and RLDRAM3. The PHY blocks in each I/O bank generate the address/control and data bus signaling protocols as well as the precision clock/data alignment required to reliably communicate with a variety of high-performance memory standards. Multiple I/O banks can be used to create wider memory interfaces. See Migration between the XCKU060-FFVA1517 and XQRKU060-CNA1509 for memory interface pinout restrictions.

Block RAM

The XQRKU060 FPGA contains a number of 36 Kb block RAMs, each with two completely independent ports that share only the stored data. Each block RAM can be configured as one 36 Kb RAM or two independent 18 Kb RAMs. Each memory access, read or write, is controlled by the clock. Connections in every block RAM column enable signals to be cascaded between vertically adjacent block RAMs, providing an easy method to create large, fast memory arrays, and FIFOs with greatly reduced power consumption.

All inputs, data, address, clock enables, and write enables are registered. The input address is always clocked (unless address latching is turned off), retaining data until the next operation. An optional output data pipeline register allows higher clock rates at the cost of an extra cycle of latency. During a write operation, the data output can reflect either the previously stored data or the newly written data, or it can remain unchanged. Block RAM sites that remain unused in the user design are automatically powered down to reduce total power consumption. There is an additional pin on every block RAM to control the dynamic power gating feature.

Programmable Data Width

Each port can be configured as 32K × 1; 16K × 2; 8K × 4; 4K × 9 (or 8); 2K × 18 (or 16); 1K × 36 (or 32); or 512 × 72 (or 64). Whether configured as block RAM or FIFO, the two ports can have different aspect ratios without any constraints. Each block RAM can be divided into two completely independent 18 Kb block RAMs that can each be configured to any aspect ratio from 16K × 1 to 512 × 36. Everything described previously for the full 36Kb block RAM also applies to each of the smaller 18Kb block RAMs. Only in simple dual-port (SDP) mode can data widths of greater than 18 bits (18 Kb RAM) or 36 bits (36 Kb RAM) be accessed. In this mode, one port is dedicated to read operation, the other to write operation. In SDP mode, one side (read or write) can be variable, while the other is fixed to 32/36 or 64/72. Both sides of the dual-port 36Kb RAM can be of variable width.

Error Detection and Correction

Each 64-bit-wide block RAM can generate, store, and utilize eight additional Hamming code bits and perform single-bit error correction and double-bit error detection (ECC) during the read process. The ECC logic can also be used when writing to or reading from external 64- to 72-bit-wide memories.

FIFO Controller

Each block RAM can be configured as a 36 Kb FIFO or an 18 Kb FIFO. The built-in FIFO controller for single-clock (synchronous) or dual-clock (asynchronous or multirate) operation increments the internal addresses and provides four handshaking flags: full, empty, programmable full, and programmable empty. The programmable flags allow the user to specify the FIFO counter values that make these flags go active. The FIFO width and depth are programmable with support for different read port and write port widths on a single FIFO. A dedicated cascade path allows for easy creation of deeper FIFOs.

Configurable Logic Block

Every configurable logic block (CLB) in the XQRKU060 FPGA contains 8 LUTs and 16 flip-flops. The LUTs can be configured as either one 6-input LUT with one output, or as two 5-input LUTs with separate outputs but common inputs. Each LUT can optionally be registered in a flip-flop. In addition to the LUTs and flip-flops, the CLB contains arithmetic carry logic and multiplexers to create wider logic functions.

Each CLB contains one slice. There are two types of slices: SLICEL and SLICEM. LUTs in the SLICEM can be configured as 64-bit RAM, as 32-bit shift registers (SRL32), or as two SRL16s. CLBs in the XQRKU060 FPGA have increased routing and connectivity compared to CLBs in previous-generation Xilinx devices. They

also have additional control signals to enable superior register packing, resulting in overall higher device utilization.

Interconnect

Various length vertical and horizontal routing resources in the XQRKU060 FPGA that span 1, 2, 4, 5, 12, or 16 CLBs ensure that all signals can be transported from source to destination with ease, providing support for the next generation of wide data buses to be routed while simultaneously improving quality of results and software run time.

Digital Signal Processing

DSP applications use many binary multipliers and accumulators, best implemented in dedicated DSP slices. The XQRKU060 FPGA has many dedicated, low-power DSP slices, combining high speed with small size while retaining system design flexibility.

Each DSP slice fundamentally consists of a dedicated 27 × 18 bit twos complement multiplier and a 48-bit accumulator. The multiplier can be dynamically bypassed, and two 48-bit inputs can feed a single-instruction-multiple-data (SIMD) arithmetic unit (dual 24-bit add/subtract/accumulate or quad 12-bit add/subtract/accumulate), or a logic unit that can generate any one of ten different logic functions of the two operands.

The DSP includes an additional pre-adder, typically used in symmetrical filters. This pre-adder improves performance in densely packed designs and reduces the DSP slice count by up to 50%. The 96-bit-wide XOR function, programmable to 12, 24, 48, or 96-bit widths, enables performance improvements when implementing forward error correction and cyclic redundancy checking algorithms.

The DSP also includes a 48-bit-wide pattern detector that can be used for convergent or symmetric rounding. The pattern detector is also capable of implementing 96-bit-wide logic functions when used in conjunction with the logic unit.

The DSP slice provides extensive pipelining and extension capabilities that enhance the speed and efficiency of many applications beyond digital signal processing, such as wide dynamic bus shifters, memory address generators, wide bus multiplexers, and memory-mapped I/O register files. The accumulator can also be used as a synchronous up/down counter.

System Monitor

The System Monitor block enhances the overall safety, security, and reliability of the system by monitoring the physical environment via on-chip power supply and temperature sensors and external channels to the ADC. Key System Monitor features are shown in Table 6.

Table 6: **Key System Monitor Features**

ADC	10-bit 200 kSPS
Interfaces	JTAG, I2C, DRP

In the XQRKU060 FPGA, sensor outputs and up to 17 user-allocated external analog inputs are digitized using a 10-bit 200 kilo-sample-per-second (kSPS) ADC, and the measurements are stored in registers that can be accessed via internal FPGA (DRP), JTAG, or I2C interfaces. The I2C interface allows the on-chip monitoring to be easily accessed by the System Manager/Host before and after device configuration.

Configuration

The XQRKU060 FPGA stores its customized configuration in SRAM-type internal latches. The configuration storage is volatile and must be reloaded whenever the device is powered up. This storage can also be reloaded at any time. Several methods and data formats for loading configuration are available, determined by the mode pins, with more dedicated configuration datapath pins to simplify the configuration process.

The XQRKU060 FPGA supports secure and non-secure boot with optional Advanced Encryption Standard - Galois/Counter Mode (AES-GCM) decryption and authentication logic. If only authentication is required, the XQRKU060 FPGA provides an alternative form of authentication in the form of RSA algorithms. For RSA authentication support in the XQRKU060 FPGA, go to *UltraScale Architecture Configuration User Guide* (UG570).

The XQRKU060 FPGA also has the ability to select between multiple configurations, and support robust field-update methodologies. This is especially useful for updates to a design after the end product has been shipped and launched. Designers can make last-minute changes right up to the launch of a spacecraft as well as in-orbit reconfiguration as algorithms change. This feature allows designers to keep their customers current with the most up-to-date design while the product is already deployed in orbit.

Configuring the FPGA

The SPI (serial NOR) interface (x1, x2, x4, and dual x4 modes) and the BPI (parallel NOR) interface (x8 and x16 modes) are two common methods used for configuring the FPGA. Users can directly connect an SPI or BPI flash to the FPGA, and the FPGA's internal configuration logic reads the bitstream out of the flash and configures itself, eliminating the need for an external controller. The FPGA automatically detects the bus width on the fly, eliminating the need for any external controls or switches. Bus widths supported are x1, x2, x4, and dual x4 for SPI, and x8 and x16 for BPI. The larger bus widths increase configuration speed and reduce the amount of time it takes for the FPGA to start up after power-on.

In master mode, the FPGA can drive the configuration clock from an internally generated clock, or for higher speed configuration, the FPGA can use an external configuration clock source. This allows high-speed configuration with the ease of use characteristic of master mode. Slave modes up to 32 bits wide that are especially useful for processor-driven configuration are also supported by the FPGA. In addition, the new media configuration access port (MCAP) provides a direct connection between the integrated block for PCIe and the configuration logic to simplify configuration over PCIe.

Configuration Memory Soft Error Detection and Correction

The XQRKU060 FPGA includes configuration memory soft error detection features and configuration interfaces that can be used to implement configuration memory error detection and correction methods. See the *UltraScale Architecture Configuration User Guide* (UG570) for further information.

When a system is simultaneously accessing the XQRKU060 configuration memory for soft error detection or correction, additional noise artifacts from the internal configuration memory system activity can impact device operation beyond the characteristics specified in this data sheet. See Additional Design Considerations for Configuration Memory Access Effects for guidance and mitigation of configuration readback induced time interval error in MMCMs and PLLs.

Migration between the XCKU060-FFVA1517 and XQRKU060-CNA1509

The XQRKU060 device is available in a ceramic flip-chip column grid array (CNA1509) package. The CNA1509 package is surface mount-compatible and uses high-temperature solder columns as interconnections to the board. Compared to the solder spheres, the columns have lower stiffness and provide a higher stand-off. These features significantly increase the reliability of the solder joints. When combined with a high-density, multi-layer ceramic substrate, this packaging technology offers a high-density, reliable packaging solution.

The XQRKU060-CNA1509 device/package is footprint-compatible with the XCKU060-FFVA1517 device/package. A PCB can be designed that supports design development with the XCKU060-FFVA1517 and migration to the XQRKU060-CNA1509. For this migration, the following provides tools design guidelines and PCB design guidelines.

For timing-compatible designs targeting the XCKU060-FFVA1517 and XQRKU060-CNA1509, use the respective `xcku060-ffva1517-1LV-i` and `xqrku060-cna1509-1M-m` selections in the Vivado® design tools. These Vivado tools part selections have similar performance.

Note: The part order code for the compatible XCKU060 device is XCKU060-1FFVA1517I.

The footprints of the FFVA1517 and CNA1509 are the same with a few exceptions listed below. The spacing between the balls of the FFVA1517 package and columns of the CNA1509 package is 1.0 mm. Refer to the mechanical drawings for differences between the package dimensions that can affect keep-out spacing, thermal design, and solderability.

The footprints of the FFVA1517 and CNA1509 are compatible when the recommendations in Table 7 are followed. The CNA1509 package does not have corresponding columns for eight ball locations near the corners of the FFVA1517 package ball grid array. See the device diagrams and mechanical drawing for details. These absent columns are indicated by the NA symbol in the XQRKU060-CNA1509 pin function list in Table 7.

Table 7: **XCKU060-FFVA1517 to XQRKU060-CNA1509 Migration Recommendations**

Pin Location	XCKU060-FFVA1517 Pin Function	XQRKU060-CNA1509 Pin Function	Recommended Board Connection/ Function Design Use
A2	GND	NA	No Connect/Do Not Use
A38	IO_L17N_T2U_N9_AD10N_46	NA	No Connect/Do Not Use
B1	NC	NA	No Connect/Do Not Use
B39	IO_L16N_T2U_N7_QBC_AD3N_46	NA	No Connect/Do Not Use
T1	NC	MGTHRXN1_224	No Connect[1]/Do Not Use
T2	NC	MGTHRXP1_224	No Connect[1]/Do Not Use
T12	GND	GND_SENSE	GND_SENSE provides direct access to the device's internal GND plane for measurements. If not used, leave unconnected/floating.
T13	VCCINT	VCCINT_SENSE	The VCCINT_SENSE pin provides direct access to the device's internal V_{CCINT} power plane. Connect to the V_{CCINT} power supply voltage sensing circuit for the device's V_{CCINT} voltage.[2]
U26	VCCINT_IO	VCCINT	Connect to V_{CCINT} power supply
W26	VCCINT_IO	VCCINT	Connect to V_{CCINT} power supply
AA26	VCCINT_IO	VCCINT	Connect to V_{CCINT} power supply
AB25	VCCINT_IO	VCCINT	Connect to V_{CCINT} power supply
AC26	VCCINT_IO	VCCINT	Connect to V_{CCINT} power supply
AV1	MGTHRXN1_224	NA	No Connect[1]/Do Not Use
AV2	MGTHRXP1_224	NC	No Connect[1]/Do Not Use
AV39	IO_L8N_T1L_N3_AD5N_25	NA	No Connect/Do Not Use
AW2	GND	NA	No Connect/Do Not Use
AW38	IO_T1U_N12_25	NA	No Connect/Do Not Use

Notes:

1. The MGTHRXN1_224/MGTHRXP1_224 receiver signals are connected to different sets of pins in the FFVA1517 package compared to the CNA1509 package. See GTH Transceiver Migration for recommended MGTHRXN1_224/MGTHRXP1_224 pin connections.
2. See V_{CCINT} Power Supply Voltage Sense Guidelines for VCCINT_SENSE guidelines. Refer to the power supply vendor's data sheet for remote sense recommendations related to the VCCINT power supply.
3. The IO_L17N_T2U_N9_AD10N_46 (A37), IO_L16P_T2U_N6_QBC_AD3P_46 (C38), and IO_L8P_T1L_N2_AD5P_25 (AV38) pins can only be used as single-ended I/O due to their unbonded complementary I/O in the CNA1509 package.

Power Supply Voltage Migration

The XQRKU060-CNA1509 ceramic package interconnect technology has higher IR drop characteristics than in the XCKU060-FFVA1517 package. A PCB that supports migration between the XQRKU060-CNA1509 and XCKU060-FFVA1517 must ensure the power supplies match the recommended operating voltages for the specific device mounted on the board. That is, if the XCKU060-FFVA1517 is mounted on the board, the power supplies must meet the recommended operating voltages specified in the *Kintex UltraScale FPGAs Data Sheet: DC and AC Switching Characteristics* (DS892). If the XQRKU060-CNA1509 is mounted on the board, use the Xilinx Power Estimator (XPE) tool to estimate power consumption and to determine the power supply voltages for the XQRKU060-CNA1509. XPE is available from the XQRKU060 area of the Xilinx Space Secure Site. XPE calculates the required regulator voltages to supply to the pins of the XQRKU060-CNA1509 based on the user power estimation. XPE factors

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in the current required and the package IR drop of the CNA1509 package to ensure die-level operating voltages for the XCKU060 device. System designers should allow for the XQRKU060-CNA1509 recommended voltage and interconnect performance differences versus the XCKU060-FFVA1517 device characteristics.

For the V_{CCINT} power supply, connect the VCCINT pins and use the VCCINT_SENSE pin per guidelines in V_{CCINT} Power Supply Voltage Sense Guidelines for the XQRKU060-CNA1509. The XQRKU060-CNA1509 V_{CCINT} power supply design and connections are compatible with the XCKU060-FFVA1517. However, the V_{CCINT} power supply voltage setting might need adjustment to match the recommended operating conditions for the XCKU060-FFVA1517.

VCCINT_IO Migration and Restrictions for SelectIO and Memory Interfaces

The XCKU060-FFVA1517 device has a separate set of VCCINT_IO pins which must be tied to the VCCINT power supply, but the XQRKU060-CNA1509 package does not have VCCINT_IO pins. Instead, the XQRKU060 V_{CCINT_IO} die pads are tied internally within the CNA1509 package to the V_{CCINT} rail. The VCCINT_IO pin locations in the FFVA1517 package are VCCINT pin locations in the CNA1509 package.

A few of the SelectIO interface pins are not bonded out in the CNA1509 package and must not be used in an FFVA1517 design that is to be migrated to a CNA1509 package. See Table 7 for the affected pins. Review each pin for specialized functions that can restrict some interface implementations. For example, the IO_L16N_T2U_N7_QBC_AD3N_46 pin (B39) is not connected in the CNA1509 package. Thus, designs have one fewer full bank clocking resource (QBC) in bank 46 in the CNA1509 package, which restricts migratable native mode interface designs from using this FFVA1517 bank 46 QBC pin. Due to this restriction certain system topologies cannot be implemented, such as systems with three x72 DDR memory interfaces.

The SelectIO signal package flight delays are different in the FFVA1517 package compared to the CNA1509 package. Designs for boards supporting migration between the CNA1509 and FFVA1517 packages should consider the impact of signal flight delay differences between these packages.

The SelectIO interfaces in the CNA1509 package have some limitations or maximum performance restrictions. QDRIV memory interfaces are not supported, and the maximum memory interface rate and maximum native-mode SelectIO interface rate are reduced. Designs for boards supporting migration between the CNA1509 and FFVA1517 packages should consider these restrictions. For the relevant interface specifications in the CNA1509 package, see Table 32 and Table 39.

GTH Transceiver Migration

If all 32 GTH transceivers are required and if migration between the FFVA1517 and CNA1509 is required, board design accommodations must be made for the MGTHRXN1_224/MGTHRXP1_224 receiver pair. The MGTHRXN1_224/MGTHRXP1_224 receiver signals are connected to different sets of pins in each package: AV1/AV2 in the FFVA1517 package and T1/T2 in the CNA1509 package. Otherwise, avoid use of the MGTHRXN1_224/MGTHRXP1_224 receiver pair when migration is required between the FFVA1517 and CNA1509. If the receiver pair is not used and if the system requires unused input pins to be tied, connect the unused MGTHRXN1_224/MGTHRXP1_224 pin locations (T1, T2, AV1, and AV2) to GND.

The GTH transceiver signal package flight delays are different in the FFVA1517 package compared to the CNA1509 package. Designs for boards supporting migration between the CNA1509 and FFVA1517 should consider the impact of signal flight delay differences between these packages.

Unsupported UltraScale Family Features in the XQRKU060 Device

Some features of the UltraScale family are not supported in the XQRKU060 device, including:

- QDRIV memory interfaces
- GTH TX buffer bypass and RX buffer bypass modes

See Migration between the XCKU060-FFVA1517 and XQRKU060-CNA1509 for native mode memory interface limitations.

RT Kintex UltraScale XQRKU060 FPGA Electrical Characteristics Introduction

The RT Kintex UltraScale XQRKU060 FPGA is available in the -1M speed grade. All supply voltage and junction temperature specifications are representative of worst-case conditions across the M-grade temperature range. The parameters included are common to popular designs and typical applications.

DC Characteristics

Table 8: **Absolute Maximum Ratings[1]**

Symbol	Description	Min	Max	Units
FPGA Logic				
V_{CCINT}	Internal supply voltage[2]	−0.500	1.100	V
V_{CCAUX}	Auxiliary supply voltage	−0.500	2.000	V
V_{CCAUX_IO}[3]	Auxiliary supply voltage for the I/O banks	−0.500	2.000	V
V_{CCBRAM}	Supply voltage for the block RAM memories	−0.500	1.100	V
V_{CCO}	Output drivers supply voltage for HR I/O banks	−0.500	3.468	V
	Output drivers supply voltage for HP I/O banks	−0.500	2.000	V
V_{REF}	Input reference voltage	−0.500	2.000	V
V_{IN}[4][5][6]	I/O input voltage for HR I/O banks	−0.400	V_{CCO} + 0.550	V
	I/O input voltage for HP I/O banks	−0.550	V_{CCO} + 0.550	V
	I/O input voltage (when V_{CCO} = 3.3V) for V_{REF} and differential I/O standards except TMDS_33[7]	−0.400	2.625	V
V_{BATT}	Key memory battery backup supply	−0.500	2.000	V

Table 8: **Absolute Maximum Ratings[1] *(Cont'd)***

Symbol	Description	Min	Max	Units
I_{DC}	Available output current at the pad	−20	20	mA
I_{RMS}	Available RMS output current at the pad	−20	20	mA
GTH Transceivers				
$V_{MGTAVCC}$	Analog supply voltage for the GTH transmitter and receiver circuits	−0.500	1.100	V
$V_{MGTAVTT}$	Analog supply voltage for the GTH transmitter and receiver termination circuits	−0.500	1.320	V
$V_{MGTVCCAUX}$	Auxiliary analog Quad PLL (QPLL) voltage supply for the GTH transceivers	−0.500	1.935	V
$V_{MGTREFCLK}$	GTH transceiver reference clocks absolute input voltage	−0.500	1.320	V
$V_{MGTAVTTRCAL}$	Analog supply voltage for the resistor calibration circuit of the GTH transceiver columns	−0.500	1.320	V
V_{IN}	Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage	−0.500	1.260	V
$I_{DCIN-FLOAT}$	DC input current for receiver input pins DC coupled RX termination = floating	–	0[8]	mA
$I_{DCIN-MGTAVTT}$	DC input current for receiver input pins DC coupled RX termination = $V_{MGTAVTT}$	–	10	mA
$I_{DCIN-GND}$	DC input current for receiver input pins DC coupled RX termination = GND	–	10	mA
$I_{DCIN-PROG}$	DC input current for receiver input pins DC coupled RX termination = Programmable	–	N/A[8]	mA
$I_{DCOUT-FLOAT}$	DC output current for transmitter pins DC coupled RX termination = floating	–	0[8]	mA
$I_{DCOUT-MGTAVTT}$	DC output current for transmitter pins DC coupled RX termination = $V_{MGTAVTT}$	–	6	mA
System Monitor				
V_{CCADC}	System Monitor supply relative to GNDADC	−0.500	2.000	V
V_{REFP}	System Monitor reference input relative to GNDADC	−0.500	2.000	V
Temperature				
T_{STG}	Storage temperature (ambient)	−65	150	°C
T_{SOL}	Maximum soldering temperature	–	220	°C
T_j	Maximum junction temperature	–	125	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. VCCINT_IO and VCCINT_SENSE are connected within the package to the internal VCCINT power plane.
3. V_{CCAUX_IO} must be connected to V_{CCAUX}.
4. The lower absolute voltage specification always applies.
5. For I/O operation, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).
6. The maximum limit applied to DC signals. For maximum undershoot and overshoot AC specifications, see Table 12 and Table 13.
7. See Table 18 for TMDS_33 specifications.
8. For more information on supported GTH transceiver terminations see the *UltraScale Architecture GTH Transceiver User Guide* (UG576).

For the recommended operating conditions in Table 9, use the Xilinx Power Estimator (XPE) tool to estimate power consumption and to determine the regulator power supply voltages for the XQRKU060-CNA1509. XPE calculates voltage levels relative to GND to supply to the pins of the XQRKU060-CNA1509 based on estimated power consumption to compensate for package IR drop. Refer to the table note references, where indicated, for further details or guidelines.

Table 9: **Recommended Operating Conditions[1]**

Symbol	Description	Min	Typ	Max[2]	Units
FPGA Logic					
V_{CCINT}[3]	Internal supply voltage	Typ – 4%	Use XPE[3]	Typ + 4%	V
V_{CCBRAM}[4]	Block RAM supply voltage	Typ – 3%[4]	Use XPE[4]	Typ + 3%[4]	V
V_{CCAUX}[5]	Auxiliary supply voltage	Typ – 3%	Use XPE	Typ + 3%	V
V_{CCAUX_IO}[5]	Auxiliary I/O supply voltage	Typ – 3%	Use XPE	Typ + 3%	V
V_{CCO}[6][7]	I/O supply voltage	Typ – 4%	Use XPE	Typ + 4%	V
V_{IN}	I/O input voltage	–0.200	–	V_{CCO} + 0.200	V
	I/O input voltage (when V_{CCO} = 3.3V) for V_{REF} and differential I/O standards except TMDS_33[8]	–	–	2.625	V
GTH Transceivers					
$V_{MGTAVCC}$[9]	Analog supply voltage for the GTH transceivers	Typ – 2%[9]	Use XPE	Typ + 2%[9]	V
$V_{MGTAVTT}$[9]	Analog supply voltage for the GTH transmitter and receiver termination circuits	Typ – 2%[9]	Use XPE	Typ + 2%[9]	V
$V_{MGTAVTTRCAL}$[9]	Analog supply voltage for the resistor calibration circuit of the GTH transceiver columns	Typ – 2%[9]	Use XPE[10]	Typ + 2%[9]	V
$V_{MGTVCCAUX}$[9]	Auxiliary analog QPLL voltage supply for the transceivers	Typ – 2%[9]	Use XPE	Typ + 2%[9]	V
SYSMON					
V_{CCADC}[11]	SYSMON supply relative to GNDADC	Typ – 3%	Use XPE	Typ + 5%	V
V_{REFP}[12]	SYSMON externally supplied reference voltage relative to VREFN	Typ – 4%	1.250	Typ + 4%	V

Table 9: **Recommended Operating Conditions[1] *(Cont'd)***

Symbol	Description	Min	Typ	Max[2]	Units
V_{BATT}[13]	Battery voltage	1.000	–	1.890	V

Notes:

1. Use the Xilinx Power Estimator (XPE) tool to estimate power consumption and to determine the regulator supply requirements for the typical voltages at the device pins relative to GND. Except for the GTH supply voltages, the min/max parameters specify the recommended voltage range that includes DC variation and AC ripple/noise. See PCB Design Guidelines for power supply guidelines.
2. The absolute maximum voltage specification always applies.
3. For V_{CCINT}, use XPE to estimate power consumption and to determine the V_{CCINT} regulator supply requirement for the typical voltage measured at the VCCINT_SENSE pin relative to GND. The VCCINT_SENSE pin provides direct access to the device's internal V_{CCINT} power plane for sensing and maintaining the V_{CCINT} voltage within the recommended operating conditions. VCCINT_IO is also connected within the package to the internal VCCINT power plane (see PCB Design Guidelines).
4. VCCBRAM is recommended to be tied to VCCINT, and when VCCBRAM is tied to VCCINT, V_{CCBRAM} is permitted to operate under the same conditions as VCCINT (Typ ±4%). Otherwise, for a separately supplied V_{CCBRAM}, use XPE to estimate power consumption and to determine the V_{CCBRAM} regulator supply requirement for the typical voltage at the VCCBRAM pin, and the recommended operating range is ±3%.
5. V_{CCAUX_IO} must be connected to V_{CCAUX}.
6. Use the XPE tool to estimate power consumption and to determine each V_{CCO} regulator supply requirement. All further references to VCCO represent the nominal signal voltage of 1.0V (HP I/O only), 1.2V, 1.35V, 1.5V, 1.8V, 2.5V (HR I/O only), or 3.3V (HR I/O only).
7. The dedicated configuration bank is an HR I/O bank with VCCO_0 support limited to 1.8V nominal when CFGBVS is tied to GND, or 2.5V or 3.3V nominal when CFGBVS is tied to VCCO_0. The VCCO_0 minimum recommended operating voltage for power on and during configuration is 1.425V. After configuration, data is retained even if VCCO_0 drops to 0V.
8. See Table 18 for TMDS_33 specifications.
9. For only the GTH voltages, the min/max parameters specify the recommended voltage range of DC variation. For optimal GTH transceiver performance, power supply noise must be less than 10 mVpp. See the *UltraScale Architecture GTH Transceiver User Guide* (UG576) for power supply and filtering guidelines.
10. When used, MGTAVTTRCAL is connected to MGTAVTT. See XPE for the $V_{MGTAVTT}$ voltage. See the *UltraScale Architecture GTH Transceiver User Guide* (UG576) for MGTAVTTRCAL guidelines.
11. See the *UltraScale Architecture System Monitor User Guide* (UG580) for V_{CCADC} supply filtering recommendations.
12. For the SYSMON reference voltage, an alternate internally-supplied, on-chip reference voltage can be used by tying VREFP and VREFN to GNDADC.
13. V_{BATT} is required only when an encryption key is stored in battery-backed RAM. If battery-backed RAM is not used, connect VBATT to either ground or VCCAUX.

Table 10: **Recommended Operating Conditions - Junction Temperature**

Symbol	Description	Min	Typ	Max	Units
Temperature					
T_j	Junction temperature operating range for M-grade devices	−55	–	125	°C

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Table 11: **DC Characteristics Over Recommended Operating Conditions**

Symbol	Description	Min	Typ[1]	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data might be lost)	0.82	–	–	V
V_{DRAUX}	Data retention V_{CCAUX} voltage (below which configuration data might be lost)	1.50	–	–	V
I_{REF}	V_{REF} leakage current per pin	–	–	15	µA
I_L	Input or output leakage current per pin (sample-tested)	–	–	20[2]	µA
C_{IN}[3]	Die input capacitance at the pad (HP I/O)	–	–	3.75	pF
	Die input capacitance at the pad (HR I/O)	–	–	7.00	pF
I_{RPU}	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO} = 3.3V	75	–	175	µA
	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO} = 2.5V	50	–	169	µA
	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO} = 1.8V	60	–	678	µA
	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO} = 1.5V	30	–	450	µA
	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO} = 1.2V	10	–	262	µA
I_{RPD}	Pad pull-down (when selected) at V_{IN} = 3.3V	60	–	190	µA
	Pad pull-down (when selected) at V_{IN} = 1.8V	29	–	685	µA
I_{CCADC}	Analog supply current per SYSMON instance in powered up state	–	–	19.2	mA
I_{BATT}[4]	Battery supply current	–	–	150	nA
Calibrated programmable on-die termination (DCI) in HP I/O banks[6] (measured per JEDEC specification)					
R[7]	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 where ODT = RTT_40	–10%[5]	40	+10%[5]	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 where ODT = RTT_48	–10%[5]	48	+10%[5]	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 where ODT = RTT_60	–10%[5]	60	+10%[5]	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_40	–10%[5]	40	+10%[5]	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_48	–10%[5]	48	+10%[5]	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_60	–10%[5]	60	+10%[5]	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_120	–10%[5]	120	+10%[5]	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_240	–10%[5]	240	+10%[5]	Ω

Table 11: **DC Characteristics Over Recommended Operating Conditions** *(Cont'd)*

Symbol	Description	Min	Typ[1]	Max	Units
Uncalibrated programmable on-die termination in HP I/Os banks (measured per JEDEC specification)					
R[7]	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where ODT = RTT_40	−50%	40	+50%	Ω
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where ODT = RTT_48	−50%	48	+50%	Ω
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where ODT = RTT_60	−50%	60	+50%	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_40	−50%	40	+50%	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_48	−50%	48	+50%	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_60	−50%	60	+50%	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_120	−50%	120	+50%	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_240	−50%	240	+50%	Ω
Uncalibrated programmable on-die termination in HR I/O banks (measured per JEDEC specification)					
R[7]	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where ODT = RTT_40	−50%	40	+50%	Ω
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where ODT = RTT_48	−50%	48	+50%	Ω
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where ODT = RTT_60	−50%	60	+50%	Ω
Internal V_{REF}	50% V_{CCO}	V_{CCO} x 0.49	V_{CCO} x 0.50	V_{CCO} x 0.51	V
	70% V_{CCO}	V_{CCO} x 0.69	V_{CCO} x 0.70	V_{CCO} x 0.71	V
Differential termination	Programmable differential termination (TERM_100)	–	100	–	Ω
n	Temperature diode ideality factor	–	1.002	–	–
r	Temperature diode series resistance	–	2	–	Ω

Notes:
1. Typical values are specified at nominal voltage, 25°C.
2. For HP I/O banks with a V_{CCO} of 1.8V and separated V_{CCO} and V_{CCAUX_IO} power supplies, the I_L maximum current is 70 μA.
3. This measurement represents the die capacitance at the pad, not including the package.
4. Maximum value specified for worst case process at 25°C.
5. If VRP resides at a different bank (DCI cascade), the range increases to ±15%.
6. VRP resistor tolerance is (240Ω ±1%)
7. On-die input termination resistance, for more information see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).
8. Use the Xilinx Power Estimator (XPE) tool to estimate static and dynamic power consumption, and to determine minimum required supply current to ensure proper power on.

Table 12: **V$_{IN}$ Maximum Allowed AC Voltage Overshoot and Undershoot for HR I/O Banks**[1][2]

AC Voltage Overshoot	% of UI	AC Voltage Undershoot	% of UI
V$_{CCO}$ + 0.30	100%	−0.30	100%
V$_{CCO}$ + 0.35	100%	−0.35	70.00%
V$_{CCO}$ + 0.40	100%	−0.40	27.00%
V$_{CCO}$ + 0.45	100%	−0.45	10.00%
V$_{CCO}$ + 0.50	85.00%	−0.50	5.00%
V$_{CCO}$ + 0.55	70.00%	−0.55	2.10%
V$_{CCO}$ + 0.60	46.60%	−0.60	1.50%
V$_{CCO}$ + 0.65	21.20%	−0.65	1.10%
V$_{CCO}$ + 0.70	9.75%	−0.70	0.60%
V$_{CCO}$ + 0.75	4.55%	−0.75	0.45%
V$_{CCO}$ + 0.80	2.15%	−0.80	0.20%
V$_{CCO}$ + 0.85	1.00%	−0.85	0.10%
V$_{CCO}$ + 0.90	0.50%	−0.90	0.05%
V$_{CCO}$ + 0.95	0.25%	−0.95	0.05%

Notes:
1. A total of 200 mA per bank should not be exceeded.
2. For UI smaller than 20 µs.

Table 13: **V$_{IN}$ Maximum Allowed AC Voltage Overshoot and Undershoot for HP I/O Banks**[1][2]

AC Voltage Overshoot	% of UI	AC Voltage Undershoot	% of UI
V$_{CCO}$ + 0.05	100%	−0.05	100%
V$_{CCO}$ + 0.10	100%	−0.10	100%
V$_{CCO}$ + 0.15	100%	−0.15	100%
V$_{CCO}$ + 0.20	100%	−0.20	100%
V$_{CCO}$ + 0.25	100%	−0.25	100%
V$_{CCO}$ + 0.30	100%	−0.30	100%
V$_{CCO}$ + 0.35	92.00%	−0.35	92.00%
V$_{CCO}$ + 0.40	70.00%	−0.40	40.00%
V$_{CCO}$ + 0.45	30.00%	−0.45	15.00%
V$_{CCO}$ + 0.50	15.00%	−0.50	10.00%
V$_{CCO}$ + 0.55	10.00%	−0.55	4.00%
V$_{CCO}$ + 0.60	8.00%	−0.60	0.00%
V$_{CCO}$ + 0.65	6.00%	−0.65	0.00%
V$_{CCO}$ + 0.70	4.00%	−0.70	0.00%
V$_{CCO}$ + 0.75	2.00%	−0.75	0.00%
V$_{CCO}$ + 0.80	2.00%	−0.80	0.00%
V$_{CCO}$ + 0.85	2.00%	−0.85	0.00%

Notes:
1. A total of 200 mA per bank should not be exceeded.
2. For UI smaller than 20 µs.

Power-On/Off Power Supply Sequencing

The recommended power-on sequence is V_{CCINT}, V_{CCBRAM}, V_{CCAUX}/V_{CCAUX_IO}, and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. V_{CCAUX} and V_{CCAUX_IO} must be connected together. When the current minimums are met, the device powers on after the V_{CCINT}, V_{CCBRAM}, V_{CCAUX}/V_{CCAUX_IO}, and V_{CCO} supplies have all passed through their power-on reset threshold voltages.

V_{CCADC} and V_{REF} can be powered at any time and have no power-up sequencing recommendations.

The recommended power-on sequence to achieve minimum current draw for the GTH transceivers is V_{CCINT}, $V_{MGTAVCC}$, $V_{MGTAVTT}$ OR $V_{MGTAVCC}$, V_{CCINT}, $V_{MGTAVTT}$. There is no recommended sequencing for $V_{MGTVCCAUX}$. Both $V_{MGTAVCC}$ and V_{CCINT} can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw. If these recommended sequences are not met, current drawn from $V_{MGTAVTT}$ can be higher than specifications during power-up and power-down.

Use the Xilinx Power Estimator (XPE) tool to estimate power supply static and dynamic operating current requirements and to determine the minimum required power supply current for proper device power-on. The XPE tool reports the minimum power-on current requirement, when a power supply's power-on current requirement exceeds the estimated operating current requirements, and when the maximum process is selected.

Table 14 shows the power supply ramp time.

Table 14: **Power Supply Ramp Time**

Symbol	Description	Min	Max	Units
T_{VCCINT}	Ramp time from GND to 95% of V_{CCINT}	0.2	40	ms
T_{VCCO}	Ramp time from GND to 95% of V_{CCO}	0.2	40	ms
T_{VCCAUX}	Ramp time from GND to 95% of V_{CCAUX}	0.2	40	ms
$T_{VCCBRAM}$	Ramp time from GND to 95% of V_{CCBRAM}	0.2	40	ms
$T_{MGTAVCC}$	Ramp time from GND to 95% of $V_{MGTAVCC}$	0.2	40	ms
$T_{MGTAVTT}$	Ramp time from GND to 95% of $V_{MGTAVTT}$	0.2	40	ms
$T_{MGTVCCAUX}$	Ramp time from GND to 95% of $V_{MGTVCCAUX}$	0.2	40	ms

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested. See Migration between the XCKU060-FFVA1517 and XQRKU060-CNA1509 for assumptions of die-level operating voltages.

Table 15: **SelectIO DC Input and Output Levels For HR I/O Banks**[1][2]

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
HSTL_I	−0.300	V_{REF} − 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} − 0.400	8.0	−8.0
HSTL_I_18	−0.300	V_{REF} − 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} − 0.400	8.0	−8.0
HSTL_II	−0.300	V_{REF} − 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} − 0.400	16.0	−16.0
HSTL_II_18	−0.300	V_{REF} − 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} − 0.400	16.0	−16.0
HSUL_12	−0.300	V_{REF} − 0.130	V_{REF} + 0.130	V_{CCO} + 0.300	20% V_{CCO}	80% V_{CCO}	0.1	−0.1
LVCMOS12	−0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.400	V_{CCO} − 0.400	Note 3	Note 3
LVCMOS15	−0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} − 0.450	Note 4	Note 4
LVCMOS18	−0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} − 0.450	Note 4	Note 4
LVCMOS25	−0.300	0.700	1.700	V_{CCO} + 0.300	0.400	V_{CCO} − 0.400	Note 4	Note 4
LVCMOS33	−0.300	0.800	2.000	3.400	0.400	V_{CCO} − 0.400	Note 4	Note 4
LVTTL	−0.300	0.800	2.000	3.400	0.400	2.400	Note 4	Note 4
SSTL12	−0.300	V_{REF} − 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	$V_{CCO}/2$ − 0.150	$V_{CCO}/2$ + 0.150	14.25	−14.25
SSTL135	−0.300	V_{REF} − 0.090	V_{REF} + 0.090	V_{CCO} + 0.300	$V_{CCO}/2$ − 0.150	$V_{CCO}/2$ + 0.150	13.0	−13.0
SSTL135_R	−0.300	V_{REF} − 0.090	V_{REF} + 0.090	V_{CCO} + 0.300	$V_{CCO}/2$ − 0.150	$V_{CCO}/2$ + 0.150	8.9	−8.9
SSTL15	−0.300	V_{REF} − 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	$V_{CCO}/2$ − 0.175	$V_{CCO}/2$ + 0.175	13.0	−13.0
SSTL15_R	−0.300	V_{REF} − 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	$V_{CCO}/2$ − 0.175	$V_{CCO}/2$ + 0.175	8.9	−8.9
SSTL18_I	−0.300	V_{REF} − 0.125	V_{REF} + 0.125	V_{CCO} + 0.300	$V_{CCO}/2$ − 0.470	$V_{CCO}/2$ + 0.470	8.0	−8.0
SSTL18_II	−0.300	V_{REF} − 0.125	V_{REF} + 0.125	V_{CCO} + 0.300	$V_{CCO}/2$ − 0.600	$V_{CCO}/2$ + 0.600	13.4	−13.4

Notes:
1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).
3. Supported drive strengths of 4, 8, or 12 mA in HR I/O banks.
4. Supported drive strengths of 4, 8, 12, or 16 mA in HR I/O banks.

Table 16: **SelectIO DC Input and Output Levels for HP I/O Banks**[1][2][3]

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
HSTL_I	−0.300	$V_{REF} − 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	0.400	$V_{CCO} − 0.400$	5.8	−5.8
HSTL_I_12	−0.300	$V_{REF} − 0.080$	$V_{REF} + 0.080$	$V_{CCO} + 0.300$	25% V_{CCO}	75% V_{CCO}	4.1	−4.1
HSTL_I_18	−0.300	$V_{REF} − 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	0.400	$V_{CCO} − 0.400$	6.2	−6.2
HSUL_12	−0.300	$V_{REF} − 0.130$	$V_{REF} + 0.130$	$V_{CCO} + 0.300$	20% V_{CCO}	80% V_{CCO}	0.1	−0.1
LVCMOS12	−0.300	35% V_{CCO}	65% V_{CCO}	$V_{CCO} + 0.300$	0.400	$V_{CCO} − 0.400$	Note 4	Note 4
LVCMOS15	−0.300	35% V_{CCO}	65% V_{CCO}	$V_{CCO} + 0.300$	0.450	$V_{CCO} − 0.450$	Note 5	Note 5
LVCMOS18	−0.300	35% V_{CCO}	65% V_{CCO}	$V_{CCO} + 0.300$	0.450	$V_{CCO} − 0.450$	Note 5	Note 5
LVDCI_15	−0.300	35% V_{CCO}	65% V_{CCO}	$V_{CCO} + 0.300$	0.450	$V_{CCO} − 0.450$	7.0	−7.0
LVDCI_18	−0.300	35% V_{CCO}	65% V_{CCO}	$V_{CCO} + 0.300$	0.450	$V_{CCO} − 0.450$	7.0	−7.0
SSTL12	−0.300	$V_{REF} − 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	$V_{CCO}/2 − 0.150$	$V_{CCO}/2 + 0.150$	8.0	−8.0
SSTL135	−0.300	$V_{REF} − 0.090$	$V_{REF} + 0.090$	$V_{CCO} + 0.300$	$V_{CCO}/2 − 0.150$	$V_{CCO}/2 + 0.150$	9.0	−9.0
SSTL15	−0.300	$V_{REF} − 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	$V_{CCO}/2 − 0.175$	$V_{CCO}/2 + 0.175$	10.0	−10.0
SSTL18_I	−0.300	$V_{REF} − 0.125$	$V_{REF} + 0.125$	$V_{CCO} + 0.300$	$V_{CCO}/2 − 0.470$	$V_{CCO}/2 + 0.470$	7.0	−7.0

Notes:
1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).
3. POD10 and POD12 DC input and output levels are shown in Table 17, Table 22, and Table 23.
4. Supported drive strengths of 2, 4, 6, or 8 mA in HP I/O banks.
5. Supported drive strengths of 2, 4, 6, 8, or 12 mA in HP I/O banks.

Table 17: **DC Input Levels for Single-ended POD10 and POD12 I/O Standards**[1][2]

I/O Standard	V_{IL}		V_{IH}	
	V, Min	V, Max	V, Min	V, Max
POD10	−0.300	$V_{REF} − 0.068$	$V_{REF} + 0.068$	$V_{CCO} + 0.300$
POD12	−0.300	$V_{REF} − 0.068$	$V_{REF} + 0.068$	$V_{CCO} + 0.300$

Notes:
1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

Table 18: **Differential SelectIO DC Input and Output Levels**

I/O Standard	V_{ICM} (V)[1]			V_{ID} (V)[2]			V_{OCM} (V)[3]			V_{OD} (V)[4]		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
BLVDS_25	0.300	1.200	1.425	0.100	–	–	–	1.250	–	Note 5		
MINI_LVDS_25	0.300	1.200	V_{CCAUX}	0.200	0.400	0.600	1.000	1.200	1.485	0.300	0.450	0.600
SUB_LVDS	0.500	0.900	1.300	0.070	–	–	0.700	0.900	1.100	0.100	0.150	0.200
LVPECL	0.300	1.200	1.425	0.100	0.350	0.600	–	–	–	–	–	–
PPDS_25	0.200	0.900	V_{CCAUX}	0.100	0.250	0.400	0.500	0.950	1.400	0.100	0.250	0.400
RSDS_25	0.300	0.900	1.500	0.100	0.350	0.600	1.000	1.200	1.485	0.100	0.350	0.600
SLVS_400_18	0.070	0.200	0.330	0.140	–	0.450	–	–	–	–	–	–
SLVS_400_25	0.070	0.200	0.330	0.140	–	0.450	–	–	–	–	–	–
TMDS_33	2.700	2.965	3.230	0.150	0.675	1.200	$V_{CCO} - 0.405$	$V_{CCO} - 0.300$	$V_{CCO} - 0.190$	0.400	0.600	0.800

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage ($Q - \overline{Q}$).
3. V_{OCM} is the output common mode voltage.
4. V_{OD} is the output differential voltage ($Q - \overline{Q}$).
5. V_{OD} for BLVDS will vary significantly depending on topology and loading.
6. LVDS_25 is specified in Table 24.
7. LVDS is specified in Table 25.

Table 19: **Complementary Differential SelectIO DC Input and Output Levels for HR I/O Banks**

I/O Standard	V_{ICM} (V)[1]			V_{ID} (V)[2]		V_{OL} (V)[3]	V_{OH} (V)[4]	I_{OL}	I_{OH}
	Min	Typ	Max	Min	Max	Max	Min	mA	mA
DIFF_HSTL_I	0.300	0.750	1.125	0.100	–	0.400	$V_{CCO} - 0.400$	8.0	−8.0
DIFF_HSTL_I_18	0.300	0.900	1.425	0.100	–	0.400	$V_{CCO} - 0.400$	8.0	−8.0
DIFF_HSTL_II	0.300	0.750	1.125	0.100	–	0.400	$V_{CCO} - 0.400$	16.0	−16.0
DIFF_HSTL_II_18	0.300	0.900	1.425	0.100	–	0.400	$V_{CCO} - 0.400$	16.0	−16.0
DIFF_HSUL_12	0.300	0.600	0.850	0.100	–	20% V_{CCO}	80% V_{CCO}	0.1	−0.1
DIFF_SSTL12	0.300	0.600	0.850	0.100	–	(V_{CCO}/2) − 0.150	(V_{CCO}/2) + 0.150	14.25	−14.25
DIFF_SSTL135	0.300	0.675	1.000	0.100	–	(V_{CCO}/2) − 0.150	(V_{CCO}/2) + 0.150	13.0	−13.0
DIFF_SSTL135_R	0.300	0.675	1.000	0.100	–	(V_{CCO}/2) − 0.150	(V_{CCO}/2) + 0.150	8.9	−8.9
DIFF_SSTL15	0.300	0.750	1.125	0.100	–	(V_{CCO}/2) − 0.175	(V_{CCO}/2) + 0.175	13.0	−13.0
DIFF_SSTL15_R	0.300	0.750	1.125	0.100	–	(V_{CCO}/2) − 0.175	(V_{CCO}/2) + 0.175	8.9	−8.9
DIFF_SSTL18_I	0.300	0.900	1.425	0.100	–	(V_{CCO}/2) − 0.470	(V_{CCO}/2) + 0.470	8.0	−8.0
DIFF_SSTL18_II	0.300	0.900	1.425	0.100	–	(V_{CCO}/2) − 0.600	(V_{CCO}/2) + 0.600	13.4	−13.4

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage.
3. V_{OL} is the single-ended low-output voltage.
4. V_{OH} is the single-ended high-output voltage.

Table 20: **Complementary Differential SelectIO DC Input and Output Levels for HP I/O Banks**[1]

I/O Standard	V_{ICM} (V)[2]			V_{ID} (V)[3]		V_{OL} (V)[4]	V_{OH} (V)[5]	I_{OL}	I_{OH}
	Min	**Typ**	**Max**	**Min**	**Max**	**Max**	**Min**	**mA**	**mA**
DIFF_HSTL_I	0.680	$V_{CCO}/2$	$(V_{CCO}/2) + 0.150$	0.100	–	0.400	$V_{CCO} - 0.400$	5.8	−5.8
DIFF_HSTL_I_12	0.400 x V_{CCO}	$V_{CCO}/2$	0.600 x V_{CCO}	0.100	–	0.250 x V_{CCO}	0.750 x V_{CCO}	4.1	−4.1
DIFF_HSTL_I_18	$(V_{CCO}/2) - 0.175$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.175$	0.100	–	0.400	$V_{CCO} - 0.400$	6.2	−6.2
DIFF_HSUL_12	$(V_{CCO}/2) - 0.120$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.120$	0.100	–	20% V_{CCO}	80% V_{CCO}	0.1	−0.1
DIFF_SSTL12	$(V_{CCO}/2) - 0.150$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.150$	0.100	–	$(V_{CCO}/2) - 0.150$	$(V_{CCO}/2) + 0.150$	8.0	−8.0
DIFF_SSTL135	$(V_{CCO}/2) - 0.150$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.150$	0.100	–	$(V_{CCO}/2) - 0.150$	$(V_{CCO}/2) + 0.150$	9.0	−9.0
DIFF_SSTL15	$(V_{CCO}/2) - 0.175$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.175$	0.100	–	$(V_{CCO}/2) - 0.175$	$(V_{CCO}/2) + 0.175$	10.0	−10.0
DIFF_SSTL18_I	$(V_{CCO}/2) - 0.175$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.175$	0.100	–	$(V_{CCO}/2) - 0.470$	$(V_{CCO}/2) + 0.470$	7.0	−7.0

Notes:
1. DIFF_POD10 and DIFF_POD12 HP I/O bank specifications are shown in Table 21, Table 22, and Table 23.
2. V_{ICM} is the input common mode voltage.
3. V_{ID} is the input differential voltage.
4. V_{OL} is the single-ended low-output voltage.
5. V_{OH} is the single-ended high-output voltage.

Table 21: **DC Input Levels for Differential POD10 and POD12 I/O Standards**[1][2]

I/O Standard	V_{ICM} (V)			V_{ID} (V)	
	Min	**Typ**	**Max**	**Min**	**Max**
DIFF_POD10	0.63	0.70	0.77	0.14	–
DIFF_POD12	0.76	0.84	0.92	0.16	–

Notes:
1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

Table 22: **DC Output Levels for Single-ended and Differential POD10 and POD12 Standards**[1][2]

Symbol	Description	V_{OUT}	Min	Typ	Max	Units
R_{OL}	Pull-down resistance	V_{OM_DC} (as described in Table 23)	36	40	44	Ω
R_{OH}	Pull-up resistance	V_{OM_DC} (as described in Table 23)	36	40	44	Ω

Notes:
1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

Table 23: **Table 22 Definitions for DC Output Levels for POD Standards**

Symbol	Description	Value	Units
V_{OM_DC}	DC output Mid measurement level (for IV curve linearity)	0.8 x V_{CCO}	V

LVDS DC Specifications (LVDS_25)

The LVDS_25 standard is available in the HR I/O banks. See the *UltraScale Architecture SelectIO Resources User Guide* (UG571) for more information.

Table 24: **LVDS_25 DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply voltage		2.375	2.500	2.625	V
V_{ODIFF}[1]	Differential Output Voltage: $(Q - \overline{Q})$, Q = High $(\overline{Q} - Q)$, $\overline{Q}$ = High	R_T = 100Ω across Q and $\overline{Q}$ signals	247	350	600	mV
V_{OCM}[1]	Output Common-Mode Voltage	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.000	1.250	1.485	V
V_{IDIFF}	Differential Input Voltage: $(Q - \overline{Q})$, Q = High $(\overline{Q} - Q)$, $\overline{Q}$ = High		100	350	600[2]	mV
V_{ICM_DC}[3]	Input Common-Mode Voltage (DC Coupling)		0.300	1.200	1.500	V
V_{ICM_AC}[4]	Input Common-Mode Voltage (AC Coupling)		0.600	–	1.100	V

Notes:

1. V_{OCM} and V_{ODIFF} values are for LVDS_PRE_EMPHASIS = FALSE.
2. Maximum V_{IDIFF} value is specified for the maximum V_{ICM} specification. With a lower V_{ICM}, a higher V_{DIFF} is tolerated only when the recommended operating conditions and overshoot/undershoot V_{IN} specifications are maintained.
3. Input common mode voltage for DC coupled configurations. EQUALIZATION = EQ_NONE (Default).
4. External input common mode voltage specification for AC coupled configurations. EQUALIZATION = EQ_LEVEL0, EQ_LEVEL1, EQ_LEVEL2, EQ_LEVEL3, EQ_LEVEL4.

LVDS DC Specifications (LVDS)

The LVDS standard is available in the HP I/O banks. See the *UltraScale Architecture SelectIO Resources User Guide* (UG571) for more information.

Table 25: **LVDS DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply voltage		1.710	1.800	1.890	V
V_{ODIFF}[1]	Differential Output Voltage $(Q - \overline{Q})$, Q = High $(\overline{Q} - Q)$, $\overline{Q}$ = High	R_T = 100Ω across Q and $\overline{Q}$ signals	247	350	600	mV
V_{OCM}[1]	Output Common-Mode Voltage	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.000	1.250	1.425	V
V_{IDIFF}	Differential Input Voltage $(Q - \overline{Q})$, Q = High $(\overline{Q} - Q)$, $\overline{Q}$ = High		100	350	600[2]	mV
V_{ICM_DC}[3]	Input Common-Mode Voltage (DC Coupling)		0.300	1.200	1.425	V
V_{ICM_AC}[4]	Input Common-Mode Voltage (AC Coupling)		0.600	–	1.100	V

Notes:

1. V_{OCM} and V_{ODIFF} values are for LVDS_PRE_EMPHASIS = FALSE.
2. Maximum V_{IDIFF} value is specified for the maximum V_{ICM} specification. With a lower V_{ICM}, a higher V_{DIFF} is tolerated only when the recommended operating conditions and overshoot/undershoot V_{IN} specifications are maintained.
3. Input common mode voltage for DC coupled configurations. EQUALIZATION = EQ_NONE (Default).
4. External input common mode voltage specification for AC coupled configurations. EQUALIZATION = EQ_LEVEL0, EQ_LEVEL1, EQ_LEVEL2, EQ_LEVEL3, EQ_LEVEL4.

AC Switching Characteristics

All values represented in this data sheet are based on the speed specifications in the Vivado® Design Suite as outlined in Table 26.

Table 26: **Speed Specification Version**

Vivado 2020.1.1	Device
1.29	XQRKU060

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance Product Specification

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting or over-reporting might still occur.

Preliminary Product Specification

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Product Specification

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes.

Testing of AC Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. All AC switching characteristics are representative of worst-case supply voltage and junction temperature conditions. For more specific, precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list.

AC switching characteristics do not cover all effects of simultaneous configuration memory access activity. See Additional Design Considerations for Configuration Memory Access Effects for guidance and mitigation of configuration readback induced time interval error in MMCMs and PLLs.

Speed Grade Designations

Table 27 correlates the current status of the Kintex UltraScale XQRKU060 FPGA.

Table 27: **Speed Grade Designations by Device**

Device	Speed Grade		
	Advance	**Preliminary**	**Production**
XQRKU060			-1M

Production Silicon and Software Status

The Vivado software and speed specifications listed in Table 28 are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 28: **XQRKU060 Minimum Production Software and Speed Specification Release**

Device	Speed Grade and Temperature Range
	-1M
XQRKU060	Vivado tools 2020.1.1 v1.29

Notes:

1. For the XQRKU060 device and -1M speed grade and temperature range, select the `xqrku060-cna1509-1M-m` part in the Vivado design tools.

Send Feedback

Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in the XQRKU060 FPGA. These values are subject to the same guidelines as the AC Switching Characteristics, page 28. In each table, the I/O bank type is either high performance (HP) or high range (HR). In LVDS component mode:

- For the input/output registers, the Vivado tools limit clock frequencies to 316.4 MHz.

- For IDDR, the Vivado tools limit clock frequencies to 632.9 MHz.

- For ODDR, the Vivado tools limit clock frequencies to 730.4 MHz.

Table 29: **LVDS Component Mode Performance**

Description	I/O Bank Type	Min	Max	Units
LVDS TX DDR (OSERDES 4:1, 8:1)	HP	0	1250	Mb/s
	HR	0	1000	Mb/s
LVDS TX SDR (OSERDES 2:1, 4:1)	HP	0	625	Mb/s
	HR	0	500	Mb/s
LVDS RX DDR (ISERDES 1:4, 1:8)[1]	HP	0	1250	Mb/s
	HR	0	1000	Mb/s
LVDS RX SDR (ISERDES 1:2, 1:4)[1]	HP	0	625	Mb/s
	HR	0	500	Mb/s

Notes:
1. LVDS receivers are typically bounded with certain applications where specific dynamic phase-alignment (DPA) or phase-tracking algorithms are used to achieve maximum performance.
2. See Additional Design Considerations for Configuration Memory Access Effects for guidance and mitigation of configuration readback induced time interval error in MMCMs and PLLs.

Table 30: **LVDS Native Mode Performance[1]**

Description	I/O Bank Type	Min	Max	Units
LVDS TX DDR (TX_BITSLICE 4:1, 8:1)	HP	300	1400	Mb/s
	HR	300	1250	Mb/s
LVDS TX SDR (TX_BITSLICE 2:1, 4:1)	HP	150	700	Mb/s
	HR	150	625	Mb/s
LVDS RX DDR (RX_BITSLICE 1:4, 1:8)[2]	HP	300	1400[3]	Mb/s
	HR	300	1250	Mb/s
LVDS RX SDR (RX_BITSLICE 1:2, 1:4)[2]	HP	150	700	Mb/s
	HR	150	625	Mb/s

Notes:
1. Native mode is supported through the High-Speed SelectIO Interface Wizard available with the Vivado Design Suite.
2. LVDS receivers are typically bounded with certain applications where specific dynamic phase-alignment (DPA) or phase-tracking algorithms are used to achieve maximum performance.
3. Asynchronous receiver performance is limited to 1250 Mb/s for -1 speed grade.
4. See Additional Design Considerations for Configuration Memory Access Effects for guidance and mitigation of configuration readback induced time interval error in MMCMs and PLLs.

Table 31: **LVDS Native-Mode 1000BASE-X Support[1]**

Description	I/O Bank Type	Support
1000BASE-X	HP	Yes

Notes:

1. 1000BASE-X support is based on the *IEEE Standard for CSMA/CD Access Method and Physical Layer Specifications* (IEEE Std 802.3-2008).

Table 32 provides the maximum data rates for applicable memory standards using the Kintex UltraScale FPGAs memory PHY. The final performance of the memory interface is determined through a complete design implemented in the Vivado Design Suite, following guidelines in the *UltraScale Architecture PCB Design User Guide* (UG583), electrical analysis, and characterization of the system.

Table 32: **Maximum Physical Interface (PHY) Rate for Memory Interfaces by I/O and Package**

Memory Standard	I/O Bank Type	DRAM Type	Value	Units
DDR4	HP	Single rank component	1866	Mb/s
		1 rank DIMM[1][2]	1866	
		2 rank DIMM[1][3]	1600	
		4 rank DIMM[1][4]	N/A	
DDR3	HP	Single rank component	1866	Mb/s
		1 rank DIMM[1][2]	1600	
		2 rank DIMM[1][3]	1333	
		4 rank DIMM[1][4]	800	
	HR	Single rank component	1066	
DDR3L	HP	Single rank component	1600	Mb/s
		1 rank DIMM[1][2]	1333	
		2 rank DIMM[1][3]	1066	
		4 rank DIMM[1][4]	606	
	HR	Single rank component	800	
QDR II+[5]	All	Single rank component	550	MHz
RLDRAM III	HP	Single rank component	933	
LPDDR3	HP	Single rank component	1600	Mb/s
	HR	Single rank component	1066	

Notes:

1. Dual in-line memory module (DIMM) includes RDIMM, SODIMM, UDIMM, and LRDIMM.
2. Includes: 1 rank 1 slot, DDP 2 rank, LRDIMM 2 or 4 rank 1 slot.
3. Includes: 2 rank 1 slot, 1 rank 2 slot, LRDIMM 2 rank 2 slot.
4. Includes: 2 rank 2 slot, 4 rank 1 slot.
5. The QDRII+ performance specifications are for burst-length 4 (BL = 4) implementations.
6. QDRIV memories are not supported.

IOB Pad Input, Output, and 3-State

Table 33 (high-range IOB (HR)) and Table 34 (high-performance IOB (HP)) summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

- $T_{INBUF\_DELAY\_PAD\_I}$ is the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.

- $T_{OUTBUF\_DELAY\_O\_PAD}$ is the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.

- $T_{OUTBUF\_DELAY\_TD\_PAD}$ is the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer. In HP I/O banks, the internal DCI termination turn-on time is always faster than $T_{OUTBUF\_DELAY\_TD\_PAD}$ when the DCITERMDISABLE pin is used. In HR I/O banks, the on-die termination turn-on time is always faster than $T_{OUTBUF\_DELAY\_TD\_PAD}$ when the INTERMDISABLE pin is used.

Table 33: **IOB High Range (HR) Switching Characteristics**

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$	$T_{OUTBUF\_DELAY\_O\_PAD}$	$T_{OUTBUF\_DELAY\_TD\_PAD}$	Units
BLVDS_25	0.64	1.62	1.66	ns
DIFF_HSTL_I_18_F	0.57	0.91	1.06	ns
DIFF_HSTL_I_18_S	0.57	1.03	1.16	ns
DIFF_HSTL_I_F	0.57	0.93	1.14	ns
DIFF_HSTL_I_S	0.57	0.96	1.23	ns
DIFF_HSTL_II_18_F	0.57	1.00	1.23	ns
DIFF_HSTL_II_18_S	0.57	1.03	1.28	ns
DIFF_HSTL_II_F	0.57	0.91	1.11	ns
DIFF_HSTL_II_S	0.57	0.99	1.20	ns
DIFF_HSUL_12_F	0.57	0.92	0.92	ns
DIFF_HSUL_12_S	0.57	1.02	1.02	ns
DIFF_SSTL12_F	0.57	0.89	1.02	ns
DIFF_SSTL12_S	0.57	1.26	1.26	ns
DIFF_SSTL135_F	0.57	0.88	1.09	ns
DIFF_SSTL135_S	0.57	0.96	1.18	ns
DIFF_SSTL135_R_F	0.57	0.91	1.06	ns
DIFF_SSTL135_R_S	0.57	1.00	1.17	ns
DIFF_SSTL15_F	0.57	0.85	1.05	ns
DIFF_SSTL15_S	0.57	0.98	1.21	ns
DIFF_SSTL15_R_F	0.57	0.92	1.09	ns
DIFF_SSTL15_R_S	0.57	1.02	1.18	ns
DIFF_SSTL18_I_F	0.57	0.94	1.19	ns
DIFF_SSTL18_I_S	0.57	1.06	1.06	ns
DIFF_SSTL18_II_F	0.57	0.90	1.12	ns
DIFF_SSTL18_II_S	0.57	1.03	1.30	ns
HSTL_I_18_F	0.59	0.93	1.08	ns

Table 33: **IOB High Range (HR) Switching Characteristics** *(Cont'd)*

I/O Standards	T$_{INBUF\_DELAY\_PAD\_I}$	T$_{OUTBUF\_DELAY\_O\_PAD}$	T$_{OUTBUF\_DELAY\_TD\_PAD}$	Units
HSTL_I_18_S	0.59	1.05	1.18	ns
HSTL_I_F	0.59	0.95	1.17	ns
HSTL_I_S	0.59	0.99	1.25	ns
HSTL_II_18_F	0.59	1.02	1.25	ns
HSTL_II_18_S	0.59	1.05	1.30	ns
HSTL_II_F	0.59	0.93	1.13	ns
HSTL_II_S	0.59	1.02	1.22	ns
HSUL_12_F	0.59	0.95	0.95	ns
HSUL_12_S	0.59	1.04	1.15	ns
LVCMOS12_F_12	0.95	1.16	1.16	ns
LVCMOS12_F_4	0.95	1.39	1.39	ns
LVCMOS12_F_8	0.95	1.19	1.19	ns
LVCMOS12_S_12	0.95	1.28	1.28	ns
LVCMOS12_S_4	0.95	1.60	1.60	ns
LVCMOS12_S_8	0.95	1.32	1.32	ns
LVCMOS15_F_12	0.88	1.18	1.18	ns
LVCMOS15_F_16	0.88	1.15	1.17	ns
LVCMOS15_F_4	0.88	1.39	1.39	ns
LVCMOS15_F_8	0.88	1.24	1.24	ns
LVCMOS15_S_12	0.88	1.30	1.30	ns
LVCMOS15_S_16	0.88	1.27	1.27	ns
LVCMOS15_S_4	0.88	1.54	1.54	ns
LVCMOS15_S_8	0.88	1.34	1.34	ns
LVCMOS18_F_12	0.80	1.26	1.26	ns
LVCMOS18_F_16	0.80	1.22	1.22	ns
LVCMOS18_F_4	0.80	1.41	1.41	ns
LVCMOS18_F_8	0.80	1.33	1.33	ns
LVCMOS18_S_12	0.80	1.35	1.35	ns
LVCMOS18_S_16	0.80	1.34	1.34	ns
LVCMOS18_S_4	0.80	1.58	1.58	ns
LVCMOS18_S_8	0.80	1.38	1.38	ns
LVCMOS25_F_12	0.91	1.81	1.81	ns
LVCMOS25_F_16	0.91	1.88	1.88	ns
LVCMOS25_F_4	0.91	2.56	2.56	ns
LVCMOS25_F_8	0.91	1.95	1.95	ns
LVCMOS25_S_12	0.91	2.47	2.47	ns
LVCMOS25_S_16	0.91	2.19	2.19	ns
LVCMOS25_S_4	0.91	3.68	3.68	ns
LVCMOS25_S_8	0.91	2.47	2.47	ns
LVCMOS33_F_12	1.03	2.24	2.24	ns

Table 33: **IOB High Range (HR) Switching Characteristics** *(Cont'd)*

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$	$T_{OUTBUF\_DELAY\_O\_PAD}$	$T_{OUTBUF\_DELAY\_TD\_PAD}$	Units
LVCMOS33_F_16	1.03	2.09	2.09	ns
LVCMOS33_F_4	1.03	2.63	2.63	ns
LVCMOS33_F_8	1.03	2.33	2.33	ns
LVCMOS33_S_12	1.03	2.48	2.48	ns
LVCMOS33_S_16	1.03	2.43	2.43	ns
LVCMOS33_S_4	1.03	3.67	3.67	ns
LVCMOS33_S_8	1.03	2.55	2.78	ns
LVDS_25	0.63	0.95	105.85	ns
LVPECL	0.63	N/A	N/A	ns
LVTTL_F_12	1.06	2.10	2.10	ns
LVTTL_F_16	1.06	2.06	2.06	ns
LVTTL_F_4	1.06	2.63	2.63	ns
LVTTL_F_8	1.06	2.23	2.23	ns
LVTTL_S_12	1.06	2.19	2.19	ns
LVTTL_S_16	1.06	2.40	2.40	ns
LVTTL_S_4	1.06	3.67	3.67	ns
LVTTL_S_8	1.06	2.47	2.51	ns
MINI_LVDS_25	0.63	0.95	105.85	ns
PPDS_25	0.63	0.95	105.85	ns
RSDS_25	0.63	0.95	105.85	ns
SLVS_400_25	0.63	N/A	N/A	ns
SSTL12_F	0.59	0.91	1.04	ns
SSTL12_S	0.59	0.98	1.11	ns
SSTL135_F	0.59	0.91	1.11	ns
SSTL135_S	0.59	0.97	1.18	ns
SSTL135_R_F	0.59	0.93	1.08	ns
SSTL135_R_S	0.59	1.03	1.19	ns
SSTL15_F	0.59	0.87	1.07	ns
SSTL15_S	0.59	1.01	1.23	ns
SSTL15_R_F	0.59	0.94	1.11	ns
SSTL15_R_S	0.59	1.04	1.21	ns
SSTL18_I_F	0.59	0.96	1.21	ns
SSTL18_I_S	0.59	1.08	1.08	ns
SSTL18_II_F	0.59	0.92	1.14	ns
SSTL18_II_S	0.59	1.05	1.32	ns
SUB_LVDS	0.63	0.95	105.85	ns
TMDS_33	0.74	0.95	105.85	ns

Table 34: **IOB High Performance (HP) Switching Characteristics**

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$	$T_{OUTBUF\_DELAY\_O\_PAD}$	$T_{OUTBUF\_DELAY\_TD\_PAD}$	Units
DIFF_HSTL_I_12_F	0.55	0.54	0.68	ns
DIFF_HSTL_I_12_M	0.55	0.60	0.76	ns
DIFF_HSTL_I_12_S	0.55	0.67	0.85	ns
DIFF_HSTL_I_18_F	0.55	0.53	0.68	ns
DIFF_HSTL_I_18_M	0.55	0.59	0.76	ns
DIFF_HSTL_I_18_S	0.55	0.67	0.86	ns
DIFF_HSTL_I_DCI_12_F	0.55	0.54	0.68	ns
DIFF_HSTL_I_DCI_12_M	0.55	0.60	0.76	ns
DIFF_HSTL_I_DCI_12_S	0.55	0.67	0.85	ns
DIFF_HSTL_I_DCI_18_F	0.55	0.53	0.68	ns
DIFF_HSTL_I_DCI_18_M	0.55	0.59	0.76	ns
DIFF_HSTL_I_DCI_18_S	0.55	0.67	0.86	ns
DIFF_HSTL_I_DCI_F	0.55	0.54	0.68	ns
DIFF_HSTL_I_DCI_M	0.55	0.60	0.76	ns
DIFF_HSTL_I_DCI_S	0.55	0.67	0.85	ns
DIFF_HSTL_I_F	0.55	0.54	0.68	ns
DIFF_HSTL_I_M	0.55	0.60	0.76	ns
DIFF_HSTL_I_S	0.55	0.67	0.85	ns
DIFF_HSUL_12_DCI_F	0.55	0.54	0.68	ns
DIFF_HSUL_12_DCI_M	0.55	0.60	0.76	ns
DIFF_HSUL_12_DCI_S	0.55	0.67	0.85	ns
DIFF_HSUL_12_F	0.55	0.54	0.68	ns
DIFF_HSUL_12_M	0.55	0.60	0.76	ns
DIFF_HSUL_12_S	0.55	0.67	0.85	ns
DIFF_POD10_DCI_F	0.55	0.55	0.73	ns
DIFF_POD10_DCI_M	0.55	0.63	0.79	ns
DIFF_POD10_DCI_S	0.55	0.74	0.88	ns
DIFF_POD10_F	0.55	0.55	0.73	ns
DIFF_POD10_M	0.55	0.63	0.79	ns
DIFF_POD10_S	0.55	0.74	0.88	ns
DIFF_POD12_DCI_F	0.55	0.55	0.73	ns
DIFF_POD12_DCI_M	0.55	0.63	0.79	ns
DIFF_POD12_DCI_S	0.55	0.74	0.88	ns
DIFF_POD12_F	0.55	0.55	0.73	ns
DIFF_POD12_M	0.55	0.63	0.79	ns
DIFF_POD12_S	0.55	0.74	0.88	ns
DIFF_SSTL12_DCI_F	0.55	0.54	0.68	ns
DIFF_SSTL12_DCI_M	0.55	0.60	0.76	ns
DIFF_SSTL12_DCI_S	0.55	0.67	0.85	ns
DIFF_SSTL12_F	0.55	0.54	0.68	ns

Table 34: **IOB High Performance (HP) Switching Characteristics** *(Cont'd)*

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$	$T_{OUTBUF\_DELAY\_O\_PAD}$	$T_{OUTBUF\_DELAY\_TD\_PAD}$	Units
DIFF_SSTL12_M	0.55	0.60	0.76	ns
DIFF_SSTL12_S	0.55	0.67	0.85	ns
DIFF_SSTL135_DCI_F	0.55	0.54	0.69	ns
DIFF_SSTL135_DCI_M	0.55	0.60	0.76	ns
DIFF_SSTL135_DCI_S	0.55	0.67	0.85	ns
DIFF_SSTL135_F	0.55	0.54	0.69	ns
DIFF_SSTL135_M	0.55	0.60	0.76	ns
DIFF_SSTL135_S	0.55	0.67	0.85	ns
DIFF_SSTL15_DCI_F	0.55	0.54	0.68	ns
DIFF_SSTL15_DCI_M	0.55	0.60	0.76	ns
DIFF_SSTL15_DCI_S	0.55	0.67	0.85	ns
DIFF_SSTL15_F	0.55	0.54	0.68	ns
DIFF_SSTL15_M	0.55	0.60	0.76	ns
DIFF_SSTL15_S	0.55	0.67	0.85	ns
DIFF_SSTL18_I_DCI_F	0.55	0.53	0.68	ns
DIFF_SSTL18_I_DCI_M	0.55	0.59	0.76	ns
DIFF_SSTL18_I_DCI_S	0.55	0.67	0.86	ns
DIFF_SSTL18_I_F	0.55	0.53	0.68	ns
DIFF_SSTL18_I_M	0.55	0.59	0.76	ns
DIFF_SSTL18_I_S	0.55	0.67	0.86	ns
HSLVDCI_15_F	0.52	0.56	0.71	ns
HSLVDCI_15_M	0.52	0.62	0.79	ns
HSLVDCI_15_S	0.52	0.69	0.88	ns
HSLVDCI_18_F	0.52	0.57	0.71	ns
HSLVDCI_18_M	0.52	0.62	0.79	ns
HSLVDCI_18_S	0.52	0.69	0.90	ns
HSTL_I_12_F	0.52	0.56	0.70	ns
HSTL_I_12_M	0.52	0.61	0.78	ns
HSTL_I_12_S	0.52	0.68	0.87	ns
HSTL_I_18_F	0.52	0.55	0.70	ns
HSTL_I_18_M	0.52	0.61	0.78	ns
HSTL_I_18_S	0.52	0.69	0.88	ns
HSTL_I_DCI_12_F	0.52	0.56	0.70	ns
HSTL_I_DCI_12_M	0.52	0.61	0.78	ns
HSTL_I_DCI_12_S	0.52	0.68	0.87	ns
HSTL_I_DCI_18_F	0.52	0.55	0.70	ns
HSTL_I_DCI_18_M	0.52	0.61	0.78	ns
HSTL_I_DCI_18_S	0.52	0.69	0.88	ns
HSTL_I_DCI_F	0.52	0.56	0.70	ns
HSTL_I_DCI_M	0.52	0.61	0.78	ns

Send Feedback

Table 34: **IOB High Performance (HP) Switching Characteristics** *(Cont'd)*

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$	$T_{OUTBUF\_DELAY\_O\_PAD}$	$T_{OUTBUF\_DELAY\_TD\_PAD}$	Units
HSTL_I_DCI_S	0.52	0.68	0.87	ns
HSTL_I_F	0.52	0.56	0.70	ns
HSTL_I_M	0.52	0.61	0.78	ns
HSTL_I_S	0.52	0.68	0.87	ns
HSUL_12_DCI_F	0.52	0.56	0.70	ns
HSUL_12_DCI_M	0.52	0.61	0.78	ns
HSUL_12_DCI_S	0.52	0.68	0.87	ns
HSUL_12_F	0.52	0.56	0.70	ns
HSUL_12_M	0.52	0.61	0.78	ns
HSUL_12_S	0.52	0.68	0.87	ns
LVCMOS12_F_2	0.74	0.79	0.79	ns
LVCMOS12_F_4	0.74	0.73	0.73	ns
LVCMOS12_F_6	0.74	0.69	0.72	ns
LVCMOS12_F_8	0.74	0.67	0.72	ns
LVCMOS12_M_2	0.74	0.85	0.85	ns
LVCMOS12_M_4	0.74	0.77	0.77	ns
LVCMOS12_M_6	0.74	0.72	0.75	ns
LVCMOS12_M_8	0.74	0.72	0.78	ns
LVCMOS12_S_2	0.74	0.96	0.96	ns
LVCMOS12_S_4	0.74	0.79	0.79	ns
LVCMOS12_S_6	0.74	0.78	0.79	ns
LVCMOS12_S_8	0.74	0.77	0.82	ns
LVCMOS15_F_12	0.58	0.71	0.81	ns
LVCMOS15_F_2	0.58	0.83	0.83	ns
LVCMOS15_F_4	0.58	0.78	0.78	ns
LVCMOS15_F_6	0.58	0.73	0.77	ns
LVCMOS15_F_8	0.58	0.72	0.78	ns
LVCMOS15_M_12	0.58	0.75	0.85	ns
LVCMOS15_M_2	0.58	0.86	0.86	ns
LVCMOS15_M_4	0.58	0.82	0.82	ns
LVCMOS15_M_6	0.58	0.78	0.82	ns
LVCMOS15_M_8	0.58	0.76	0.83	ns
LVCMOS15_S_12	0.58	0.75	0.83	ns
LVCMOS15_S_2	0.58	0.91	0.91	ns
LVCMOS15_S_4	0.58	0.84	0.84	ns
LVCMOS15_S_6	0.58	0.82	0.84	ns
LVCMOS15_S_8	0.58	0.79	0.83	ns
LVCMOS18_F_12	0.54	0.78	0.90	ns
LVCMOS18_F_2	0.54	1.15	1.15	ns
LVCMOS18_F_4	0.54	0.89	0.89	ns

Table 34: **IOB High Performance (HP) Switching Characteristics** *(Cont'd)*

I/O Standards	T$_{INBUF\_DELAY\_PAD\_I}$	T$_{OUTBUF\_DELAY\_O\_PAD}$	T$_{OUTBUF\_DELAY\_TD\_PAD}$	Units
LVCMOS18_F_6	0.54	0.83	0.88	ns
LVCMOS18_F_8	0.54	0.81	0.89	ns
LVCMOS18_M_12	0.54	0.81	0.92	ns
LVCMOS18_M_2	0.54	1.19	1.19	ns
LVCMOS18_M_4	0.54	0.92	0.92	ns
LVCMOS18_M_6	0.54	0.87	0.90	ns
LVCMOS18_M_8	0.54	0.85	0.92	ns
LVCMOS18_S_12	0.54	0.84	0.92	ns
LVCMOS18_S_2	0.54	1.25	1.25	ns
LVCMOS18_S_4	0.54	0.93	0.93	ns
LVCMOS18_S_6	0.54	0.89	0.90	ns
LVCMOS18_S_8	0.54	0.86	0.90	ns
LVDCI_15_F	0.58	0.56	0.71	ns
LVDCI_15_M	0.58	0.62	0.79	ns
LVDCI_15_S	0.58	0.69	0.88	ns
LVDCI_18_F	0.54	0.57	0.71	ns
LVDCI_18_M	0.54	0.62	0.79	ns
LVDCI_18_S	0.54	0.69	0.90	ns
LVDS	0.51	0.72	890.28	ns
POD10_DCI_F	0.52	0.56	0.74	ns
POD10_DCI_M	0.52	0.65	0.81	ns
POD10_DCI_S	0.52	0.76	0.89	ns
POD10_F	0.52	0.56	0.74	ns
POD10_M	0.52	0.65	0.81	ns
POD10_S	0.52	0.76	0.89	ns
POD12_DCI_F	0.52	0.56	0.74	ns
POD12_DCI_M	0.52	0.65	0.81	ns
POD12_DCI_S	0.52	0.76	0.89	ns
POD12_F	0.52	0.56	0.74	ns
POD12_M	0.52	0.65	0.81	ns
POD12_S	0.52	0.76	0.89	ns
SLVS_400_18	0.51	N/A	N/A	ns
SSTL12_DCI_F	0.52	0.56	0.70	ns
SSTL12_DCI_M	0.52	0.61	0.78	ns
SSTL12_DCI_S	0.52	0.68	0.87	ns
SSTL12_F	0.52	0.56	0.70	ns
SSTL12_M	0.52	0.61	0.78	ns
SSTL12_S	0.52	0.68	0.87	ns
SSTL135_DCI_F	0.52	0.56	0.70	ns
SSTL135_DCI_M	0.52	0.61	0.78	ns

Table 34: **IOB High Performance (HP) Switching Characteristics** *(Cont'd)*

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$	$T_{OUTBUF\_DELAY\_O\_PAD}$	$T_{OUTBUF\_DELAY\_TD\_PAD}$	Units
SSTL135_DCI_S	0.52	0.68	0.87	ns
SSTL135_F	0.52	0.56	0.70	ns
SSTL135_M	0.52	0.61	0.78	ns
SSTL135_S	0.52	0.68	0.87	ns
SSTL15_DCI_F	0.52	0.56	0.70	ns
SSTL15_DCI_M	0.52	0.61	0.78	ns
SSTL15_DCI_S	0.52	0.68	0.87	ns
SSTL15_F	0.52	0.56	0.70	ns
SSTL15_M	0.52	0.61	0.78	ns
SSTL15_S	0.52	0.68	0.87	ns
SSTL18_I_DCI_F	0.52	0.55	0.70	ns
SSTL18_I_DCI_M	0.52	0.61	0.78	ns
SSTL18_I_DCI_S	0.52	0.69	0.88	ns
SSTL18_I_F	0.52	0.55	0.70	ns
SSTL18_I_M	0.52	0.61	0.78	ns
SSTL18_I_S	0.52	0.69	0.88	ns
SUB_LVDS	0.51	0.72	890.28	ns

Table 35 specifies the values of $T_{OUTBUF\_DELAY\_TE\_PAD}$ and $T_{INBUF\_DELAY\_IBUFDIS\_O}$. $T_{OUTBUF\_DELAY\_TE\_PAD}$ is the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state). $T_{INBUF\_DELAY\_IBUFDIS\_O}$ is the IOB delay from IBUFDISABLE to O output. In HP I/O banks, the internal DCI termination turn-off time is always faster than $T_{OUTBUF\_DELAY\_TE\_PAD}$ when the DCITERMDISABLE pin is used. In HR I/O banks, the internal IN_TERM termination turn-off time is always faster than $T_{OUTBUF\_DELAY\_TE\_PAD}$ when the INTERMDISABLE pin is used.

Table 35: **IOB 3-state Output Switching Characteristics**

Symbol	Description	Value	Units
$T_{OUTBUF\_DELAY\_TE\_PAD}$[1]	T input to pad high-impedance for HR I/O banks	1.69	ns
	T input to pad high-impedance for HP I/O banks	0.78	ns
$T_{INBUF\_DELAY\_IBUFDIS\_O}$	IBUF turn-on time from IBUFDISABLE to O output for HR I/O banks	0.68	ns
	IBUF turn-on time from IBUFDISABLE to O output for HP I/O banks	1.49	ns

Notes:

1. The $T_{OUTBUF\_DELAY\_TE\_PAD}$ values are applicable to single-ended I/O standards. For true differential standards, the values are larger. Use the Vivado timing report for the most accurate timing values for your configuration.

I/O Standard Adjustment Measurement Methodology

Input Delay Measurements

Table 36 shows the test setup parameters used for measuring input delay.

Table 36: **Input Delay Measurement Methodology**

Description	I/O Standard Attribute	V_L [1][2]	V_H [1][2]	V_{MEAS} [1][4][6]	V_{REF} [1][3][5]
LVCMOS, 1.2V	LVCMOS12	0.1	1.1	0.6	–
LVCMOS, LVDCI, HSLVDCI, 1.5V	LVCMOS15, LVDCI_15, HSLVDCI_15	0.1	1.4	0.75	–
LVCMOS, LVDCI, HSLVDCI, 1.8V	LVCMOS18, LVDCI_18, HSLVDCI_18	0.1	1.7	0.9	–
LVCMOS, 2.5V	LVCMOS25	0.1	2.4	1.25	–
LVCMOS, 3.3V	LVCMOS33	0.1	3.2	1.65	–
LVTTL, 3.3V	LVTTL	0.1	3.2	1.65	–
HSTL (high-speed transceiver logic), Class I, 1.2V	HSTL_I_12	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.60
HSTL, Class I and II, 1.5V	HSTL_I, HSTL_II	$V_{REF} - 0.65$	$V_{REF} + 0.65$	V_{REF}	0.75
HSTL, Class I and II, 1.8V	HSTL_I_18, HSTL_II_18	$V_{REF} - 0.8$	$V_{REF} + 0.8$	V_{REF}	0.90
HSUL (high-speed unterminated logic), 1.2V	HSUL_12	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.60
SSTL (stub series terminated logic), 1.2V	SSTL12	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.60
SSTL, 1.35V	SSTL135, SSTL135_R	$V_{REF} - 0.575$	$V_{REF} + 0.575$	V_{REF}	0.675
SSTL, 1.5V	SSTL15, SSTL15_R	$V_{REF} - 0.65$	$V_{REF} + 0.65$	V_{REF}	0.75
SSTL, Class I and II, 1.8V	SSTL18_I, SSTL18_II	$V_{REF} - 0.8$	$V_{REF} + 0.8$	V_{REF}	0.90
POD10, 1.0V	POD10	$V_{REF} - 0.6$	$V_{REF} + 0.6$	V_{REF}	0.70
POD12, 1.2V	POD12	$V_{REF} - 0.74$	$V_{REF} + 0.74$	V_{REF}	0.84
DIFF_HSTL, Class I, 1.2V	DIFF_HSTL_I_12	$0.6 - 0.125$	$0.6 + 0.125$	0 [6]	–
DIFF_HSTL, Class I and II,1.5V	DIFF_HSTL_I, DIFF_HSTL_II	$0.75 - 0.125$	$0.75 + 0.125$	0 [6]	–
DIFF_HSTL, Class I and II, 1.8V	DIFF_HSTL_I_18, DIFF_HSTL_II_18	$0.9 - 0.125$	$0.9 + 0.125$	0 [6]	–
DIFF_HSUL, 1.2V	DIFF_HSUL_12	$0.6 - 0.125$	$0.6 + 0.125$	0 [6]	–
DIFF_SSTL, 1.2V	DIFF_SSTL12	$0.6 - 0.125$	$0.6 + 0.125$	0 [6]	–
DIFF_SSTL135/DIFF_SSTL135_R, 1.35V	DIFF_SSTL135, DIFF_SSTL135_R	$0.675 - 0.125$	$0.675 + 0.125$	0 [6]	–
DIFF_SSTL15/DIFF_SSTL15_R, 1.5V	DIFF_SSTL15, DIFF_SSTL15_R	$0.75 - 0.125$	$0.75 + 0.125$	0 [6]	–
DIFF_SSTL18_I/DIFF_SSTL18_II, 1.8V	DIFF_SSTL18_I, DIFF_SSTL18_II	$0.9 - 0.125$	$0.9 + 0.125$	0 [6]	–
DIFF_POD10, 1.0V	DIFF_POD10	$0.70 - 0.125$	$0.70 + 0.125$	0 [6]	–
DIFF_POD12, 1.2V	DIFF_POD12	$0.84 - 0.125$	$0.84 + 0.125$	0 [6]	–

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Table 36: **Input Delay Measurement Methodology** *(Cont'd)*

Description	I/O Standard Attribute	V_L[1][2]	V_H[1][2]	V_{MEAS} [1][4][6]	V_{REF} [1][3][5]
LVDS (low-voltage differential signaling), 1.8V	LVDS	0.9 − 0.125	0.9 + 0.125	0[6]	–
LVDS_25, 2.5V	LVDS_25	1.25 − 0.125	1.25 + 0.125	0[6]	–
SUB_LVDS, 1.8V	SUB_LVDS	0.9 − 0.125	0.9 + 0.125	0[6]	–
SLVS, 1.8V	SLVS_400_18	0.9 − 0.125	0.9 + 0.125	0[6]	–
SLVS, 2.5V	SLVS_400_25	1.25 − 0.125	1.25 + 0.125	0[6]	–
LVPECL, 2.5	LVPECL	1.25 − 0.125	1.25 + 0.125	0[6]	–
BLVDS_25, 2.5V	BLVDS_25	1.25 − 0.125	1.25 + 0.125	0[6]	–
MINI_LVDS_25, 2.5V	MINI_LVDS_25	1.25 − 0.125	1.25 + 0.125	0[6]	–
PPDS_25	PPDS_25	1.25 − 0.125	1.25 + 0.125	0[6]	–
RSDS_25	RSDS_25	1.25 − 0.125	1.25 + 0.125	0[6]	–
TMDS_33	TMDS_33	3 − 0.125	3 + 0.125	0[6]	–

Notes:

1. The input delay measurement methodology parameters for LVDCI are the same for LVCMOS standards of the same voltage. Input delay measurement methodology parameters for HSLVDCI are the same as for HSTL_II standards of the same voltage. Parameters for all other DCI standards are the same for the corresponding non-DCI standards.
2. Input waveform switches between V_L and V_H.
3. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical.
4. Input voltage level from which measurement starts.
5. This is an input voltage reference that bears no relation to the V_{REF}/V_{MEAS} parameters found in IBIS models and/or noted in Figure 3.
6. The value given is the differential input voltage.

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Output Delay Measurements

Output delays are measured with short output traces. Standard termination was used for all testing. The propagation delay of the trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in Figure 3 and Figure 4.
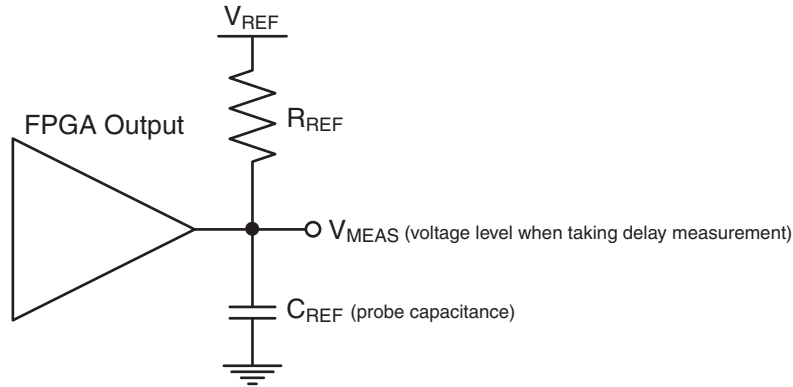
Figure 3: **Single-Ended Test Setup**
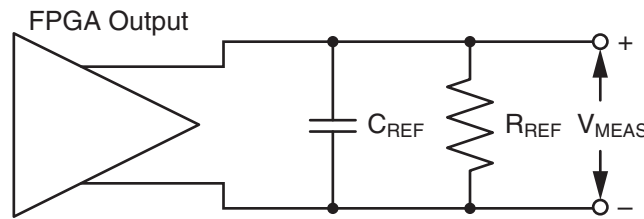
Figure 4: **Differential Test Setup**

Parameters V_{REF}, R_{REF}, C_{REF}, and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using this method:

1. Simulate the output driver of choice into the generalized test setup using values from Table 37.

2. Record the time to V_{MEAS}.

3. Simulate the output driver of choice into the actual PCB trace and load using the appropriate IBIS model or capacitance value to represent the load.

4. Record the time to V_{MEAS}.

5. Compare the results of step 2 and step 4. The increase or decrease in delay yields the actual propagation delay of the PCB trace.

Table 37: **Output Delay Measurement Methodology**

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF}[1] (pF)	V_{MEAS} (V)	V_{REF} (V)
LVCMOS, 1.2V	LVCMOS12	1M	0	0.6	0
LVCMOS 1.5V	LVCMOS15	1M	0	0.75	0
LVCMOS 1.8V	LVCMOS18	1M	0	0.9	0
LVCMOS, 2.5V	LVCMOS25	1M	0	1.25	0
LVCMOS, 3.3V	LVCMOS33	1M	0	1.65	0
LVTTL, 3.3V	LVTTL	1M	0	1.65	0
LVDCI/HSLVDCI, 1.5V	LVDCI_15, HSLVDCI_15	50	0	V_{REF}	0.75
LVDCI/HSLVDCI, 1.8V	LVDCI_18, HSLVDCI_18	50	0	V_{REF}	0.9
HSTL (high-speed transceiver logic), Class I, 1.2V	HSTL_I_12	50	0	V_{REF}	0.6
HSTL, Class I, 1.5V	HSTL_I	50	0	V_{REF}	0.75
HSTL, Class II, 1.5V	HSTL_II	25	0	V_{REF}	0.75
HSTL, Class I, 1.8V	HSTL_I_18	50	0	V_{REF}	0.9
HSTL, Class II, 1.8V	HSTL_II_18	25	0	V_{REF}	0.9
HSUL (high-speed unterminated logic), 1.2V	HSUL_12	50	0	V_{REF}	0.6
SSTL12, 1.2V	SSTL12	50	0	V_{REF}	0.6
SSTL135/SSTL135_R, 1.35V	SSTL135, SSTL135_R	50	0	V_{REF}	0.675
SSTL15/SSTL15_R, 1.5V	SSTL15, SSTL15_R	50	0	V_{REF}	0.75
SSTL (stub series terminated logic), Class I and Class II, 1.8V	SSTL18_I, SSTL18_II	50	0	V_{REF}	0.9
POD10, 1.0V	POD10	50	0	V_{REF}	1.0
POD12, 1.2V	POD12	50	0	V_{REF}	1.2
DIFF_HSTL, Class I, 1.2V	DIFF_HSTL_I_12	50	0	V_{REF}	0.6
DIFF_HSTL, Class I and II, 1.5V	DIFF_HSTL_I, DIFF_HSTL_II	50	0	V_{REF}	0.75
DIFF_HSTL, Class I and II, 1.8V	DIFF_HSTL_I_18, DIFF_HSTL_II_18	50	0	V_{REF}	0.9
DIFF_HSUL_12, 1.2V	DIFF_HSUL_12	50	0	V_{REF}	0.6
DIFF_SSTL12, 1.2V	DIFF_SSTL12	50	0	V_{REF}	0.6
DIFF_SSTL135/DIFF_SSTL135_R, 1.35V	DIFF_SSTL135, DIFF_SSTL135_R	50	0	V_{REF}	0.675
DIFF_SSTL15/DIFF_SSTL15_R, 1.5V	DIFF_SSTL15, DIFF_SSTL15_R	50	0	V_{REF}	0.75
DIFF_SSTL18, Class I and II, 1.8V	DIFF_SSTL18_I, DIFF_SSTL18_II	50	0	V_{REF}	0.9
DIFF_POD10, 1.0V	DIFF_POD10	50	0	V_{REF}	1.0
DIFF_POD12, 1.2V	DIFF_POD12	50	0	V_{REF}	1.2
LVDS (low-voltage differential signaling), 1.8V	LVDS	100	0	0[2]	0
LVDS, 2.5V	LVDS_25	100	0	0[2]	0
BLVDS (Bus LVDS), 2.5V	BLVDS_25	100	0	0[2]	0
Mini LVDS, 2.5V	MINI_LVDS_25	100	0	0[2]	0
PPDS_25	PPDS_25	100	0	0[2]	0
RSDS_25	RSDS_25	100	0	0[2]	0

Table 37: **Output Delay Measurement Methodology** *(Cont'd)*

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF}[1] (pF)	V_{MEAS} (V)	V_{REF} (V)
SUB_LVDS	SUB_LVDS	100	0	0[2]	0
TMDS_33	TMDS_33	50	0	0[2]	3.3

Notes:

1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. The value given is the differential output voltage.

Block RAM and FIFO Switching Characteristics

Table 38: **Block RAM and FIFO Switching Characteristics**

Symbol	Description	Value	Units
Maximum Frequency			
$F_{MAX\_WF\_NC}$	Block RAM (Write First and No Change modes)	525	MHz, Max
F_{MAX_RF}	Block RAM (Read First mode)	400	MHz, Max
F_{MAX_FIFO}	FIFO in all modes without ECC	525	MHz, Max
F_{MAX_ECC}	Block RAM and FIFO in ECC configuration without PIPELINE	390	MHz, Max
	Block RAM and FIFO in ECC configuration with PIPELINE and Block RAM in Write First or No Change mode	525	MHz, Max
	Block RAM in ECC configuration in Read First mode with PIPELINE	400	MHz, Max
$F_{MAX\_ADDREN\_RDADDRCHANGE}$	Block RAM with address enable and read address change compare turned on.	400	MHz, Max
$T_{PW\_WF\_NC}$[1]	Block RAM in WRITE_FIRST and NO_CHANGE modes and FIFO. Clock High/Low pulse width	952	ps, Min
T_{PW_RF}[1]	Block RAM in READ_FIRST modes. Clock High/Low pulse width	1250	ps, Min
Block RAM and FIFO Clock-to-Out Delays			
T_{RCKO_DO}	Clock CLK to DOUT output (without output register)	1.64	ns, Max
$T_{RCKO\_DO\_REG}$	Clock CLK to DOUT output (with output register)	0.49	ns, Max

Notes:

1. The MMCM and PLL DUTY_CYCLE attribute should be set to 50% to meet the pulse width requirements at the higher frequencies.

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Input/Output Delay Switching Characteristics

Table 39: **Input/Output Delay Switching Characteristics**

Symbol	Description	Value	Units
F_{REFCLK}	Reference clock frequency for IDELAYCTRL (in component mode)	200 to 800	MHz
	Reference clock frequency when using BITSLICE_CONTROL with REFCLK (in native mode (for RX_BITSLICE only))	200 to 800	MHz
	Reference clock frequency for BITSLICE_CONTROL with PLL_CLK (in native mode)[1]	200 to 1866	MHz
T_{MINPER_CLK}	Minimum period for IODELAY CLK	3.160	ns, Min
T_{MINPER_RST}	Minimum reset pulse width	52.00	ns, Min
$T_{IDELAY\_RESOLUTION}/$ $T_{ODELAY\_RESOLUTION}$	IDELAY/ODELAY chain resolution	2.5 to 15	ps

Notes:

1. PLL settings could restrict the minimum allowable data rate. For example, when using a PLL with CLKOUTPHY_MODE = VCO_HALF, the minimum frequency is PLL_F_{VCOMIN}/2.

2. See Additional Design Considerations for Configuration Memory Access Effects for guidance and mitigation of configuration readback induced time interval error in MMCMs and PLLs.

DSP48 Slice Switching Characteristics

Table 40: **DSP48 Slice Switching Characteristics**

Symbol	Description	Value	Units
Maximum Frequency			
F_{MAX}	With all registers used	594	MHz, Max
F_{MAX_PATDET}	With pattern detector	512	MHz, Max
$F_{MAX\_MULT\_NOMREG}$	Two register multiply without MREG	361	MHz, Max
$F_{MAX\_MULT\_NOMREG\_PATDET}$	Two register multiply without MREG with pattern detect	326	MHz, Max
$F_{MAX\_PREADD\_NOADREG}$	Without ADREG	358	MHz, Max
$F_{MAX\_NOPIPELINEREG}$	Without pipeline registers (MREG, ADREG)	260	MHz, Max
$F_{MAX\_NOPIPELINEREG\_PATDET}$	Without pipeline registers (MREG, ADREG) with pattern detect	238	MHz, Max

Clock Buffers and Networks

Table 41: **Clock Buffers Switching Characteristics**

Symbol	Description	Value	Units
Global Clock Switching Characteristics (Including BUFGCTRL)			
F_{MAX}	Maximum frequency of a global clock tree (BUFG)	630	MHz, Max
Global Clock Buffer with Input Divide Capability (BUFGCE_DIV)			
F_{MAX}	Maximum frequency of a global clock buffer with input divide capability (BUFGCE_DIV)	630	MHz, Max
Global Clock Buffer with Clock Enable (BUFGCE)			
F_{MAX}	Maximum frequency of a global clock buffer with clock enable (BUFGCE)	630	MHz, Max
Leaf Clock Buffer with Clock Enable (BUFCE_LEAF)			
F_{MAX}	Maximum frequency of a leaf clock buffer with clock enable (BUFCE_LEAF)	630	MHz, Max
GTH Clock Buffer with Clock Enable and Clock Input Divide Capability (BUFG_GT)			
F_{MAX}	Maximum frequency of a serial transceiver clock buffer with clock enable and clock input divide capability	512	MHz, Max

MMCM Switching Characteristics

Table 42: **MMCM Specification**

Symbol	Description	Value	Units
MMCM_F_{INMAX}	Maximum input clock frequency	800	MHz
MMCM_F_{INMIN}	Minimum input clock frequency	10	MHz
MMCM_$F_{INJITTER}$	Maximum input clock period jitter	< 20% of clock input period or 1 ns Max	
MMCM_F_{INDUTY}	Input duty cycle range: 10–49 MHz	25–75	%
	Input duty cycle range: 50–199 MHz	30–70	%
	Input duty cycle range: 200–399 MHz	35–65	%
	Input duty cycle range: 400–499 MHz	40–60	%
	Input duty cycle range: >500 MHz	45–55	%
MMCM_F_{MIN_PSCLK}	Minimum dynamic phase shift clock frequency	0.01	MHz
MMCM_F_{MAX_PSCLK}	Maximum dynamic phase shift clock frequency	450	MHz
MMCM_F_{VCOMIN}	Minimum MMCM VCO frequency	600	MHz
MMCM_F_{VCOMAX}	Maximum MMCM VCO frequency	1200	MHz
MMCM_$F_{BANDWIDTH}$	Low MMCM bandwidth at typical[1]	1.00	MHz
	High MMCM bandwidth at typical[1]	4.00	MHz
MMCM_$T_{STATPHAOFFSET}$	Static phase offset of the MMCM outputs[2]	0.12	ns
MMCM_$T_{OUTJITTER}$	MMCM output jitter	Note 3	
MMCM_$T_{OUTDUTY}$	MMCM output clock duty cycle precision[4]	0.20	ns
MMCM_$T_{LOCKMAX}$	MMCM maximum lock time for MMCM_F_{PFDMIN} frequencies above 20 MHz	100	μs
	MMCM maximum lock time for MMCM_F_{PFDMIN} frequencies from 10 MHz to 20 MHz	200	μs
MMCM_F_{OUTMAX}	MMCM maximum output frequency	630	MHz
MMCM_F_{OUTMIN}	MMCM minimum output frequency[4][5]	4.69	MHz
MMCM_$T_{EXTFDVAR}$	External clock feedback variation	< 20% of clock input period or 1 ns Max	
MMCM_$RST_{MINPULSE}$	Minimum reset pulse width	5.00	ns
MMCM_F_{PFDMAX}	Maximum frequency at the phase frequency detector	450	MHz
MMCM_F_{PFDMIN}	Minimum frequency at the phase frequency detector	10	MHz
MMCM_$T_{FBDELAY}$	Maximum delay in the feedback path	5 ns Max or one clock cycle	
MMCM_F_{DRPCLK_MAX}	Maximum DRP clock frequency	200	MHz

Notes:

1. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any MMCM outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard. Also, see Additional Design Considerations for Configuration Memory Access Effects for guidance and mitigation of configuration readback induced time interval error in MMCMs and PLLs.
4. Includes global clock buffer.
5. Calculated as $F_{VCO}/128$ assuming output duty cycle is 50%.

PLL Switching Characteristics

Table 43: **PLL Specification**[1]

Symbol	Description	Value	Units
PLL_F$_{INMAX}$	Maximum input clock frequency	800	MHz
PLL_F$_{INMIN}$	Minimum input clock frequency	70	MHz
PLL_F$_{INJITTER}$	Maximum input clock period jitter	< 20% of clock input period or 1 ns Max	
PLL_F$_{INDUTY}$	Input duty cycle range: 70–399 MHz	35–65	%
	Input duty cycle range: 400–499 MHz	40–60	%
	Input duty cycle range: >500 MHz	45–55	%
PLL_F$_{VCOMIN}$	Minimum PLL VCO frequency	600	MHz
PLL_F$_{VCOMAX}$	Maximum PLL VCO frequency	1200	MHz
PLL_T$_{STATPHAOFFSET}$	Static phase offset of the PLL outputs[2]	0.12	ns
PLL_T$_{OUTJITTER}$	PLL output jitter	Note 3	
PLL_T$_{OUTDUTY}$	PLL CLKOUT0/CLKOUT0B/CLKOUT1/CLKOUT1B duty-cycle precision[4]	0.20	ns
PLL_T$_{LOCKMAX}$	PLL maximum lock time	100	µs
PLL_F$_{OUTMAX}$	PLL maximum output frequency at CLKOUT0/CLKOUT0B/CLKOUT1/CLKOUT1B	630	MHz
	PLL maximum output frequency at CLKOUTPHY	2400	MHz
PLL_F$_{OUTMIN}$	PLL minimum output frequency at CLKOUT0/CLKOUT0B/CLKOUT1/CLKOUT1B[5]	4.69	MHz
	PLL minimum output frequency at CLKOUTPHY	2 x VCO mode: 1200 1 x VCO mode: 600 0.5 x VCO mode: 300	MHz
PLL_RST$_{MINPULSE}$	Minimum reset pulse width	5.00	ns
PLL_F$_{PFDMAX}$	Maximum frequency at the phase frequency detector	600	MHz
PLL_F$_{PFDMIN}$	Minimum frequency at the phase frequency detector	70	MHz
PLL_F$_{BANDWIDTH}$	PLL bandwidth at typical	15	MHz
PLL_F$_{DRPCLK\_MAX}$	Maximum DRP clock frequency	200	MHz

Notes:
1. The PLL does not filter typical spread-spectrum input clocks because they are usually far below the loop filter frequencies.
2. The static offset is measured between any PLL outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard. Also, see Additional Design Considerations for Configuration Memory Access Effects for guidance and mitigation of configuration readback induced time interval error in MMCMs and PLLs.
4. Includes global clock buffer.
5. Calculated as F$_{VCO}$/128 assuming output duty cycle is 50%.

Device Pin-to-Pin Output Parameter Guidelines

The pin-to-pin numbers in Table 44 are based on the clock root placement in the center of the device. The actual pin-to-pin values will vary if the root placement selected is different. Consult the Vivado Design Suite timing report for the actual pin-to-pin values.

Table 44: **Pin-to-Pin Output Parameter Guidelines**

Symbol	Description	Value	Units
SSTL15 Global Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *without* MMCM/PLL			
T_{ICKOF}	Global clock input and output flip-flop *without* MMCM/PLL (near clock region)	7.19	ns
SSTL15 Global Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *without* MMCM/PLL			
T_{ICKOF_FAR}	Global clock input and output flip-flop *without* MMCM/PLL (far clock region)	8.22	ns
SSTL15 Global Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, with MMCM			
$T_{ICKOFMMCMCC}$	Global clock input and output flip-flop *with* MMCM	2.41	ns
SSTL15 Global Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, with PLL			
$T_{ICKOF\_PLL\_CC}$	Global clock input and output flip-flop *with* PLL	6.95	ns

Notes:
1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column.
2. MMCM and PLL output jitter are already included in the timing calculation. Also, see Additional Design Considerations for Configuration Memory Access Effects for guidance and mitigation of configuration readback induced time interval error in MMCMs and PLLs.

Table 45: **Source Synchronous Output Characteristics (Component Mode)**

Symbol	Description	Value	Units
$T_{OUTPUT\_LOGIC\_DELAY\_VARIATION}$	Delay mismatch across a transmit bus when using component mode output logic (ODDRE1, OSERDESE3) within a bank.	100	ps

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Device Pin-to-Pin Input Parameter Guidelines

The pin-to-pin numbers in Table 46 through Table 47 are based on the clock root placement in the center of the device. The actual pin-to-pin values will vary if the root placement selected is different. Consult the Vivado Design Suite timing report for the actual pin-to-pin values.

Table 46: **Global Clock Input Setup and Hold With MMCM**

Symbol	Description	Value		Units
Input Setup and Hold Time Relative to Global Clock Input Signal using SSTL15 Standard.[1][2][3]				
T$_{PSMMCMCC\_KU060}$	Global clock input and input flip-flop (or latch) with MMCM	Setup	2.55	ns
T$_{PHMMCMCC\_KU060}$		Hold	−0.15	ns

Notes:
1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, slowest temperature, and slowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, fastest temperature, and fastest voltage.
2. This table lists representative values where one global clock input drives one vertical clock line in each accessible column.
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.
4. See Additional Design Considerations for Configuration Memory Access Effects for guidance and mitigation of configuration readback induced time interval error in MMCMs and PLLs.

Table 47: **Global Clock Input Setup and Hold With PLL**

Symbol	Description	Value		Units
Input Setup and Hold Time Relative to Global Clock Input Signal using SSTL15 Standard.[1][2][3]				
T$_{PSPLLCC\_KU060}$	Global clock input and input flip-flop (or latch) with PLL	Setup	−0.78	ns
T$_{PHPLLCC\_KU060}$		Hold	2.98	ns

Notes:
1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, slowest temperature, and slowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, fastest temperature, and fastest voltage.
2. This table lists representative values where one global clock input drives one vertical clock line in each accessible column.
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.
4. See Additional Design Considerations for Configuration Memory Access Effects for guidance and mitigation of configuration readback induced time interval error in MMCMs and PLLs.

Table 48: **Sampling Window**

Symbol	Description	Value	Units
T_{SAMP_BUFG}[1]	Total sampling error of the Kintex UltraScale FPGAs DDR input registers, measured across voltage, temperature, and process.	610	ps
T_{SAMP_NATIVE_DPA}	Receive sampling error for RX_BITSLICE when using dynamic phase alignment.	150	ps
T_{SAMP_NATIVE_BISC}	Receive sampling error for RX_BITSLICE when using built-in self-calibration (BISC).	110	ps

Notes:

1. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include: CLK0 MMCM jitter, MMCM accuracy (phase offset), and MMCM phase shift resolution. These measurements do not include package or clock tree skew. For detailed component mode sampling window calculations using the parameters in this table, see the *Designing Using SelectIO Interface Component Primitives* (XAPP1324) application note. Also, see Additional Design Considerations for Configuration Memory Access Effects for guidance and mitigation of configuration readback induced time interval error in MMCMs and PLLs.

Table 49: **Input Logic Characteristics for Dynamic Phase Aligned Applications (Component Mode)**

Symbol	Description	Value	Units
T_{INPUT_LOGIC_UNCERTAINTY}	Accounts for the setup/hold and any pattern dependent jitter for the input logic (input register, IDDRE1, or ISERDESE3).	40	ps
T_{CAL_ERROR}	Calibration error associated with quantization effects based on the IDELAY resolution. Calibration must be performed for each input pin to ensure optimal performance.	24	ps

Notes:

1. See Additional Design Considerations for Configuration Memory Access Effects for guidance and mitigation of configuration readback induced time interval error in MMCMs and PLLs.

Package Parameter Guidelines

The parameters in this section provide the necessary values for calculating timing budgets for clock transmitter and receiver data-valid windows.

Table 50: **Package Skew**

Symbol	Description	Device	Package	Value	Units
PKGSKEW	Package Skew	XQRKU060	CNA1509	247	ps

Notes:

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from die pad to ball.
2. Package delay information is available for these device/package combinations. This information can be used to deskew the package.
3. See Additional Design Considerations for Configuration Memory Access Effects for guidance and mitigation of configuration readback induced time interval error in MMCMs and PLLs.

GTH Transceiver Specifications

GTH Transceiver DC Input and Output Levels

Table 51 summarizes the DC specifications of the GTH transceivers in Kintex UltraScale FPGAs. Consult the *UltraScale Architecture GTH Transceiver User Guide* (UG576) for further details.

Table 51: **GTH Transceiver DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV_{PPIN}	Differential peak-to-peak input voltage (external AC coupled)	>10.3125 Gb/s	150	–	1250	mV
		6.6 Gb/s to 10.3125 Gb/s	150	–	1250	mV
		≤ 6.6 Gb/s	150	–	2000	mV
V_{IN}	Single-ended input voltage. Voltage measured at the pin referenced to GND.	DC coupled $V_{MGTAVTT}$ = 1.2V	–400	–	$V_{MGTAVTT}$	mV
V_{CMIN}	Common mode input voltage	DC coupled $V_{MGTAVTT}$ = 1.2V	–	2/3 $V_{MGTAVTT}$	–	mV
D_{VPPOUT}	Differential peak-to-peak output voltage[1]	Transmitter output swing is set to 1100	800	–	–	mV
$V_{CMOUTDC}$	Common mode output voltage: DC coupled (equation based)	When remote RX is terminated to GND	$V_{MGTAVTT}/2 - D_{VPPOUT}/4$			mV
		When remote RX termination is floating	$V_{MGTAVTT} - D_{VPPOUT}/2$			mV
		When remote RX is terminated to V_{RX_TERM}[2]	$V_{MGTAVTT} - \frac{D_{VPPOUT}}{4} - \left(\frac{V_{MGTAVTT} - V_{RX\_TERM}}{2}\right)$			mV
$V_{CMOUTAC}$	Common mode output voltage: AC coupled (equation based)		$V_{MGTAVTT} - D_{VPPOUT}/2$			mV
R_{IN}	Differential input resistance		–	100	–	Ω
R_{OUT}	Differential output resistance		–	100	–	Ω
T_{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew		–	–	10	ps
C_{EXT}	Recommended external AC coupling capacitor[3]		–	100	–	nF

Notes:

1. The output swing and pre-emphasis levels are programmable using the attributes discussed in the *UltraScale Architecture GTH Transceiver User Guide* (UG576), and can result in values lower than reported in this table.
2. V_{RX_TERM} is the remote RX termination voltage.
3. Other values can be used as appropriate to conform to specific protocols and standards.
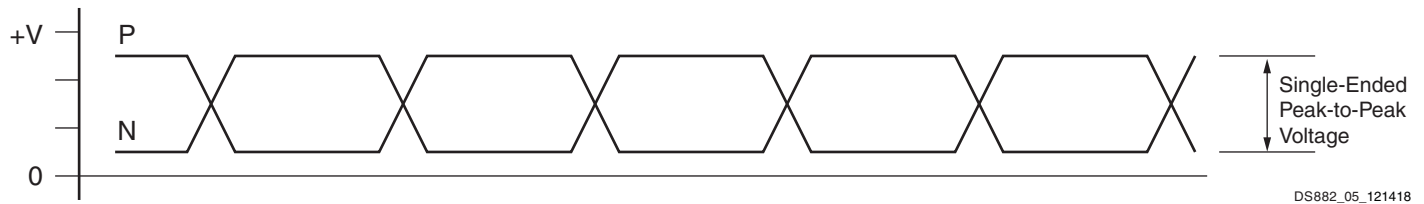
Figure 5: **Single-Ended Peak-to-Peak Voltage**

Differential peak-to-peak voltage = (Single-ended peak-to-peak voltage) x 2
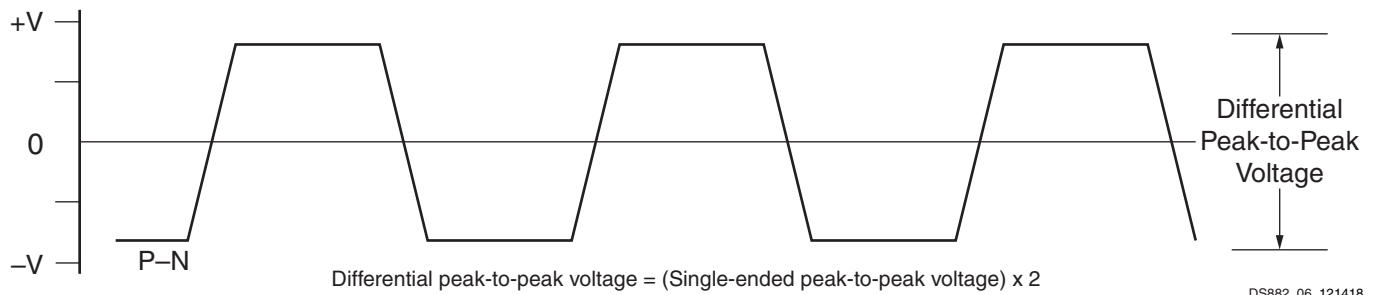
Figure 6: **Differential Peak-to-Peak Voltage**

Table 52 and Table 53 summarize the DC specifications of the GTH transceivers input and output clocks in Kintex UltraScale FPGAs. Consult the *UltraScale Architecture GTH Transceiver User Guide* (UG576) for further details.

Table 52: **GTH Transceiver Clock DC Input Level Specification**

Symbol	DC Parameter	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage	250	–	2000	mV
R_{IN}	Differential input resistance	–	100	–	Ω
C_{EXT}	Required external AC coupling capacitor	–	10	–	nF

Table 53: **GTH Transceiver Clock Output Level Specification**

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{OL}	Output low voltage for P and N	$R_T = 100\Omega$ across P and N signals	–	400	–	mV
V_{OH}	Output high voltage for P and N	$R_T = 100\Omega$ across P and N signals	–	760	–	mV
V_{DDOUT}	Differential output voltage (P–N), P = High (N–P), N = High	$R_T = 100\Omega$ across P and N signals	–	±360	–	mV
V_{CMOUT}	Common mode voltage	$R_T = 100\Omega$ across P and N signals	–	580	–	mV

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GTH Transceiver Switching Characteristics

Consult the *UltraScale Architecture GTH Transceiver User Guide* (UG576) for further information.

Table 54: **GTH Transceiver Performance**

Symbol	Description	Output Divider	Value		Units
F$_{GTHMAX}$	GTH maximum line rate		12.5		Gb/s
F$_{GTHMIN}$	GTH minimum line rate		0.5		Gb/s
			Min	Max	
F$_{GTHCRANGE}$	CPLL line rate range[1]	1	4.0	8.5	Gb/s
		2	2.0	4.25	Gb/s
		4	1.0	2.125	Gb/s
		8	0.5	1.0625	Gb/s
		16	N/A	N/A	Gb/s
			Min	Max	
F$_{GTHQRANGE1}$	QPLL0 line rate range[2]	1	9.8	12.5	Gb/s
		2	4.9	8.1875	Gb/s
		4	2.45	4.0938	Gb/s
		8	1.225	2.0469	Gb/s
		16	0.6125	1.0234	Gb/s
			Min	Max	
F$_{GTHQRANGE2}$	QPLL1 line rate range[3]	1	8.0	12.5	Gb/s
		2	4.0	6.5	Gb/s
		4	2.0	3.25	Gb/s
		8	1.0	1.625	Gb/s
		16	0.5	0.8125	Gb/s
			Min	Max	
F$_{CPLLRANGE}$	CPLL frequency range		2.0	4.25	GHz
F$_{QPLL0RANGE}$	QPLL0 frequency range		9.8	16.375	GHz
F$_{QPLL1RANGE}$	QPLL1 frequency range		8.0	13.0	GHz

Notes:
1. The values listed are the rounded results of the calculated equation (2 x CPLL_Frequency)/Output_Divider.
2. The values listed are the rounded results of the calculated equation (QPLL0_Frequency)/Output_Divider.
3. The values listed are the rounded results of the calculated equation (QPLL1_Frequency)/Output_Divider.

Table 55: **GTH Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics**

Symbol	Description	Value	Units
F$_{GTHDRPCLK}$	GTHDRPCLK maximum frequency	250	MHz

Table 56: **GTH Transceiver Reference Clock Switching Characteristics**

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{GCLK}	Reference clock frequency range		60	–	820	MHz
T_{RCLK}	Reference clock rise time	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle	Transceiver PLL only	40	50	60	%
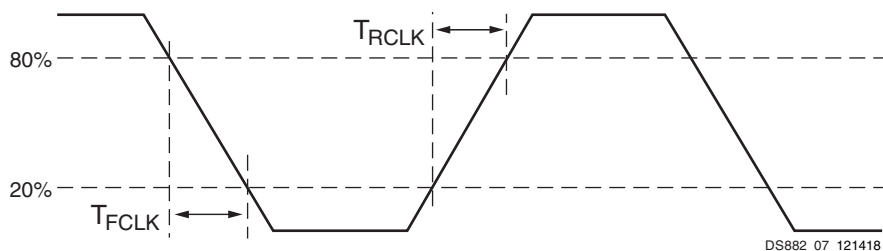
Figure 7: **Reference Clock Timing Parameters**

Table 57: **GTH Transceiver Reference Clock Oscillator Selection Phase Noise Mask**

Symbol	Description	Offset Frequency	Min	Typ	Max	Units
$QPLL_{REFCLKMASK}$[1][2]	QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency = 312.5 MHz.	10 kHz	–	–	–105	dBc/Hz
		100 kHz	–	–	–124	
		1 MHz	–	–	–130	
$CPLL_{REFCLKMASK}$[1][2]	CPLL reference clock select phase noise mask at REFCLK frequency = 312.5 MHz.	10 kHz	–	–	–105	dBc/Hz
		100 kHz	–	–	–124	
		1 MHz	–	–	–130	
		50 MHz	–	–	–140	

Notes:
1. For reference clock frequencies other than 312.5 MHz, adjust the phase-noise mask values by 20 x Log(N/312.5) where N is the new reference clock frequency in MHz.
2. This reference clock phase-noise mask is superseded by any reference clock phase-noise mask that is specified in a supported protocol, e.g., PCIe.

Table 58: **GTH Transceiver PLL/Lock Time Adaptation**

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{LOCK}	Initial PLL lock		–	–	1	ms
T_{DLOCK}	Clock recovery phase acquisition and adaptation time for decision feedback equalizer (DFE).	After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input.	–	50,000	37×10^6	UI
	Clock recovery phase acquisition and adaptation time for low-power mode (LPM) when the DFE is disabled.		–	50,000	2.3×10^6	UI

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Table 59: **GTH Transceiver User Clock Switching Characteristics**[1]

Symbol	Description	Data Width Conditions (Bit)		Value	Units
		Internal Logic	**Interconnect Logic**		
$F_{TXOUTPMA}$	TXOUTCLK maximum frequency sourced from OUTCLKPMA			390.625	MHz
$F_{RXOUTPMA}$	RXOUTCLK maximum frequency sourced from OUTCLKPMA			390.625	MHz
$F_{TXOUTPROGDIV}$	TXOUTCLK maximum frequency sourced from TXPROGDIVCLK			511.719	MHz
$F_{RXOUTPROGDIV}$	RXOUTCLK maximum frequency sourced from RXPROGDIVCLK			511.719	MHz
F_{TXIN}	TXUSRCLK maximum frequency	16	16, 32	390.625	MHz
		32	32, 64	390.625	MHz
		20	20, 40	312.500	MHz
		40	40, 80	312.500	MHz
F_{RXIN}	RXUSRCLK maximum frequency	16	16, 32	390.625	MHz
		32	32, 64	390.625	MHz
		20	20, 40	312.500	MHz
		40	40, 80	312.500	MHz
F_{TXIN2}	TXUSRCLK2 maximum frequency	16	16	390.625	MHz
		16, 32	32	390.625	MHz
		32	64	195.313	MHz
		20	20	312.500	MHz
		20, 40	40	312.500	MHz
		40	80	156.250	MHz
F_{RXIN2}	RXUSRCLK2 maximum frequency	16	16	390.625	MHz
		16, 32	32	390.625	MHz
		32	64	195.313	MHz
		20	20	312.500	MHz
		20, 40	40	312.500	MHz
		40	80	156.250	MHz

Notes:

1. Clocking must be implemented as described in *UltraScale Architecture GTH Transceiver User Guide* (UG576).
2. The TX buffer bypass and RX buffer bypass modes are not supported.

Table 60: **GTH Transceiver Transmitter Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTHTX}	Serial data rate range		0.500	–	F_{GTHMAX}	Gb/s
T_{RTX}	TX rise time	20%–80%	–	21	–	ps
T_{FTX}	TX fall time	80%–20%	–	21	–	ps
T_{LLSKEW}	TX lane-to-lane skew[1]		–	–	500	ps
$V_{TXOOBVDPP}$	Electrical idle amplitude		–	–	15	mV
$T_{TXOOBTRANSITION}$	Electrical idle transition time		–	–	140	ns
$T_{J12.5\_QPLL}$	Total jitter[2][4]	12.5 Gb/s	–	–	0.28	UI
$D_{J12.5\_QPLL}$	Deterministic jitter[2][4]		–	–	0.17	UI
$T_{J12.5\_CPLL}$	Total jitter[3][4]	12.5 Gb/s	–	–	0.33	UI
$D_{J12.5\_CPLL}$	Deterministic jitter[3][4]		–	–	0.17	UI
$T_{J11.3\_QPLL}$	Total jitter[2][4]	11.3 Gb/s	–	–	0.28	UI
$D_{J11.3\_QPLL}$	Deterministic jitter[2][4]		–	–	0.17	UI
$T_{J10.3\_QPLL}$	Total jitter[2][4]	10.3 Gb/s	–	–	0.28	UI
$D_{J10.3\_QPLL}$	Deterministic jitter[2][4]		–	–	0.17	UI
$T_{J10.3\_CPLL}$	Total jitter[3][4]	10.3 Gb/s	–	–	0.33	UI
$D_{J10.3\_CPLL}$	Deterministic jitter[3][4]		–	–	0.17	UI
$T_{J9.8\_QPLL}$	Total jitter[2][4]	9.8 Gb/s	–	–	0.28	UI
$D_{J9.8\_QPLL}$	Deterministic jitter[2][4]		–	–	0.17	UI
$T_{J9.8\_CPLL}$	Total jitter[3][4]	9.8 Gb/s	–	–	0.28	UI
$D_{J9.8\_CPLL}$	Deterministic jitter[3][4]		–	–	0.17	UI
$T_{J8.0\_CPLL}$	Total jitter[3][4]	8.0 Gb/s	–	–	0.32	UI
$D_{J8.0\_CPLL}$	Deterministic jitter[3][4]		–	–	0.17	UI
$T_{J6.6\_CPLL}$	Total jitter[3][4]	6.6 Gb/s	–	–	0.30	UI
$D_{J6.6\_CPLL}$	Deterministic jitter[3][4]		–	–	0.15	UI
$T_{J5.0}$	Total jitter[3][4]	5.0 Gb/s	–	–	0.30	UI
$D_{J5.0}$	Deterministic jitter[3][4]		–	–	0.15	UI
$T_{J4.25}$	Total jitter[3][4]	4.25 Gb/s	–	–	0.30	UI
$D_{J4.25}$	Deterministic jitter[3][4]		–	–	0.15	UI
$T_{J4.0L}$	Total jitter[3][4]	4.0 Gb/s[5]	–	–	0.32	UI
$D_{J4.0L}$	Deterministic jitter[3][4]		–	–	0.16	UI
$T_{J3.2}$	Total jitter[3][4]	3.2 Gb/s[6]	–	–	0.20	UI
$D_{J3.2}$	Deterministic jitter[3][4]		–	–	0.10	UI
$T_{J2.5}$	Total jitter[3][4]	2.5 Gb/s[7]	–	–	0.20	UI
$D_{J2.5}$	Deterministic jitter[3][4]		–	–	0.10	UI
$T_{J1.25}$	Total jitter[3][4]	1.25 Gb/s[8]	–	–	0.15	UI
$D_{J1.25}$	Deterministic jitter[3][4]		–	–	0.06	UI

Table 60: **GTH Transceiver Transmitter Switching Characteristics** *(Cont'd)*

Symbol	Description	Condition	Min	Typ	Max	Units
T_{J500}	Total jitter[3][4]	500 Mb/s[9]	–	–	0.10	UI
D_{J500}	Deterministic jitter[3][4]		–	–	0.03	UI

Notes:

1. Using same REFCLK input with TX phase alignment enabled for up to four fully populated GTH Quads at maximum line rate.
2. Using QPLL_FBDIV = 40, 40-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
3. Using CPLL_FBDIV = 2, 40-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
4. All jitter values are based on a bit-error ratio of 10^{-12}.
5. CPLL frequency at 2.0 GHz and TXOUT_DIV = 1
6. CPLL frequency at 3.2 GHz and TXOUT_DIV = 2.
7. CPLL frequency at 2.5 GHz and TXOUT_DIV = 2.
8. CPLL frequency at 2.5 GHz and TXOUT_DIV = 4.
9. CPLL frequency at 2.0 GHz and TXOUT_DIV = 4.

Table 61: **GTH Transceiver Receiver Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTHRX}	Serial data rate		0.500	–	F_{GTHMAX}	Gb/s
$T_{RXELECIDLE}$	Time for RXELECIDLE to respond to loss or restoration of data		–	10	–	ns
$R_{XOOBVDPP}$	OOB detect threshold peak-to-peak		60	–	150	mV
R_{XSST}	Receiver spread-spectrum tracking[1]	Modulated at 33 kHz	–5000	–	0	ppm
R_{XRL}	Run length (CID)		–	–	256	UI
$R_{XPPMTOL}$	Data/REFCLK PPM offset tolerance	Bit rates ≤ 6.6 Gb/s	–1250	–	1250	ppm
		Bit rates > 6.6 Gb/s and ≤ 8.0 Gb/s	–700	–	700	ppm
		Bit rates > 8.0 Gb/s	–200	–	200	ppm
SJ Jitter Tolerance[2]						
$J_{T\_SJ12.5}$	Sinusoidal jitter (QPLL)[3]	12.5 Gb/s	0.30	–	–	UI
$J_{T\_SJ11.3}$	Sinusoidal jitter (QPLL)[3]	11.3 Gb/s	0.30	–	–	UI
$J_{T\_SJ10.3\_QPLL}$	Sinusoidal jitter (QPLL)[3]	10.3 Gb/s	0.30	–	–	UI
$J_{T\_SJ10.3\_CPLL}$	Sinusoidal jitter (CPLL)[3]	10.3 Gb/s	0.30	–	–	UI
$J_{T\_SJ9.8}$	Sinusoidal jitter (QPLL)[3]	9.8 Gb/s	0.30	–	–	UI
$J_{T\_SJ8.0\_QPLL}$	Sinusoidal jitter (QPLL)[3]	8.0 Gb/s	0.44	–	–	UI
$J_{T\_SJ8.0\_CPLL}$	Sinusoidal jitter (CPLL)[3]	8.0 Gb/s	0.42	–	–	UI
$J_{T\_SJ6.6\_CPLL}$	Sinusoidal jitter (CPLL)[3]	6.6 Gb/s	0.44	–	–	UI
$J_{T\_SJ5.0}$	Sinusoidal jitter (CPLL)[3]	5.0 Gb/s	0.44	–	–	UI
$J_{T\_SJ4.25}$	Sinusoidal jitter (CPLL)[3]	4.25 Gb/s	0.44	–	–	UI
$J_{T\_SJ4.0L}$	Sinusoidal jitter (CPLL)[3]	4.0 Gb/s[4]	0.45	–	–	UI
$J_{T\_SJ3.75}$	Sinusoidal jitter (CPLL)[3]	3.75 Gb/s	0.44	–	–	UI
$J_{T\_SJ3.2}$	Sinusoidal jitter (CPLL)[3]	3.2 Gb/s[5]	0.45	–	–	UI
$J_{T\_SJ2.5}$	Sinusoidal jitter (CPLL)[3]	2.5 Gb/s[6]	0.50	–	–	UI
$J_{T\_SJ1.25}$	Sinusoidal jitter (CPLL)[3]	1.25 Gb/s[7]	0.50	–	–	UI
J_{T_SJ500}	Sinusoidal jitter (CPLL)[3]	500 Mb/s	0.40	–	–	UI

Table 61: **GTH Transceiver Receiver Switching Characteristics** *(Cont'd)*

Symbol	Description	Condition	Min	Typ	Max	Units
SJ Jitter Tolerance with Stressed Eye[2]						
$J_{T\_TJSE3.2}$	Total jitter with stressed eye[8]	3.2 Gb/s	0.70	–	–	UI
$J_{T\_TJSE6.6}$		6.6 Gb/s	0.70	–	–	UI
$J_{T\_SJSE3.2}$	Sinusoidal jitter with stressed eye[8]	3.2 Gb/s	0.10	–	–	UI
$J_{T\_SJSE6.6}$		6.6 Gb/s	0.10	–	–	UI

Notes:
1. Using RXOUT_DIV = 1, 2, and 4.
2. All jitter values are based on a bit error ratio of 10^{-12}.
3. The frequency of the injected sinusoidal jitter is 10 MHz.
4. CPLL frequency at 2.0 GHz and RXOUT_DIV = 1
5. CPLL frequency at 3.2 GHz and RXOUT_DIV = 2.
6. CPLL frequency at 2.5 GHz and RXOUT_DIV = 2.
7. CPLL frequency at 2.5 GHz and RXOUT_DIV = 4.
8. Composite jitter with RX equalizer enabled. DFE disabled.

GTH Transceiver Electrical Compliance

The *UltraScale Architecture GTH Transceiver User Guide* (UG576) contains recommended use modes that ensure compliance for the protocols listed in Table 62. The transceiver wizard provides the recommended settings for those use cases and for protocol specific characteristics.

Table 62: **GTH Transceiver Protocol List**

Protocol	Specification	Serial Rate (Gb/s)	Electrical Compliance
CAUI-10	IEEE 802.3-2012	10.3125	Compliant
nPPI	IEEE 802.3-2012	10.3125	Compliant
10GBASE-KR	IEEE 802.3-2012	10.3125	Compliant
SFP+	SFF-8431 (SR and LR)	9.95328–11.10	Compliant
XFP	INF-8077i, revision 4.5	10.3125	Compliant
RXAUI	CEI-6G-SR	6.25	Compliant
5.0G Ethernet	IEEE 802.3bx (PAR)	5.0	Compliant
QSGMII	QSGMII v1.2 (Cisco Systems, ENG-46158)	5.0	Compliant
XAUI	IEEE 802.3-2012	3.125	Compliant
2.5G Ethernet	IEEE 802.3bx (PAR)	2.5	Compliant
1000BASE-X	IEEE 802.3-2012	1.25	Compliant
OTU2	ITU G.8251	10.709225	Compliant
OTU4 (OTL4.10)	OIF-CEI-11G-SR	11.180997	Compliant
OC-3/12/48/192	GR-253-CORE	0.1555–9.956	Compliant
Interlaken	OIF-CEI-6G, OIF-CEI-11G-SR	4.25–12.5	Compliant
PCIe Gen1, 2, 3	PCI Express Base 3.0	2.5, 5.0, and 8.0	Compliant
UHD-SDI[1]	SMPTE ST-2081 6G, SMPTE St-2082 12G	6 and 12	Compliant
SDI[1]	SMPTE 424M-2006	0.27—2.97	Compliant
CPRI™	CPRI_v_6_1_2014-07-01	0.6144–12.165	Compliant
HDMI™[2]	HDMI 2.0	All	Compliant
Passive Optical Network (PON)	10G-EPON, 1G-EPON, NG-PON2, XG-PON, and 2.5G-PON	0.155–10.3125	Compliant
JESD204a/b	OIF-CEI-6G, OIF-CEI-11G	3.125–12.5	Compliant
Serial RapidIO	RapidIO Specification 3.1	1.25–10.3125	Compliant
DisplayPort (Source Only)	DP 1.2B CTS	1.62–5.4	Compliant
Fibre Channel	FC-PI-4	1.0625–12.5	Compliant
SATA Gen1, 2, 3	Serial ATA Revision 3.0 Specification	1.5, 3.0, and 6.0	Compliant
SAS Gen1, 2, 3	T10/BSR INCITS 519	3.0, 6.0, and 12.0	Compliant
SFI-5	OIF-SFI5-01.0	0.625–12.5	Compliant

Notes:
1. SDI protocols require external circuitry to achieve compliance.
2. HDMI protocols require external circuitry to achieve compliance.

GTH Transceiver Protocol Jitter Characteristics

For Table 63 through Table 68, the *UltraScale Architecture GTH Transceiver User Guide* (UG576) contains recommended settings for optimal usage of protocol specific characteristics.

Table 63: **Gigabit Ethernet Protocol Characteristics (GTH Transceivers)**

Description	Line Rate (Mb/s)	Min	Max	Units
Gigabit Ethernet Transmitter Jitter Generation				
Total transmitter jitter (T_TJ)	1250	–	0.24	UI
Gigabit Ethernet Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	1250	0.749	–	UI

Table 64: **XAUI Protocol Characteristics (GTH Transceivers)**

Description	Line Rate (Mb/s)	Min	Max	Units
XAUI Transmitter Jitter Generation				
Total transmitter jitter (T_TJ)	3125	–	0.35	UI
XAUI Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	3125	0.65	–	UI

Table 65: **PCI Express Protocol Characteristics (GTH Transceivers)**[1]

Standard	Description	Condition	Line Rate (Mb/s)	Min	Max	Units
PCI Express Transmitter Jitter Generation						
PCI Express Gen 1	Total transmitter jitter		2500	–	0.25	UI
PCI Express Gen 2	Total transmitter jitter		5000	–	0.25	UI
PCI Express Gen 3[2]	Total transmitter jitter uncorrelated		8000	–	31.25	ps
	Deterministic transmitter jitter uncorrelated			–	12	ps
PCI Express Receiver High Frequency Jitter Tolerance						
PCI Express Gen 1	Total receiver jitter tolerance		2500	0.65	–	UI
PCI Express Gen 2[2]	Receiver inherent timing error		5000	0.40	–	UI
	Receiver inherent deterministic timing error			0.30	–	UI
PCI Express Gen 3[2]	Receiver sinusoidal jitter tolerance	0.03 MHz–1.0 MHz	8000	1.00	–	UI
		1.0 MHz–10 MHz		Note 3	–	UI
		10 MHz–100 MHz		0.10	–	UI

Notes:
1. Tested per card electromechanical (CEM) methodology.
2. Using common REFCLK.
3. Between 1 MHz and 10 MHz the minimum sinusoidal jitter roll-off with a slope of 20 dB/decade.

Table 66: **CEI-6G and CEI-11G Protocol Characteristics (GTH Transceivers)**

Description	Line Rate (Mb/s)	Interface	Min	Max	Units
CEI-6G Transmitter Jitter Generation					
Total transmitter jitter[1]	4976–6375	CEI-6G-SR	–	0.3	UI
		CEI-6G-LR	–	0.3	UI
CEI-6G Receiver High Frequency Jitter Tolerance					
Total receiver jitter tolerance[1]	4976–6375	CEI-6G-SR	0.6	–	UI
		CEI-6G-LR	0.95	–	UI
CEI-11G Transmitter Jitter Generation					
Total transmitter jitter[2]	9950–11100	CEI-11G-SR	–	0.3	UI
		CEI-11G-LR/MR	–	0.3	UI
CEI-11G Receiver High Frequency Jitter Tolerance					
Total receiver jitter tolerance[2]	9950–11100	CEI-11G-SR	0.65	–	UI
		CEI-11G-MR	0.65	–	UI
		CEI-11G-LR	0.825	–	UI

Notes:
1. Tested at most commonly used line rate of 6250 Mb/s using 390.625 MHz reference clock.
2. Tested at line rate of 9950 Mb/s using 155.46875 MHz reference clock and 11100 Mb/s using 173.4375 MHz reference clock.

Table 67: **SFP+ Protocol Characteristics (GTH Transceivers)**

Description	Line Rate (Mb/s)	Min	Max	Units
SFP+ Transmitter Jitter Generation				
Total transmitter jitter	9830.40[1]	–	0.28	UI
	9953.00			
	10312.50			
	10518.75			
	11100.00			
SFP+ Receiver Frequency Jitter Tolerance				
Total receiver jitter tolerance	9830.40[1]	0.7	–	UI
	9953.00			
	10312.50			
	10518.75			
	11100.00			

Notes:
1. Line rate used for CPRI over SFP+ applications.

Table 68: **CPRI Protocol Characteristics (GTH Transceivers)**

Description	Line Rate (Mb/s)	Min	Max	Units
CPRI Transmitter Jitter Generation				
Total transmitter jitter	614.4	–	0.35	UI
	1228.8	–	0.35	UI
	2457.6	–	0.35	UI
	3072.0	–	0.35	UI
	4915.2	–	0.3	UI
	6144.0	–	0.3	UI
	9830.4	–	Note 1	UI
CPRI Receiver Frequency Jitter Tolerance				
Total receiver jitter tolerance	614.4	0.65	–	UI
	1228.8	0.65	–	UI
	2457.6	0.65	–	UI
	3072.0	0.65	–	UI
	4915.2	0.95	–	UI
	6144.0	0.95	–	UI
	9830.4	Note 1	–	UI

Notes:

1. Tested per SFP+ specification, see Table 67.

Integrated Interface Block for PCI Express Designs

More information and documentation on solutions for PCI Express designs can be found at PCI Express.

Table 69: **Maximum Performance for PCI Express Designs**

Symbol	Description	Value	Units
$F_{PIPECLK}$	Pipe clock maximum frequency	250.00	MHz
$F_{CORECLK}$	Core clock maximum frequency	500.00[1]	MHz
$F_{USERCLK}$	User clock maximum frequency	250.00	MHz
F_{DRPCLK}	DRP clock maximum frequency	250.00	MHz

Notes:

1. Refer to the *UltraScale Devices Gen3 Integrated Block for PCI Express v4.4 LogiCORE IP Product Guide* (PG156) for information regarding x8 Gen 3 operation in the -1 speed grade.

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System Monitor Specifications

Table 70: **SYSMON Specifications**

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
V_{CCADC} = 1.8V ±3%, V_{REFP} = 1.25V, V_{REFN} = 0V, ADCCLK = 5.2 MHz, T_j = −40°C to 100°C, typical values at T_j = 40°C							
ADC Accuracy[1]						
Resolution			10	–	–	Bits
Integral nonlinearity[2]	INL		–	–	±2	LSBs
Differential nonlinearity	DNL	No missing codes, guaranteed monotonic	–	–	±1	LSBs
Offset error		Offset calibration enabled	–	–	±2	LSBs
Gain error			–	–	±0.4	%
Sample rate			–	–	0.2	MS/s
RMS code noise		External 1.25V reference	–	–	1	LSBs
		On-chip reference	–	1	–	LSBs
ADC Accuracy at Extended Temperatures						
Resolution		T_j = −55°C to 125°C	10	–	–	Bits
Integral nonlinearity	INL	T_j = −55°C to 125°C	–	–	±2	LSBs
Differential nonlinearity	DNL	No missing codes, guaranteed monotonic T_j = −55°C to 125°C	–	–	±1	
Analog Inputs[2]						
ADC input ranges		Unipolar operation	0	–	1	V
		Bipolar operation	−0.5	–	+0.5	V
		Unipolar common mode range (FS input)	0	–	+0.5	V
		Bipolar common mode range (FS input)	+0.5	–	+0.6	V
Maximum external channel input ranges		Adjacent channels set within these ranges should not corrupt measurements on adjacent channels	−0.1	–	V_{CCADC}	V
On-Chip Sensor Accuracy						
Temperature sensor error[1]		T_j = −40°C to 100°C (with external REF)	–	–	±4	°C
		T_j = −55°C to 125°C (with external REF)	–	–	±4.5	°C
		T_j = −40°C to 100°C (with external REF)	–	–	±5	°C
		T_j = −55°C to 125°C (with external REF)	–	–	±6.5	°C
Supply sensor error[3]		T_j = −40°C to 100°C (with external REF)	–	–	±1	%
		T_j = −55°C to 125°C (with external REF)	–	–	±2	%
		T_j = −40°C to 100°C (with external REF)	–	–	±1.5	%
		T_j = −55°C to 125°C (with external REF)	–	–	±2.5	%

Table 70: **SYSMON Specifications** *(Cont'd)*

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
Conversion Rate[4]						
Conversion time—continuous	t_{CONV}	Number of ADCCLK cycles	26	–	32	Cycles
Conversion time—event	t_{CONV}	Number of ADCCLK cycles	–	–	21	Cycles
DRP clock frequency	DCLK	DRP clock frequency	8	–	250	MHz
ADC clock frequency	ADCCLK	Derived from DCLK	1	–	5.2	MHz
DCLK duty cycle			40	–	60	%
SYSMON Reference[5]						
External reference	V_{REFP}	Externally supplied reference voltage	1.20	1.25	1.30	V
On-chip reference		Ground V_{REFP} pin to AGND, $T_j = -40°C$ to $100°C$	1.23125	1.25	1.26875	V
		Ground V_{REFP} pin to AGND, $T_j = -55°C$ to $125°C$	1.225	1.25	1.275	V

Notes:

1. ADC offset errors are removed by enabling the ADC automatic offset calibration feature. The values are specified for when this feature is enabled.
2. See the *Analog Input* section in the *UltraScale Architecture System Monitor User Guide* (UG580).
3. Supply sensor offset and gain errors are removed by enabling the automatic offset and gain calibration feature. The values are specified for when this feature is enabled.
4. See the *Adjusting the Acquisition Settling Time* section in the *UltraScale Architecture System Monitor User Guide* (UG580).
5. Any variation in the reference voltage from the nominal $V_{REFP} = 1.25V$ and $V_{REFN} = 0V$ will result in a deviation from the ideal transfer function. This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric type applications allowing reference to vary by ±4% is permitted.

I2C Interfaces

Table 71: **I2C Fast Mode Interface Switching Characteristics[1]**

Symbol	Description	Min	Typ	Max	Units
T_{DCFCLK}	SCL duty cycle	–	50	–	%
T_{FCKO}	SDAO clock-to-out delay	–	–	900	ns
T_{FDCK}	SDAI setup time	100	–	–	ns
F_{FCLK}	SCL clock frequency	–	–	400	kHz

Notes:

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.

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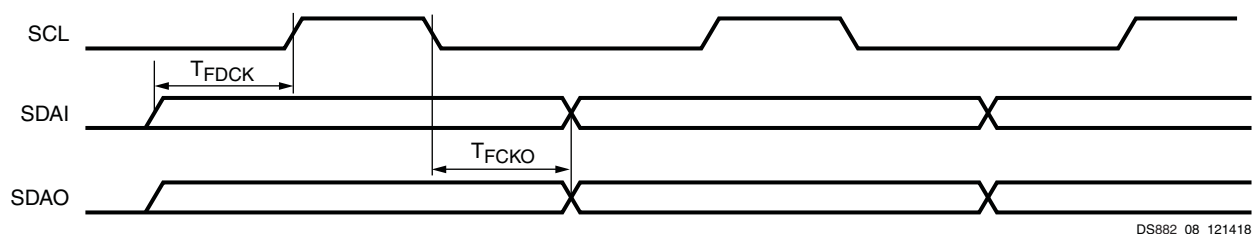
Figure 8: **I2C Fast Mode Interface Timing Diagram**

Table 72: **I2C Standard Mode Interface Switching Characteristics**[1]

Symbol	Description	Min	Typ	Max	Units
T_{DCSCLK}	SCL duty cycle	–	50	–	%
T_{SCKO}	SDAO clock-to-out delay	–	–	3450	ns
T_{SDCK}	SDAI setup time	250	–	–	ns
F_{SCLK}	SCL clock frequency	–	–	100	kHz

Notes:

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.
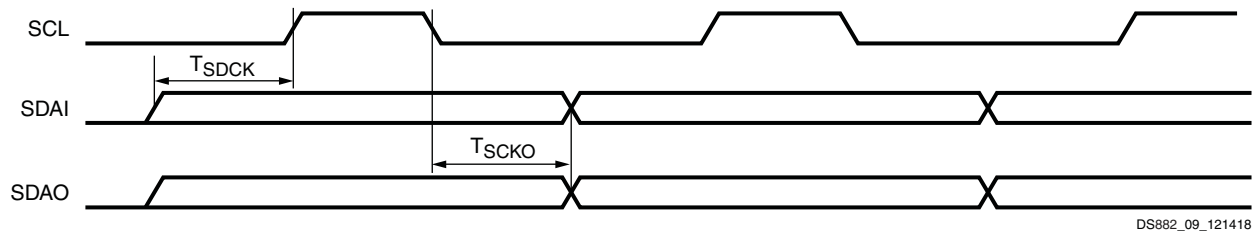
Figure 9: **I2C Standard Mode Interface Timing Diagram**

Configuration Switching Characteristics

Table 73: **Configuration Switching Characteristics**

Symbol	Description		Value	Units
Power-up Timing Characteristics				
T_{PL}	Program latency		7.5	ms, Max
T_{POR}	Power-on reset (40 ms ramp rate time)		57	ms, Max
			0	ms, Min
	Power-on reset with POR override (2 ms ramp rate time)		15	ms, Max
			5	ms, Min
$T_{PROGRAM}$	Program pulse width		250	ns, Min
CCLK Output (Master Mode)				
T_{ICCK}	Master CCLK output delay from INIT_B		150	ns, Min
T_{MCCKL}[1]	Master CCLK clock Low time duty cycle		40/60	%, Min/Max
T_{MCCKH}	Master CCLK clock High time duty cycle		40/60	%, Min/Max
F_{MCCK}	Master CCLK frequency	SPI x2/x4/x8 BPI x8/x16	150	MHz, Max
		SPI x1 and serial	150	MHz, Max
		SelectMAP	125	MHz, Max
F_{MCCK_START}	Master CCLK frequency at start of configuration		3	MHz, Typ
$F_{MCCKTOL}$	Frequency tolerance, master mode with respect to nominal CCLK		±35	%, Max
CCLK Input (Slave Modes)				
T_{SCCKL}	Slave CCLK clock minimum Low time		2.5	ns, Min
T_{SCCKH}	Slave CCLK clock minimum High time		2.5	ns, Min

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Table 73: **Configuration Switching Characteristics** *(Cont'd)*

Symbol	Description		Value	Units
F$_{SCCK}$	Slave CCLK frequency	Serial	150	MHz, Max
		SelectMAP	125	MHz, Max
EMCCLK Input (Master Mode)				
T$_{EMCCKL}$	External master CCLK Low time		2.5	ns, Min
T$_{EMCCKH}$	External master CCLK High time		2.5	ns, Min
F$_{EMCCK}$	External master CCLK frequency	SPI x1/x2/x4/x8 BPI x8/x16	150	MHz, Max
		Serial	150	MHz, Max
		SelectMAP	125	MHz, Max
Internal Configuration Access Port				
F$_{ICAPCK}$	Internal configuration access port (ICAPE3)		200	MHz, Max
Master/Slave Serial Mode Programming Switching				
T$_{DCCK}$/T$_{CCKD}$	D$_{IN}$ setup/hold		3.0/0	ns, Min
T$_{CCO}$	D$_{OUT}$ clock to out		8	ns, Max
SelectMAP Mode Programming Switching				
T$_{SMDCCK}$/T$_{SMCCKD}$	D[31:00] setup/hold		3.5/0	ns, Min
T$_{SMCSCCK}$/T$_{SMCCKCS}$	CSI_B setup/hold		4.0/0	ns, Min
T$_{SMWCCK}$/T$_{SMCCKW}$	RDWR_B setup/hold		10.0/0	ns, Min
T$_{SMCKCSO}$	CSO_B clock to out (330Ω pull-up resistor required)		7	ns, Max
T$_{SMCO}$	D[31:00] clock to out in readback		8	ns, Max
F$_{RBCCK}$	Readback frequency		125	MHz, Max
Boundary-Scan Port Timing Specifications				
T$_{TAPTCK}$/T$_{TCKTAP}$	TMS and TDI setup/hold		3.0/2.0	ns, Min
T$_{TCKTDO}$	TCK falling edge to TDO output		7	ns, Max
F$_{TCK}$	TCK frequency		66	MHz, Max
BPI Master Flash Mode Programming Switching				
T$_{BPICCO}$	A[28:00], RS[1:0], FCS_B, FOE_B, FWE_B, ADV_B clock to out		10	ns, Max
T$_{BPIDCC}$/T$_{BPICCD}$	D[15:00] setup/hold		3.5/0	ns, Min
SPI Master Flash Mode Programming Switching				
T$_{SPIDCC}$/T$_{SPICCD}$	D[03:00] setup/hold		3.0/0	ns, Min
T$_{SPIDCC}$/T$_{SPICCD}$	D[07:04] setup/hold		3.5/0	ns, Min
T$_{SPICCM}$	MOSI clock to out		8.0	ns, Max
T$_{SPICCM2}$	D[04] clock to out		10.0	ns, Max
T$_{SPICCFC}$	FCS_B clock to out		8.0	ns, Max
T$_{SPICCFC2}$	FCS2_B clock to out		10.0	ns, Max
DNA Port Switching				
F$_{DNACK}$	DNA port frequency		200	MHz, Max
STARTUPE3 Ports				
T$_{USRCCLKO}$	STARTUPE3 USRCCLKO input port to CCLK pin output delay		1.00/7.50	ns, Min/Max

Table 73: **Configuration Switching Characteristics** *(Cont'd)*

Symbol	Description	Value	Units
T_{DO}	DO[3:0] ports to D03-D00 pins output delay	1.00/8.40	ns, Min/Max
T_{DTS}	DTS[3:0] ports to D03-D00 pins 3-state delays	1.00/9.00	ns, Min/Max
T_{FCSBO}	FCSBO port to FCS_B pin output delay	1.00/8.60	ns, Min/Max
T_{FCSBTS}	FCSBTS port to FCS_B pin 3-state delay	1.00/8.60	ns, Min/Max
$T_{USRDONEO}$	USRDONEO port to DONE pin output delay	1.00/10.40	ns, Min/Max
$T_{USRDONETS}$	USRDONETS port to DONE pin 3-state delay	1.00/10.40	ns, Min/Max
T_{DI}	D03-D00 pins to DI[3:0] ports input delay	0.5/3.5	ns, Min/Max
$F_{CFGMCLK}$	STARTUPE3 CFGMCLK output frequency	50	MHz, Typ
$F_{CFGMCLKTOL}$	STARTUPE3 CFGMCLK output frequency tolerance	±15	%, Max
Startup Timing			
T_{DCI_MATCH}	Specifies a stall in the startup cycle until the digitally controlled impedance (DCI) match signals are asserted.	4	ms, Max

Notes:
1. When the CCLK is sourced from the EMCCLK pin with a divide-by-one setting, the external EMCCLK must meet this duty-cycle requirement.
2. See Additional Design Considerations for Configuration Memory Access Effects for guidance and mitigation of configuration readback induced time interval error in MMCMs and PLLs.

eFUSE Programming Conditions

Table 74: **eFUSE Programming Conditions**[1]

Symbol	Description	Min	Typ	Max	Units
I_{FS}	V_{CCAUX} supply current	–	–	115	mA
T_j	Temperature range	–40	–	125	°C

Notes:
1. Do not program eFUSE during device configuration (e.g., during configuration, during configuration readback, or when readback CRC is active).

Additional Design Considerations for Configuration Memory Access Effects

For XQRKU060 designs, where configuration memory read or write access activity can occur while the design is operating in the device, additional considerations must be applied to the design to mitigate potential additional time interval error (TIE) jitter on the MMCM and PLL clock outputs.

Configuration Memory Access Incurs Additional TIE Jitter in MMCMs and PLLs

Configuration memory read and write access involves logic transitions on internal configuration data lines that, in an UltraScale device, can couple into the VCO circuits in the MMCMs and PLLs. This combination

of configuration activity and coupling can result in varying amounts of increased TIE jitter on the clock outputs of the MMCMs and PLLs.

The resulting total TIE jitter increase on a clock output due to configuration memory access is a function of input clock frequency, VCO frequency (M divider value), and the type of clock management element used (MMCM, PLL, or MMCM-to-PLL cascade). The additional TIE jitter effect due to configuration memory access is worse for an MMCM than for a PLL.

The MMCMs/PLLs residing in different I/O banks are affected independently because adjacent I/O banks are in different rows in the UltraScale device architecture, and separate internal horizontal configuration data lines independently access configuration memories within each row. Table 75 contains references for assessing the potential TIE jitter increase on clock outputs from PLLs and MMCMs.

Table 75: **Reference for Additional PLL TIE Jitter from Configuration Memory Access Activity**

REFCLK Frequency (MHz)	Additional PLL TIE Jitter (ps)
$F_{IN} > 400$	±125
$200 < F_{IN} \leq 400$	±175
$100 < F_{IN} \leq 200$	±240
$F_{IN} \leq 100$ (except M = 16)	±260
$F_{IN} \leq 100$ (M = 16)	±190

For MMCMs, Equation 1 is a reference for additional MMCM TIE jitter from configuration memory access activity.

$$\text{Additional MMCM TIE Jitter (ps)} = A \times F_{IN}(\text{reference frequency in MHz}) + B \qquad \textit{Equation 1}$$

where:

$A = -0.27 \times (M)^2 + 19.86 \times (M) - 956.26$

$B = -0.047 \times (M)^3 + 6.68 \times (M)^2 - 283.27 \times (M) + 6703.6$

M = Feedback divide ratio = VCO frequency/Reference frequency

Examples of Potentially Affected Designs and Mitigation Recommendations

The following are examples of the kinds of designs affected by the additional TIE jitter from configuration memory access activity and the mitigation recommendations for each.

Use Case 1: Designs with Synchronous Clock Domain Crossing Between Clocks

Designs involving synchronous clock domain crossing (CDC) between clocks from the following can be affected:

- MMCM and a PLL (including MMCM-to-PLL cascade and MMCM)
- Two MMCMs in different banks

- Two PLLs in different banks
- MMCM-to-PLL cascade and PLL, even if in the same bank

The additional TIE jitter can cause a timing margin reduction in the CDC paths involving clocks from the clocking configurations described above.

Use Case 1 - Design Recommendations

Apply the following steps for designs having use case 1:

1. Use Table 75 and Equation 1 as references for assessing the potential TIE jitter increase based on the clock topology used.

2. Apply the factors from the above references as an additional timing constraint to the affected CDC paths.

3. If there is enough timing margin left with the additional constraints, the system is immune to the additional TIE jitter from configuration memory accesses and no further design actions are needed.

4. If there is insufficient timing margin with the additional constraints, apply one or more of the following mitigation steps until there is enough timing margin:

   o Consolidate the critical paths to use only one clock management element. If possible, use one PLL to clock the entire path

   o Replace an MMCM implementation with a PLL implementation

   o Avoid or remove MMCM-to-PLL cascade

   o Increase the input clock frequency to the maximum possible frequency

   o Increase the VCO frequency to the maximum allowed

Use Case 2 - Designs with System Synchronous or Asynchronous SelectIO Receiver Interfaces

Designs with system synchronous (or synchronous phase unknown) or asynchronous SelectIO receiver interfaces can be affected. The additional TIE jitter can reduce the overall receiver margins in I/O interfaces requiring static or dynamic phase tracking to center the data with respect to an asynchronous or synchronous phase-unknown clock coming into the device and through an MMCM or a PLL.

Use Case 2 - Design Recommendations

Apply the following steps for designs having use case 2:

1. Use Table 75 and Equation 1 as references for assessing the potential TIE jitter increase based on the clock topology used.

2. Apply the above factor as additional error (data valid window closure) for the receiver margin calculations.

3. If there is enough receiver margin left with the additional error factor, the receiver interface is immune to configuration memory access induced jitter and no further design actions are needed.

4. If there is insufficient receiver margin with the additional error factor, apply one or more of the following mitigation steps to the receiver until there is enough receiver margin:

   o Replace an MMCM implementation with a PLL implementation

   o Avoid or remove MMCM-to-PLL cascade

   o Increase the input clock frequency to the maximum possible frequency

   o Increase the VCO frequency to the maximum allowed

Use Case 3 - Designs with Transmit Interfaces without an Associated Forwarded Clock

Designs with transmit interfaces with no associated forwarded clock (such as system synchronous or asynchronous interface transmitters) can be affected. These effects can manifest as additional transmit error (data valid window closure) to the receiver margin calculations.

Use Case 3 - Design Recommendations

Apply the following steps for designs having use case 3:

1. Use Table 75 and Equation 1 as references for assessing the potential TIE jitter increase based on the clock topology used.

2. Apply the above factor as additional transmit error (data valid window closure) for the receiver margin calculations.

3. If there is enough receiver margin left with the additional transmit error factor, the interface is immune to configuration memory access induced jitter and no further design actions are needed.

4. If there is insufficient receiver margin with the additional transmit error factor, apply one or more of the following mitigation steps to the transmitter until there is enough receiver margin:

   o Replace an MMCM implementation with a PLL implementation

   o Avoid or remove MMCM-to-PLL cascade

   o Increase the input clock frequency to the maximum possible frequency

   o Increase the VCO frequency to the maximum allowed

Use Case 4 - Designs with Source Synchronous Transmit Interfaces with Data/Clock and MMCMs or PLLs Spanning Multiple Banks

Designs with source synchronous transmit interfaces with data/clock spanning more than one bank that are clocked by clock management elements (MMCMs or PLLs) from multiple banks can be affected. This will lower the system margin on interfaces that span multiple banks, are clocked by MMCMs or PLLs from more than one bank, and are required to have a fixed phase relationships at the receiver.

Use Case 4 - Design Recommendations

Apply the following steps for designs having use case 4:

1. Use Table 75 and Equation 1 as references for assessing the potential TIE jitter increase based on the clock topology used.

2. Apply the above factor as additional transmit error (data valid window closure) for the receiver margin calculations.

3. If there is enough receiver margin left with the additional transmit error factor, the interface is immune to configuration memory access induced jitter and no further design actions are needed.

4. If there is insufficient receiver margin with the additional transmit error factor, apply one or more of the following mitigation steps to the transmitter until there is enough receiver margin:

   o Consolidate the interface to use only one clock management element. If possible, use one PLL to clock the entire interface.

   o Replace an MMCM implementation with a PLL implementation

   o Avoid or remove MMCM-to-PLL cascade

   o Increase the input clock frequency to the maximum possible frequency

   o Increase the VCO frequency to the maximum allowed

PCB Design Guidelines

Refer to the *UltraScale Architecture PCB Design User Guide* (UG583) and UltraScale and *UltraScale and UltraScale+ FPGAs Packaging and Pinouts Product Specification* (UG575) for general UltraScale device PCB design recommendations and for the assumptions on which the guidelines are based. The following sections describe PCB design recommendations that are specific to the XQRKU060-CNA1509 device and that supersede recommendations in *UltraScale Architecture PCB Design User Guide* and *UltraScale and UltraScale+ FPGAs Packaging and Pinouts Product Specification*.

RECOMMENDED: *Refer to the Kintex UltraScale and Virtex UltraScale FPGAs Schematic Review Checklist (XTP344) for a comprehensive checklist for schematic review which complements the information in the UltraScale Architecture PCB Design User Guide.*

For PCBs supporting migration between the XCKU060-FFVA1517 and XQRKU060-CNA1509, see Migration between the XCKU060-FFVA1517 and XQRKU060-CNA1509 for additional PCB design considerations.

Pad Land Dimensions

Xilinx provides the diameter of a land pad on the package side. This information is required prior to the start of the board layout so the board pads can be designed to match the package side land geometry. The package land pad diameter is provided in Table 76. Typical PCB dimensions are described in Figure 10 and summarized in Table 76. These are guidelines only and can vary depending on PCB vendor and assembly capability. Non-solder mask defined (NSMD) pads on the board are suggested to allow a clearance between the land metal (diameter L) and the solder mask opening (diameter M) as shown in Figure 10. The space between the NSMD pad and the solder mask as well as the actual signal trace widths depend on the capability of the PCB manufacturing process.
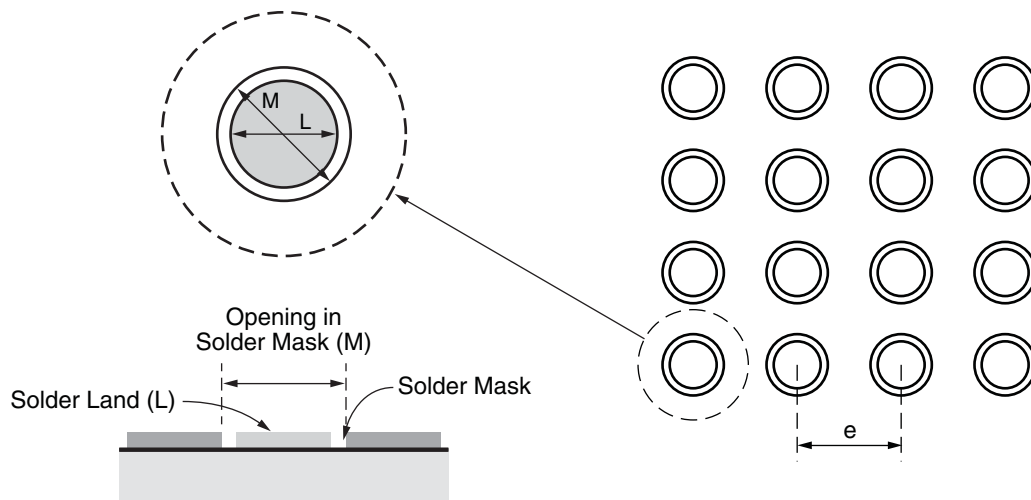
Figure 10: **Suggested Board Layout of Soldered Pads**

Table 76: **Recommended Dimensions**

Description	Reference	Dimension (mm)
Package Land Pad Diameter		0.80
Solder Land Diameter	L	0.80
Opening in Solder Mask Diameter	M	0.90
Solder (Ball) Land Pitch	e	1.00

Power Supply Voltage Requirements

Use XPE to estimate power consumption and to determine the typical voltage for each power supply. The power supplies should be set to supply the typical voltage from the XPE results to the device pins. See special instructions for the V_{CCINT} power supply below. Separate power supplies are recommended for the GTH transceiver. Other supplies can be combined when the typical voltages from XPE are within ±1% of each other and when the recommended operating ranges of all combined supplies can be met.

V_{CCINT} Power Supply Voltage Sense Guidelines

For V_{CCINT}, use XPE to estimate power consumption and to determine the VCCINT regulator supply requirement for the typical voltage measured at the VCCINT_SENSE pin relative to GND. The VCCINT_SENSE pin provides direct access to the device's internal VCCINT power plane for sensing and maintaining the device's V_{CCINT} voltage within the recommended operating conditions. A typical example of VCCINT and VCCINT_SENSE power supply connections is shown in Figure 11.
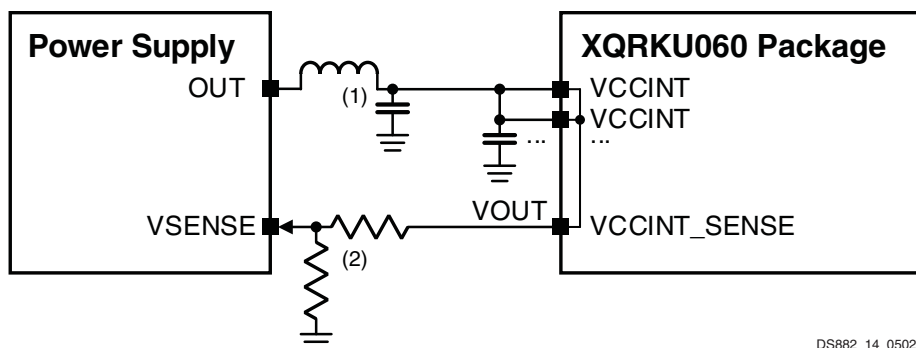
Figure 11: **Typical VCCINT Power Supply with Voltage Sense Circuit**

Notes for Figure 11:

1. Refer to the power supply vendor's data sheet for output circuit recommendations.

2. Use XPE to estimate power consumption and to determine the VOUT voltage. Refer to the power supply vendor's data sheet for VSENSE circuit recommendations.

Refer to the power supply vendor's data sheet for power supply circuit PCB layout recommendations. Voltage sense line layout recommendations typically include:

- Use a controlled impedance (50Ω) trace from the VCCINT_SENSE pin to the power solution sense circuit.

- Route the sense line away from switching sources.

- Avoid routing the sense line near and under power supply outputs and associated inductors.

- Keep the sense circuits close to the power regulator and the circuit traces short.

- Leave the GND_SENSE pin floating.

Recommended PCB Capacitors per Device

Example decoupling capacitor quantities for the XQRKU060-CNA1509 device are listed in Table 77 to Table 81. The optimized quantities of PCB decoupling capacitors assume that the voltage regulators have stable output voltages and meet the regulator manufacturer's minimum output capacitance requirements. These recommendations assume a regulator (DC) tolerance of ±2% and an AC tolerance of ±1%, except for V_{CCINT} which assumes an AC tolerance of ±2%. The total of the DC and AC tolerances must be within the recommended operating conditions specified in Table 9.

Table 77: **Decoupling Capacitor Quantities for V$_{CCINT}$ with Sample Step Currents**

VCCINT/VCCBRAM/VCCINT_IO Combined or VCCINT/VCCINT_IO Combined[1]					
Step current (A)	330 µF	47 µF	10 µF	1.0 µF	0.22 µF
6	3	6	30	30	40
5	2	5	19	21	25
4	1	4	16	16	16
3	1	2	8	8	8

Table 77: **Decoupling Capacitor Quantities for V$_{CCINT}$ with Sample Step Currents** *(Cont'd)*

VCCINT/VCCBRAM/VCCINT_IO Combined or VCCINT/VCCINT_IO Combined[1]					
Step current (A)	330 µF	47 µF	10 µF	1.0 µF	0.22 µF
2	1	1	3	3	3

Notes:
1. VCCINT_IO is tied internally in the CNA1509 package to VCCINT.
2. Step current is typically a fraction of dynamic current; roughly 15–33%.

Table 78: **Decoupling Capacitor Quantities for V$_{CCBRAM}$**

V$_{CCBRAM}$	
47 µF	10 µF
1	1

Table 79: **Decoupling Capacitor Quantities for V$_{CCAUX}$/V$_{CCAUX\_IO}$**

V$_{CCAUX}$/V$_{CCAUX\_IO}$ (combined)	
47 µF	10 µF
1	1

Notes:
1. Based on 2.0A of I$_{CCAUX}$ + I$_{CCAUX\_IO}$ dynamic current.

Table 80: **Decoupling Capacitor Quantities for V$_{CCO}$ per Bank**

V$_{CCO\_HP}$ (per bank) or V$_{CCO\_HR}$ (per bank)	
47 µF	10 µF
1	1

Notes:
1. When combining banks, one 47 µF can power up to four connected banks.

Table 81: **Decoupling Capacitor Specifications and Sample Part Numbers**

Value (µF)	Case	Type	ESR (mΩ)	ESL (nH)	Sample Part Number
330	X	Tant Poly	5.84	1.90	Kemet T541X337M010AH6510
47	X	Tant Poly	15.22	1.90	Kemet T541X476M035AH6510
10	1210	X7R	20	1.62	
1.0	0805	X7R	19	2.50	
0.22	0603	X7R	12	2.50	

Decoupling methods other than those presented in these tables can be used, but the decoupling network should be designed to meet or exceed the performance of the simple decoupling networks presented here. The impedance of the alternate network is recommended to be less than or equal to that of the recommended network across frequencies from 100 kHz to approximately 10 MHz.

The capacitor numbers shown in Table 77 are based on the following example assumptions:

V$_{CCINT}$ recommended operating range (total tolerance) from Table 9 = 4%

Assumed V$_{CCINT}$ power supply DC tolerance = 2%

Therefore, allowable V_{CCINT} power distribution AC ripple = 4% − 2% = 2%

The target impedance is calculated using the 2% AC ripple along with the current estimates from XPE for the resource utilization assumptions found in *UltraScale Architecture PCB Design User Guide* (UG583) to arrive at the capacitor recommendations. Target impedance is given by Equation 2:

$$Z_{target} = VoltageRailValue \times (\% \, Ripple / 100) / StepLoadCurrent \qquad \textit{Equation 2}$$

For each supply refer to Table 9 for the recommended operating range, and then apply a DC tolerance assumption to assess the allowable AC ripple within the recommended operating range as shown in the V_{CCINT} example above. VCCBRAM is recommended to be tied to VCCINT, and when VCCBRAM is tied to VCCINT, VCCBRAM is permitted to operate under the same conditions as VCCINT for DC tolerance and AC ripple. VCCINT, VCCAUX, and VCCBRAM capacitors are listed as the quantity per device, while VCCO capacitors are listed as the quantity per I/O bank.

For decoupling networks required for the GTH transceiver power supplies, refer to the *UltraScale Architecture GTH Transceiver User Guide* (UG576).

GTH Right-North Power Supply Group Pins

The CNA1509 package has GTH right-north (RN) power supply group pins. However, there are no right-north GTH Quads in the XQRKU060 device (or XCKU060 device). Each set of GTH RN power supply group pins are tied to respective power planes within the package, but are not used and should be treated as unused GTH power supply groups. See the "GTH Transceiver PCB Design Checklist" table in the *UltraScale Architecture GTH Transceiver User Guide* (UG576) for recommended GTH power supply group pin connections that are not used.

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Packaging

Introduction

Ceramic flip-chip column grid array (CN) packages are surface mount-compatible packages using high-temperature solder columns as interconnections to the board. Compared to the solder spheres, the columns have lower stiffness and provide a higher stand-off. These features significantly increase the reliability of the solder joints. When combined with a high-density, multi-layer ceramic substrate, this packaging technology offers a high-density, reliable packaging solution.

CNA1509 Package Construction and Key Features

- Qualified per MIL-PRF-38535

- Non-hermetic multi-layer ceramic substrate

- High planarity and excellent thermal stability at high temperature

- CTE matches well with the silicon die

- Low corrosion sensitivity

- Meets JEDEC MSL-1

- Meets outgas requirements (ASTM E 595-93 and ECSS-Q-ST-70-02C, TML < 1%, CVCM < 0.1%)

- 80% Pb/20% Sn core columns with Cu ribbon

- 37% Pb/63% Sn die solder bumps

- Nickel-plated aluminum silicon carbide (Al-SiC) heat-spreader

IMPORTANT: *The material used for the CNA1509 package lid is nickel-plated Al-SiC, which is conductive and not connected to ground in the package. The Al-SiC lid should be externally connected to system ground to avoid collecting charges in space environments. When attaching heat spreader on the lid, use an electrically conductive adhesive (such as silver-filled epoxy).*
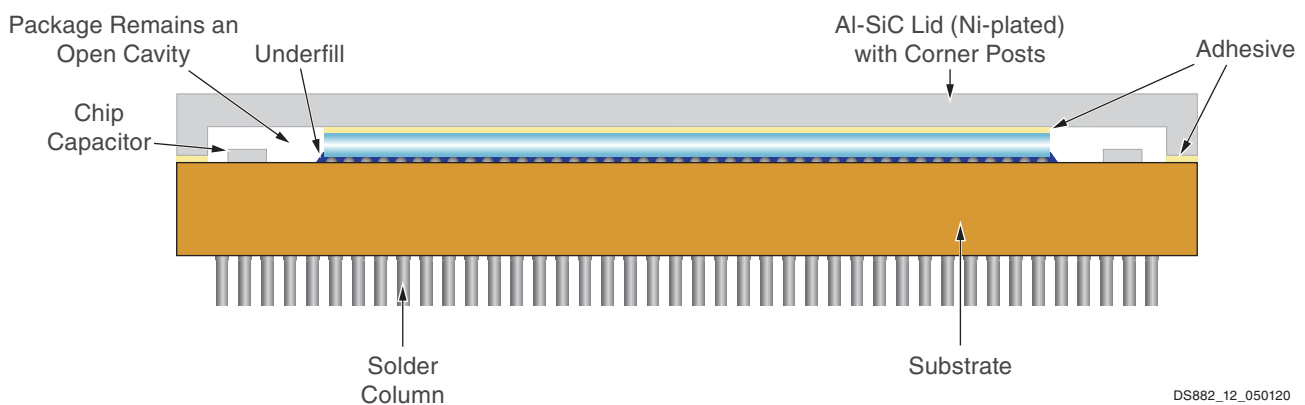
Figure 12: **CNA1509 Package Construction with 40 mm × 40 mm Lid**

The XQRKU060 is available in a CNA1509 package. For pin definitions, consult the *UltraScale and UltraScale+ FPGAs Packaging and Pinouts Product Specification* (UG575).

Table 82: **Package Specifications**

Package	Description	Package Specifications		
		Package Type	Pitch (mm)	Size (mm)
CNA1509	Ceramic Flip-Chip Column Grid Array	CCGA	1.0	40 x 40

Table 83: **XQRKU060-CNA1509 I/O Pins**

Total User I/O		Differential I/O	
HR	HP	HR	HP
104	516	96	474

Pin Definition

Table 84 lists the pin definitions used in the XQRKU060-CNA1509 device package.

Table 84: **Pin Definitions**

Pin Name	Type	Direction	Description
User I/O Pins			
IO_L[*1 to 24*][P or N]_T[*0 to 3*] [*U or L*]_N[*0 to 12*]_ [multi-function]_[bank number] or IO_T[*0 to 3*][*U or L*]_N[*0 to 12*]_[multi-function]_[bank number]			
	Dedicated	Input/Output	Most user I/O pins are capable of differential signaling and can be implemented as pairs. Each user I/O pin name consists of several indicator labels, where: • IO indicates a user I/O pin. • L[*1 to 24*] indicates a unique differential pair with P (positive) and N (negative) sides. User I/O pins without the L indicator are single-ended. • T[*0 to 3*][*U or L*] indicates the assigned byte group and nibble location (upper or lower portion) within that group for the pin. • N[*0 to 12*] the number of the I/O within its byte group. • [*multi-function*] indicates any other functions that the pin can provide. If not used for this function, the pin can be a user I/O. • [*bank number*] indicates the assigned bank for the user I/O pin.
User I/O Multi-Function Pins			
GC	Multi-function	Input/Output	Four global clock (GC) pin pairs are in each bank. GC pins have direct access to the global clock buffers, MMCMs, and PLLs that are in the clock management tile (CMT) adjacent to the same I/O bank. GC inputs provide dedicated, high-speed access to the internal global and regional clock resources. GC inputs use dedicated routing and must be used for clock inputs where the timing of various clocking features is imperative. GC pins can be treated as user I/O when not used as input clocks. Up-to-date information about designing with the GC pin is available in the *UltraScale Architecture Clocking Resources User Guide* (UG572).

Table 84: **Pin Definitions** *(Cont'd)*

Pin Name	Type	Direction	Description
VRP[1]	Multi-function	N/A	This pin is for the DCI voltage reference resistor of P transistor (per bank, to be pulled Low with a reference resistor).
DBC QBC	Multi-function	Input	Byte lane clock (DBC and QBC) input pin pairs are clock inputs directly driving source synchronous clocks to the bit slices in the I/O banks. In memory applications, these are also known as DQS. For more information, consult the *UltraScale Architecture SelectIO Resources User Guide* (UG571).
PERSTN[*0 to 1*]	Multi-function	Input	Default reset pin locations for the integrated block for PCI Express.
User I/O Multi-Function Configuration Pins			
For further descriptions, including configuration modes and recommended external pull-up/pull-down resistors, see the *UltraScale Architecture Configuration User Guide* (UG570).			
EMCCLK	Multi-function	Input	External master configuration clock.
DOUT_CSO_B	Multi-function	Output	Data output for serial daisy-chaining or active-Low chip-select output for SelectMAP daisy-chaining.
D[*04 to 31*]	Multi-function	Bidirectional	Configuration data pins.
A[*00 to 28*]	Multi-function	Output	Address output.
CSI_ADV_B	Multi-function	Input or Output	Active-Low chip-select input or address valid output.
FOE_B	Multi-function	Output	Active-Low flash output enable.
FWE_FCS2_B	Multi-function	Output	Active-Low flash write-enable for BPI flash or flash chip-select for second SPI (x8) flash.
RS[*0 to 1*]	Multi-function	Output	Revision select outputs.
Dedicated (Bank 0) Configuration Pins[2]			
For more information see the *UltraScale Architecture Configuration User Guide* (UG570).			
M[*0 to 2*]_0	Dedicated	Input	Configuration mode selection.
INIT_B_0	Dedicated	Bidirectional (open-drain)	Active-Low initialization
CFGBVS_0	Dedicated	Input	Bank 0 and bank 65 voltage select. This pin determines the I/O voltage operating range and voltage tolerance for the dedicated configuration bank 0 and multi-function bank 65. Connect CFGBVS High or Low per the bank voltage requirements. • V_{CCO_0} = 2.5V or 3.3V, tie CFGBVS High (connect to V_{CCO_0}). • V_{CCO_0} = 1.5V or 1.8V, tie CFGBVS Low (connect to GND) *CAUTION! To avoid device damage, this pin must be connected correctly to either V_{CCO_0} or GND.*

Table 84: **Pin Definitions** *(Cont'd)*

Pin Name	Type	Direction	Description
PUDC_B_0	Dedicated	Input	Active-Low input enables internal pull-ups during configuration on all SelectIO pins: 0 = Weak preconfiguration I/O pull-up resistors enabled. 1 = Weak preconfiguration I/O pull-up resistors disabled.
POR_OVERRIDE	Dedicated	Input	All configuration modes Power-on reset delay override. *CAUTION! Do not allow this pin to float before and during configuration. This pin must be tied to V_{CCINT} or GND. Do not connect to V_{CCO_0}.* Information about designing with the POR_OVERRIDE pin is available in the *UltraScale Architecture Configuration User Guide* (UG570).
DONE_0	Dedicated	Bidirectional	Active-High, DONE indicates successful completion of configuration.
PROGRAM_B_0	Dedicated	Input	Active Low, asynchronous reset to configuration logic.
TDO_0	Dedicated	Output	JTAG test data output.
TDI_0	Dedicated	Input	JTAG test data input.
RDWR_FCS_B_0	Dedicated	Input/ Output	Input control signal for SelectMAP data bus direction: High for reading or Low for writing configuration data. Or, active-Low flash chip-select output.
TMS_0	Dedicated	Input	JTAG test mode data select.
TCK_0	Dedicated	Input	JTAG test clock
CCLK_0	Dedicated	Input/ Output	Configuration clock. Output in Master mode or input in Slave mode.
D00_MOSI_0	Dedicated	Bidirectional	Data Bit 0 or SPI master-output
D01_DIN_0	Dedicated	Bidirectional	Data Bit 1 or serial mode data input
D02_0	Dedicated	Bidirectional	Data Bit 2
D03_0	Dedicated	Bidirectional	Data Bit 3
Other Dedicated Pins			
DXN	Dedicated	N/A	Temperature-sensing diode pins (Anode: DXP; Cathode: DXN). The thermal diode is accessed by using the DXP and DXN pins in bank 0. When not used, tie to GND. To use the thermal diode an appropriate external thermal monitoring IC must be added. Consult the external thermal monitoring IC data sheet for usage guidelines.
DXP			
System Monitor Pins[3]			
AD[0 to 15][P or N]	Multi-function	Input	System Monitor differential auxiliary analog inputs 0–15.
VCCADC	Dedicated	N/A	System Monitor analog positive supply voltage.
GNDADC	Dedicated	N/A	System Monitor analog ground reference.
VREFP	Dedicated	N/A	Voltage reference input.

Table 84: **Pin Definitions** *(Cont'd)*

Pin Name	Type	Direction	Description
VREFN	Dedicated	N/A	Voltage reference GND.
VP	Dedicated	Input	System Monitor dedicated differential analog input (positive side).
VN	Dedicated	Input	System Monitor dedicated differential analog input (negative side).
I2C_SCLK	Multi-function	Bidirectional	I2C serial clock. Directly connected to the System Monitor DRP interface for I2C operation configuration. *IMPORTANT: Because the SYSMON I2C interface is active after power-on, this pin should only be used for I2C access until after configuration.*
I2C_SDA	Multi-function	Bidirectional	I2C serial data line. Directly connected to the System Monitor DRP interface for I2C operation configuration. *IMPORTANT: Because the SYSMON I2C interface is active after power-on, this pin should only be used for I2C access until after configuration.*
Power/Ground Pins			
For more information on voltage specifications see the *UltraScale device data sheets*.			
GND	Dedicated	N/A	Ground.
GND_SENSE	Dedicated	N/A	The GND_SENSE pin provides direct access to device's internal GND plane for measurements.
VCCINT	Dedicated	N/A	Power-supply pins for the internal logic.
VCCINT_IO	Dedicated	N/A	VCCINT_IO is a power supply for I/O banks in Kintex UltraScale devices. The XQRKU60-CNA1509 does not have any VCCINT_IO pins. Instead, VCCINT_IO is tied internally in the CNA1509 package to VCCINT. See Migration between the XCKU060-FFVA1517 and XQRKU060-CNA1509 for more information.
VCCINT_SENSE	Dedicated	N/A	The VCCINT_SENSE pin provides direct access to the device's internal VCCINT power plane for sensing and maintaining the device's VCCINT voltage.
VCCAUX	Dedicated	N/A	Power-supply pins for auxiliary circuits.
VCCAUX_IO	Dedicated	N/A	Auxiliary power-supply pins for the I/O banks. VCCAUX_IO must be connected to VCCAUX on the board.
VCCBRAM	Dedicated	N/A	Block RAM power supply pins.
VBATT	Dedicated	N/A	Decryptor key memory backup supply; this pin should be tied to the appropriate V_{CC} or GND when not used.
VCCO_[bank number]	Dedicated	N/A	Power-supply pins for the output drivers (per bank).
VREF_[bank number]	Dedicated	N/A	These are input threshold voltage pins.

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Table 84: **Pin Definitions** *(Cont'd)*

Pin Name	Type	Direction	Description
Multi-gigabit Serial Transceiver Pins (GTHE3)			
For more information on the GTH transceivers see the *UltraScale Architecture GTH Transceiver User Guide* (UG576).			
MGTHRX[P or N][0 to 3] _[GT quad number]	Dedicated	Input	Differential receive port GTH Quad.
MGTHTX[P or N][0 to 3] _[GT quad number]	Dedicated	Output	Differential transmit port GTH Quad.
MGTAVCC_[L, RN, or RS][4]	Dedicated	Input	Analog power-supply pin for the receiver and transmitter internal circuits.
MGTAVTT_[L, RN, or RS][4]	Dedicated	Input	Analog power-supply pin for the transmit driver.
MGTVCCAUX_[L, RN, or RS][4]	Dedicated	Input	Auxiliary analog Quad PLL (QPLL) voltage supply for the transceivers.
MGTREFCLK[0 or 1] [P or N]	Dedicated	Input	Differential reference clock for the transceivers.
MGTAVTTRCAL_[L, RN, or RS][4]	Dedicated	N/A	Precision reference resistor pin for internal calibration termination.
MGTRREF_[L, RN, or RS][4]	Dedicated	Input	Precision reference resistor pin for internal calibration termination.

Notes:

1. See the DCI sections in *UltraScale Architecture SelectIO Resources User Guide* (UG571) for more information on the VRP pins.

2. All dedicated configuration pins are powered by V_{CCO_0}.

3. See the *UltraScale Architecture System Monitor User Guide* (UG580) for the default connections required to support on-chip monitoring.

4. L (left), RN (right-north), or RS (right-south) signify the GTH transceiver Quad power supply groups. The pins for each RN power supply group are tied to a respective power plane inside the device package but are not used.

Bank Diagram

The following is a diagram of the I/O banks, GTH banks, integrated PCIe block, system monitor, and configuration blocks. Bank diagram explanations follow the figure.

GTH Quad 128 X0Y16-X0Y19 [L] (RCAL)	HP I/O Bank 48	HP I/O Bank 68	PCIe X0Y2	GTH Quad 228 X1Y16-X1Y19 [RS]
GTH Quad 127 X0Y12-X0Y15 [L]	HP I/O Bank 47	HP I/O Bank 67	PCIe X0Y1	GTH Quad 227 X1Y12-X1Y15 [RS]
GTH Quad 126 X0Y8-X0Y11 [L]	HP I/O Bank 46 (partial)	HP I/O Bank 66	SYSMON Configuration	GTH Quad 226 X1Y8-X1Y11 [RS] (RCAL)
HP I/O Bank 25 (partial)	HP I/O Bank 45	HR I/O Bank 65	Configuration	GTH Quad 225 X1Y4-X1Y7 [RS]
HP I/O Bank 24	HP I/O Bank 44	HR I/O Bank 64	PCIe X0Y0	GTH Quad 224 X1Y0-X1Y3 [RS]

X22267-070120

Figure 13: **XQRKU060 Banks in CNA1509 Package**

GTH Columns

- One GTH Quad = four transceivers = four GTHE3 primitives.

- The XY coordinates shown in each Quad correspond to the transceiver channel number found in the pin names for that Quad.

- GTH transceiver banks belong to a power supply group. The power supply group is shown in brackets [ ], where L = left power supply group and RS = right-south power supply group.

- Quads labeled with RCAL specify the location of the RCAL master within the set of Quads belonging to each power supply group.

I/O Banks

- Each user I/O bank has a total of 52 I/Os where 48 can be used as differential (24 differential pairs) or single-ended I/Os. The remaining four function only as single-ended I/Os. All 52 pads of a bank are not always bonded out to pins.

- A limited number of banks have fewer than 52 SelectIO pins. These banks are labeled as partial.

- Adjacent to each bank is a physical layer (PHY) containing a CMT and other clock resources.

- Adjacent to each bank and PHY is a tile of logic resources that makes up a clock region.

- Banks are arranged in columns and separated into rows that are pitch-matched with the adjacent PHY, clock regions, and GTH blocks.

Clocking

- Each bank has four pairs of global clock (GC) inputs for four differential or four single-ended clock inputs. Single-ended clock inputs should be connected to the P-side of the differential pair.

- Clock signals are distributed through global buffers driving routing and distribution networks to reach any clock region, I/O, or transceiver.

- Global clock inputs can connect to an MMCM and two PLLs within the horizontally adjacent CMT.

Bank Locations of Dedicated and Multi-Function Pins

- Bank 0 contains the dedicated configuration pins. Bank 65 contains the multi-function configuration pins.

- The multi-function configuration bank 65 is shown adjacent to the configuration block. Special consideration must be taken when using bank 65 I/O under certain conditions. See the *State of I/Os During and After Configuration* and the *Special DCI Requirements in Some Banks* sections of *UltraScale Architecture SelectIO Resources User Guide* (UG571) for details.

- All dedicated configuration I/Os (bank 0) and HR I/Os are 1.5V to 3.3V capable.

SYSMON, Configuration, and PCIe Integrated Blocks

- Configuration: Configuration block.

- SYSMON/Configuration: Block shared between SYSMON and configuration.

- PCIe: Integrated block for PCIe.

ASCII Pinout File

The ASCII pinout file for the XQRKU060-CNA1509 is available at
https://www.xilinx.com/support/packagefiles/usapackages/xqrku060cna1509pkg.txt.

The ASCII pinout file includes:

- Device/package name (family-device-package) with date and time of creation
- Six columns containing data for each pin:
  a. Pin—Pin location on the package.
  b. Pin Name—The name of the assigned pin.
  c. Memory Byte Group—Memory byte group between 0 and 3 split into upper (U) and lower (L) halves. For more information on the memory byte group, see the *UltraScale Architecture FPGAs Memory IP Product Guide* (PG150).
  d. Bank—Bank number.
  e. I/O Type—CONFIG, HR, HP, or GTH depending on the I/O type. For more information on the I/O types, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571) and *UltraScale Architecture GTH Transceiver User Guide* (UG576).
  f. Super Logic Region—Not applicable (NA) for the XQRKU060. (This is for devices implemented with stacked silicon interconnect (SSI) technology with multiple super logic region (SLR) in the devices.)
- Total number of pins in the package.

Device Diagrams

The diagrams in this section show a top-view perspective of the package pinout. Figure 14 shows the location of each user I/O and GTH transceiver and the respective bank or GTH Quad. Figure 15 shows the location of every power pin, dedicated pin, and multi-function configuration pin in the package.
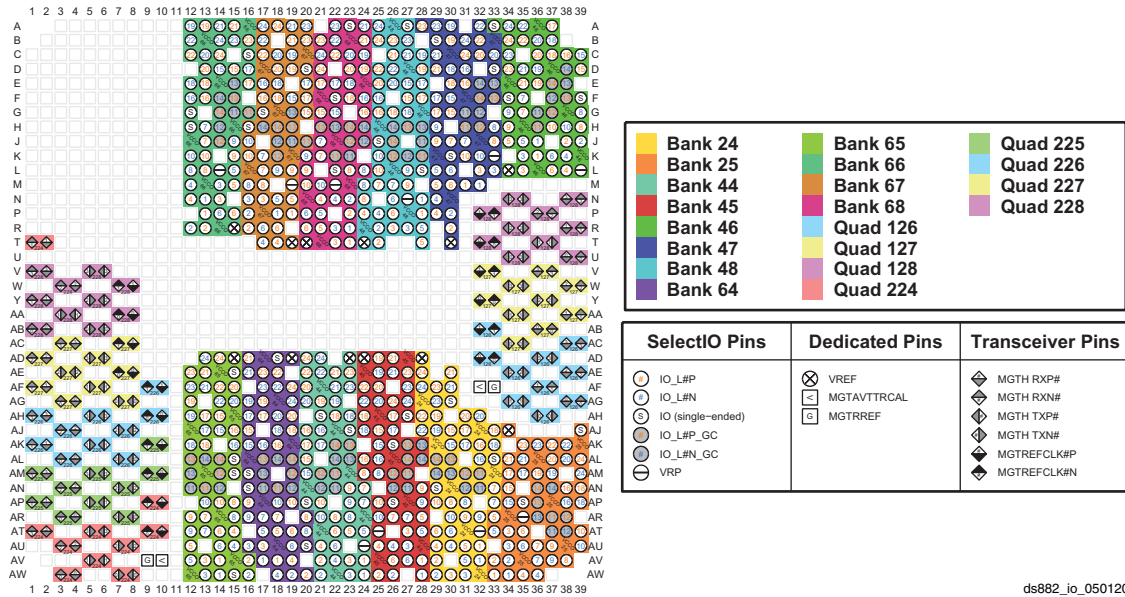
Figure 14: **I/O Bank Diagram**
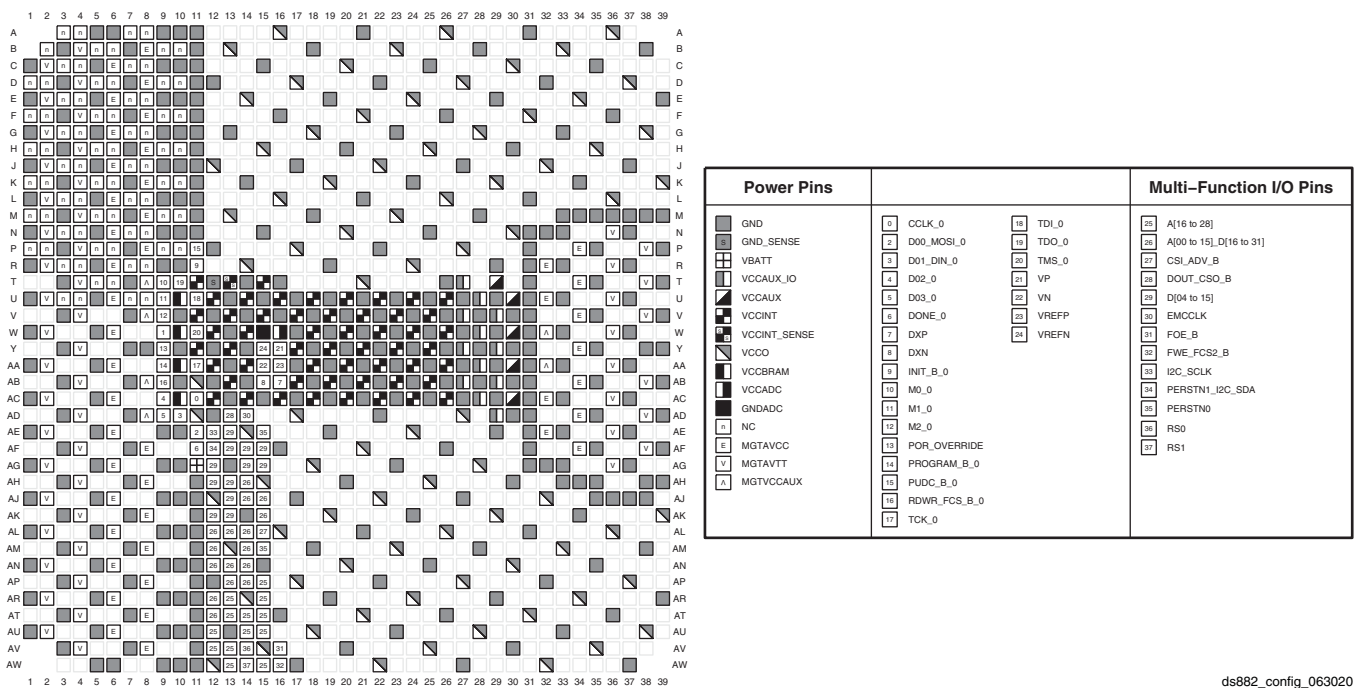
Figure 15: **Configuration/Power Diagram**

Mechanical Drawing

BOTTOM VIEW

TOP VIEW

PIN 1

PIN 1

39.50 MAX.
(LID)

39.50 MAX.
(LID)

LID

CHIP

SEATING PLANE

C0.25X45
(TYP.)

Øb
(1509X)

SOLDER COLUMN

C0.50X45
(3X)

SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	8.09	8.53	8.97	
A₁	2.05	2.20	2.35	
A₂	5.89	6.33	6.77	
D/E	40.00 BASIC			
D₁/E₁	38.00 BASIC			
e	1.00 BASIC			
Øb	0.41	0.51	0.61	
aaa			0.15	
ccc			0.35	
ddd			0.30	
eee			0.10	
M	39			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M−1994

2. SYMBOL 'M' IS THE COLUMN MATRIX SIZE

3. SOLDER COLUMNS ARE 80%Pb/20%Sn WITH COPPER RIBBON

ds882_cna1509_xqrku060_050520

Figure 16: **Package Dimensions for CNA1509**

IMPORTANT: *The material used for the CNA1509 package lid is nickel-plated Al-SiC, which is conductive and not connected to ground in the package. The Al-SiC lid should be externally connected to system ground to avoid collecting charges in space environments. When attaching heat spreader on the lid, use an electrically conductive adhesive (such as silver-filled epoxy).*

## Daisy Chain Package

The XQDAISY-CNA1509 part is a version of the CNA1509 package with daisy chain connectivity and the same package dimensions as the CNA1509.

ds882_mbs0417-2_050520

Figure 17: **XQDAISY-CNA1509 Daisy Chain Pattern (Bottom View)**

Netlist

DAISY CHAIN BALL PAIRS

NET No.	BALL PAIR
1	D1 E1
2	F1 G1
3	H1 J1
4	K1 L1
5	M1 N1
6	P1 R1
7	T1 U1
8	V1 W1
9	Y1 AA1
10	AB1 AC1
11	AD1 AE1
12	AF1 AG1
13	AH1 AJ1
14	AK1 AL1
15	AM1 AN1
16	AP1 AR1
17	AT1 AU1
18	C2 D2
19	E2 F2
20	G2 H2
21	J2 K2
22	L2 M2
23	N2 P2
24	R2 T2
25	U2 V2
26	W2 Y2
27	AA2 AB2
28	AC2 AD2
29	AE2 AF2
30	AG2 AH2
31	AJ2 AK2
32	AL2 AM2
33	AN2 AP2
34	AR2 AT2
35	AU2 AV2
36	A3 B3
37	B2 C1
38	D3 E3
39	F3 G3
40	H3 J3
41	K3 L3
42	M3 N3
43	P3 R3
44	T3 U3
45	V3 W3
46	Y3 AA3
47	AB3 AC3
48	AD3 AE3
49	AF3 AG3
50	AH3 AJ3
51	AK3 AL3
52	AM3 AN3
53	AP3 AR3
54	AT3 AU3
55	C3 C4
56	E4 F4
57	G4 H4
58	J4 K4
59	L4 M4
60	N4 P4
61	R4 T4
62	U4 V4
63	W4 Y4
64	AA4 AB4
65	AC4 AD4
66	AE4 AF4
67	AG4 AH4
68	AJ4 AK4
69	AL4 AM4
70	AN4 AP4
71	AR4 AT4
72	AV3 AV4
73	AW3 AW4
74	A4 A5
75	B4 B5
76	D4 D5
77	F5 G5
78	H5 J5
79	K5 L5
80	M5 N5
81	P5 R5
82	T5 U5
83	V5 W5
84	Y5 AA5
85	AB5 AC5
86	AD5 AE5
87	AF5 AG5
88	AH5 AJ5
89	AK5 AL5
90	AM5 AN5
91	AP5 AR5
92	AU4 AU5
93	C5 C6
94	E5 E6
95	G6 H6
96	J6 K6
97	L6 M6
98	N6 P6
99	R6 T6
100	U6 V6
101	W6 Y6
102	AA6 AB6
103	AC6 AD6
104	AE6 AF6
105	AG6 AH6
106	AJ6 AK6
107	AL6 AM6
108	AN6 AP6
109	AT5 AT6
110	AV5 AV6
111	AW5 AW6
112	A6 A7
113	B6 B7
114	D6 D7
115	F6 F7
116	H7 J7
117	K7 L7
118	M7 N7
119	P7 R7
120	T7 U7
121	V7 W7
122	Y7 AA7
123	AB7 AC7
124	AD7 AE7
125	AF7 AG7
126	AH7 AJ7
127	AK7 AL7
128	AM7 AN7
129	AR6 AR7
130	AU6 AU7
131	C7 C8
132	E7 E8
133	G7 G8
134	J8 K8
135	L8 M8
136	N8 P8
137	R8 T8
138	U8 V8
139	W8 Y8
140	AA8 AB8
141	AC8 AD8
142	AE8 AF8
143	AG8 AH8
144	AJ8 AK8
145	AL8 AM8
146	AP7 AP8
147	AT7 AT8
148	AV7 AV8
149	AW7 AW8
150	A8 A9
151	B8 B9
152	D8 D9
153	F8 F9
154	H8 H9
155	K9 L9
156	M9 N9
157	P9 R9
158	T9 U9
159	V9 W9
160	Y9 AA9
161	AB9 AC9
162	AD9 AE9
163	AF9 AG9
164	AH9 AJ9
165	AK9 AL9
166	AN8 AN9
167	AR8 AR9
168	AU8 AU9
169	C9 C10
170	E9 E10
171	G9 G10
172	J9 J10
173	L10 M10
174	N10 P10
175	R10 T10
176	U10 V10
177	W10 Y10
178	AA10 AB10
179	AC10 AD10
180	AE10 AF10
181	AG10 AH10
182	AJ10 AK10
183	AM9 AM10
184	AP9 AP10
185	AT9 AT10
186	AV9 AV10
187	AW9 AW10
188	A10 A11
189	B10 B11
190	D10 D11
191	F10 F11
192	H10 H11
193	K10 K11
194	M11 N11
195	P11 R11
196	T11 U11
197	V11 W11
198	Y11 AA11
199	AB11 AC11
200	AD11 AE11
201	AF11 AG11
202	AH11 AJ11
203	AL10 AL11
204	AN10 AN11
205	AR10 AR11
206	AU10 AU11
207	C11 C12
208	E11 E12
209	G11 G12
210	J11 J12
211	L11 L12
212	N12 P12
213	R12 T12
214	U12 V12
215	W12 Y12
216	AA12 AB12
217	AC12 AD12
218	AE12 AF12
219	AG12 AH12
220	AK11 AK12
221	AM11 AM12
222	AP11 AP12
223	AT11 AT12
224	AV11 AV12
225	AW11 AW12
226	A12 A13
227	B12 B13
228	D12 D13
229	F12 F13
230	H12 H13
231	K12 K13
232	M12 M13
233	P13 R13
234	T13 U13
235	V13 W13
236	Y13 AA13
237	AB13 AC13
238	AD13 AE13
239	AF13 AG13
240	AJ12 AJ13
241	AL12 AL13
242	AN12 AN13
243	AR12 AR13
244	AU12 AU13
245	C13 C14
246	E13 E14
247	G13 G14
248	J13 J14
249	L13 L14
250	N13 N14
251	R14 T14
252	U14 V14
253	W14 Y14
254	AA14 AB14
255	AC14 AD14
256	AE14 AF14
257	AH13 AH14
258	AK13 AK14
259	AM13 AM14
260	AP13 AP14
261	AT13 AT14
262	AV13 AV14
263	AW13 AW14
264	A14 A15
265	B14 B15
266	D14 D15
267	F14 F15
268	H14 H15
269	K14 K15
270	M14 M15
271	P14 P15
272	T15 U15
273	V15 W15
274	Y15 AA15
275	AB15 AC15
276	AD15 AE15
277	AG14 AG15
278	AJ14 AJ15
279	AL14 AL15
280	AN14 AN15
281	AR14 AR15
282	AU14 AU15
283	C15 C16
284	E15 E16
285	G15 G16
286	J15 J16
287	L15 L16
288	N15 N16
289	R15 R16
290	U16 V16
291	W16 Y16
292	AA16 AB16
293	AC16 AD16
294	AF15 AF16
295	AH15 AH16
296	AK15 AK16
297	AM15 AM16
298	AP15 AP16
299	AT15 AT16
300	AV15 AV16
301	AW15 AW16
302	A16 A17
303	B16 B17
304	D16 D17
305	F16 F17
306	H16 H17
307	K16 K17
308	M16 M17
309	P16 P17
310	T16 T17
311	V17 W17
312	Y17 AA17
313	AB17 AC17
314	AE16 AE17
315	AG16 AG17
316	AJ16 AJ17
317	AL16 AL17
318	AN16 AN17
319	AR16 AR17
320	AU16 AU17
321	C17 C18
322	E17 E18
323	G17 G18
324	J17 J18
325	L17 L18
326	N17 N18
327	R17 R18
328	U17 U18
329	W18 Y18
330	AA18 AB18
331	AD17 AD18
332	AF17 AF18
333	AH17 AH18
334	AK17 AK18
335	AM17 AM18
336	AP17 AP18
337	AT17 AT18
338	AV17 AV18
339	AW17 AW18
340	A18 A19
341	B18 B19
342	D18 D19
343	F18 F19
344	H18 H19
345	K18 K19
346	M18 M19
347	P18 P19
348	T18 T19
349	V18 V19
350	Y19 AA19
351	AC18 AC19
352	AE18 AE19
353	AG18 AG19
354	AJ18 AJ19
355	AL18 AL19
356	AN18 AN19
357	AR18 AR19
358	AU18 AU19
359	C19 C20
360	E19 E20
361	G19 G20
362	J19 J20
363	L19 L20
364	N19 N20
365	R19 R20
366	U19 U20
367	V19 V20
368	AB19 AB20
369	AD19 AD20
370	AF19 AF20
371	AH19 AH20
372	AK19 AK20
373	AM19 AM20
374	AP19 AP20
375	AT19 AT20
376	AV19 AV20
377	AW19 AW20
378	A20 A21
379	B20 B21
380	D20 D21
381	F20 F21
382	H20 H21
383	K20 K21
384	M20 M21
385	P20 P21
386	T20 T21
387	V20 V21
388	W21 Y21
389	AA20 AA21
390	AC20 AC21
391	AE20 AE21
392	AG20 AG21
393	AJ20 AJ21
394	AL20 AL21
395	AN20 AN21
396	AR20 AR21
397	AU20 AU21
398	C21 C22
399	E21 E22
400	G21 G22
401	J21 J22
402	L21 L22
403	N21 N22
404	R21 R22
405	U21 U22
406	V22 W22
407	Y22 AA22
408	AB21 AB22
409	AD21 AD22
410	AF21 AF22
411	AH21 AH22
412	AK21 AK22
413	AM21 AM22
414	AP21 AP22
415	AT21 AT22
416	AV21 AV22
417	AW21 AW22
418	A22 A23
419	B22 B23
420	D22 D23
421	F22 F23
422	H22 H23
423	K22 K23
424	M22 M23
425	P22 P23
426	T22 T23
427	U23 V23
428	W23 Y23
429	AA23 AB23
430	AC22 AC23
431	AE22 AE23
432	AG22 AG23
433	AJ22 AJ23
434	AL22 AL23
435	AN22 AN23
436	AR22 AR23
437	AU22 AU23
438	C23 C24
439	E23 E24
440	G23 G24
441	J23 J24
442	L23 L24
443	N23 N24
444	R23 R24
445	T24 U24
446	V24 W24
447	Y24 AA24
448	AB24 AC24
449	AD23 AD24
450	AF23 AF24
451	AH23 AH24
452	AK23 AK24
453	AM23 AM24
454	AP23 AP24
455	AT23 AT24
456	AV23 AV24
457	AW23 AW24
458	A24 A25
459	B24 B25
460	D24 D25
461	F24 F25
462	H24 H25
463	K24 K25
464	M24 M25
465	P24 P25
466	R25 T25
467	U25 V25
468	W25 Y25
469	AA25 AB25
470	AC25 AD25
471	AE24 AE25
472	AG24 AG25
473	AJ24 AJ25
474	AL24 AL25
475	AN24 AN25
476	AR24 AR25
477	AU24 AU25
478	C25 C26
479	E25 E26
480	G25 G26
481	J25 J26
482	L25 L26
483	N25 N26
484	P26 R26
485	T26 U26
486	V26 W26
487	Y26 AA26
488	AB26 AC26
489	AD26 AE26
490	AF25 AF26
491	AH25 AH26
492	AK25 AK26
493	AM25 AM26
494	AP25 AP26
495	AT25 AT26
496	AV25 AV26
497	AW25 AW26
498	A26 A27
499	B26 B27
500	D26 D27
501	F26 F27
502	H26 H27
503	K26 K27
504	M26 M27
505	N27 P27
506	R27 T27
507	U27 V27
508	W27 Y27
509	AA27 AB27
510	AC27 AD27
511	AE27 AF27
512	AG26 AG27
513	AJ26 AJ27
514	AL26 AL27
515	AN26 AN27
516	AR26 AR27
517	C27 C28
518	E27 E28
519	G27 G28
520	J27 J28
521	L27 L28
522	M28 N28
523	R28 T28
524	P28 R28
525	T28 U28
526	V28 W28
527	Y28 AA28
528	AB28 AC28
529	AD28 AE28
530	AF28 AG28
531	AH27 AH28
532	AK27 AK28
533	AM27 AM28
534	AP27 AP28
535	AT27 AT28
536	AV27 AV28
537	AW27 AW28
538	A28 A29
539	B28 B29
540	D28 D29
541	F28 F29
542	H28 H29
543	K28 K29
544	L29 M29
545	N29 P29
546	R29 T29
547	U29 V29
548	W29 Y29
549	AA29 AB29
550	AC29 AD29
551	AE29 AF29
552	AG29 AH29
553	AJ28 AJ29
554	AL28 AL29
555	AN28 AN29
556	AR28 AR29
557	AU28 AU29
558	C29 C30
559	E29 E30
560	G29 G30
561	J29 J30
562	K30 L30
563	M30 N30
564	P30 R30
565	T30 U30
566	V30 W30
567	Y30 AA30
568	AB30 AC30
569	AD30 AE30
570	AF30 AG30
571	AH30 AJ30
572	AK29 AK30
573	AM29 AM30
574	AP29 AP30
575	AT29 AT30
576	AV29 AV30
577	AW29 AW30
578	A30 A31
579	B30 B31
580	D30 D31
581	F30 F31
582	H30 H31
583	J31 K31
584	L31 M31
585	N31 P31
586	R31 T31
587	U31 V31
588	W31 Y31
589	AA31 AB31
590	AC31 AD31
591	AE31 AF31
592	AG31 AH31
593	AJ31 AK31
594	AL30 AL31
595	AN30 AN31
596	AR30 AR31
597	AU30 AU31
598	C31 C32
599	E31 E32
600	G31 G32
601	H32 J32
602	K32 L32
603	M32 N32
604	P32 R32
605	T32 U32
606	V32 W32
607	Y32 AA32
608	AB32 AC32
609	AD32 AE32
610	AF32 AG32
611	AH32 AJ32
612	AK32 AL32
613	AM31 AM32
614	AP31 AP32
615	AT31 AT32
616	AV31 AV32
617	AW31 AW32
618	A32 A33
619	B32 B33
620	D32 D33
621	F32 F33
622	G33 H33
623	J33 K33
624	L33 M33
625	N33 P33
626	R33 T33
627	U33 V33
628	W33 Y33
629	AA33 AB33
630	AC33 AD33
631	AE33 AF33
632	AG33 AH33
633	AJ33 AK33
634	AL33 AM33
635	AN32 AN33
636	AR32 AR33
637	AU32 AU33
638	C33 C34
639	E33 E34
640	F34 G34
641	H34 J34
642	K34 L34
643	M34 N34
644	P34 R34
645	T34 U34
646	V34 W34
647	Y34 AA34
648	AB34 AC34
649	AD34 AE34
650	AF34 AG34
651	AH34 AJ34
652	AK34 AL34
653	AM34 AN34
654	AP33 AP34
655	AT33 AT34
656	AV33 AV34
657	AW33 AW34
658	A34 A35
659	B34 B35
660	D34 D35
661	E35 F35
662	G35 H35
663	J35 K35
664	L35 M35
665	N35 P35
666	R35 T35
667	U35 V35
668	W35 Y35
669	AA35 AB35
670	AC35 AD35
671	AE35 AF35
672	AG35 AH35
673	AJ35 AK35
674	AL35 AM35
675	AN35 AP35
676	AR34 AR35
677	AU34 AU35
678	C35 C36
679	D36 E36
680	F36 G36
681	H36 J36
682	K36 L36
683	M36 N36
684	P36 R36
685	T36 U36
686	V36 W36
687	Y36 AA36
688	AB36 AC36
689	AD36 AE36
690	AF36 AG36
691	AH36 AJ36
692	AK36 AL36
693	AM36 AN36
694	AP36 AR36
695	AT35 AT36
696	AV35 AV36
697	AW35 AW36
698	A36 A37
699	B36 B37
700	C37 D37
701	E37 F37
702	G37 H37
703	J37 K37
704	L37 M37
705	N37 P37
706	R37 T37
707	U37 V37
708	W37 Y37
709	AA37 AB37
710	AC37 AD37
711	AE37 AF37
712	AG37 AH37
713	AJ37 AK37
714	AL37 AM37
715	AN37 AP37
716	AR37 AT37
717	AU36 AU37
718	B38 C38
719	D38 E38
720	F38 G38
721	H38 J38
722	K38 L38
723	M38 N38
724	P38 R38
725	T38 U38
726	V38 W38
727	Y38 AA38
728	AB38 AC38
729	AD38 AE38
730	AF38 AG38
731	AH38 AJ38
732	AK38 AL38
733	AM38 AN38
734	AP38 AR38
735	AT38 AU38
736	AV37 AV38
737	C39 D39
738	E39 F39
739	G39 H39
740	J39 K39
741	L39 M39
742	N39 P39
743	R39 T39
744	U39 V39
745	W39 Y39
746	AA39 AB39
747	AC39 AD39
748	AE39 AF39
749	AG39 AH39
750	AJ39 AK39
751	AL39 AM39
752	AN39 AP39
753	AR39 AT39
754	AU39 AV38
755	Y20 Not paired

ds882_mbs0417-3_050520

Figure 18: **XQDAISY-CNA1509 Daisy Chain Netlist**

Package Markings

A device-specific bar code is marked on each device. Refer to the bar code for further information.

Figure 19: **Package Marking**

Packing and Shipping

Table 85: **Standard Device Counts per Tray and Box**

Maximum Number of Devices Per Tray	Maximum Number of Units In One Internal Box
1	4

Guidelines for Xilinx CN Package Handling and Assembly

The XQRKU060 FPGA is packaged in a CNA1509 package. Ceramic flip-chip (CN) packages are ceramic column grid array (CCGA) packages, which are robust and reliable. These packages use high-lead (Pb) solder columns (instead of solder balls) to create a higher standoff and more flexible interconnection, which achieves a significant increase in reliability. A lid covers the die and ceramic chip capacitors. The columns are attached to the packages at suppliers after being fully screened to MIL-PRF-38535 requirements. The devices are packed in shipping trays, with one unit per tray to avoid unnecessary handling.

Like BGA packages, all of the interconnections cannot be inspected after board mount, so care must be taken to implement good handling and process controls. With their higher standoff height, columns are more susceptible to handling damage than solder balls.

This section contains guidelines to properly unpack, handle, inspect, and assemble Xilinx CN packages. The design and process requirements should be compatible with standard surface mount technology (SMT) equipment and with total assembly requirements as driven by other components on the product.

Product Unpacking

Xilinx recommends that extreme care be taken when removing the parts from the trays. Special care must be taken when unpacking CN parts.

1. Handle the box with extreme care.

2. After the dry pack bag is opened, remove the banded tray from the bag, carefully hold positive downward pressure on top of the tray while cutting the heat-sealed black plastic bands.

3. Check for tray orientation. All trays have a corner bevel and must have the correct orientation.

4. Check for tray separation. Trays should be slightly interlocked with no product exposed.

5. If the product is not to be used immediately, keep the tray banded and sealed in a dry pack bag with desiccator until needed.

Proceed with the following steps when ready to assemble hardware:

1. Carefully cut bands holding trays together.

    Caution! Be careful when cutting the sealed bands. After the sealed bands on the trays are cut, the tray can shift, possibly damaging or bending columns.

2. Gently place the unbanded tray on a firm surface.

    Caution! Do not apply a jarring downward force when placing the tray on the surface.

3. After the product tray has been unboxed and the bands cut, fasten the product trays securely at all areas with rubber bands to keep the trays interlocked and the product secured.

4. Foam pads are present between each tray to protect the product. These pads should be removed just before the product is to be placed in automated or manual placement tools.

5. Carefully remove the package inside each tray by removing each in a vertical upward motion. Remove the parts from the tray at a 90° angle to prevent columns from being bent. It is best to use an automatic pick and place machine to remove the parts.

    Caution! Do not use a rolling or angular motion to remove the package. Doing so might bend columns or cause damage.

6. If packing concerns are identified, hold all packing materials with the product and notify the proper personnel for corrective action.

Product Handling and Inspection

All Xilinx CCGA package die are flip-chip and bumped with solder bumps. The package substrate is ceramic. The bumped die is flipped and reflowed to the ceramic substrate at assembly. A moisture resistant epoxy underfill encapsulates the bumps. The columns are high lead solid solder columns. The package lid is attached with a thermal epoxy adhesive (see Figure 20).
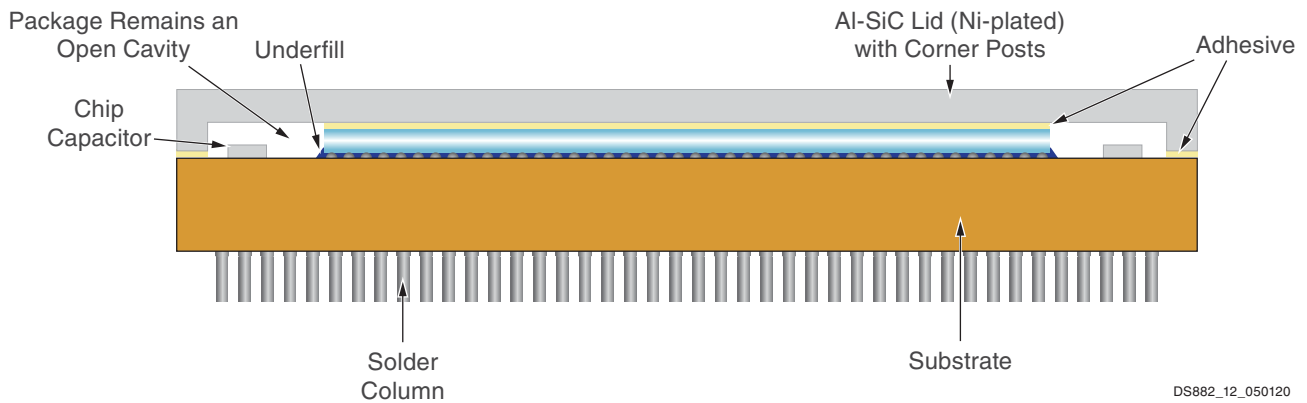
Figure 20: **CN Package Construction**

Any inspection of parts should be made while keeping the part in its shipping tray because the columns might be damaged if the part is manually handled or removed from the tray. Careful handling of the parts during board mount is recommended to ensure no damage to the chip capacitors or columns occurs.

Board-Level Mounting

Xilinx recommends the customer perform a visual inspection at different steps of the process to ensure that no damage has been induced to the package, columns, board mount, or decoupling chip capacitors due to mishandling issues. Parts should not be removed from the trays until they are mounted to the board.

Note: The design and process requirements should be compatible with standard SMT equipment and with total assembly requirements as driven by other components on the product.

Component Placement

Xilinx device packages must be placed accurately according to their geometry outline. Positioning packages manually via hand mounting is not recommended.

Typical component placement accuracies of ±50 µm can be achieved using standard pick and placement machine equipment with vision system. The PCB and the components are optically checked and measured and the components are placed on the PCB in specific programmed positions based on the PCB CAD information. The pick and placement machine vision system detects the fiducials on the PCB immediately prior to mounting the FPGA. Recognition of the packages is performed by the vision system to ensure correct centering of the FPGA placement on the PCB pad array.

The following setup conditions are important for the pick and placement systems:

* The pick and placement nozzle type should be sized to the dimensions of the Xilinx device. The nozzle needs to firmly hold the device package during the pick and placement stage. The appropriate nozzle type for the device package can be chosen from the manual provided by the pick and placement equipment company.

* To ensure the proper identification of the device package by the vision system, a suitable lighting system and the correct choice of the features of the measuring method are essential. The most

suitable settings can be chosen from the manual provided by the pick and placement equipment company.

- To avoid solder bridging or solder smear, ensure the proper placement force of the device package during placement on the PCB. Excessive placement force can lead to excess solder paste and cause solder bridging. However, a slight placement force can lead to insufficient solder paste contact between the device package solder balls and the solder paste, causing solder defects including open solder joints or badly centered packages.

Soldering Guidelines

Like BGA packages, the CNA1509 package board-level assembly process involves screen printing, solder reflow, and post reflow washing. To implement and control the production of surface-mount assemblies, the dynamics of the solder reflow process and how each element of the process is related to the end result must be thoroughly understood.

RECOMMENDED: *Qualify the PCB assembly process using package samples.*

The primary phases of the reflow process are:

- Melting the particles in the solder paste

- Wetting the surfaces to be joined

- Solidifying the solder into a strong metallurgical bond

Solder Paste Guidelines

Solder paste consists of solder alloy and a flux system. A typical solder paste composition by volume is split between about 50% alloy and 50% flux. The metal load mass (solder alloy powder) is around 90%, with the remaining 10% mass a flux system. The primary purpose of the flux system is to remove the contaminations from the solder joints during the soldering process. The capability of removing contaminations is determined by the activation level of the type of solder paste. A no-clean solder paste is preferred to eliminate any risk of improper cleaning that could leave active residue beneath the device and other bottom termination components (BTCs). The paste must be suitable for printing the solder stencil aperture dimensions. Type 4 paste is recommended for better paste release performance. When using a solder paste, you must adhere to the handling recommendations of the paste manufacturer.

Solder Stencil

Solder paste is applied to PCB metal pads by screen printing. The volume of the printed solder paste is determined by the stencil aperture and the stencil thickness. In most cases, the thickness of a stencil must be matched to the needs of all components on the PCB. Stencil apertures should be a circular shape. To ensure a uniform and high-solder paste transfer to the PCB, laser-cut (mostly made from stainless steel) with nickel blanking is preferred. A uniform stencil aperture opening of 19.7 mils round is recommended for packages smaller than 45 mm x 45 mm, matching the PCB pad size for a 1 mm pitch package.

Solder Reflow Guidelines

The infrared reflow (IR) process is strongly dependent on equipment and loading. Components might overheat due to lack of thermal constraints. Unbalanced loading can lead to significant temperature variation on the board. These guidelines are intended to assist users in avoiding damage to the components; the actual profile should be determined by those using these guidelines. For complete information on package moisture/reflow classification and package reflow conditions, refer to the latest Joint IPC/JEDEC standard J-STD-020. For multiple devices in a single board and because of surrounding component differences, check all device sites for varying temperatures.

Xilinx recommends using the reflow profile recommended by the solder paste supplier. For the cleaning process, Xilinx recommends caustic solvents *not be used* during the cleaning cycle. Xilinx recommends using deionized water rinse and bake. The recommended maximum reflow temperature is 220°C. However, a maximum peak temperature of 235°C can be acceptable. Due to the large CCGA package size and weight, make sure the reflow profile (temperature vs. time) is properly adjusted to avoid cold solder joints. Mechanical samples (XQDAISY-CNA1509) are available for purchase to develop proper reflow profiles.

For solder joint test method (X-rays, X-ray CT, and fiberscope) of inline or failure detection in evaluation test (crack, void, and alignment), transmission X-ray can detect solder bridging, and X-ray laminography can detect solder joint opens.

Rework

Xilinx does not recommend any rework or staking of the CN package.

Typical Conditions for IR Reflow Soldering of Ceramic Column Grid Array Packages

Figure 21 shows typical conditions for solder reflow processing of Sn/Pb soldering using IR/convection for ceramic column grid array packages (CN). Both IR and convection furnaces are used for assembly. The moisture sensitivity of the surface mount device (SMD) must be verified prior to surface-mount flow.
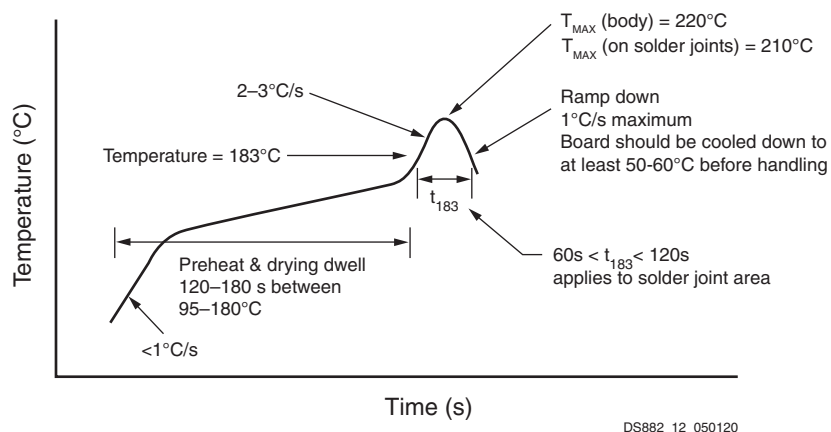

Figure 21: **CN Package Soldering Guidelines**

Notes for Figure 21:

1. Maximum temperature range = 220°C (body). Minimum temperature range = 205°C (solder joints).

2. Preheat dwell 95–180°C for 120–180 seconds.

3. IR reflow must be performed on dry packages.

4. Board should be cooled down to at least 50-60ºC before handling.

5. Reflow atmosphere of nitrogen is recommended.

6. These parameters are guidelines only. Always use the best manufacturing practices.

For sophisticated boards with a substantial mix of large and small components, it is critical to minimize the ∆T across the board (<10°C) to minimize board warpage and thus, attain higher assembly yields. Minimizing the ∆T is accomplished by using a slower rate in the warm-up and preheating stages.

It is also important to minimize the temperature gradient on the component between the top surface and bottom side, especially during the cooling down phase. The key is to optimize cooling while maintaining a minimal temperature differential between the top surface of the package and the solder joint area. The temperature differential between the top surface of the component and the solder balls should be maintained at less than 7°C during the critical region of the cooling phase of the reflow process. This critical region is in the part of the cooling phase where the balls are not completely solidified to the board yet, usually between the 200°C–217°C range. To efficiently cool the parts, divide the cooling section into multiple zones with each zone operating at different temperatures.

The optimal profile must take into account the solder paste/flux used, the size of the board, the density of the components on the board, and the mix between large components and smaller, lighter components. Profiles should be established for all new board designs using thermocouples at multiple locations on the component. In addition, if there is a mixture of devices on the board, the profile should be checked at various locations on the board. Ensure that the minimum reflow temperature is reached to reflow the larger components and at the same time, the temperature does not exceed the threshold temperature that might damage the smaller, heat sensitive components.

Post Reflow/Cleaning/Washing

A no-clean or a water-soluble solder paste is recommended. If cleaning is required, it is recommended to use a water-soluble paste and then wash with deionized water in a washer. Baking after the water wash is recommended to prevent fluid accumulation. Cleaning surfactants or solvents are not recommended because some cleaning solutions might contain chemicals that can compromise the lid adhesive, thermal compound, or components inside the package. If cleaning surfactants or solvents are used, follow the manufacturer's guidelines for cleaning and ensure that no chemical residue remains on the device. These are guidelines only. Always use manufacturing best practices.

Strain Gauge Measurement

Strain gauge measurements are recommended to be done at each process step that has the potential to cause excessive board flexing leading to solder joint cracking. Assembly processes where strain gauge measurements are recommended include:

•   PCB router (during PCB loading/unloading into fixture and during the routing process)

•   PTH solder assembly during top-catch loading/unloading

- Press fit assembly during press base and tooling loading/unloading and during machine pressing process
- DIMM memory (during PCB loading/unloading and during insertion/removal of DIMM)
- Heat-sink assembly process (during PCB loading/unloading and during entire screw assembly process)
- X-ray fixture (during PCBA loading/unloading)

Strain gauge measurements should be in the range of ±500 µstrain. Dye and pry analysis is required to confirm if the measured strain causes solder joint cracking. It is recommended to conduct dye and pry analysis for any strain reading greater than 500 µstrain.

Conformal Coating

Xilinx does not have information regarding the reliability of flip-chip column grid array packages on a board after exposure to any specific conformal coating process. Therefore, any process using conformal coating should be qualified for the specific use case to cover the materials and process steps.

Note: Xilinx does not recommend using Toluene-based conformal coatings because they can weaken the lid adhesive used in Xilinx packages.

Edge Bonding

Edge bonding is not recommended for the CNA1509 package.

Thermal Specifications

UltraScale devices are implemented in the 20 nm process technology. Unlike features in an ASIC or a microprocessor, the combination of FPGA features used in a user application is not known to the component supplier. Therefore, it remains a challenge for Xilinx to predict the power requirements of a given FPGA when it leaves the factory. Accurate estimates are obtained when the board design takes shape. For this purpose, Xilinx offers and supports a suite of integrated device power analysis tools to help users quickly and accurately estimate their design power requirements. UltraScale devices are supported similarly to previous FPGA products. The variability of design power requirements makes it difficult to apply fixed thermal solutions to fit all users. Therefore, Xilinx devices do not come with preset thermal solutions. Your design operating conditions dictate the appropriate solution.

Thermal Resistance Data

The XQRKU060 FPGA is offered exclusively in the CNA1509 package for high thermal cycle reliability. Table 86 shows the thermal resistance data for the XQRKU060-CNA1509 device. The data includes junction-to-ambient in still air, junction-to-case, and junction-to-board data based on standard JEDEC four-layer measurements.

IMPORTANT: *The data in Table 86 is for device/package comparison purposes only. Attempts to recreate this data are only valid using the transient 2-phase measurement techniques outlined in JESD51-14.*

Table 86: **Thermal Resistance Data for XQRKU060-CNA1509**

Package Body Size (mm)	θ$_{JB}$ (°C/W)[2]	θ$_{JC}$ (°C/W)[2]	θ$_{JA}$ (°C/W)[2]	θ$_{JA-Effective}$ (°C/W)[1][2]		
				@250 LFM	**@500 LFM**	**@750 LFM**
40 x 40	2.08	0.16	6.9	4.3	3.6	3.5

Notes:

1. All θ$_{JA-Effective}$ values assume no heat sink and include thermal dissipation through a standard JEDEC four-layer board. The Xilinx power estimation tools (Vivado Power Analysis and Xilinx Power Estimator), which require detailed board dimensions and layer counts, are useful for deriving more precise θ$_{JA-Effective}$ values.
2. This data is for device/package comparison purposes only. Attempts to recreate this data are only valid using the transient 2-phase measurement techniques outlined in JESD51-14.

Support for Thermal Models

Table 86 provides the traditional thermal resistance data for the XQRKU060-CNA1509 device. These resistances are measured using a prescribed JEDEC standard that might not necessarily reflect your actual board conditions and environment. The quoted θ$_{JA}$ and θ$_{JC}$ numbers are environmentally dependent, and JEDEC has traditionally recommended that these be used with that awareness. For more accurate junction temperature prediction, these might not be enough, and a system-level thermal simulation might be required.

Though Xilinx continues to support these figure of merit data, a boundary conditions independent thermal resistor network (Delphi) model is offered. This compact model seeks to capture the thermal behavior of the package more accurately at predetermined critical points (junction, case, top, and leads) with the reduced set of nodes as illustrated in Figure 22.
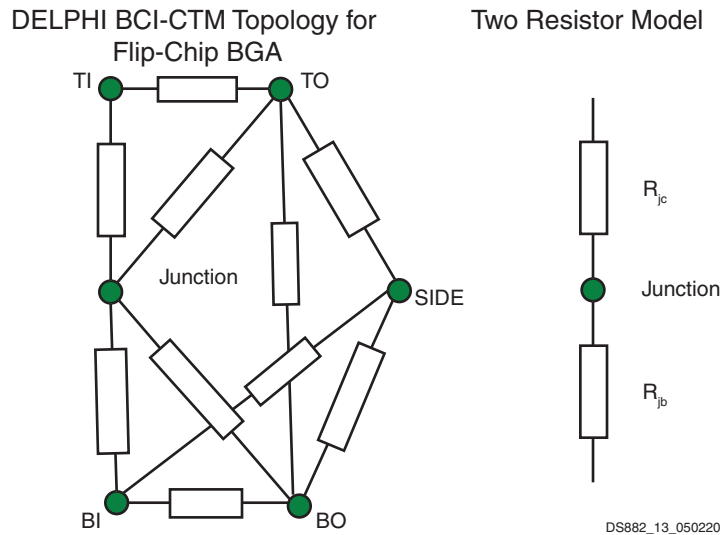

Figure 22: **Thermal Model Topologies**

Unlike a full 3D model, this model is computationally efficient and works well in an integrated system simulation environment.

RECOMMENDED: *Xilinx recommends use of the Delphi thermal model during thermal modeling of a package. The Delphi thermal model includes consideration of the thermal interface material parameters and the manufacture variation on the thermal solution. Examples of manufacture variations include the tolerance in airflow from a fan, the*

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tolerance on performance of the heat pipe and vapor chamber, and the manufacture variation of the attachment of fins to the heat-sink base and the flatness of the surface.

Package Coefficients

Table 87: **CNA1509 Package Coefficients**

Package Component	Description	Value
Substrate	Alumina (Ceramic)	–
	Coefficient of Thermal Expansion	7.1 ppm/°C
	Thermal Conductivity	14 W/m°C
	Dielectric Constant	9.8 at 1 MHz 9.5 at 10 GHZ
	Young's Modulus	310 GPa
Lid	Aluminum Silicon Carbide (Al-SiC-9)	–
	Coefficient of Thermal Expansion	8.75 ppm/°C
	Thermal Conductivity	190 W/m°C
	Young's Modulus	188 GPa

Refer to the *Thermal Management Strategy*, *Heat Sink Guidelines for Bare-die Flip-Chip Packages*, and *Mechanical and Thermal Design Guidelines for Lidless Flip-chip Packages* chapters of *UltraScale and UltraScale+ FPGAs Packaging and Pinouts Product Specification* (UG575) for thermal management and heat sink guidelines.

IMPORTANT: *The column grid array (CNA1509) package requires a different applied pressure from heat sink to the package via thermal interface materials than the ball grid array (BGA) packages described in UltraScale and UltraScale+ FPGAs Packaging and Pinouts Product Specification (UG575). The applied pressure on the CNA1509 package must be in the range of 10 to 25 psi for optimum performance of the thermal interface material (TIM) between the package and the heat sink. Thermocouples should not be present between the package and the heat sink, because their presence will degrade the thermal contact and result in incorrect thermal measurements. The best practice is to select the appropriate pressure (in the 10 to 25 psi range) for the optimum thermal contact performance between the package and the thermal system solution, and the mechanical integrity of the package (with the thermal solution to pass all mechanical stress and vibration qualification tests). The material used for the CNA1509 package lid is nickel-plated Al-SiC, which is conductive and not connected to ground in the package. The Al-SiC lid should be externally connected to system ground to avoid collecting charges in space environments. When attaching heat spreader on the lid, use an electrically conductive adhesive (such as silver-filled epoxy).*

Reliability

For the 20 nm UltraScale device reliability qualifications and soft error rates, refer to the *Device Reliability Report* (UG116). This report contains reliability qualifications of devices, wafer processes, and packages.

Ordering Information

The ordering information is shown in Figure 23.
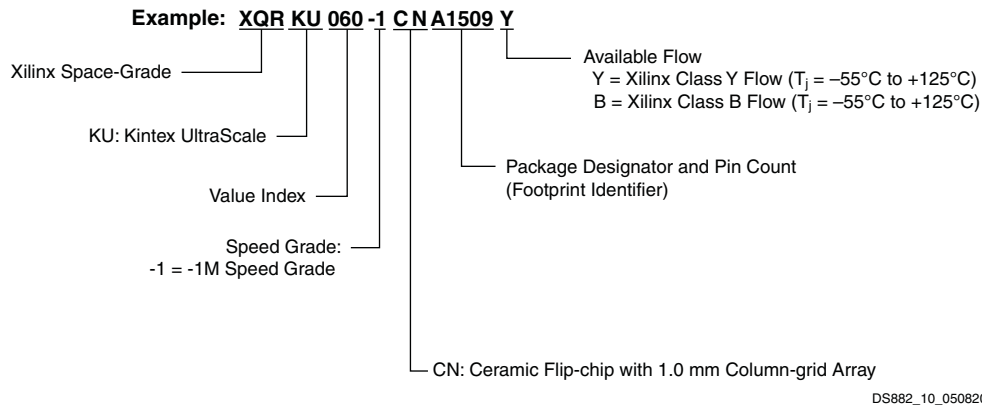
Figure 23: **Radiation Tolerant Kintex UltraScale XQRKU060 FPGA Ordering Information**

Note: For the XQRKU060-1CNA1509 parts, select the `xqrku060-cna1509-1M-m` part in the Vivado design tools.

The CNA1509 daisy chain package part number is XQDAISY-CNA1509. Xilinx class B and class Y manufacturing flows are compliant with MIL-PRF-38535 and are shown in Table 88.

Table 88: **Xilinx Class B and Class Y Manufacturing Flows**

Flow	Xilinx Class B	Xilinx Class Y
Wafer Sort	✓	✓
Bumping	✓	✓
Assembly (per MIL-STD-883)	✓	✓
Bond Pull (Extended Pull Test)	N/A	N/A
Die Shear (1 unit/lot)	✓	✓
Die Visual Inspection	✓ (cond B)	✓ (cond A)
Pre-Cap Source Inspections (cond A)	N/A	✓
Serialization	✓	✓
Temperature Cycling (cycles)	100	100
Constant Acceleration	✓	✓
PIND	N/A	N/A
Seal (Fine/Gross Leak Test)	N/A	N/A
X-Ray	N/A	N/A
Room Test	✓	✓
Pre Burn-in Electrical Test	@25°C, 128°C, −55°C	@25°C, 128°C, −55°C
Dynamic Burn-in (@ 125°C)	160 Hrs	240 Hrs
Post Burn-in Test @ 25°C with Read & Record	N/A	✓
Static Burn-in (144 hours @ 125°C)	N/A	✓
Group A Post Burn-in Test @ 25°C with Read & Record	✓	✓

Table 88: **Xilinx Class B and Class Y Manufacturing Flows** *(Cont'd)*

Flow	Xilinx Class B	Xilinx Class Y
Group A Final Test @ −55°C with Read & Record	✓	✓
Group A Final Test @ 128°C with Read & Record	✓	✓
Column Attach	✓	✓
100% QA Electrical @ 25°C	✓	✓
Visual Inspection	✓	✓
Group B Lot Specific	✓	✓
Group C Sample to 44k device hours	✓	✓
Group D	✓	✓
Group E Total Ionizing Dose	N/A	✓
DPA/Ion Milling	N/A	✓

Revision History

The following table shows the revision history for this document.

Section	Revision Summary
12/17/2020 Version 1.2	
Table 81	Updated case and sample part numbers for 330 µF and 47 µF capacitors.
CNA1509 Package Construction and Key Features and Mechanical Drawing	Added note about grounding CNA1509 lid.
Table 86	Updated θ_{JB}, θ_{JC}, θ_{JA}, and $\theta_{JA\text{-Effective}}$ values.
Package Coefficients	Updated note with information about grounding CNA1509 lid.
09/08/2020 Version 1.1	
General updates	• Updated from Advance Product Specification to Product Specification. • Updated to Vivado tools version 2020.1.1.
Table 1	Updated SEU_{CRAM} and SEU_{BRAM} typical values.
VCCINT_IO Migration and Restrictions for SelectIO and Memory Interfaces	• Updated first paragraph. • Added paragraph about SelectIO interfaces.
Table 27 and Table 28	Updated to production release for the XQRKU060-CNA1509 device in -1M speed grade in the Vivado Design Suite 2020.1.1.
CNA1509 Package Construction and Key Features	Updated references to standards for outgas requirements.
Table 84	• Updated description of GC pins. • Corrected MGT pin names.
Figure 13	Corrected block labels.
SYSMON, Configuration, and PCIe Integrated Blocks	Updated PCIe bullet.

Section	Revision Summary
Figure 15	Reduced legend.
05/19/2020 Version 1.0	
Initial release	N/A

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