

Introduction

The IDELAYCTRL module provides a reference clock input that allows internal circuitry to derive a voltage bias, independent of PVT (process, voltage, and temperature) variations, in order to define precise delay tap values for the associated IDELAYx and ODELAYx components.

Additional Information

See the [product page](#).

Features

Not applicable.

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family ⁽¹⁾	UltraScale+™, UltraScale™, Zynq® -7000, Artix®-7, Virtex® -7, Kintex®-7.
Supported User Interfaces	N/A
Provided with Core	
Design Files	VHDL
Example Design	Not Provided
Test Bench	Not Provided
Constraints File	None
Simulation Model	VHDL
Supported S/W Driver	N/A
Tested Design Flows⁽²⁾	
Design Entry	Vivado® Design Suite
Simulation	For supported simulators, see the Xilinx Design Tools: Release Notes Guide .
Synthesis	For IP that ships with source code only, provide the synthesis tools that have been tested or indicate Not Provided.
Support	
Provided by Xilinx at the Xilinx Support web page	

Notes:

1. For a complete listing of supported devices, see the Vivado IP catalog.
2. For the supported versions of the tools, see the [Xilinx Design Tools: Release Notes Guide](#).

Overview

The IDELAYCTRL primitive is used in conjunction with the IDELAY primitive. The RDY output of the IDELAYCTRL primitive indicates when the IDELAYx or ODELAYx modules in the specific region are calibrated. At least one of these primitives must be instantiated when using IDELAYx or ODELAYx.

Block Diagram

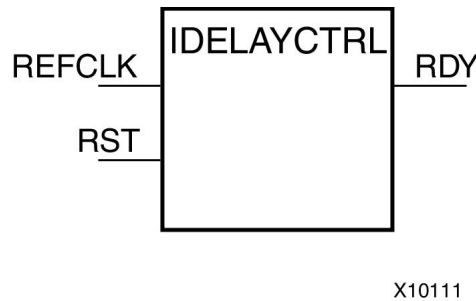


Figure 1: Utility IDELAYCTRL Logic Block Diagram

I/O Signals

Table 1: I/O Signals

Signal	Type	Width	Description
RDY	Output	1	The ready (RDY) signal indicates when the IDELAYx and ODELAYx modules in the specific region are calibrated. The RDY signal is deasserted if REFCLK is held High or Low for one clock period or more. If RDY is deasserted Low, the IDELAYCTRL module must be reset. If not needed, RDY to be unconnected/ ignored.
REFCLK	Input	1	Time reference to IDELAYCTRL to calibrate all IDELAYx and ODELAYx modules in the same region. REFCLK can be supplied directly from a user-supplied source or the MMCME2/PLLE2 and must be routed on a global clock buffer.
RST	Input	1	Active-High asynchronous reset. To ensure proper IDELAYEx and ODELAYEx operation, IDELAYCTRL must be reset after configuration and the REFCLK signal is stable. A reset pulse width Tidelayctrl_rpw is required.

- RST (Module reset) - Resets the IDELAYCTRL circuitry. The RST signal is an active-high asynchronous reset. To reset the IDELAYCTRL, assert it High for at least 50 ns.
- REFCLK (Reference Clock) - Provides a voltage bias, independent of process, voltage, and temperature variations, to the tap-delay lines in the IOBs. The frequency of REFCLK must be 200 MHz to guarantee the tap-delay value specified in the applicable data sheet.

- RDY (Ready Output) - Indicates the validity of the reference clock input, REFCLK. When REFCLK disappears (that is, REFCLK is held High or Low for one clock period or more), the RDY signal is deasserted.

Design Implementation

Design Tools

Note: This IP can only be used in Vivado® IP integrator. It is not designed to be used in an RTL-only design flow within the Vivado Design Suite.

HDL code for the IDELAYCTRL primitive is generated by the Vivado IP integrator.

Target Technology

The target technologies are UltraScale+™, UltraScale™, Zynq®-7000, and 7 series devices.

Technical Support

Xilinx provides technical support at the [Xilinx Support web page](#) for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support if you do any of the following:

- Implement the solution in devices that are not defined in the documentation.
- Customize the solution beyond that allowed in the product documentation.
- Change any section of the design labeled DO NOT MODIFY.

To contact Xilinx Technical Support, navigate to the [Xilinx Support web page](#).

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Revision History

The following table shows the revision history for this document:

Date	Version	Revision
04/06/2016	1.0	Initial Xilinx release of this product brief

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