

SMPTE ST 2059 v1.0

LogiCORE IP Product Guide

Vivado Design Suite

PG244 (v1.0) April 6, 2016

Discontinued IP

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Discontinued IP

Introduction

The Xilinx® LogiCORE™ IP Society of Motion Picture and Television Engineers (SMPTE)® ST 2059 core is a module for broadcast and professional AV applications that require synchronization/genlocking of video and/or audio to a precision time protocol (PTP) Grandmaster, in accordance with the SMPTE ST 2059 standards. This includes the generation of master-locked video and/or audio PLL reference clocks. The IP core is designed to work with a SMPTE ST 2059 software stack, running under Linux on a MicroBlaze™ processor system using the IEEE 1588-capable AXI Ethernet Subsystem IP.

Features

- Generates video and/or audio alignment (synchronization) signals such as black burst, DARS for audio and SMPTE ST12-1 Time Code, in accordance with SMPTE ST 2059-1 standard
- Incorporates very high precision IEEE 1588 real-time counter (RTC) timer
- Supports generation of SMPTE ST12-1 Time Code (hours, minutes, seconds, and frame number)
- Supports drop frame time code
- Includes PTP master-locked reference clock generators for external video and/or audio PLLs
- Includes a software stack (driver and daemon) to be used with Linux
- Control of the core and reading status information can be done through a software user interface

LogiCORE™ IP Facts Table	
Core Specifics	
Supported Device Family ⁽¹⁾	UltraScale+™ Families UltraScale™ Architecture Zynq®-7000 All Programmable SoC 7 Series
Supported User Interfaces	AXI4-Lite
Resources	Performance and Resource Utilization web page
Provided with Core	
Design Files	Encrypted HDL
Example Design	Not Provided
Test Bench	VHDL
Constraints File	Xilinx Design Constraints (XDC)
Simulation Model	Encrypted RTL
Supported S/W Driver	Not Provided
Tested Design Flows⁽²⁾	
Design Entry	Vivado® Design Suite
Simulation	For supported simulators, see the Xilinx Design Tools: Release Notes Guide .
Synthesis	Vivado Synthesis
Support	
Provided by Xilinx at the Xilinx Support web page	

Notes:

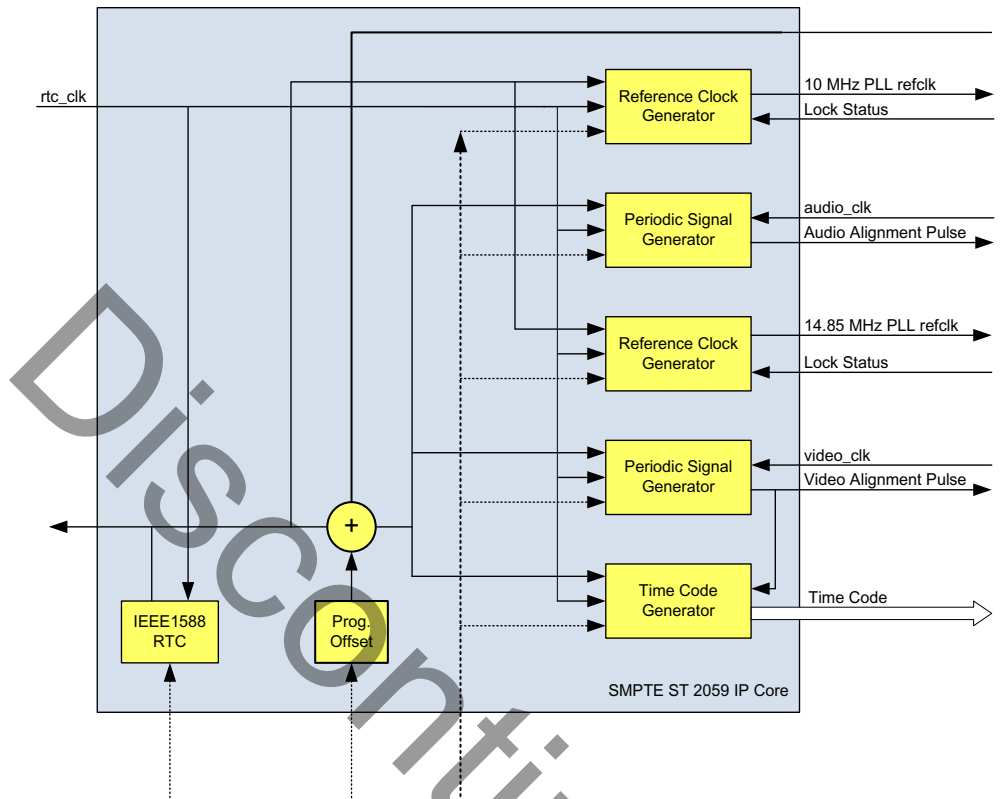
1. For a complete list of supported devices, see the Vivado IP catalog.
2. For the supported versions of the tools, see the [Xilinx Design Tools: Release Notes Guide](#).

Overview

The Xilinx® LogiCORE™ IP SMPTE® ST 2059 core supports the SMPTE standards defining a mechanism for the deterministic generation of timing signals for video and audio systems. It is intended to be used to time synchronize related signals. Using a SMPTE-defined profile of the IEEE 1588 standard, SMPTE ST 2059 is intended to be used to time synchronize related signals in a broadcast or professional audio/video environment. Synchronization (typically using genlock in current systems) is vital in many broadcast applications where all signals are locked to the same time base and with a relative phase with respect to a master time generator. This makes seamless switching between multiple cameras, or mixing a live presenter with graphics, possible.

The core is connected to the IEEE 1588 system to allow communicating over Ethernet to the Grandmaster and locking its real-time clock (RTC) to it. This locked RTC is used to generate audio and/or video reference clocks and alignment pulses. Also, a time code vector is generated from this RTC. The initialization and control of the core is done by a software stack, consisting of a Linux driver and daemon.

Figure 1-1 shows the SMPTE ST 2059 IP core block diagram.



X15986-031616

Figure 1-1: SMPTE ST 2059 Block Diagram

It contains the following functions:

- **IEEE 1588 RTC Timer** – This is the 80-bit PTP clock counter (48-bit seconds, 32-bit nanoseconds), with internal 32-bit fractional precision (resolution 2 to 32 nanoseconds)
- **Reference Clock Generator(s)** – This generates a master locked reference signal for an external video- or audio PLL to lock to.
- **Programmable Offset** – This can be used to add a positive or negative phase offset to the actual PTP time from the RTC. The position of the alignment pulses and the time code can be moved with this offset.
- **Periodic Signal Generator(s)** – This generates the alignment pulses on the target clock domain, in accordance with ST 2059-1
- **Time Code Generator** – This generates a time code vector (HH:MM:SS:FF), in binary coded decimal (BCD) format.

Applications

Applications include synchronization of professional video- and/or audio sources and sinks, over IP networks and time code generation.

Licensing and Ordering Information

This Xilinx LogiCORE IP module is provided under the terms of the [Xilinx Core License Agreement](#). The module is shipped as part of the Vivado Design Suite. For full access to all core functionalities in simulation and in hardware, you must purchase a license for the core. Contact your local Xilinx sales representative for information on pricing and availability.

For more information, visit the SMPTE ST 2059 [product web page](#).

Information about other Xilinx LogiCORE IP modules is available at the [Xilinx Intellectual Property](#) page. For information on pricing and availability of other Xilinx LogiCORE IP modules and tools, contact your [local Xilinx sales representative](#).

Product Specification

Standards

The SMPTE® ST 2059 core is compliant with the AXI4-Lite interconnect standard. The function of the core is compliant with the SMPTE 2059 standards.

Performance

The following sections detail the performance characteristics of the SMPTE ST 2059 core.

For full details about performance and resource utilization, visit the [Performance and Resource Utilization web page](#).

Maximum Frequencies

The maximum achievable clock frequency can vary. The maximum achievable clock frequency and all resource counts can be affected by other tool options, additional logic in the device, using a different version of Xilinx® tools, and other factors.

Latency

One important performance factor for any SMPTE ST 2059 solution is its latency, which defines the time needed for a slave to synchronize with the selected Grandmaster. SMPTE ST 2059-2:2015 provides a guideline to permit a slave to be synchronized within 5 seconds of its connection to the operational PTP network. As a reference, a slave is considered to be locked with the Grandmaster when its 1 PPS is within 1,000 ns comparing to the 1 PPS from the Grandmaster.

As a reference, the following latency is achieved using Oregano Systems syn1588® PCIe NIC as Grandmaster. SMPTE ST 2059 slave is running on a KC705 board.

[Table 2-1](#) shows that 1,000 ns lock range is achieved within 2.63 seconds from the SMPTE ST 2059 slave that is connected to the operational PTP network. The 100 ns lock range is achieved after 6.135 seconds, which means the jitter between SMPTE ST 2059 slave and Grandmaster is below 100 ns after 6+ seconds.

Table 2-1: SMPTE ST 2059 Lock Range

Lock Range	Latency (Time to Lock)
1,000 (range = 501 to 1,000 ns)	2.63 seconds
500 (range = 201 to 500 ns)	3.13 seconds
200 (range = 101 to 200 ns)	5.631 seconds
100 (range = 0 to 100 ns)	6.135 seconds

Resource Utilization

For full details about performance and resource utilization, visit the [Performance and Resource Utilization web page](#).

Port Descriptions

The SMPTE ST 2059 core uses industry standard control and data interfaces to connect to other system components. The following sections describe the various interfaces available with the core. [Figure 2-1](#) shows an I/O diagram of the core. The presence of the Audio, Video, and Time Code pins depends on the settings configured through the Vivado Integrated Design Environment (IDE).



X16279-030416

Figure 2-1: SMPTE ST 2059 I/O Diagram

AXI4-Lite Control Interface

The AXI4-Lite interface allows you to dynamically control parameters within the core. Core configuration can be accomplished using an AXI4-Lite master state machine, or an embedded ARM[®] or soft system processor such as MicroBlaze[™]. The SMPTE ST 2059 core can be controlled through the AXI4-Lite interface by using read and write transactions to the SMPTE ST 2059 IP register space.

The AXI4-Lite slave interface facilitates integrating the core into a processor system, or along with other video or AXI4-Lite compliant IP, connected through the AXI4-Lite interface to an AXI4-Lite master.

Table 2-2 shows the AXI4-Lite control interface signals.

Table 2-2: AXI4-Lite Control Interface Signals

Signal Name	I/O	Width	Description
s_axi_clk	I	1	Clock
s_axi_aresetn	I	1	AXI4-Lite Active-Low reset
s_axi_awaddr	I	12	AXI4-Lite Write Address Bus
s_axi_awvalid	I	1	AXI4-Lite Write Address Channel Write Address Valid
s_axi_wdata	I	32	AXI4-Lite Write Data Bus
s_axi_wstrb	I	4	AXI4-Lite Write Data Channel Data Byte Strobes
s_axi_wvalid	I	1	AXI4-Lite Write Data Channel Write Data Valid
s_axi_awready	O	1	AXI4-Lite Write Address Channel Write Address Ready. Indicates IP module ready to accept the write address.
s_axi_wready	O	1	AXI4-Lite Write Data Channel Write Data Ready. Indicates IP module is ready to accept the write data.
s_axi_bresp	O	2	AXI4-Lite Write Response Channel. Indicates results of the write transfer.
s_axi_bvalid	O	1	AXI4-Lite Write Response Channel Response Valid. Indicates response is valid.
s_axi_bready	I	1	AXI4-Lite Write Response Channel Ready. Indicates target is ready to receive response.
s_axi_arvalid	I	1	AXI4-Lite Read Address Channel Read Address Valid
s_axi_arready	O	1	Ready. Indicates IP module is ready to accept the read address.
s_axi_araddr	I	12	AXI4-Lite Read Address Bus
s_axi_rready	I	1	AXI4-Lite Read Data Channel Read Data Ready. Indicates target is ready to accept the read data.
s_axi_rdata	O	32	AXI4-Lite Read Data Bus
s_axi_rresp	O	2	AXI4-Lite Read Response Channel Response. Indicates results of the read transfer.
s_axi_rvalid	O	1	AXI4-Lite Read Data Channel Read Data Valid

RTC Interface

The RTC interface connects to the system timer input on an IEEE 1588 timestamping capable Ethernet MAC.

Table 2-3: RTC Interface Signals

Signal Name	I/O	Width	Description
rtc_clk	I	1	RTC Clock
rtc_reset	I	1	RTC Clock Domain Reset
rtc_time_ptp_ns	O	32	RTC Nanoseconds Output (to Ethernet MAC)
rtc_time_ptp_sec	O	48	RTC Seconds Output (to Ethernet MAC)
one_pps_pulse	O	1	1PPS Output

Video Alignment Interface

Table 2-4: Video Alignment Interface Signals

Signal Name	I/O	Width	Description
video_clk	I	1	Video Clock
video_alignment_pulse_out	O	1	Video Alignment Pulse Output (in video clock domain)
videopll_refclk_out	O	1	Reference Clock Output for External Video PLL (that supplies the video clock)
videopll_refclk_locked	I	1	External PLL Locked Indicator Input

Audio Alignment Interface

Table 2-5: Audio Alignment Interface Signals

Signal Name	I/O	Width	Description
audio_clk	I	1	Audio Clock
audio_alignment_pulse_out	O	1	Audio Alignment Pulse Output (in audio clock domain)
audiopll_refclk_out	O	1	Reference Clock Output for External Audio PLL (that supplies the video clock)
audiopll_refclk_locked	I	1	External PLL Locked Indicator Input

Time Code Interface

Table 2-6: Time Code Interface Signals

Signal Name	I/O	Width	Description
tc_hours_out	O	6	BCD representation of the hours in the time code
tc_minutes_out	O	7	BCD representation of the minutes in the time code
tc_seconds_out	O	7	BCD representation of the seconds in the time code

Table 2-6: Time Code Interface Signals (Cont'd)

Signal Name	I/O	Width	Description
tc_frames_out	O	6	BCD representation of the frame in the time code
tc_drop_frames_out	O	1	
tc_color_frame_out	O	1	

Register Space

Table 2-7 shows the SMPTE ST 2059 register map.

Table 2-7: SMPTE ST 2059 Register Map

Address (Hex)	Register Name	Access Type	Default Value (Hex)	Description	
IEEE 1588 RTC Timer					
0x000	RTC_CTRL	R/W	0x00000000	RTC Control	
				Bits	Value
				31:6	Reserved
				5	Set RTC offset (on rising edge)
				4	Reserved
				3	Set RTC time (on rising edge)
				2	Set RTC period (on rising edge)
				0	Get RTC time (on rising edge)
0x010	RTC_TIME_SEC_H	R/W	0x00000000	RTC Time Seconds High	
				Bits	Value
				31:16	0x0000
15:0	Seconds value Bits[47:32]				
0x014	RTC_TIME_SEC_L	R/W	0x00000000	RTC Time Seconds Low	
				Bits	Value
31:0	Seconds value Bits[31:0]				
0x018	RTC_TIME_NS	R/W	0x00000000	RTC Time Nanoseconds	
				Bits	Value
				31:30	00
29:0	Nanoseconds value				

Table 2-7: SMPTE ST 2059 Register Map (Cont'd)

Address (Hex)	Register Name	Access Type	Default Value (Hex)	Description	
0x020	RTC_PERIOD_H	R/W	0x00000000	RTC Period Integer	
				Bits	Value
				31:8	0x000000
				7:0	Nanoseconds, integer part
0x024	RTC_PERIOD_L	R/W	0x00000000	RTC Period Fraction	
				Bits	Value
				31:0	Nanoseconds, fractional part
0x034	RTC_OFFSET_SEC_H	R/W	0x00000000	RTC Offset Seconds High	
				Bits	Value
				31:16	0x0000
				15:0	Seconds value Bits[47:32]
0x038	RTC_OFFSET_SEC_L	R/W	0x00000000	RTC Offset Seconds Low	
				Bits	Value
				31:0	Seconds value Bits[31:0]
0x03C	RTC_OFFSET_NSEC	R/W	0x00000000	RTC Offset Nanoseconds	
				Bits	Value
				31:0	Nanoseconds value
Programmable PTP Time Offset					
0x400	PCR_CTRL	R/W	0x00000000	PTP Offset Control	
				Bits	Value
				31:5	Reserved
				4	Set PTP time offset (on rising edge)
				3:1	Reserved
0	Get time, after offset (on rising edge)				
0x404	PCR_STATUS	R	0x00000000	PTP Offset Status	
				Bits	Value
				31:1	Reserved
				0	0 = Get time not completed yet 1 = Get time OK

Table 2-7: SMPTE ST 2059 Register Map (Cont'd)

Address (Hex)	Register Name	Access Type	Default Value (Hex)	Description						
0x410	PCR_OFFSET_SEC_H	R/W	0x00000000	PTP Offset Seconds High <table border="1"> <thead> <tr> <th>Bits</th> <th>Value</th> </tr> </thead> <tbody> <tr> <td>31:16</td> <td>0x0000</td> </tr> <tr> <td>15:0</td> <td>Seconds value Bits[47:32]</td> </tr> </tbody> </table>	Bits	Value	31:16	0x0000	15:0	Seconds value Bits[47:32]
Bits	Value									
31:16	0x0000									
15:0	Seconds value Bits[47:32]									
0x414	PCR_OFFSET_SEC_L	R/W	0x00000000	PTP Offset Seconds Low <table border="1"> <thead> <tr> <th>Bits</th> <th>Value</th> </tr> </thead> <tbody> <tr> <td>31:0</td> <td>Seconds value Bits[31:0]</td> </tr> </tbody> </table>	Bits	Value	31:0	Seconds value Bits[31:0]		
Bits	Value									
31:0	Seconds value Bits[31:0]									
0x418	PCR_OFFSET_NS	R/W	0x00000000	PTP Offset Nanoseconds <table border="1"> <thead> <tr> <th>Bits</th> <th>Value</th> </tr> </thead> <tbody> <tr> <td>31:0</td> <td>Nanoseconds value</td> </tr> </tbody> </table>	Bits	Value	31:0	Nanoseconds value		
Bits	Value									
31:0	Nanoseconds value									
0x434	PCR_PTPTIME_SEC_H	R	0x00000000	PTP Time After Offset, Seconds High <table border="1"> <thead> <tr> <th>Bits</th> <th>Value</th> </tr> </thead> <tbody> <tr> <td>31:16</td> <td>0x00000000</td> </tr> <tr> <td>15:0</td> <td>Seconds value Bits[47:32]</td> </tr> </tbody> </table>	Bits	Value	31:16	0x00000000	15:0	Seconds value Bits[47:32]
Bits	Value									
31:16	0x00000000									
15:0	Seconds value Bits[47:32]									
0x438	PCR_PTPTIME_SEC_L	R	0x00000000	PTP Time After Offset, Seconds Low <table border="1"> <thead> <tr> <th>Bits</th> <th>Value</th> </tr> </thead> <tbody> <tr> <td>31:0</td> <td>Seconds value Bits[31:0]</td> </tr> </tbody> </table>	Bits	Value	31:0	Seconds value Bits[31:0]		
Bits	Value									
31:0	Seconds value Bits[31:0]									
0x43C	PCR_PTPTIME_NS	R	0x00000000	PTP Time After Offset, Nanoseconds <table border="1"> <thead> <tr> <th>Bits</th> <th>Value</th> </tr> </thead> <tbody> <tr> <td>31:0</td> <td>Nanoseconds value</td> </tr> </tbody> </table>	Bits	Value	31:0	Nanoseconds value		
Bits	Value									
31:0	Nanoseconds value									

Table 2-7: SMPTE ST 2059 Register Map (Cont'd)

Address (Hex)	Register Name	Access Type	Default Value (Hex)	Description														
Video Periodic Signal Generator																		
0x440	VIDEO_PSG_CTRL	R/W	0x00000000	Video PSG Control <table border="1"> <thead> <tr> <th>Bits</th> <th>Value</th> </tr> </thead> <tbody> <tr> <td>31:5</td> <td>Reserved</td> </tr> <tr> <td>4</td> <td>1 = Reset</td> </tr> <tr> <td>3</td> <td>Set number of clocks per period (on rising edge)</td> </tr> <tr> <td>2</td> <td>Set alignment pulse expected time (on rising edge)</td> </tr> <tr> <td>1</td> <td>Clear time program error (on rising edge)</td> </tr> <tr> <td>0</td> <td>Clear realignment occurred flag (on rising edge)</td> </tr> </tbody> </table>	Bits	Value	31:5	Reserved	4	1 = Reset	3	Set number of clocks per period (on rising edge)	2	Set alignment pulse expected time (on rising edge)	1	Clear time program error (on rising edge)	0	Clear realignment occurred flag (on rising edge)
Bits	Value																	
31:5	Reserved																	
4	1 = Reset																	
3	Set number of clocks per period (on rising edge)																	
2	Set alignment pulse expected time (on rising edge)																	
1	Clear time program error (on rising edge)																	
0	Clear realignment occurred flag (on rising edge)																	
0x444	VIDEO_PSG_STATUS	R	0x00000000	Video PSG Status <table border="1"> <thead> <tr> <th>Bits</th> <th>Value</th> </tr> </thead> <tbody> <tr> <td>31:2</td> <td>Reserved</td> </tr> <tr> <td>1</td> <td>1 = Time programming error</td> </tr> <tr> <td>0</td> <td>1 = Realignment occurred</td> </tr> </tbody> </table>	Bits	Value	31:2	Reserved	1	1 = Time programming error	0	1 = Realignment occurred						
Bits	Value																	
31:2	Reserved																	
1	1 = Time programming error																	
0	1 = Realignment occurred																	
0x448	VIDEO_PSG_PULSE_EXP_TIME_SEC_H	R/W	0x00000000	Expected Pulse Time, Seconds High <table border="1"> <thead> <tr> <th>Bits</th> <th>Value</th> </tr> </thead> <tbody> <tr> <td>31:16</td> <td>0x0000</td> </tr> <tr> <td>15:0</td> <td>Seconds value Bits[47:32]</td> </tr> </tbody> </table>	Bits	Value	31:16	0x0000	15:0	Seconds value Bits[47:32]								
Bits	Value																	
31:16	0x0000																	
15:0	Seconds value Bits[47:32]																	
0x44C	VIDEO_PSG_PULSE_EXP_TIME_SEC_L	R/W	0x00000000	Expected Pulse Time, Seconds Low <table border="1"> <thead> <tr> <th>Bits</th> <th>Value</th> </tr> </thead> <tbody> <tr> <td>31:0</td> <td>Seconds value Bits[31:0]</td> </tr> </tbody> </table>	Bits	Value	31:0	Seconds value Bits[31:0]										
Bits	Value																	
31:0	Seconds value Bits[31:0]																	
0x450	VIDEO_PSG_PULSE_EXP_TIME_NS	R/W	0x00000000	Expected Pulse Time, Nanoseconds <table border="1"> <thead> <tr> <th>Bits</th> <th>Value</th> </tr> </thead> <tbody> <tr> <td>31:0</td> <td>Nanoseconds value</td> </tr> </tbody> </table>	Bits	Value	31:0	Nanoseconds value										
Bits	Value																	
31:0	Nanoseconds value																	
0x454	VIDEO_PSG_NR_OF_CLKS_PERIOD	R/W	0x00000000	Number of Clocks Per Period <table border="1"> <thead> <tr> <th>Bits</th> <th>Value</th> </tr> </thead> <tbody> <tr> <td>31:0</td> <td>Number of clocks per period</td> </tr> </tbody> </table>	Bits	Value	31:0	Number of clocks per period										
Bits	Value																	
31:0	Number of clocks per period																	

Table 2-7: SMPTE ST 2059 Register Map (Cont'd)

Address (Hex)	Register Name	Access Type	Default Value (Hex)	Description	
Video PLL Reference Clock Generator					
0x500	V_REFCLK_CTRL	R/W	0x00000000	Reference Clock Generator Control	
				Bits	Value
				31:3	Reserved
				2	Clear PLL lock lost (on rising edge)
1	0 = Enable generator output 1 = Disable generator output				
0	Load phase incremter parameters (on rising edge)				
0x504	V_REFCLK_STATUS	R	0x00000000	Reference Clock Generator Status	
				Bits	Value
				31:3	Reserved
				2	1 = External PLL lock was lost
1	Reserved				
0	1 = External PLL locked				
0x508	V_REFCLK_PH_INCR_NUMERATOR	R/W	0x00000000	Phase Incremter Numerator Parameter	
				Bits	Value
31:0	Numerator value				
0x50C	V_REFCLK_PH_INCR_DENOMINATOR	R/W	0x00000000	Phase Incremter Denominator Parameter	
				Bits	Value
31:0	Denominator value				
0x510	V_REFCLK_PH_STDINC_NS	R/W	0x00000000	Phase Incremter Default Increment Parameter	
				Bits	Value
31:0	Default increment value				

Table 2-7: SMPTE ST 2059 Register Map (Cont'd)

Address (Hex)	Register Name	Access Type	Default Value (Hex)	Description	
Audio PLL Reference Clock Generator					
0x520	A_REFCLK_CTRL	R/W	0x00000000	Reference Clock Generator Control	
				Bits	Value
				31:3	Reserved
				2	Clear PLL lock lost (on rising edge)
1	0 = Enable generator output 1 = Disable generator output				
0	Load incremter parameters (on rising edge)				
0x524	A_REFCLK_STATUS	R	0x00000000	Reference Clock Generator Status	
				Bits	Value
				31:3	Reserved
				2	1 = External PLL lock was lost
1	Reserved				
0	1 = External PLL locked				
0x528	A_REFCLK_PH_INCR_NUMERATOR	R/W	0x00000000	Phase Incremter Numerator Parameter	
				Bits	Value
31:0	Numerator value				
0x52C	A_REFCLK_PH_INCR_DENOMINATOR	R/W	0x00000000	Phase Incremter Denominator Parameter	
				Bits	Value
31:0	Denominator value				
0x530	A_REFCLK_PH_STDINC_NS	R/W	0x00000000	Phase Incremter Default Increment Parameter	
				Bits	Value
31:0	Default increment value				

Table 2-7: SMPTE ST 2059 Register Map (Cont'd)

Address (Hex)	Register Name	Access Type	Default Value (Hex)	Description	
Audio Periodic Signal Generator					
0x540	AUDIO_PSG_CTRL	R/W	0x00000000	Audio PSG Control	
				Bits	Value
				31:5	Reserved
				4	1 = Reset
				3	Set number of clocks per period (on rising edge)
				2	Set alignment pulse expected time (on rising edge)
				1	Clear time program error (on rising edge)
0	Clear realignment occurred flag (on rising edge)				
0x544	AUDIO_PSG_STATUS	R	0x00000000	Audio PSG Status	
				Bits	Value
				31:2	Reserved
1	1 = Time programming error				
0	1 = Realignment occurred				
0x548	AUDIO_PSG_PULSE_EXP_TIME_SEC_H	R/W	0x00000000	Expected Pulse Time, Seconds High	
				Bits	Value
				31:16	0x0000
15:0	Seconds value Bits[47:32]				
0x54C	AUDIO_PSG_PULSE_EXP_TIME_SEC_L	R/W	0x00000000	Expected Pulse Time, Seconds Low	
				Bits	Value
				31:0	Seconds value Bits[31:0]
0x550	AUDIO_PSG_PULSE_EXP_TIME_NS	R/W	0x00000000	Expected Pulse Time, Nanoseconds	
				Bits	Value
				31:0	Nanoseconds value
0x554	AUDIO_PSG_NR_OF_CLKS_PERIOD	R/W	0x00000000	Number of Clocks Per Period	
				Bits	Value
				31:0	Number of clocks per period

Table 2-7: SMPTE ST 2059 Register Map (Cont'd)

Address (Hex)	Register Name	Access Type	Default Value (Hex)	Description										
Time Code Generator														
0x800	TCG_CTRL	R/W	0x00000000	Time Code Generator Control <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Bits</th> <th>Value</th> </tr> </thead> <tbody> <tr> <td>31:1</td> <td>Reserved</td> </tr> <tr> <td>0</td> <td>Load TCG (p)reset time (on rising edge)</td> </tr> </tbody> </table>	Bits	Value	31:1	Reserved	0	Load TCG (p)reset time (on rising edge)				
Bits	Value													
31:1	Reserved													
0	Load TCG (p)reset time (on rising edge)													
0x804	TCG_MODES	R/W	0x00000001	Time Code Generator Modes <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Bits</th> <th>Value</th> </tr> </thead> <tbody> <tr> <td>31:1</td> <td>Reserved</td> </tr> <tr> <td>0</td> <td>1 = Enable drop frames</td> </tr> </tbody> </table>	Bits	Value	31:1	Reserved	0	1 = Enable drop frames				
Bits	Value													
31:1	Reserved													
0	1 = Enable drop frames													
0x808	TCG_SETTINGS	R/W	0x0000021E	Time Code Generator Settings <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Bits</th> <th>Value</th> </tr> </thead> <tbody> <tr> <td>31:12</td> <td>Reserved</td> </tr> <tr> <td>11:8</td> <td>Alignment interval divide value</td> </tr> <tr> <td>7:5</td> <td>Reserved</td> </tr> <tr> <td>4:0</td> <td>Number of frames (24/25/30)</td> </tr> </tbody> </table>	Bits	Value	31:12	Reserved	11:8	Alignment interval divide value	7:5	Reserved	4:0	Number of frames (24/25/30)
Bits	Value													
31:12	Reserved													
11:8	Alignment interval divide value													
7:5	Reserved													
4:0	Number of frames (24/25/30)													
0x810	TCG_RESET_TIME_SEC_H	R/W	0x00000000	TCG (P)reset Time, Seconds High <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Bits</th> <th>Value</th> </tr> </thead> <tbody> <tr> <td>31:16</td> <td>Reserved</td> </tr> <tr> <td>15:0</td> <td>Seconds Bits[47:32]</td> </tr> </tbody> </table>	Bits	Value	31:16	Reserved	15:0	Seconds Bits[47:32]				
Bits	Value													
31:16	Reserved													
15:0	Seconds Bits[47:32]													
0x814	TCG_RESET_TIME_SEC_L	R/W	0x00000000	TCG (P)reset Time, Seconds Low <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Bits</th> <th>Value</th> </tr> </thead> <tbody> <tr> <td>31:0</td> <td>Seconds Bits[31:0]</td> </tr> </tbody> </table>	Bits	Value	31:0	Seconds Bits[31:0]						
Bits	Value													
31:0	Seconds Bits[31:0]													
0x818	TCG_RESET_TIME_NS	R/W	0x00000000	TCG (P)reset Time, Nanoseconds <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Bits</th> <th>Value</th> </tr> </thead> <tbody> <tr> <td>31:0</td> <td>Nanoseconds</td> </tr> </tbody> </table>	Bits	Value	31:0	Nanoseconds						
Bits	Value													
31:0	Nanoseconds													

Table 2-7: SMPTE ST 2059 Register Map (Cont'd)

Address (Hex)	Register Name	Access Type	Default Value (Hex)	Description	
0x820	TCG_RESET_NEW_TIME	R/W	0x00000000	TCG New (P)reset Values	
				Bits	Value
				31:29	Reserved
				28:24	Hours
				23:22	Reserved
				21:16	Minutes
				15:14	Reserved
				13:8	Seconds
	7:5	Reserved			
	4:0	Frames			
0x824	TCG_RESET_STATUS	R	0x00000000	Time Code Generator (P)reset Status	
				Bits	Value
				31:2	Reserved
				1	1 = Time code (p)reset as requested
	0	1 = New time code could not be loaded			

RTC_CTRL (0x000) Register

The RTC_CTRL register contains three control bits for activating the new configuration of the IEEE 1588 RTC timer, and one control/status bit for initiating the readback of the current PTP time. Bit[0] initiates the readback of the current PTP time. Reading back Bit[0] returns the status of the readback of current PTP time.

If this bit returns 1, the readback process is complete, and the PTP time is available for reading by the host CPU in RTC_TIME_SEC_H, RTC_TIME_SEC_L, and RTC_TIME_NS registers. Bit[2] of the RTC_CTRL register activates the new setting for the RTC period in RTC_PERIOD_H and RTC_PERIOD_L registers.

Bit[3] activates the new setting of RTC_TIME in RTC_TIME_SEC_H, RTC_TIME_SEC_L, and RTC_TIME_NS registers. And finally, Bit[5] activates the new setting of the time offset in RTC_OFFSET_SEC_H, RTC_OFFSET_SEC_L, and RTC_OFFSET_NSEC registers. All of the activations are performed on a 0 to 1 change of the associated control bits.

RTC_TIME_SEC_H (0x010) Register

After completing a time readback action, triggered by RTC_CTRL Bit[0], this register contains Bits[47:32] of the 48 bits seconds count. This register can also be written to, like the RTC_TIME_SEC_L and RTC_TIME_NS registers, to activate a new time setting of the RTC (through the RTC_CTRL Bit[3]).



RECOMMENDED: Xilinx does not recommend this, use a time offset instead (using registers RTC_OFFSET_SEC_H, RTC_OFFSET_SEC_L and RTC_OFFSET_NS).

RTC_TIME_SEC_L (0x014) Register

After completing a time readback action, triggered by RTC_CTRL Bit[0], this register contains Bits[31:0] of the 48 bits seconds count. This register can also be written to, like the RTC_TIME_SEC_H and RTC_TIME_NS registers, to activate a new time setting of the RTC (through the RTC_CTRL Bit[3]).



RECOMMENDED: Xilinx does not recommend this, use a time offset instead (using registers RTC_OFFSET_SEC_H, RTC_OFFSET_SEC_L and RTC_OFFSET_NS).

RTC_TIME_NS (0x018) Register

After completing a time readback action, triggered by RTC_CTRL Bit[0], this register contains the nanoseconds count. This register can also be written to, like the RTC_TIME_SEC_H and RTC_TIME_SEC_L registers, to activate a new time setting of the RTC (through the RTC_CTRL Bit[3]).



RECOMMENDED: Xilinx does not recommend this, use a time offset instead (using registers RTC_OFFSET_SEC_H, RTC_OFFSET_SEC_L and RTC_OFFSET_NS).

RTC_PERIOD_H (0x020) Register

This register (Bits[7:0]) contains the integer nanosecond part of the time increment per `rtc_clk` clock cycle.

RTC_PERIOD_L (0x024) Register

This register (Bits[31:0]) contains the fractional nanosecond part of the time increment per `rtc_clk` clock cycle. The resolution of the time increment is 2^{-32} ns.

RTC_OFFSET_SEC_H (0x034) Register

This register (Bits[15:0]) contains the upper 16 bits of the offset seconds. The offset can only be positive. After RTC_OFFSET_SEC_H, RTC_OFFSET_SEC_L and RTC_OFFSET_NSEC registers are configured, the newly configured offset can be activated by RTC_CTRL Bit[5].



RECOMMENDED: *Xilinx recommends to always adjust the time offset using the RTC_OFFSET_* registers, and not to use the set time method (RTC_CLRL Bit[3]).*

RTC_OFFSET_SEC_L (0x038) Register

This register contains the lower 32 bits of the offset seconds. The offset can only be positive. After RTC_OFFSET_SEC_H, RTC_OFFSET_SEC_L, and RTC_OFFSET_NSEC registers are configured, the newly configured offset can be activated by RTC_CTRL Bit[5].



RECOMMENDED: *Xilinx recommends to always adjust the time offset using the RTC_OFFSET_* registers, and not to use the set time method (RTC_CLRL Bit[3]).*

RTC_OFFSET_NSEC (0x03C) Register

This register contains the offset nanoseconds. The offset can only be positive. After RTC_OFFSET_SEC_H, RTC_OFFSET_SEC_L, and RTC_OFFSET_NSEC registers are configured, the newly configured offset can be activated by RTC_CTRL Bit[5].



RECOMMENDED: *Xilinx recommends to always adjust the time offset using the RTC_OFFSET_* registers, and not to use the set time method (RTC_CLRL Bit[3]).*

PCR_CTRL (0x400) Register

Bit[4] of this register controls the activation of a programmable positive or negative offset which is configured through registers PCR_OFFSET_SEC_H, PCR_OFFSET_SEC_L, and PCR_OFFSET_NS. The purpose of this offset is to shift the alignment pulses, time code, and 1pps pulse forward or backward without affecting the reference clock generators for the external PLLs. Bit[0] of the PCR_CTRL register activates readback of the PTP time after the offset. All of the activations are performed on a 0 to 1 change of the associated control bits.

PCR_STATUS (0x404) Register

Bit[0] of this register returns the status of the readback of the PTP time after offset. If this bit returns 1, the readback process is complete, and the time is available for reading by the host CPU in PCR_PTPTIME_SEC_H, PCR_PTPTIME_SEC_L, and PCR_PTPTIME_NS registers.

PCR_OFFSET_SEC_H (0x410) Register

This register (Bits[15:0]) contains Bits[47:32] of the 48-bit signed offset seconds value, which needs to be applied to the time coming from the RTC.

PCR_OFFSET_SEC_L (0x414) Register

This register contains Bits[31:0] of the 48-bit signed offset seconds value, which needs to be applied to the time coming from the RTC.

PCR_OFFSET_NS (0x418) Register

This register contains Bits[31:0] of the 32-bit signed offset nanoseconds value, which needs to be applied to the time coming from the RTC. Note that when the seconds offset value is negative, the nanoseconds must also be either zero or negative. For example in the case of shifting 1.5 seconds backwards, the seconds offset value needs to be `0xFFFF_FFFFFFFF` (-1), and the nanoseconds offset value needs to be `0xE2329B00` (-500,000,000).

PCR_PTPTIME_SEC_H (0x434) Register

After completing a time readback action, triggered by PCR_CTRL Bit[0], this register contains Bits[47:32] of the seconds count after the offset.

PCR_PTPTIME_SEC_L (0x438) Register

After completing a time readback action, triggered by PCR_CTRL Bit[0], this register contains Bits[31:0] of the seconds count after the offset.

PCR_PTPTIME_NS (0x43C) Register

After completing a time readback action, triggered by PCR_CTRL Bit[0], this register contains the nanoseconds count after the offset.

VIDEO_PSG_CTRL (0x440) Register

Bit[4] of this register puts the Video alignment pulse generator in reset when 1. A zero has to be written to this register bit to get the generator out of reset again. Bit[3] activates the new setting of the VIDEO_PSG_NR_OF_CLKS_PERIOD register. Bit[2] activates the new setting of the VIDEO_PSG_PULSE_EXP_TIME_SEC_H, VIDEO_PSG_PULSE_EXP_TIME_SEC_L, and VIDEO_PSG_PULSE_EXP_TIME_NS registers. Bit[1] clears the time programming error flag, and Bit[0] clears the realignment occurred flag. The activations and clears are performed on a 0 to 1 change of the associated control bits.

VIDEO_PSG_STATUS (0x444) Register

Bit[1] in this register reflects the time programming error flag. This error flag is set (1) when during the activation of the pulse expected time, as configured in the VIDEO_PSG_PULSE_EXP_TIME_SEC_H, VIDEO_PSG_PULSE_EXP_TIME_SEC_L, and VIDEO_PSG_PULSE_EXP_TIME_NS registers, the current time is already beyond that time.

This flag can be cleared by writing a 0, 1 sequence to VIDEO_PSG_CTRL Bit[1]. Bit[0] in the VIDEO_PSG_STATUS register reflects the realignment occurred flag. This flag is set (1) when at the expected time no alignment pulse was found, which resets an internal counter in order for the next alignment pulse to be at the correct time. The realignment occurred flag can be reset by writing a 0, 1 sequence to VIDEO_PSG_CTRL Bit[1].

VIDEO_PSG_PULSE_EXP_TIME_SEC_H (0x448) Register

This register (Bits[15:0]) contains Bits[47:32] of the 48-bit seconds part of the pulse expected time value. The pulse expected time should always be a time in the future, at the moment of activation, otherwise the time programming error flag will be raised. Along with the contents of the VIDEO_PSG_PULSE_EXP_TIME_SEC_L and VIDEO_PSG_PULSE_EXP_TIME_NS registers, the contents in this register are activated by writing a 0, 1 sequence to VIDEO_PSG_CTRL Bit[2].

VIDEO_PSG_PULSE_EXP_TIME_SEC_L (0x44C) Register

This register contains Bits[31:0] of the 48-bit seconds part of the pulse expected time value. Along with the contents of the VIDEO_PSG_PULSE_EXP_TIME_SEC_H and VIDEO_PSG_PULSE_EXP_TIME_NS registers, the contents in this register are activated by writing a 0, 1 sequence to VIDEO_PSG_CTRL Bit[2].

VIDEO_PSG_PULSE_EXP_TIME_NS (0x450) Register

This register contains the nanoseconds part of the pulse expected time value. Along with the contents of the VIDEO_PSG_PULSE_EXP_TIME_SEC_H and VIDEO_PSG_PULSE_EXP_TIME_SEC_L registers, the contents in this register are activated by writing a 0, 1 sequence to VIDEO_PSG_CTRL Bit[2].

VIDEO_PSG_NR_OF_CLKS_PERIOD (0x454) Register

This register contains the number of clocks (in the `video_clk` domain) between two alignment pulses. The setting is activated by writing a 0, 1 sequence to VIDEO_PSG_CTRL Bit[3].

V_REFCLK_CTRL (0x500) Register

Bit[2] in this register clears the "PLL lock lost" status bit, when a 0, 1 sequence is written to this bit. Bit[1] in this register disables the video PLL reference clock generator when 1. When this bit is 0, the generator is enabled. Bit[0] activates a new configuration by writing a 0, 1 sequence to it. The configuration is defined by the contents of V_REFCLK_PH_INCR_NUMERATOR, V_REFCLK_PH_INCR_DENOMINATOR, and V_REFCLK_PH_STDINC_NS registers.

V_REFCLK_STATUS (0x504) Register

Bit[0] reflects the actual status of the `videopl1_refclk_locked` input. If this input is High, the status bit returns 1. Bit[2] is the "PLL lock lost" indicator. This bit is set when the lock is lost (`videopl1_refclk_locked` input is 0). It can only be cleared by V_REFCLK_CTRL Bit[2].

V_REFCLK_PH_INCR_NUMERATOR (0x508) Register

This register contains the 32-bit numerator parameter value for the video PLL reference clock generator. Along with the denominator and default increment parameters the configuration is activated by writing a 0, 1 sequence to V_REFCLK_CTRL Bit[0].

To determine the values of the parameters for the reference clock generator for a specific frequency f_{refgen} (in Hz), follow the following steps:

First, find the value of the default increment, T_s . This is the rounded down (to integer number of ns) value of the half-clock period:

Default increment:

$$T_s = \text{floor}\left(\frac{10^9}{2 \times f_{refgen}}\right) [ns]$$

Then calculate the error as a rational number:

$$err = \frac{10^9 - T_s \times 2 \times f_{refgen}}{2 \times f_{refgen}} = \frac{\text{numerator}}{\text{denominator}}$$

If necessary, prime factorization can be used for both numerator and denominator to find values that are small enough to fit in a 32-bit unsigned integer.

V_REFCLK_PH_INCR_DENOMINATOR (0x50C) Register

This register contains the 32-bit denominator parameter value for the video PLL reference clock generator. Along with the numerator and default increment parameters the configuration is activated by writing a 0, 1 sequence to V_REFCLK_CTRL Bit[0].

V_REFCLK_PH_STDINC_NS (0x510) Register

This register contains the 32-bit default increment parameter value (in ns) for the video PLL reference clock generator. Along with the numerator and denominator parameters the configuration is activated by writing a 0, 1 sequence to V_REFCLK_CTRL Bit[0].

A_REFCLK_CTRL (0x520) Register

Bit[2] in this register clears the "PLL lock lost" status bit, when a 0, 1 sequence is written to this bit. Bit[1] in this register disables the audio PLL reference clock generator when 1. When this bit is 0, the generator is enabled. Bit[0] activates a new configuration by writing a 0, 1 sequence to it. The configuration is defined by the contents of A_REFCLK_PH_INCR_NUMERATOR, A_REFCLK_PH_INCR_DENOMINATOR, and A_REFCLK_PH_STDINC_NS registers.

A_REFCLK_STATUS (0x524) Register

Bit[0] reflects the status of the `audiopl1_refclk_locked` input. If this input is High, the status bit returns 1. Bit[2] is the "PLL lock lost" indicator. This bit is set when the lock is lost (`audiopl1_refclk_locked` input is 0). It can only be cleared by A_REFCLK_CTRL Bit[2].

A_REFCLK_PH_INCR_NUMERATOR (0x528) Register

This register contains the 32-bit numerator parameter value for the audio PLL reference clock generator. Along with the denominator and default increment parameters the configuration is activated by writing a 0, 1 sequence to A_REFCLK_CTRL Bit[0].

To determine the values of the parameters for the reference clock generator for a specific frequency f_{refgen} (in Hz), follow the following steps:

First, find the value of the default increment, T_s . This is the rounded down (to integer number of ns) value of the half-clock period:

Default increment:

$$T_s = \text{floor}\left(\frac{10^9}{2 \times f_{refgen}}\right) [ns]$$

Then calculate the error as a rational number:

$$err = \frac{10^9 - T_s \times 2 \times f_{refgen}}{2 \times f_{refgen}} = \frac{\text{numerator}}{\text{denominator}}$$

If necessary, prime factorization can be used for both numerator and denominator to find values that are small enough to fit in a 32-bit unsigned integer.

A_REFCLK_PH_INCR_DENOMINATOR (0x52C) Register

This register contains the 32-bit denominator parameter value for the audio PLL reference clock generator. Along with the numerator and default increment parameters, the configuration is activated by writing a 0, 1 sequence to A_REFCLK_CTRL Bit[0].

A_REFCLK_PH_STDINC_NS (0x530) Register

This register contains the 32-bit default increment parameter value (in ns) for the audio PLL reference clock generator. Along with the numerator and denominator parameters, the configuration is activated by writing a 0, 1 sequence to A_REFCLK_CTRL Bit[0].

AUDIO_PSG_CTRL (0x540) Register

Bit[4] of this register puts the Audio alignment pulse generator in reset when 1. A zero has to be written to this register bit to get the generator out of reset again. Bit[3] activates the new setting of the AUDIO_PSG_NR_OF_CLKS_PERIOD register. Bit[2] activates the new setting of the AUDIO_PSG_PULSE_EXP_TIME_SEC_H, AUDIO_PSG_PULSE_EXP_TIME_SEC_L, and AUDIO_PSG_PULSE_EXP_TIME_NS registers. Bit[1] clears the time programming error flag, and Bit[0] clears the realignment occurred flag. The activations and clears are performed on a 0 to 1 change of the associated control bits.

AUDIO_PSG_STATUS (0x544) Register

Bit[1] in this register reflects the time programming error flag. This error flag is set (1) when during the activation of the pulse expected time, as configured in the AUDIO_PSG_PULSE_EXP_TIME_SEC_H, AUDIO_PSG_PULSE_EXP_TIME_SEC_L, and AUDIO_PSG_PULSE_EXP_TIME_NS registers, the current time is already beyond that time. This flag can be cleared by writing a 0, 1 sequence to AUDIO_PSG_CTRL Bit[1]. Bit[0] in the AUDIO_PSG_STATUS register reflects the realignment occurred flag. This flag is set (1) when at the expected time no alignment pulse was found, which resets an internal counter in order for the next alignment pulse to be at the correct time. The realignment occurred flag can be reset by writing a 0, 1 sequence to AUDIO_PSG_CTRL Bit[1].

AUDIO_PSG_PULSE_EXP_TIME_SEC_H (0x548) Register

This register (Bits[15:0]) contains Bits[47:32] of the 48-bit seconds part of the pulse expected time value. The pulse expected time should always be a time in the future, at the moment of activation, otherwise the time programming error flag is raised. Along with the contents of the AUDIO_PSG_PULSE_EXP_TIME_SEC_L and AUDIO_PSG_PULSE_EXP_TIME_NS registers, the contents in this register are activated by writing a 0, 1 sequence to AUDIO_PSG_CTRL Bit[2].

AUDIO_PSG_PULSE_EXP_TIME_SEC_L (0x54C) Register

This register contains Bits[31:0] of the 48-bit seconds part of the pulse expected time value. Along with the contents of the AUDIO_PSG_PULSE_EXP_TIME_SEC_H and AUDIO_PSG_PULSE_EXP_TIME_NS registers, the contents in this register are activated by writing a 0, 1 sequence to AUDIO_PSG_CTRL Bit[2].

AUDIO_PSG_PULSE_EXP_TIME_NS (0x550) Register

This register contains the nanoseconds part of the pulse expected time value. Along with the contents of the AUDIO_PSG_PULSE_EXP_TIME_SEC_H and AUDIO_PSG_PULSE_EXP_TIME_SEC_L registers, the contents in this register are activated by writing a 0, 1 sequence to AUDIO_PSG_CTRL Bit[2].

AUDIO_PSG_NR_OF_CLKS_PERIOD (0x554) Register

This register contains the number of clocks (in the `audio_clk` domain) between two alignment pulses. The setting is activated by writing a 0, 1 sequence to AUDIO_PSG_CTRL Bit[3].

TCG_CTRL (0x800) Register

Bit[0] of this register arms the time code generator when a 0, 1 sequence is written to this control bit. To arm the time code generator means activating the configuration as (previously) written to the registers TCG_RESET_TIME_SEC_H, TCG_RESET_TIME_SEC_L, TCG_RESET_TIME_NS, and TCG_RESET_NEW_TIME.

TCG_MODES (0x804) Register

Bit[0] of this register controls the enabling of drop frames in the generated time code.

TCG_SETTINGS (0x808) Register

Bits[11:8] in this register contain the so-called alignment divider value. For example, on a 60Hz video frame rate, this value must be 2 because the frame number range is 00 to 29.

Bits[4:0] in this register contain the number of frames in the time code, which can be 24, 25, or 30.

TCG_RESET_TIME_SEC_H (0x810) Register

This register (Bits[15:0]) contains Bits[47:32] of the 48-bit seconds part of the PTP time (after the offset). The time code generator starts waiting for the video frame alignment pulse to (p)reset the time code at the output to the time code as configured in the TCG_RESET_NEW_TIME register.

TCG_RESET_TIME_SEC_L (0x814) Register

This register contains Bits[31:0] of the 48-bit seconds part of the PTP time (after the offset). The time code generator starts waiting for the video frame alignment pulse to (p)reset the time code at the output to the time code as configured in the TCG_RESET_NEW_TIME register.

TCG_RESET_TIME_NS (0x818) Register

This register contains the nanoseconds part of the PTP time (after the offset). The time code generator starts waiting for the video frame alignment pulse to (p)reset the time code at the output to the time code as configured in the TCG_RESET_NEW_TIME register.

TCG_RESET_NEW_TIME (0x820) Register

This register contains the new time code value that should be output, aligned at the first video alignment pulse after the reset time.

```

bit 28:24 :hours
bit 21:16 :minutes
bit 13:8  :seconds
bit 4:0   :frames

```

TCG_RESET_STATUS (0x824) Register

This register contains the Time Code Generator reset status bits. Bit[0] represents the status of whether a new time code can be loaded or not. If Bit[0] is 1, it means new time code could not be loaded. Bit[1] of this register represents this time code generator reset status. If Bit[1] is 1, it means time code has been reset as requested. Bit[31:2] are reserved for future usage.

Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the core.

Figure 3-1 shows an example of the functional system architecture of the SMPTE ST 2059 slave module. Note that the diagram does not show items like register interfaces, AXI buses, etc. Just the functions, their partitioning in hardware, software, as well as their interactions are shown here.

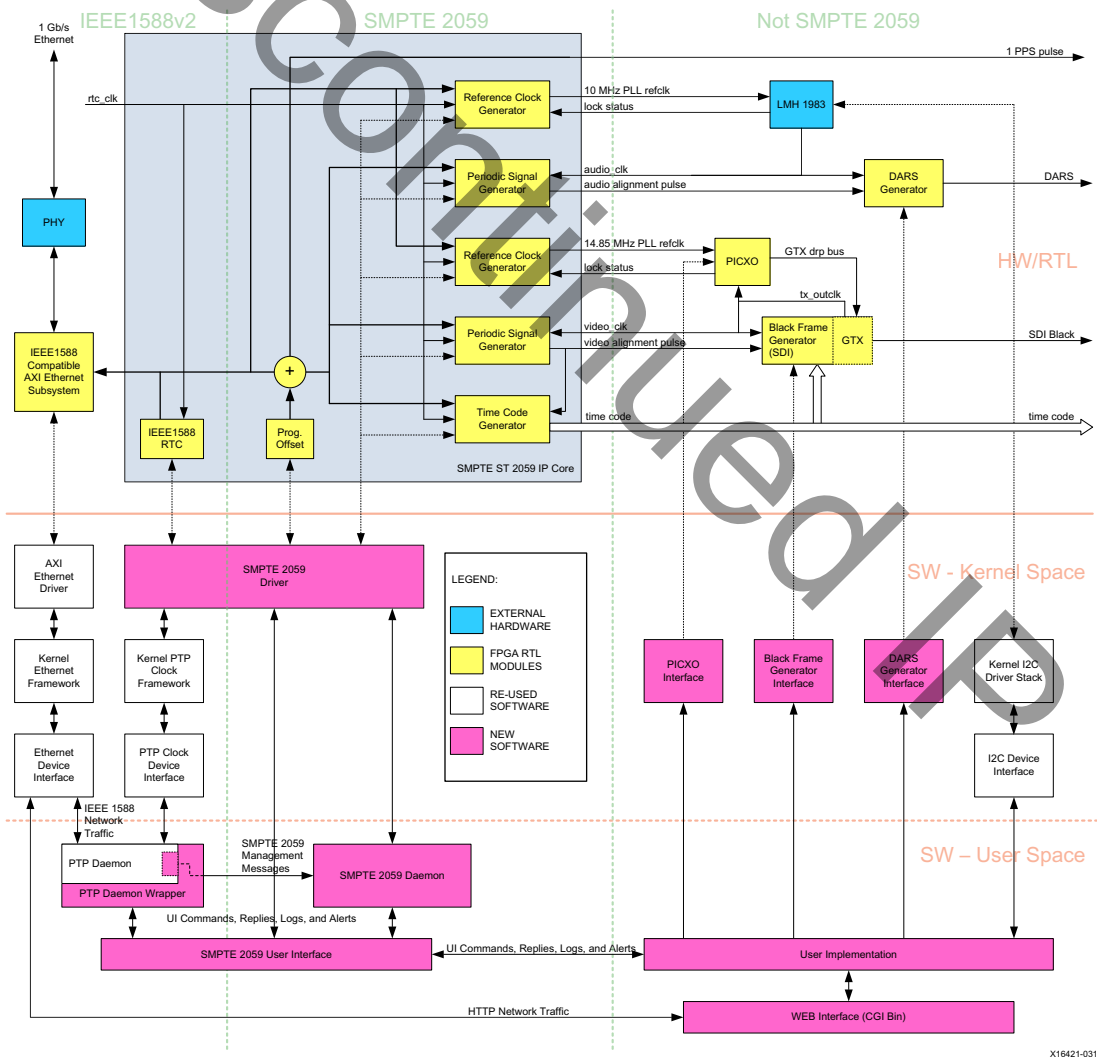


Figure 3-1: SMPTE ST 2059 Functional System Architecture Diagram

The SMPTE ST 2059 core connects to a Xilinx Ethernet MAC subsystem which is configured to have IEEE1588 timestamping enabled, through which the core is communicating with the Grandmaster. Synchronization is achieved by means of timestamping IEEE1588 PTP event packets, and measuring time offsets and delays, by comparing master and slave timestamps. As a guideline, if the offset is below 1,000 ns, the synchronization is considered to be achieved. The SMPTE ST2059-1 standard defines how video and audio signals are aligned to an epoch, and at which values of the PTP clock these signals shall recur. The SMPTE ST 2059 module generates relevant video, audio, and time code reference signals in accordance with the SMPTE ST2059-1 standard.

The SMPTE ST 2059 core generates “synchronized” PLL reference signals with programmable frequency which can be fed into an external clock generator to generate video, audio clock to be used in video, and audio sync signal generation.

For instance, the audio clock, along with the audio alignment pulse, is used to feed the Digital Audio Reference Signal (DARS) generator.

The same PLL reference signal can also be used in adjacent with the Phase Interpolator Controlled XTAL Oscillator (PICXO) to generate video stream which is locked to the master clock from PTP. For more information about PICXO, see *All Digital VCXO Replacement for Gigabit Transceiver Applications (7-Series/Zynq-7000)* (XAPP589) [Ref 4]. The video PLL reference clock can typically be set to 14.85 or 14.85/1.001 MHz. The video clock, along with the video alignment pulse, feed the SDI black frame generator to create synchronized video stream.

The Time Code Generator produces the SMPTE ST12-1 Time Code as function of the PTP time. This Time Code is fed to the SDI black frame generator so that the Time Code can be embedded in the SDI black reference signal.

Clocking

The SMPTE ST 2059 IP core has the following clock domains:

- AXI4-Lite clock domain recommended running at 100 MHz
- RTC clock domain at 125 MHz
- Video clock domain at 148.50 MHz/74.25 MHz (and /1.001 rate)
- Audio clock domain at 98.304 MHz/90.3168 MHz

The video and audio clock domain existence depends on the availability of the associated ports, which can be selected during customization of the core.

Resets

The SMPTE ST 2059 IP core has the following resets:

- AXI4-Lite domain reset, `s_axi_aresetn`
- RTC domain reset, `rtc_reset`

Design Flow Steps

This chapter describes customizing and generating the core, constraining the core, and the simulation, synthesis and implementation steps that are specific to this IP core. More detailed information about the standard Vivado® design flows and the IP integrator can be found in the following Vivado Design Suite user guides:

- *Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator* (UG994) [Ref 5]
- *Vivado Design Suite User Guide: Designing with IP* (UG896) [Ref 6]
- *Vivado Design Suite User Guide: Getting Started* (UG910) [Ref 7]
- *Vivado Design Suite User Guide: Logic Simulation* (UG900) [Ref 8]

Customizing and Generating the Core

This section includes information about using Xilinx tools to customize and generate the core in the Vivado Design Suite.

If you are customizing and generating the core in the Vivado IP integrator, see the *Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator* (UG994) [Ref 5] for detailed information. IP integrator might auto-compute certain configuration values when validating or generating the design. To check whether the values do change, see the description of the parameter in this chapter. To view the parameter value, run the `validate_bd_design` command in the Tcl console.

You can customize the IP for use in your design by specifying values for the various parameters associated with the IP core using the following steps:

1. Select the IP from the Vivado IP catalog.
2. Double-click the selected IP or select the **Customize IP** command from the toolbar or right-click menu.

For details, see the *Vivado Design Suite User Guide: Designing with IP* (UG896) [Ref 6] and the *Vivado Design Suite User Guide: Getting Started* (UG910) [Ref 7].

Note: Figures in this chapter are illustrations of the Vivado Integrated Design Environment (IDE). The layout depicted here might vary from the current version.

Vivado Integrated Design Environment

The SMPTE ST 2059 core is configured to meet the specific needs of the developer before instantiation through the Vivado IDE. This section provides a quick reference to parameters that can be configured at generation time.

Figure 4-1 shows the SMPTE ST 2059 Vivado IDE main configuration screen.

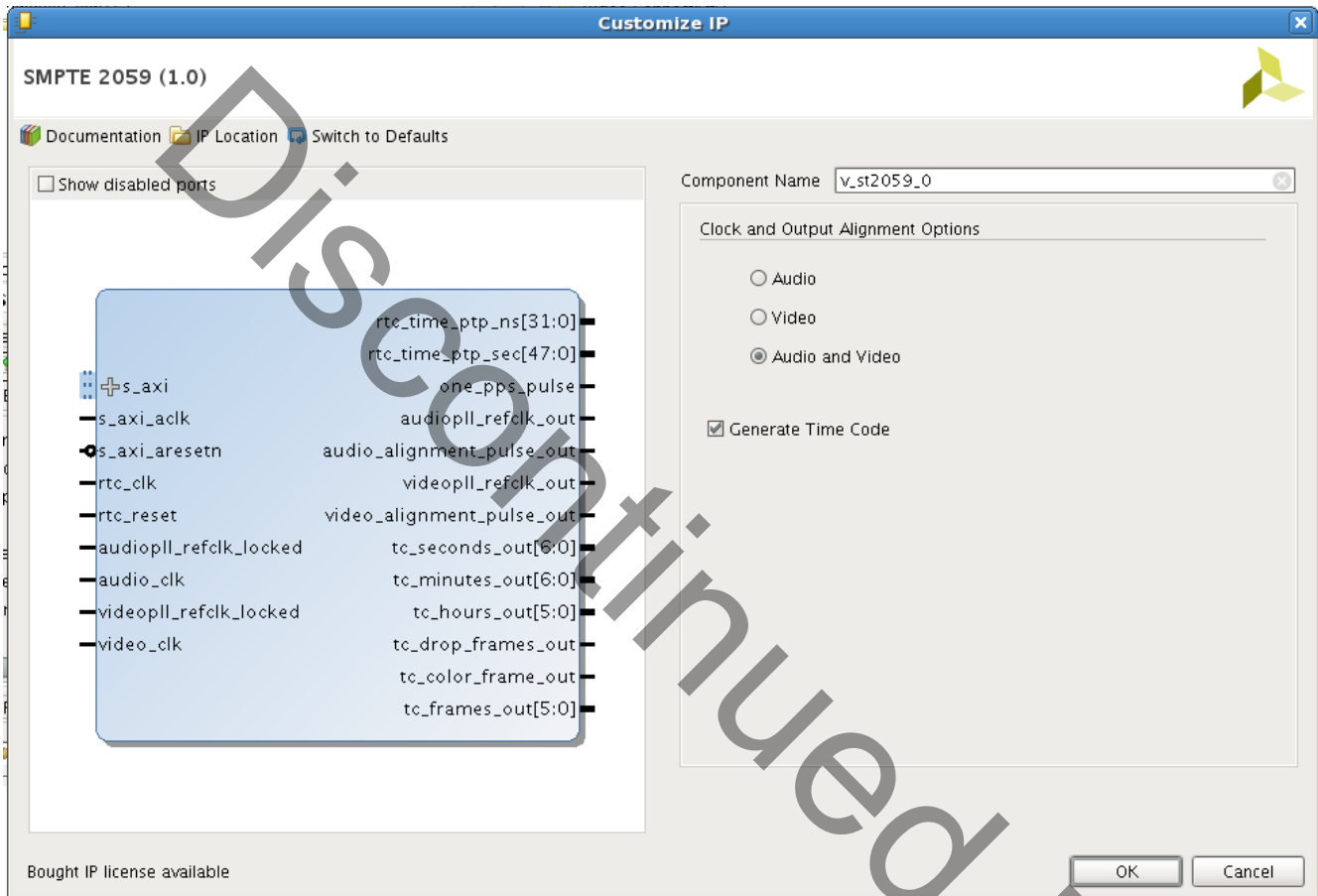


Figure 4-1: SMPTE ST 2059 Customize IP – Audio and Video with Generate Time Code

The screen displays a representation of the IP symbol on the left side, and the parameter assignments on the right side, which are described as follows:

- **Component Name** – The component name is used as the base name of output files generated for the module. Names must begin with a letter and must be composed from characters: a to z, 0 to 9 and "_".

Note: The name v_st2059 cannot be used as a component name.

- **Clock and Output Alignment Options** – Specifies whether to use Audio only, Video only, or Audio and Video.

- **Generate Time Code** – Specifies whether to generate Time Code output. This option is only available when Video is included in the **Clock and Output Alignment Options**.

Figure 4-2 shows the SMPTE ST 2059 Vivado IDE main configuration screen with the **Video** option with **Generate Time Code** checked.

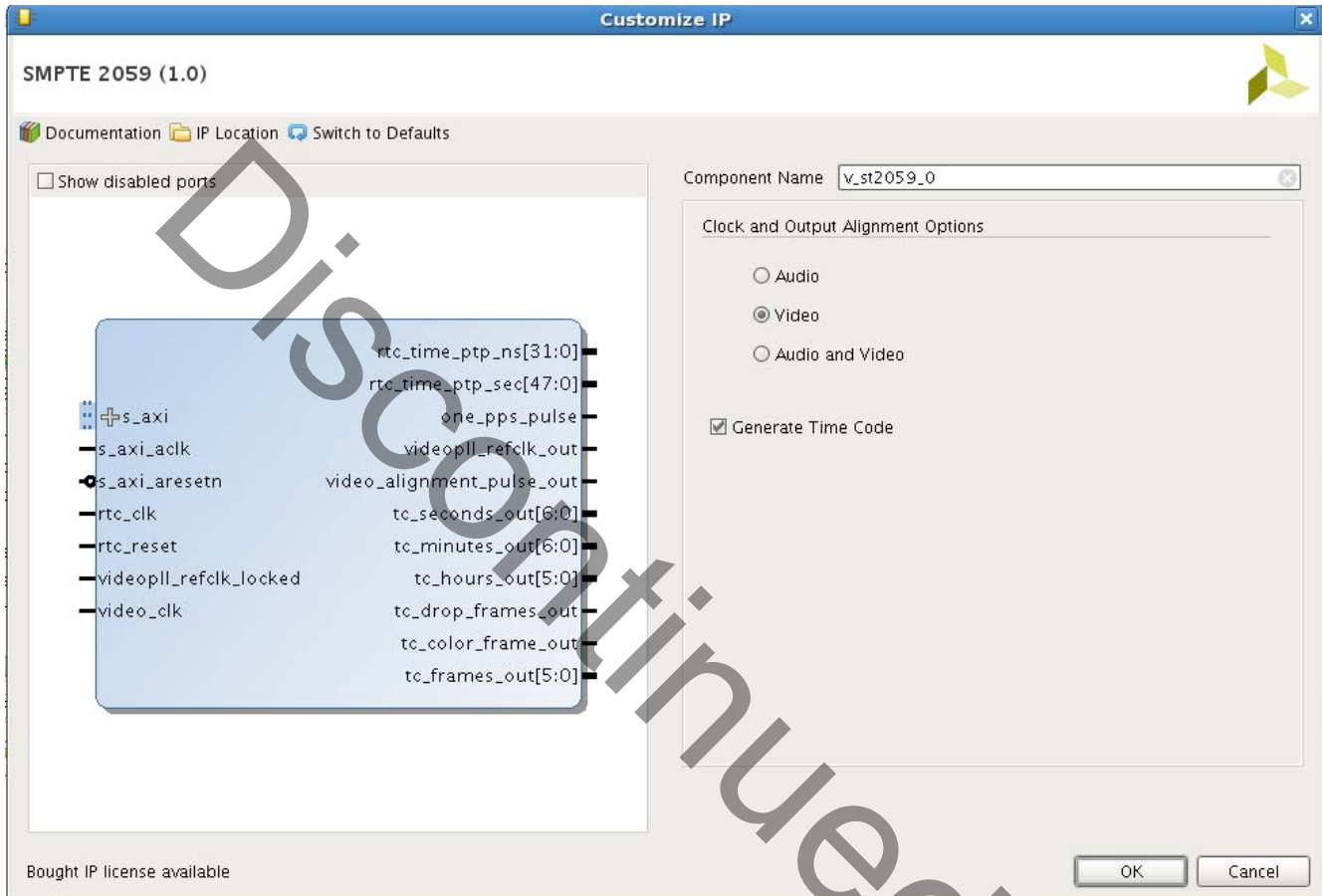


Figure 4-2: SMPTE ST 2059 Customize IP – Video with Generate Time Code

Figure 4-3 shows the SMPTE ST 2059 Vivado IDE main configuration screen with the **Audio** option.

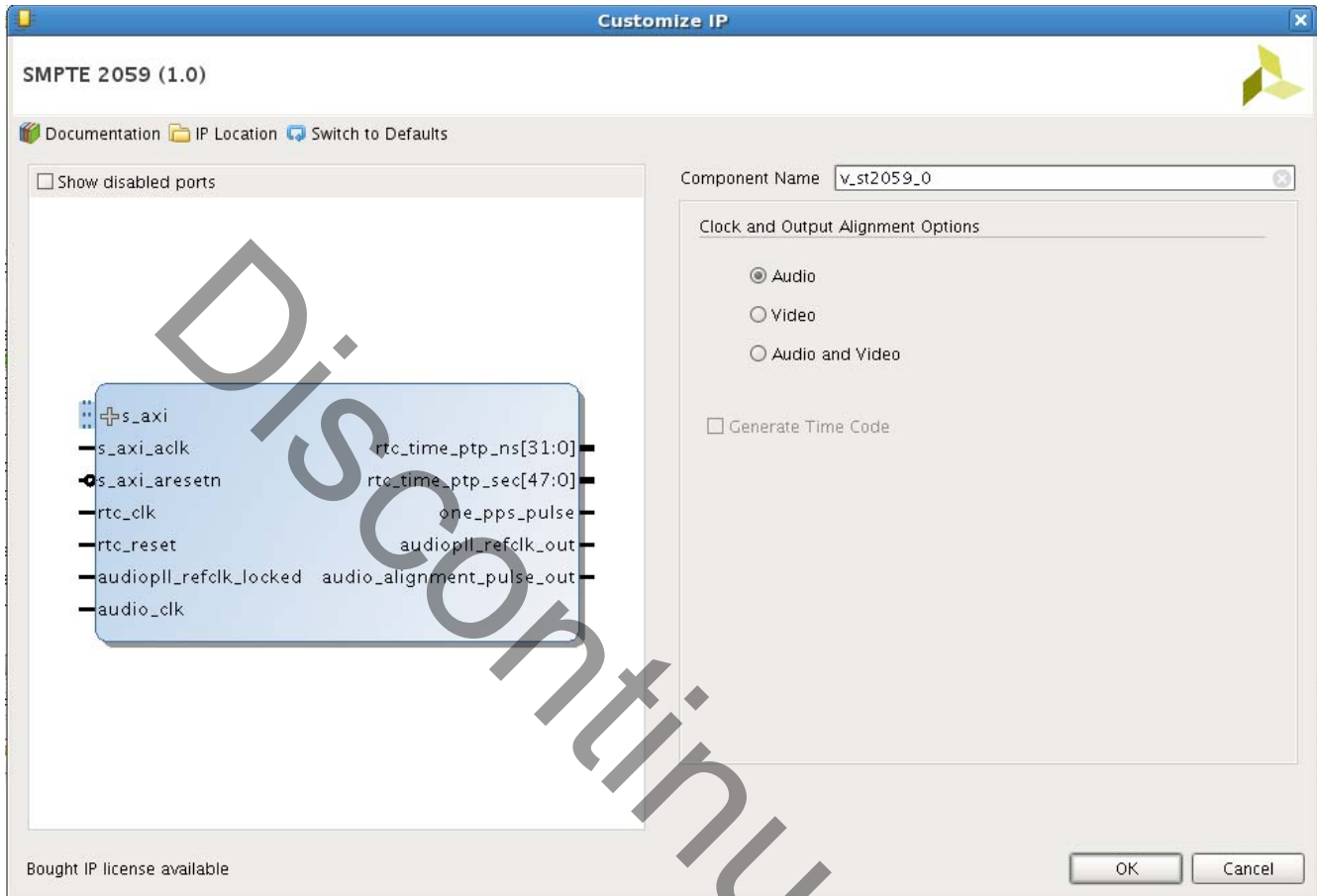


Figure 4-3: SMPTE ST 2059 Customize IP – Audio

Figure 4-4 shows the SMPTE ST 2059 Vivado IDE main configuration screen with the **Video** option.

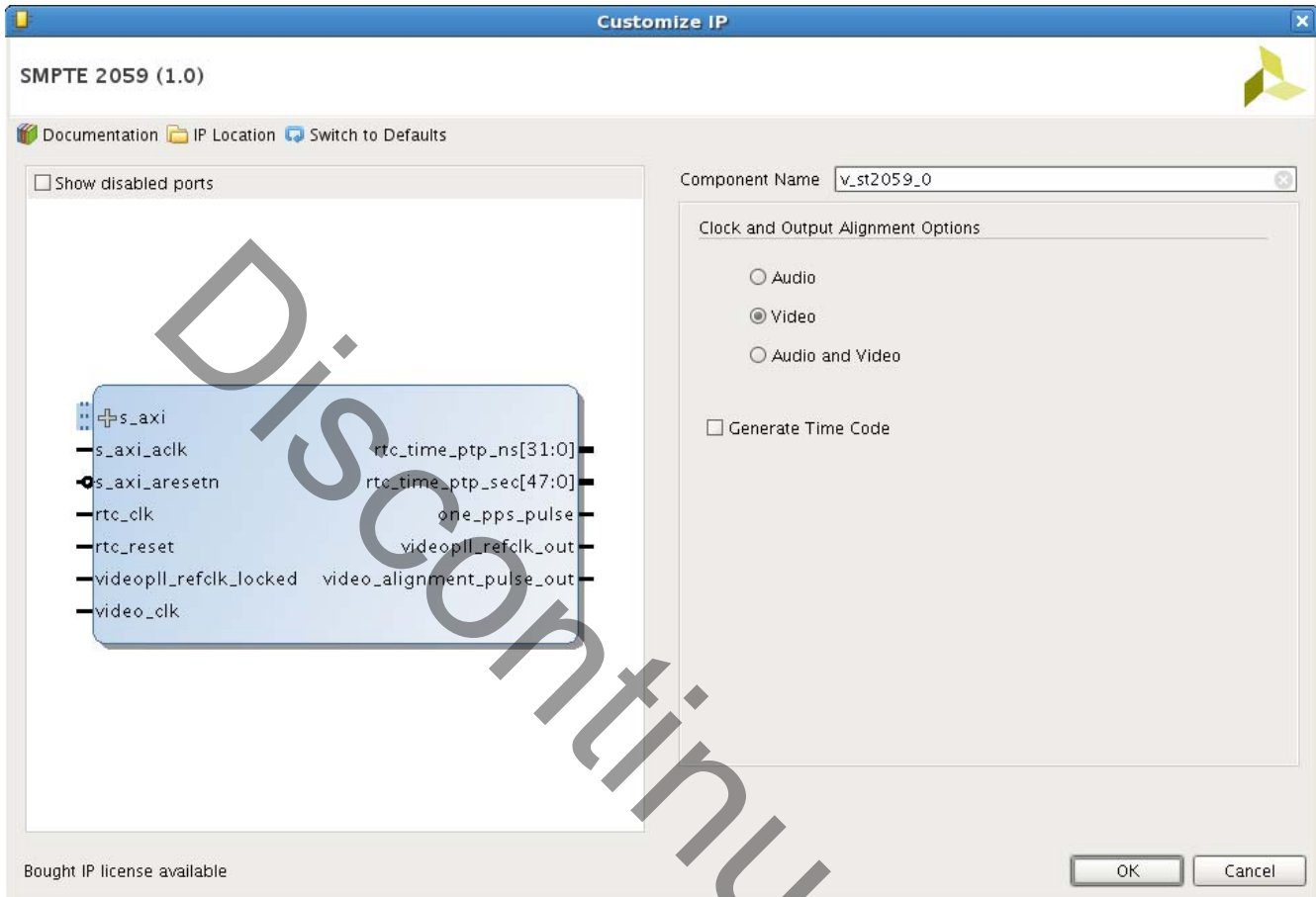


Figure 4-4: SMPTE ST 2059 Customize IP – Video

User Parameters

Table 4-1 shows the relationship between the fields in the Vivado IDE and the User Parameters (which can be viewed in the Tcl Console).

Table 4-1: Vivado IDE Parameter to User Parameter Relationship

Vivado IDE Parameter/Value ⁽¹⁾	User Parameter/Value ⁽¹⁾	Default Value
Clock and Output Alignment Options		Audio and Video
Audio	C_VID_REFCLK_EN/0 C_AUD_REFCLK_EN/1	
Video	C_VID_REFCLK_EN/1 C_AUD_REFCLK_EN/0	
Audio and Video	C_VID_REFCLK_EN/1 C_AUD_REFCLK_EN/1	

Table 4-1: Vivado IDE Parameter to User Parameter Relationship (Cont'd)

Vivado IDE Parameter/Value ⁽¹⁾	User Parameter/Value ⁽¹⁾	Default Value
Generate Time Code	C_INCLUDE_TIMECODE	1

Notes:

- Parameter values are listed in the table where the Vivado IDE parameter value differs from the user parameter value. Such values are shown in this table as indented below the associated parameter.

Output Generation

For details, see the *Vivado Design Suite User Guide: Designing with IP* (UG896) [Ref 6].

Constraining the Core

This section contains information about constraining the core in the Vivado Design Suite.

Required Constraints

Constraints required for the core are clock frequency constraints for the clock domains described in [Clocking in Chapter 3](#). Paths between the clock domains are constrained with a `max_delay` constraint and use the `datapathonly` flag, causing setup and hold checks to be ignored for signals that cross clock domains. These constraints are provided in the Xilinx Design Constraints (XDC) constraints file included with the core.

Device, Package, and Speed Grade Selections

This section is not applicable for this IP core.

Clock Frequencies

See [Maximum Frequencies in Chapter 2](#).

Clock Management

See [Clocking in Chapter 3](#). The SMPTE ST 2059 core does not have any specific requirement for clock management.

However, the peripheral modules might have the clock that is connected to the `rtc_clk` input is provided through the AXI Ethernet Subsystem, which contains the `IBUFDS_GTE2` and `BUFG` primitives for the 125 MHz.

Clock Placement

The SMPTE ST 2059 core can use any clock as long as the peripheral modules can be supported in the selected devices. For example, 1588 Enabled AXI Ethernet Subsystem, PICXO, etc.

Banking

No specific requirement on which bank to choose for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

The SMPTE ST 2059 core does not have any specific requirement on I/O standards. However, because it is used together with the AXI 1G Ethernet Subsystem, any requirements are needed by the AXI Ethernet Subsystem are inherited.

Simulation

For comprehensive information about Vivado simulation components, as well as information about using supported third-party tools, see the *Vivado Design Suite User Guide: Logic Simulation* (UG900) [Ref 8].



IMPORTANT: For cores targeting 7 series or Zynq-7000 devices, UNIFAST libraries are not supported. Xilinx IP is tested and qualified with UNISIM libraries only.

Synthesis and Implementation

For details about synthesis and implementation, see the *Vivado Design Suite User Guide: Designing with IP* (UG896) [Ref 6].

Test Bench

This chapter contains information about the test bench provided in the Vivado® Design Suite.

Demonstration Test Bench

A demonstration test bench is provided with the core which enables you to observe core behavior in a typical scenario. This test bench is generated together with the core in Vivado Design Suite. In this test bench, frequencies for video clock, audio clock, RTC clock, and AXI4-Lite CPU clocks are pre-defined.

By design, the DUT is able to output four types of signals, which are RTC, audio alignment pulses, video alignment pulses, and time code. Based on the Vivado Integrated Design Environment (IDE) options selected, the DUT outputs all or a subset of these four types of signals and the test bench generates stimulus accordingly. Checkers are designed in the test bench to check the correctness of the output signals. Status is reported during and at the end of the test.

Directory and File Contents

The following file is expected to be generated in the demonstration test bench output directory:

The test bench:

```
tb_<IP_instance_name>.v
```

Test Bench Structure

The top-level entity is `tb_<IP_instance_name>`.

It instantiates the following module:

```
dut
```

The SMPTE ST 2059 core instance under test.

Migrating and Upgrading

This appendix contains information about upgrading to a more recent version of the IP core.

Upgrading in the Vivado Design Suite

This section is not applicable for the first release of the core.

Discontinued IP

Debugging

This appendix includes details about resources available on the Xilinx Support website and debugging tools.

Finding Help on Xilinx.com

To help in the design and debug process when using the SMPTE ST 2059, the [Xilinx Support web page](#) contains key resources such as product documentation, release notes, answer records, information about known issues, and links for obtaining further product support.

Documentation

This product guide is the main document associated with the SMPTE ST 2059. This guide, along with documentation related to all products that aid in the design process, can be found on the [Xilinx Support web page](#) or by using the Xilinx Documentation Navigator.

Download the Xilinx Documentation Navigator from the [Downloads page](#). For more information about this tool and the features available, open the online help after installation.

Answer Records

Answer Records include information about commonly encountered problems, helpful information on how to resolve these problems, and any known issues with a Xilinx product. Answer Records are created and maintained daily ensuring that users have access to the most accurate information available.

Answer Records for this core can be located by using the Search Support box on the main [Xilinx support web page](#). To maximize your search results, use proper keywords such as

- Product name
- Tool message(s)
- Summary of the issue encountered

A filter search is available after results are returned to further target the results.

Master Answer Record for the SMPTE ST 2059

AR: [66768](#)

Technical Support

Xilinx provides technical support at the [Xilinx Support web page](#) for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support if you do any of the following:

- Implement the solution in devices that are not defined in the documentation.
- Customize the solution beyond that allowed in the product documentation.
- Change any section of the design labeled DO NOT MODIFY.

To contact Xilinx Technical Support, navigate to the [Xilinx Support web page](#).

Debug Tools

There are many tools available to address SMPTE ST 2059 design issues. It is important to know which tools are useful for debugging various situations.

Vivado Design Suite Debug Feature

The Vivado® Design Suite debug feature inserts logic analyzer and virtual I/O cores directly into your design. The debug feature also allows you to set trigger conditions to capture application and integrated block port signals in hardware. Captured signals can then be analyzed. This feature in the Vivado IDE is used for logic debugging and validation of a design running in Xilinx devices.

The Vivado logic analyzer is used with the logic debug IP cores, including:

- ILA 2.0 (and later versions)
- VIO 2.0 (and later versions)

See the *Vivado Design Suite User Guide: Programming and Debugging* (UG908) [\[Ref 9\]](#).

Hardware Debug

Hardware issues can range from link bring-up to problems seen after hours of testing. This section provides debug steps for common issues. The Vivado debug feature is a valuable resource to use in hardware debug. The signal names mentioned in the following individual sections can be probed using the debug feature for debugging the specific problems.

General Checks

Ensure that all the timing constraints for the core were properly incorporated from the example design and that all constraints were met during implementation.

- Does it work in post-place and route timing simulation? If problems are seen in hardware but not in timing simulation, this could indicate a PCB issue. Ensure that all clock sources are active and clean.
- If using MMCMs in the design, ensure that all MMCMs have obtained lock by monitoring the `locked` port.
- If your outputs go to 0, check your licensing.

Interface Debug

AXI4-Lite Interfaces

Read from a register that does not have all 0s as a default to verify that the interface is functional. Output `s_axi_arready` asserts when the read address is valid, and output `s_axi_rvalid` asserts when the read data/response is valid. If the interface is unresponsive, ensure that the following conditions are met:

- The `s_axi_aclk` and `aclk` inputs are connected and toggling.
- The interface is not being held in reset, and `s_axi_areset` is an active-Low reset.
- The interface is enabled, and `s_axi_aclken` is active-High (if used).
- The main core clocks are toggling and that the enables are also asserted.
- If the simulation has been run, verify in simulation and/or a debug feature capture that the waveform is correct for accessing the AXI4-Lite interface.

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see [Xilinx Support](#).

References

These documents provide supplemental material useful with this product guide:

1. *SMPTE ST 2059-1:2015 Generation and Alignment of Interface Signals to the SMPTE Epoch* [web page](#), registration required
2. *SMPTE ST 2059-2:2015 SMPTE Profile for Use of IEEE-1588 Precision Time Protocol in Professional Broadcast Applications* [web page](#), registration required
3. *IEEE 1588-2008 Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems* [web page](#), registration required
4. *All Digital VCXO Replacement for Gigabit Transceiver Applications (7 Series/Zynq-7000)* ([XAPP589](#))
5. *Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator* ([UG994](#))
6. *Vivado Design Suite User Guide: Designing with IP* ([UG896](#))
7. *Vivado Design Suite User Guide: Getting Started* ([UG910](#))
8. *Vivado Design Suite User Guide: Logic Simulation* ([UG900](#))
9. *Vivado Design Suite User Guide: Programming and Debugging* ([UG908](#))
10. *Vivado Design Suite User Guide: Implementation* ([UG904](#))

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
04/06/2016	1.0	Initial Xilinx release.

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