UHD SDI Audio v1.0

LogiCORE IP Product Guide

Vivado Design Suite

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IP Facts

The Xilinx® UHD SDI Audio Core is configurable as an Audio Embedder or an Audio Extractor. When configured as an Audio Embedder, it can embed up to 16 channels (8 channel pairs) of synchronous audio onto an SDI stream. Similarly, when configured as an Audio Extractor, it can extract up to 16 channels (8 channel pairs) of synchronous audio from the incoming SDI stream. In both the configurations, it supports multiple audio sample rates (32 KHz, 44.1 KHz and 48 KHz). It is designed in accordance with SMPTE ST 272 for SD-SDI and SMPTE ST 299-1 for HD/3G/6G/12G-SDI.

The SDI Audio Embedder allows embedding of AES3 audio packets coming over AXI4-Stream audio interface to the user selected audio groups. Similarly, SDI Audio Extractor allows extraction of audio data from the user selected audio groups and output them in AES3 format on AXI4-Stream audio interface.

This IP includes standard bus interfaces to the AMBA® AXI4-Lite and AXI4-Stream interfaces, allowing for easier integration of the IP with other Audio Interface IPs for further processing of audio data.

Features

- Configurable as an Audio Embedder or an Audio Extractor.
- Common features between the Audio Embedder and the Audio Extractor modes.
  - Supports up to 16 channels (8 channel pairs) of synchronous audio.
  - Multiple audio sample rates (32 KHz, 44.1 KHz and 48 KHz).
  - Audio sample length of 20/24-bit.
  - AXI4-Stream interface to carry audio samples in AES3 format.
  - Programmable maximum audio channels.
  - Programmable audio group for embedding and extraction of audio.
  - AXI4-Lite and port based interface for configuration of the core.
  - Detects the presence of pre-embedded audio groups on SDI interface.

- Key features of the Audio Embedder
  - Control packets are inserted on appropriate lines.
  - Pre-embedded audio packets on selected group are overwritten with new packets.
- Key features of the Audio Extractor
  - Reports parity and checksum errors.
  - Supports extraction of 192 bit channel status.
  - Muting of user selected audio channel on AXI4-Stream interface.

IP Facts

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family[1]	UltraScale+™Families, Zynq® UltraScale+™ MPSoC, UltraScale Architecture
Supported User Interfaces	AXI4-Stream, AXI4-Lite, and Native SDI
Resources	Performance and Resource Use web page
Provided with Core	
Design Files	Register Transfer Lever (RTL)
Example Design	Verilog
Test Bench	Not Provided
Constraints File	XDC
Simulation Model	Not Provided
Supported S/W Driver[2]	Standalone
Tested Design Flows[3]	
Design Entry	Vivado Design Suite
Simulation	For supported simulators, see the Xilinx Design Tools: Release Notes Guide.
Synthesis	Vivado Synthesis
Support	
Provided by Xilinx® at the Xilinx Support web page	

Notes:

1. For a complete list of supported devices, see the Vivado IP catalog.
2. Standalone driver details can be found in the software development kit (SDK) directory (<install_directory>/SDK/<release>/data/embeddedsw/doc/xilinx_drivers.htm). Linux OS and driver support information is available from the Xilinx Wiki page.
3. For the supported versions of the tools, see the Xilinx Design Tools: Release Notes Guide.

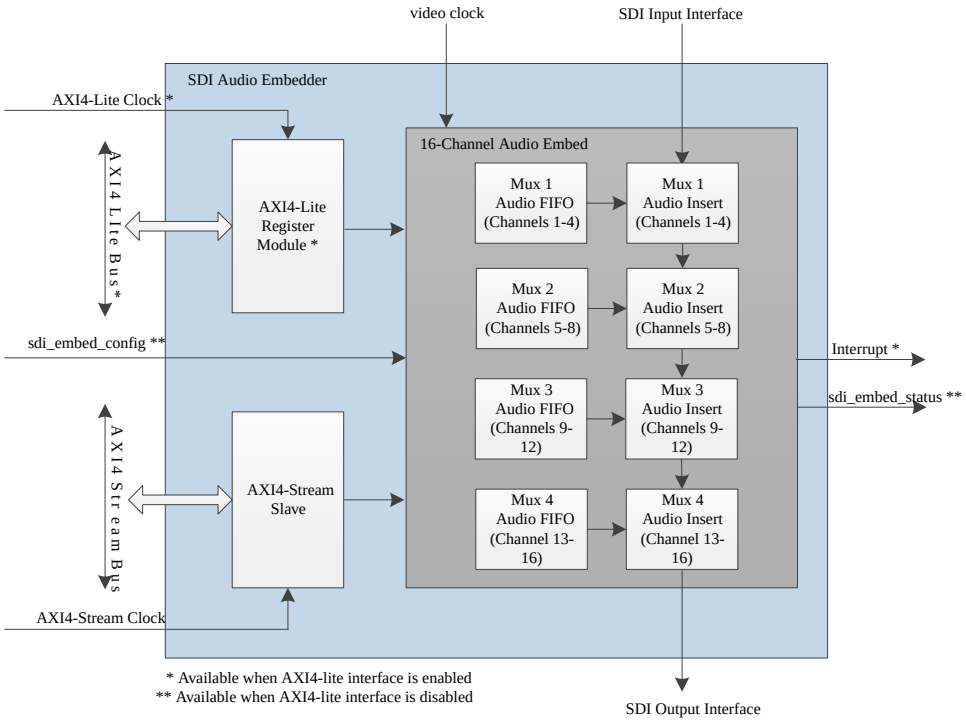
Overview

The Xilinx® UHD SDI Audio IP core can be configured as an Audio Embedder or an Audio Extractor.

- **Audio Embedder Configuration:** Receives audio data on AXI4-Stream slave interface and video data on SDI input interface. Audio embedded video data is sent back to the SDI Transmitter on SDI output interface.
- **Audio Extractor Configuration:** Receives audio embedded video data on the SDI input interface. Extracted audio data is sent out on AXI4-Stream master interface.

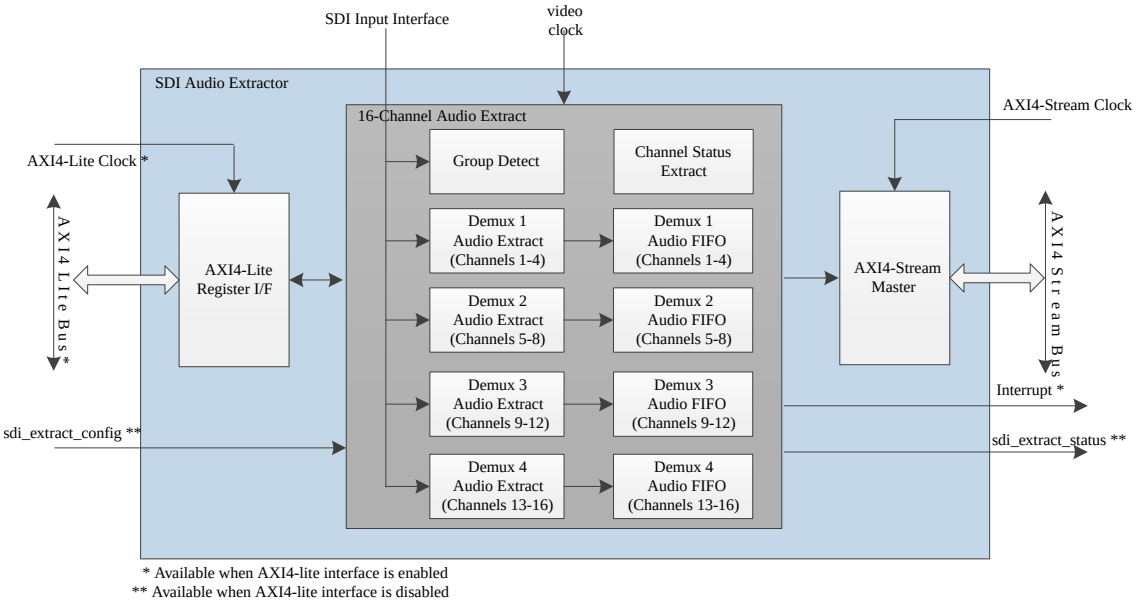
The following figure shows the top level block diagram of SDI Audio Embedder in 16 channel configuration.

Figure 1: **Block Diagram of SDI Audio Embedder**



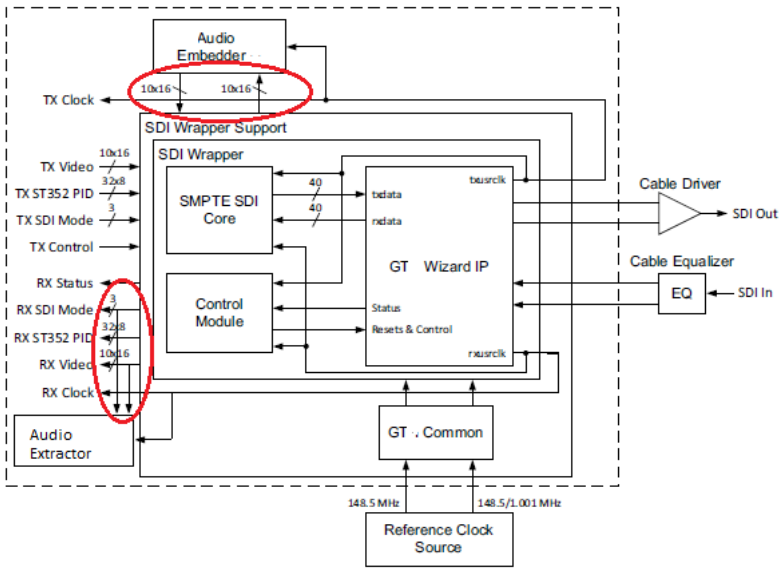
The following figure shows the top level block diagram of SDI Audio Extractor in 16 channel configuration

Figure 2: **Block Diagram of SDI Audio Extractor**



The following figure highlights the interface between the typical Xilinx SDI core and the Audio Embedder and Extractor.

Figure 3: **Block Diagram of SDI Core with Audio Embedder and Extractor**



Applications

- SDI Audio Embedding
- SDI Audio Extraction

Unsupported Features

- Audio sample rate of 96 KHz is not supported
- The 16-way data stream interleaving is not supported when SDI Audio core is used with Xilinx UHD SDI Transmitter/Receiver subsystem.
- In non-SD SDI mode, SDI Audio core does not support Luma and CbCr multiplexed on single data stream (Luma and CbCr should be on separate data streams).

Licensing and Ordering

This Xilinx® LogiCORE™ IP module is provided at no additional cost with the Xilinx® Vivado® under the terms of the Xilinx End User License.

Product Specification

The Xilinx® UHD SDI Audio IP core is configurable as an Audio Embedder or an Audio Extractor. The UHD SDI Audio core is designed in accordance with the SMPTE ST 272 for SD-SDI and SMPTE ST 299-1 for HD/3G/6G/12G-SDI.

The SDI Audio Embedder consists of the following sub-blocks:

- AXI4-Lite Register Module (when AXI4-Lite is enabled)
- AXI4-Stream Slave
- Audio Multiplexers
- Audio Group Detect

The SDI Audio Extractor consists of the following sub-blocks:

- AXI4-Lite Register Module (when AXI4-Lite is enabled)
- AXI4-Stream Master
- Audio De-multiplexers
- Audio Group Detect
- Channel Status Extract

For a description of the Audio Embedder and Extractor sub-blocks, see Programmable Maximum Audio Channels (PMAC), AES3 Data Format, and AXI4-Stream Audio Interface. These concepts are explained in the following sections.

Programmable Maximum Audio Channels (PMAC)

In an Audio Embedder generated with Maximum Audio Channels set to 'N', AXI4-Stream Slave module waits for 'N' number of audio samples (one sample per channel) to be received from external AXI4-Stream interface master before sending them on to audio multiplexer engines for insertion. Similarly, In an Audio Extractor generated with Maximum Audio Channels set to 'N', AXI4-Stream Master module wait for 'N' number of audio samples (one sample per channel) to be received from audio de-multiplexer engines before sending them out on audio interface to the external AXI4-Stream interface slave. In both the scenarios, 'N' is an important number conveying the number of audio channels that Audio Embedder or Extractor should work on.

In order to support the flexible number of audio channels with in the Maximum Audio Channels (MAC) set during the core generation, SDI Audio Embedder and Extractor provides Programmable Maximum Audio Channels (PMAC) control. User need to make sure that PMAC is an even number and it should be less than or equal to the MAC.

The PMAC overwrites the MAC value and limits the Audio Embedder or Extractor generated to support higher channels to work with lower channel source or sink. One of the use cases is integrating 2 channel Xilinx AES3/SPDIF core with the Audio Embedder or Extractor core generated to support 16 channels.

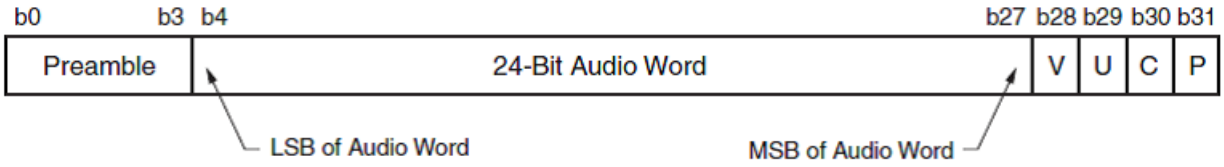
IMPORTANT!: *Due to a limitation in the blanking period available, a maximum of 8 audio channels per data stream can be embedded or extracted in 2048x1080p/i 29.97/30 Hz & 4096x2160p/i 29.97/30 Hz video resolutions.*

Note: Programming a PMAC (Register offset – 0x1C) is mandatory even if it is same as the MAC set during core generation.

AES3 Data Format

This section focuses on the standard two-channel PCM audio described in the AES3 specification.The basic data structure of AES3 is called a sub-frame. Each 32-bit sub-frame contains a single audio sample for one audio channel along with a few other bits of information as shown in the following figure. A sub-frame begins with a 4-bit preamble. The audio word can be either 24 bits or 20 bits. Following the audio word are the valid (V), user data (U), channel status (C), and parity (P) bits.

Figure 4: **AES3 Subframe Format with 24-Bit Audio Sample**



The preamble provides the start of the audio block (0x1) and audio channel information (0x2 - Channel 1 of pair and 0x3 - Channel 2 of pair). Bits[27:4] carry the audio data MSB bit at the 27th position and the LSB position is based on the audio sample length. Bit[28] provides the audio validity information. Bit[29] carries the user data information, and Bit[30] carries the channel status bit. Bit[31] is the even parity over 32 bits except for the preamble bits.

Two consecutive subframes, one for each of the two audio channels, form a complete frame. Frames are grouped together in blocks of 192 frames. This grouping of frames into blocks serves to define the beginning and ending points for the sequence of channel status and user data bits.

AXI4-Stream Audio Interface

The AXI4-Stream Audio Interface carries audio samples in AES3 format. The data width over the AXI4-Stream Audio Interface is fixed at 32 bits to carry one sub-frame as shown in the Figure 4: AES3 Subframe Format with 24-Bit Audio Sample. The TID indicates the channel number of the audio sample data (TID is 0 for channel 1 and TID is 1 for channel 2).

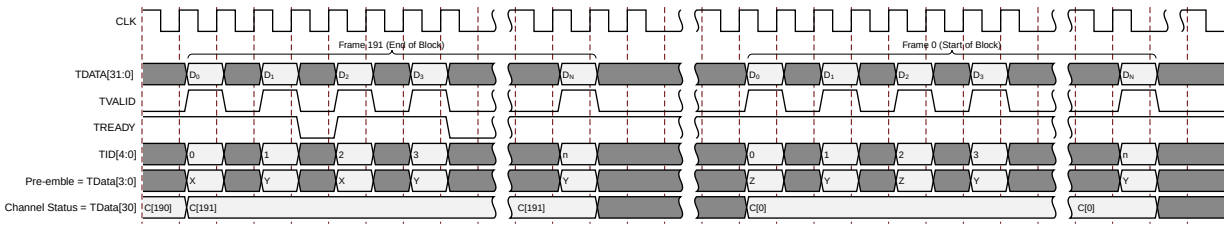
The following figure highlights the mapping of AXI4-Stream TID when PMAC is set to 16. Audio data on AXI4-Stream interface start with TID of 0 and increments all the way to 15 (PMAC-1).

Figure 5: **Mapping of AXI4-Stream TID in 16 Channel System**

Channel Number	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Channel Pair Number	1		2		3		4		5		6		7		8	
Channel in Pair	1	2	1	2	1	2	1	2	1	2	1	2	1	2	1	2
AXI4-Stream TID	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

When PMAC is set to N, N number of audio samples (each from individual channel) form a frame. Group of 192 frames form a block. The following figure highlights the frame structure and the block transition in multi-channel AXI4-Stream Audio Interface.

Figure 6: **Multi-Channel AXI4-Stream Audio Interface**



AXI4-Lite Register Module

The AXI4-Lite Register Module provides the read/write control logic for the core register set. The registers are accessible by the external AXI4-Lite master. The data width of the AXI4-Lite interface is fixed at 32 bits.

The interrupt control and soft reset functionality are also implemented as part of the register module. The core register set can be reset by writing 0x1 to the soft reset register (offset - 0x04).

AXI4-Stream Slave

The audio interface to an Audio Embedder is a 32-bit AXI4-Stream slave bus. AXI4-Stream Slave module generates the handshaking signal `s_axis_tready` after receiving the streaming data (`s_axis_tdata`), data valid signal (`s_axis_tvalid`), and channel number identification (`s_axis_tid`). This also generates the Channel FIFO write control signals and transfers the data received from the AXI4-Stream interface to the Channel FIFO Module. If any of the Channel FIFOs are full, this module stops receiving the audio samples by driving the handshake signal `s_axis_tready` low.

The AXI4-Stream Slave module strictly expects audio channels on the AXI4-Stream Interface to come in an incremental order. For example, when PMAC is set to N, audio for channel 1 (TID = 0) should be followed by channel 2 (TID = 1) which should then be followed by incremental channels all the way to channel N (TID = N-1). The AXI4-Stream Slave module tracks the expected TID and drops the samples that do not match the expected TID. On reset, expected TID is 0 which increments to 1 when an audio sample with TID 0 is received. After receiving the audio sample from the N'th audio channel, the expected TID rolls back to 0.

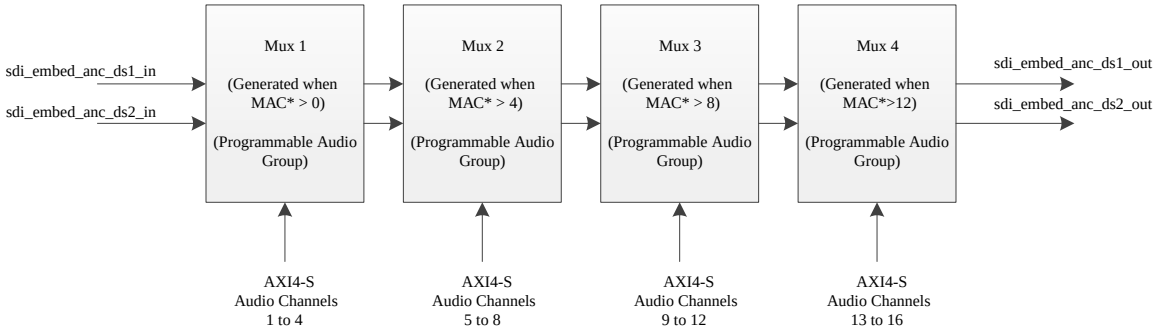
In an Audio Embedder configured for N number of audio channels (PMAC set to N), AXI4-Stream Slave module waits for N number of audio samples (one sample per channel) to be received from an external AXI4-Stream interface master before sending the samples on to the audio multiplexer engines for insertion.

***Note*:** The Audio Embedder strictly expects audio samples to be distributed on AXI4-Stream slave interface as per the audio sample rate. For example, in a 48 KHz audio sample rate, only one audio sample (for all channels) should be placed on AXI4-Stream Interface for every 48 KHz clock period.

Audio Multiplexer

Embedding of audio in SDI is performed on group granularity (each group consist of 4 audio channels). In an Audio Embedder generated with Maximum Audio Channels set to 16, four instances of audio multiplexer engines each working on a different group are daisy-chained as shown in the following figure. Audio samples on AXI4-Stream interface with TID 0 to 3 (Channel 1 to Channel 4) are embedded onto the selected group by Mux 1 instance. Similarly, audio samples with TID 4 to 7, 8 to 11 and 12 to 15 are embedded by Mux 2, 3 and 4 instances respectively.

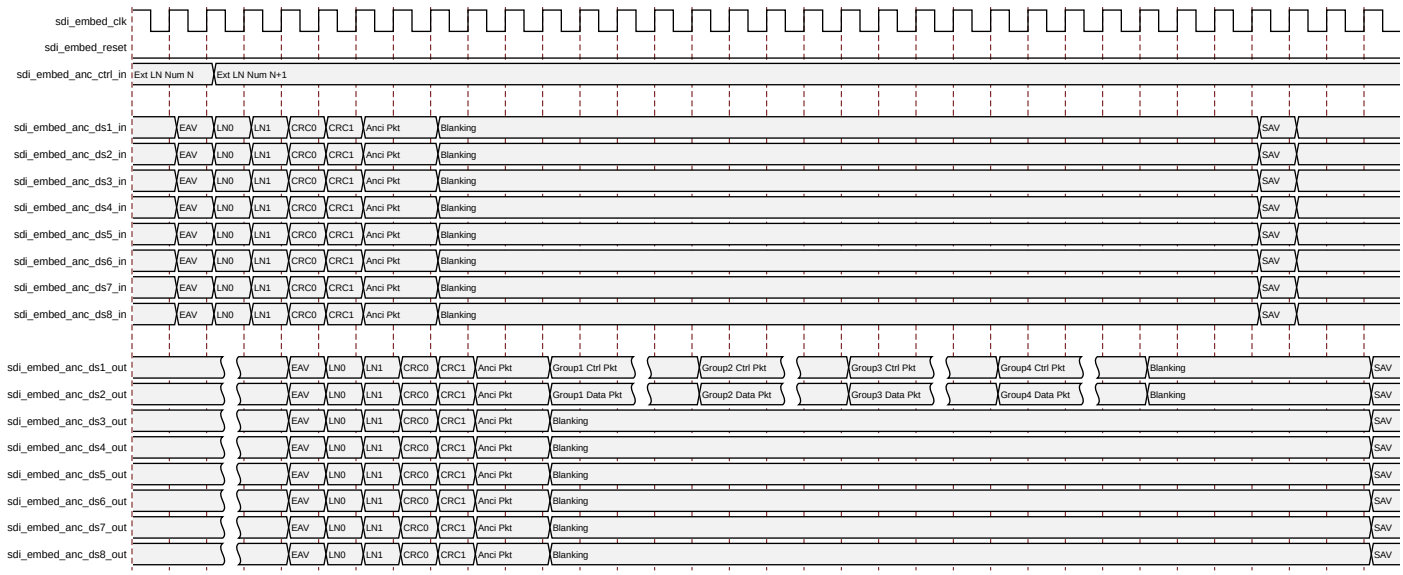
Figure 7: **Embedding Multiple Audio Groups**



In SD-SDI mode, as per SMPTE ST 272, up to 16 channels of audio should be inserted on data stream 1. In non-SD modes, as per SMPTE ST 299-1, up to 16 channels of audio should be inserted onto data stream 1 and 2. Audio control packets are inserted on data stream 1 (`sdi_embed_anc_ds1_in`) and audio data packets are inserted on data stream 2 (`sdi_embed_anc_ds2_in`). Remaining data streams from SDI Transmitter are delayed to match the audio insertion latency on data stream 1 and 2. Audio embedded and latency matched data streams are sent back to the SDI Transmitter for further processing.

The following figure highlights the SDI Interface to the Audio Embedder in 12G SDI mode with 8 data streams. Audio Embedder bypass the non-audio ancillary packets before inserting the audio packets into the blanking region.

Figure 8: **SDI Interface Diagram of Audio Embedder**



Audio Group Detect

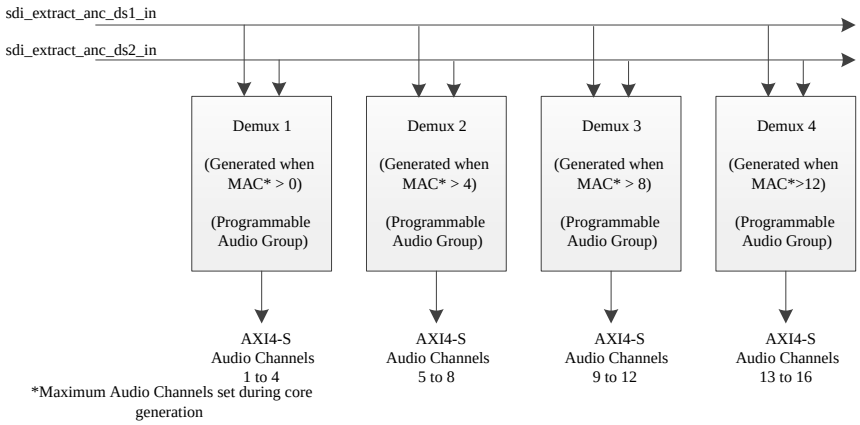
Audio group detect module checks for the presence of audio control packets in the SDI input interface. List of audio groups detected are reported through the host registers/status signals and an interrupt is asserted to indicate the change in groups present.

Audio Embedder can use this information to configure the audio multiplexer engines to retain the pre-embedded audio groups and to insert the new audio data on to unoccupied groups. Similarly, Audio Extractor can use this information to configure the audio de-multiplexer engines to extract the audio data from the groups that are present on the SDI interface.

Audio De-Multiplexer

Extraction of audio in SDI is performed on group granularity (each group consist of 4 audio channels). In an Audio Extractor generated with Maximum Audio Channels set to 16, four instances of audio de-multiplexer engines each working on a different group are connected in parallel as shown in the following figure. Extracted audio channels from the audio de-multiplexer engines are sent to the AXI4-Stream Master module. Audio samples extracted by Demux 1 instance are sent on AXI4-Stream interface with TID 0 to 3 (Channel 1 to Channel 4). Similarly, Audio samples extracted from Demux 2, 3, and 4 instances are sent with TID 4 to 7, 8 to 11 and 12 to 15 respectively.

Figure 9: **Extracting Multiple Audio Groups**



In SD-SDI mode, as per SMPTE ST 272, up to 16 channels of audio should be extracted from data stream 1. In non-SD modes, as per SMPTE ST 299-1, up to 16 channels of audio should be extracted from data stream 1 and 2. Audio control packets are extracted from data stream 1 (`sdi_extract_anc_ds1_in`) and data packets are extracted from data stream 2 (`sdi_extract_anc_ds2_in`).

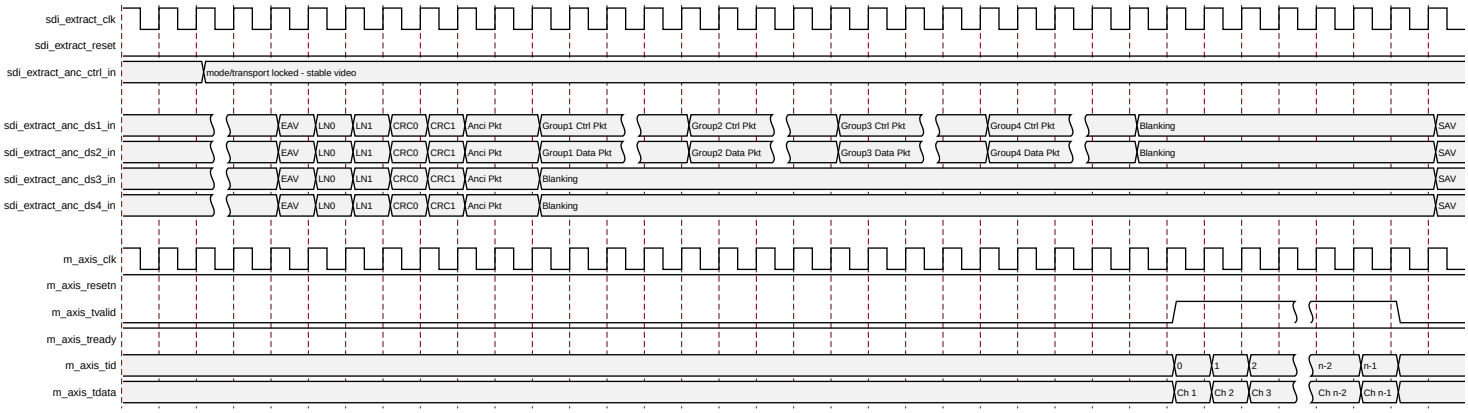
***Note*:** Data stream 3 and 4 are used to support 32-channel audio extraction in future versions of the core.

AXI4-Stream Master

The audio interface to an Audio Extractor is a 32-bit AXI4-Stream master bus. The AXI4-Stream Master module transfers the 32-bit data read from the non-empty FIFO's to the AXI4-Stream interface. The corresponding data valid signal (`m_axis_tvalid`) is set and the channel identifier signal (`m_axis_tid`) is driven with the corresponding channel number. This module depends on the handshaking signal m_axis_tready issued from the AXI4-Stream interface target slave for completion of the transfer.

In an Audio Extractor configured for N audio channels (PMAC set to N), AXI4-Stream Master Module wait for ‘N’ number of audio samples (one sample per channel) to be received from audio de-multiplexer engines before sending them out on audio interface to the external AXI4-Stream interface slave. The following figure highlights the interface diagram of the Audio Extractor.

Figure 10: **Interface Diagram of Audio Extractor**



Channel Status Extract

Extraction of channel status bits into channel status registers is configurable. Channel Status registers hold the 192-bit channel status information received over the SDI. This channel status information is captured from first audio channel, assuming that all the channels carry the same channel status. These registers are updated after one complete audio block is received. An interrupt is asserted to indicate the change in channel status information.

Standards

The UHD SDI Audio core is designed in accordance with the SMPTE ST 272 for SD-SDI and SMPTE ST 299-1 for HD/3G/6G/12G-SDI.

Performance

For full details about performance and resource use, visit the Performance and Resource Use web page.

Maximum Frequencies

Maximum frequency of AXI4-Stream and AXI4-Lite interface clock is 200 MHz.

In 12G-SDI mode, the maximum frequency of the video clock is 297 MHz. In 6G-SDI, 3G-SDI, and SD-SDI modes, the maximum frequency of the video clock is 148.5 MHz. In HD-SDI mode, the maximum frequency of the video clock is 74.25 MHz.

Resource Use

For full details about performance and resource use, visit the Performance and Resource Use web page.

Port Descriptions

The SDI Audio Embedder and Extractor I/O signals are listed and described in this section.

SDI Audio Embedder Input/output (I/O) Signals

The SDI Audio Embedder Input/output (I/O) signals are listed and described in the following sections.

Configuration Interface [when AXI4-Lite interface is enabled]

Table 1: **SDI Audio Embedder I/O Signal Description**

Port Name	Width	I/O	Description
s_axi_aclk	1	Input	AXI4-Lite clock
s_axi_aresetn	1	Input	AXI4-Lite reset, Active-Low
s_axi_awaddr	32	Input	AXI4-Lite Write address
s_axi_awprot	3	Input	Write protection
s_axi_awvalid	1	Input	Write address valid
s_axi_awready	1	Output	Write address ready
s_axi_wdata	32	Input	Write data bus
s_axi_wstrb	4	Input	Write strobes
s_axi_wvalid	1	Input	Write valid
s_axi_wready	1	Output	Write ready
s_axi_bresp	2	Output	Write response
s_axi_bvalid	1	Output	Write response valid
s_axi_bready	1	Input	Response ready
s_axi_araddr	32	Input	Read address
s_axi_arprot	3	Input	Read protection

Table 1: **SDI Audio Embedder I/O Signal Description** *(cont'd)*

Port Name	Width	I/O	Description
s_axi_arvalid	1	Input	Read address valid
s_axi_arready	1	Output	Read address ready
s_axi_rdata	32	Output	Read data bus
s_axi_rresp	2	Output	Read response
s_axi_rvalid	1	Output	Read valid
s_axi_rready	1	Input	Read ready

Configuration Interface [when AXI4-Lite interface is disabled]

When AXI4-Lite interface is disabled, register set is not instantiated in the core. Configuration and status are provided using the `sdi_embed_config` and the `sdi_embed_status` signals respectively.

Table 2: **SDI Audio Embedder I/O Signal Description**

Port Name	Width	I/O	Description
sdi_embed_config	64	Input	See SDI Audio Embedder Register Space for detailed information on the fields mentioned below [0] - embed_enable [1] - rate_control_enable [2] - soft_reset_core [3] - ext_ln_en [8:4]- line_std [9] - sd_samp_size_24 [12:10] - smpl_rate [17:13]- prog_max_audio_chan [18] - reserved [20:19] - mux 1 aud_group_sel [26:21] - reserved [28:27] - mux 2 aud_group_sel [34:29] - reserved [36:35] - mux 3 aud_group_sel [42:37] - reserved [44:43] - mux 4 aud_group_sel [63:45] - reserved
sdi_embed_status	64	Output	See SDI Audio Embedder Register Space for detailed information on the fields mentioned below [7:0] - reserved [8] - aud_group_change [9] - reserved [13:10] - group_present_val [17:14] - reserved [21:18] - max_audio_channels [23:22] - uhdsdi_standard [24] - audio_function [25] - axi_lite [63:26] - reserved

AXI4-Stream Slave Interface [Audio Input]

Table 3: **SDI Audio Embedder I/O Signal Description**

Port Name	Width	I/O	Description
s_axis_clk	1	Input	AXI4-Stream clock
s_axis_resetn	1	Input	AXI4-Stream reset, Active-Low
s_axis_tvalid	1	Input	AXI4-Stream Valid

Table 3: **SDI Audio Embedder I/O Signal Description** *(cont'd)*

Port Name	Width	I/O	Description
s_axis_tready	1	Output	AXI4-Stream Ready
s_axis_tdata	32	Input	AXI4-Stream Data
s_axis_tid	log base 2 (Maximum Audio Channels)	Input	AXI4-Stream Identifier s_axis_tid width is: • 1 when Maximum Audio Channels is 2 • 2 when Maximum Audio Channels is 4 • 3 when Maximum Audio Channels is 6 or 8 • 4 when Maximum Audio Channels is 10, 12, 14 or 16

Reset Output Interface

Table 4: **SDI Audio Embedder I/O Signal Description**

Port Name	Width	I/O	Description
sdi_embed_reset_out	1	Output	This signal, when set to 1, indicates that SDI Audio Embedder is under reset.

SDI Input Interface

Table 5: **SDI Audio Embedder I/O Signal Description**

Port Name	Width	I/O	Description
sdi_embed_clk	1	Input	This is the video clock
sdi_embed_reset	1	Input	Video reset, Active-High
sdi_embed_anc_ctrl_in	32	Input	Ancillary control information from the Xilinx UHD SDI Transmitter Subsystem [0] - Clock enable in SD-SDI mode [1] - Clock enable in non-SD mode [12:2] - External line number. In general, externally provided line numbers must be used in cases where valid line numbers have not yet been embedded in the input video stream. [13] - SDI Transmitter Reset. This signal, when set to 1, indicates that SDI Transmitter is under reset. [31:14] - Reserved
sdi_embed_anc_ds1_in	10	Input	Data stream 1. In SD mode this is interleaved Y/C. In HD and 3GA modes, this is the Y channel. In 3GB mode, this is the link A Y channel. In 6G and 12G modes, this is ds1.
sdi_embed_anc_ds2_in	10	Input	Data stream 2. Not used in SD mode. In HD and 3GA modes, this is the C channel. In 3GB mode, this is the link A C channel. In 6G and 12G modes, this is ds2.

Table 5: **SDI Audio Embedder I/O Signal Description** *(cont'd)*

Port Name	Width	I/O	Description
sdi_embed_anc_ds3_in	10	Input	Data stream 3. Not used in SD, HD, and 3GA modes. In 3GB mode, this is the link B Y channel. In 6G and 12G modes this is ds3.
sdi_embed_anc_ds4_in	10	Input	Data stream 4. Not used in SD, HD, and 3GA modes. In 3GB mode, this is the link B C channel. In 6G and 12G modes this is ds4.
sdi_embed_anc_ds5_in through sdi_embed_anc_ds16_in	10	Input	Additional data stream ports. The number of ports that are active depend on the number of data streams interleaved on the SDI signal. These ports are never active in SD, HD, or 3G modes.

SDI Output Interface

Table 6: **SDI Audio Embedder I/O Signal Description**

Port Name	Width	I/O	Description
sdi_embed_anc_ds1_out	10	Output	Data stream 1. In SD mode this is interleaved Y/C. In HD and 3GA modes, this is the Y channel. In 3GB mode, this is the link A Y channel. In 6G and 12G modes, this is ds1.
sdi_embed_anc_ds2_out	10	Output	Data stream 2. Not used in SD mode. In HD and 3GA modes, this is the C channel. In 3GB mode, this is the link A C channel. In 6G and 12G modes, this is ds2.
sdi_embed_anc_ds3_out	10	Output	Data stream 3. Not used in SD, HD, and 3GA modes. In 3GB mode, this is the link B Y channel. In 6G and 12G modes, this is ds3.
sdi_embed_anc_ds4_out	10	Output	Data stream 4. Not used in SD, HD, and 3GA modes. In 3GB mode, this is the link B C channel. In 6G and 12G modes, this is ds4.
sdi_embed_anc_ds5_out through sdi_embed_anc_ds16_out	10	Output	Additional data stream ports. The number of ports that are active depend on the number of data streams interleaved on the SDI signal. These ports are never active in SD, HD, or 3G modes.

Interrupt Interface [when AXI4-Lite interface is enabled]

Table 7: **SDI Audio Embedder I/O Signal Description**

Port Name	Width	I/O	Description
interrupt	1	Output	Interrupt

SDI Audio Extractor Input/Output (I/O) Signals

The Audio Extractor Input/Output (I/O) signals are listed and described in the following sections.

Configuration Interface [when AXI4-Lite Interface is Enabled]

Table 8: **SDI Audio Extractor I/O Signal Description**

Port Name	I/O	Clock	Description
s_axi_aclk	1	Input	AXI4-Lite clock
s_axi_aresetn	1	Input	AXI4-Lite reset, Active-Low
s_axi_awaddr	32	Input	Write address
s_axi_awprot	3	Input	Write protection
s_axi_awvalid	1	Input	Write address valid
s_axi_awready	1	Output	Write address ready
s_axi_wdata	32	Input	Write data bus
s_axi_wstrb	4	Input	Write strobes
s_axi_wvalid	1	Input	Write valid
s_axi_wready	1	Output	Write ready
s_axi_bresp	2	Output	Write response
s_axi_bvalid	1	Output	Write response valid
s_axi_bready	1	Input	Response ready
s_axi_araddr	32	Input	Read address
s_axi_arprot	3	Input	Read protection
s_axi_arvalid	1	Input	Read address valid
s_axi_arready	1	Output	Read address ready
s_axi_rdata	32	Output	Read data bus
s_axi_rresp	2	Output	Read response
s_axi_rvalid	1	Output	Read valid
s_axi_rready	1	Input	Read ready

Configuration Interface [when AXI4-Lite Interface is Disabled]

When AXI4-Lite interface is disabled, register set is not instantiated in the core. Configuration and status is provided through `sdi_extract_config` and `sdi_extract_status` respectively.

Table 9: **SDI Audio Extractor I/O Signal Description**

Port Name	I/O	Clock	Description
sdi_extract_config	64	Input	See SDI Audio Extractor Register Space for detailed information on the fields mentioned below [0] - extract_enable [1] reserved [2] - soft_reset_core [3] - clk_phase [7:4] - reserved [12:8] - prog_max_audio_chan [13] - reserved [15:14] - demux 1 aud_group_sel [19:16] - demux 1 mute_chan [20] - reserved [22:21] - demux 2 aud_group_sel [26:23] - demux 2 mute_chan [27] - reserved [29:28] - demux 3 aud_group_sel [33:30] - demux 3 mute_chan [34] - reserved [36:35] - demux 4 aud_group_sel [40:37] - demux 4 mute_chan [63:41] - reserved
sdi_extract_status	300	Output	See SDI Audio Extractor Register Space for detailed information on the fields mentioned below. [7:0] - reserved [8] - aud_group_change [9] - ctrl_pkt_change [10] - chan_status_change [11] - smpl_fifo_overflow [12] - parity_err [13] - checksum_err [14] - reserved [18:15] - group_present_val [30:19] - group_smpl_rate [46:31] - group_act_chan [238:47] - chan_status [242:239] - max_audio_channels [244:243] - uhdsdi_standard [245] - audio_function [246] - axi_lite [247] - chan_status_extract [299:248] - reserved

SDI Input Interface

Table 10: **SDI Audio Extractor I/O Signal Description**

Port Name	I/O	Clock	Description
sdi_extract_clk	1	Input	This is the video clock
sdi_extract_reset	1	Input	Video reset, Active-High

Table 10: **SDI Audio Extractor I/O Signal Description** *(cont'd)*

Port Name	I/O	Clock	Description
sdi_extract_anc_ctrl_in	32	Input	Ancillary control information from the Xilinx UHD SDI Receiver Subsystem. [0] - `rx_ce`. This signal is the video clock enable from the receiver [3:1] - `rx_mode`. This signal indicates the current SDI mode of the receiver • 000 = HD • 001 = SD • 010 = 3G • 100 = 6G • 101 = 12G 1000/1000 • 110 = 12G 1000/1001 [7:4] - `rx_t_family`. This signal indicate the video format family • 0000 - SMPTE ST 274 1920 x 1080 • 0001 SMPTE ST 296 1280 x 720 • 0010 SMPTE 2048-2 2048 x 1080 • 0011 SMPTE 295 1920 x 1080 • 1000 NTSC 720 x 486 • 1001 PAL 720 x 576 • 1111 Unknown [8] - `rx_mode_locked`. When the receiver locks to the correct SDI mode, the `rx_mode_locked` goes High. [9] `rx_t_locked`. This signal is 1 when the transport detection function in the receiver has identified the transport format of the SDI signal [13:10] `rx_t_rate`. This signal indicates the frame rate of the transport. • 0000 - None • 0010 - 23.98 Hz • 0011 - 24 Hz • 0100 - 47.95 • Hz 0101 - 25 Hz • 0110 - 29.97 Hz • 0111 - 30 Hz • 1000 - 48 Hz • 1001 - 50 Hz • 1010 - 59.94 Hz • 1011 - 60 Hz • Others - Reserved [14] `rx_t_scan`. This signal indicates whether the transport is interlaced (Low) or progressive (High). [15] - `rx_rst_int_sys`. This signal when set to 1 indicate that SDI Receiver is under reset. [31:16] Reserved

Table 10: **SDI Audio Extractor I/O Signal Description** *(cont'd)*

Port Name	I/O	Clock	Description
sdi_extract_anc_ds1_in	10	Input	Data stream 1. In SD mode this is interleaved Y/C. In HD and 3GA modes, this is the Y channel. In 3GB mode, this is the link A Y channel. In 6G and 12G modes, this is ds1.
sdi_extract_anc_ds2_in	10	Input	Data stream 2. Not used in SD mode. In HD and 3GA modes, this is the C channel. In 3GB mode, this is the link A C channel. In 6G and 12G modes, this is ds2.
sdi_extract_anc_ds3_in	10	Input	Data stream 3. Not used in SD, HD, and 3GA modes. In 3GB mode, this is the link B Y channel. In 6G and 12G modes this is ds3.
sdi_extract_anc_ds4_in	10	Input	Data stream 4. Not used in SD, HD, and 3GA modes. In 3GB mode, this is the link B C channel. In 6G and 12G modes this is ds4.

AXI4-Stream Master Interface [Audio Output]

Table 11: **SDI Audio Extractor I/O Signal Description**

Port Name	I/O	Clock	Description
m_axis_clk	1	Input	AXI4-Stream clock
m_axis_resetn	1	Input	AXI4-Stream reset, Active-low
m_axis_tvalid	1	Output	AXI4-Stream Valid Out
m_axis_tready	1	Input	AXI4-Stream Ready
m_axis_tdata	32	Output	AXI4-Stream Data
m_axis_tid	log base 2 (Maximum Audio Channels)	Output	AXI4-Stream Identifier m_axis_tid width is set to: • 1 when Maximum Audio Channels is 2 • 2 when Maximum Audio Channels is 4 • 3 when Maximum Audio Channels is 6 or 8 • 4 when Maximum Audio Channels is 10, 12, 14 or 16

Reset Output Interface

Table 12: **SDI Audio Extractor I/O Signal Description**

Port Name	I/O	Clock	Description
sdi_extract_reset_out	1	Output	This signal, when set to 1, indicates that Audio Extractor is under reset. Downstream IP's can use this signal as reset.

Interrupt Interface [when AXI4-Lite interface is enabled]

Table 13: **SDI Audio Extractor I/O Signal Description**

Port Name	I/O	Clock	Description
interrupt	1	Output	Interrupt

SDI Audio Embedder Register Space

The following table specifies the offset address, register name, and accessibility of each firmware addressable registers within the SDI Audio Embedder. User access to each register is from an offset to the base address.

Table 15: **Register Address Space - SDI Audio Embedder**

Offset	Name	Description
0x00	Module Control Register	Controls enabling and disabling of the IP
0x04	Soft Reset Register	Soft reset control for core register set and data path
0x08	Reserved	N/A
0x0C	Interrupt Enable Register	Interrupt enable register
0x10	Interrupt Status Register	Interrupt status register
0x14	Video Control Register	Video control (External line number and video resolution)
0x18	Audio Control Register	Audio control (sample depth, sample rate and rate control)
0x1C	Programmable Maximum Audio Channels (PMAC)	Register to overwrite Maximum Audio Channels set during core generation
0x20	Mux 1 Control Register	Selects the audio group for Mux 1 instance. Enabled when PMAC > 0.
0x24	Mux 2 Control Register	Selects the audio group for Mux 2 instance. Enabled when PMAC > 4.
0x28	Mux 3 Control Register	Selects the audio group for Mux 3 instance. Enabled when PMAC > 8.
0x2C	Mux 4 Control Register	Selects the audio group for Mux 4 instance. Enabled only when PMAC > 12.
0x30	Reserved	N/A
0x34	Reserved	N/A
0x38	Reserved	N/A
0x3C	Reserved	N/A
0x40	Group Presence Register	Conveys the presence of pre-embedded audio groups
0x44 to 0xF8	Reserved	N/A

Table 15: **Register Address Space - SDI Audio Embedder** *(cont'd)*

Offset	Name	Description
0xFC	GUI Parameters	Conveys the parameters chosen during core generation

Module Control Register (0x00)

Table 16: **Module Control Register - Audio Embedder**

Bit	Field Name	Access Type	Description
31:1	Reserved	Not applicable	Reserved Default value - 0
0	embed_enable	R/W	When set to 1, this bit enables audio embedding. Set this bit after all other configuration is complete. Default value - 0

Soft Reset Register (0x04)

Table 17: **Soft Reset Register - Audio Embedder**

Bit	Field Name	Access Type	Description
31:2	Reserved	N/A	Reserved Default value - 0
1	soft_reset_core	R/W	When set to 1, this bit resets the internal FIFO's and the AXI4-Stream interface. Core register set and interrupts are not covered under this reset. Default value - 0
0	soft_reset_config	RW1C	When set to 1, this bit resets the core register set and the interrupts. Default value - 0

Interrupt Enable Register (0x0C)

Table 18: **Interrupt Enable Register - Audio Embedder**

Bit	Field Name	Access Type	Description
31:1	Reserved	N/A	Reserved Default value - 0
0	aud_group_change_det	R/W	When set to 1, this bit checks for the change in the presence of audio groups in the incoming SDI stream. Default value - 0

Interrupt Status Register (0x10)

Table 19: **Interrupt Status Register - Audio Embedder**

Bit	Field Name	Access Type	Description
31:1	Reserved	N/A	Reserved Default value - 0
0	aud_group_change	RW1C	When set to 1, this bit indicates the change in the presence of audio groups in the incoming SDI stream. Default value - 0

Video Control Register (0x14)

Table 20: **Video Control Register - Audio Embedder**

Bit	Field Name	Access Type	Description
31:6]	Reserved	N/A	Reserved Default value - 0
5	ext_ln_en	R/W	This bit selects the source of video line number. • 0 - Uses line numbers decoded from video stream • 1 - Uses line numbers from ancillary control bus “sdi_embed_anc_ctrl_in” Default value - 0

Table 20: **Video Control Register - Audio Embedder** *(cont'd)*

Bit	Field Name	Access Type	Description
4:0	line_std	R/W	This signal indicates the video format as shown below. For SD/HD/3G-A/6G/12G-SDI, • 00000 - SMPTE 260M 1035i – 30 Hz • 00001 - SMPTE 295M 1080i – 25 Hz • 00010 - SMPTE 274M 1080i or 1080sF - 29.97, 30 Hz • 00011 - SMPTE 274M 1080i or 1080sF - 25 Hz • 00100 - SMPTE 274M 1080p - 29.97, 30 Hz • 00101 - SMPTE 274M 1080p – 25 Hz • 00110 - SMPTE 274M 1080p - 23.98, 24 Hz • 00111 - SMPTE 296M 720p - 59.94, 60 Hz • 01000 - SMPTE 274M 1080sF - 23.98, 24 Hz • 01001 - SMPTE 296M 720p – 50 Hz • 01010 - SMPTE 296M 720p – 29.97, 30 Hz • 01011 - SMPTE 296M 720p – 25 Hz • 01100 - SMPTE 296M 720p - 23.98, 24 Hz • 01101 - SMPTE 274M 1080p – 59.94, 60 Hz (3G-SDI level A only) • 01110 - SMPTE 274M 1080p – 50 Hz (3G-SDI level A only) • 01111 - Reserved • 10000 - NTSC • 10001 - PAL • 10010 - SMPTE 2036-1 or 2048-1 2160p - 23.98 Hz • 10011 - SMPTE 2036-1 or 2048-1 2160p – 24 Hz • 10100 - SMPTE 2036-1 or 2048-1 2160p – 25 Hz • 10101 - SMPTE 2036-1 or 2048-1 2160p - 29.97 Hz • 10110 - SMPTE 2036-1 or 2048-1 2160p – 30 Hz • 10111 - 2048-1 2160p – 47.95, 48 Hz • 11000 - SMPTE 2036-1 or 2048-1 2160p - 50 Hz • 11001 - SMPTE 2036-1 or 2048-1 2160p – 59.94, 60 Hz • 11010 –2048x1080i - 29.97, 30 Hz • 11011 – 2048x1080i - 25 Hz • 11100 - SMPTE 2048-2 1080p – 29.97, 30 Hz • 11101 – SMPTE 2048-2 1080p – 23.98, 24, 25 Hz • 11110 - SMPTE 2048-2 1080p – 47.95, 48, 50, 59.94, 60 Hz (3G-SDI level A only) • 11111 – Reserved For 3G-B Dual Stream SDI, • Configure the video standard of data stream 1 & 2 (from the above list) For 3G-B Dual Link SDI, • 00100 - SMPTE 274M 1080p – 59.94, 60 Hz (3G-SDI level B-DL) • 00101 - SMPTE 274M 1080p – 50 Hz (3G-SDI level B-DL) • 11100 - SMPTE 2048-2 1080p – 59.94, 60 Hz (3G-SDI level B-DL) • 11101 - SMPTE 2048-2 1080p – 47.95, 48, 50 Hz (3G-SDI level B-DL) Default value - 0

Audio Control Register (0x18)

Table 21: **Audio Control Register - Audio Embedder**

Bit	Field Name	Access Type	Description
31:5	Reserved	N/A	Reserved Default value - 0
4	rate_control_enable	R/W	This bit controls the rate at which audio samples are inserted on to the SDI stream. • 0 - Audio samples are inserted as and when they are available in the channel FIFOs. • 1 - Number of audio samples per video line are limited based on video resolution, frame rate and audio sample rate. Default value - 0
3	sd_samp_size_24	R/W	This bit indicates the audio sample size in SD mode. Extended data packets are inserted in case of 24-bit audio sample. • 0 - 20 bit audio sample • 1 - 24 bit audio sample Default value - 0
2:0	smpl_rate	R/W	This signal indicates the audio sample rate that should be sent as part of Audio Control Packet. • 000 - 48 KHz • 001 - 44.1 KHz • 010 - 32 KHz • Others - Reserved Default value - 0

Programmable Maximum Audio Channels (0x1C)

Table 22: **Programmable Maximum Audio Channels - Audio Embedder**

Bit	Field Name	Access Type	Description
31:5	Reserved	N/A	Reserved Default value - 0
4:0	prog_max_audio_chan	R/W	Programmable Maximum Audio Channels. This signal overwrites the Maximum Audio Channels set during core generation. Default value - 0

Mux 1 Control Register (0x20)

Table 23: **Mux 1 Control Register - Audio Embedder**

Bit	Field Name	Access Type	Description
31:2	Reserved	N/A	Reserved Default value - 0
1:0	aud_group_sel	R/W	Group number on which data coming on AXI4-Stream interface with TID 0, 1, 2, and 3 to be embedded. • 0 - Group 1 • 1 - Group 2 • 2 - Group 3 • 3 - Group 4 Default value - 0

Mux 2 Control Register (0x24)

Table 24: **Mux 2 Control Register - Audio Embedder**

Bit	Field Name	Access Type	Description
31:2	Reserved	N/A	Reserved Default value - 0
1:0	aud_group_sel	R/W	Group number on which data coming on AXI4-Stream interface with TID 4, 5, 6, and 7 to be embedded. • 0 - Group 1 • 1 - Group 2 • 2 - Group 3 • 3 - Group 4 Default value - 0

Mux 3 Control Register (0x28)

Table 25: **Mux 3 Control Register - Audio Embedder**

Bit	Field Name	Access Type	Description
31:2	Reserved	N/A	Reserved Default value - 0

Table 25: **Mux 3 Control Register - Audio Embedder** *(cont'd)*

Bit	Field Name	Access Type	Description
1:0	aud_group_sel	R/W	Group number on which data coming on AXI4-Stream interface with TID 8, 9, 10, and 11 to be embedded. • 0 - Group 1 • 1 - Group 2 • 2 - Group 3 • 3 - Group 4 Default value - 0

Mux 4 Control Register (0x2C)

Table 26: **Mux 4 Control Register - Audio Embedder**

Bit	Field Name	Access Type	Description
31:2	Reserved	N/A	Reserved Default value - 0
1:0	aud_group_sel	R/W	Group number on which data coming on AXI4-Stream interface with TID 12, 13, 14, and 15 to be embedded. • 0 - Group 1 • 1 - Group 2 • 2 - Group 3 • 3 - Group 4 Default value - 0

Group Presence Register (0x40)

Table 27: **Group Presence Register - Audio Embedder**

Bit	Field Name	Access Type	Description
31:4	Reserved	N/A	Reserved Default value - 0

Table 27: **Group Presence Register - Audio Embedder** *(cont'd)*

Bit	Field Name	Access Type	Description
3:0	group_present_val	R	Each bit when set to 1, indicates the detection of audio group on the incoming SDI stream. • Bit[0] - Group 1 present • Bit[1] - Group 2 present • Bit[2] - Group 3 present • Bit[3] - Group 4 present Default value - 0

GUI Parameters (0xFC)

Table 28: **GUI Parameters - Audio Embedder**

Bit	Field Name	Access Type	Description
31:8	Reserved	Not applicable	Reserved. Default value - 0
7	axi_lite	R	This signal conveys the Configuration interface selected during core generation • 0 - AXI4-Lite disabled • 1 - AXI4-Lite enabled Default value - 1
6	audio_function	R	This signal conveys the Audio Function selected during core generation • 0 - Embed • 1 - Extract Default value - 0
5:4	uhdsdi_standard	R	This signal conveys the SDI Standard selected during core generation • 0 - 3G_SDI • 1 - 6G_SDI • 2 - 12G_SDI_8DS • 3 - 12G_SDI_16DS Default value - 3

Table 28: **GUI Parameters - Audio Embedder** *(cont'd)*

Bit	Field Name	Access Type	Description
3:0	max_audio_channels	R	This signal conveys the Maximum Audio Channels selected during core generation • 0 - 2 Channels • 1 - 4 Channels • 2 - 6 Channels • 3 - 8 Channels • 4 - 10 Channels • 5 - 12 Channels • 6 - 14 Channels • 7 - 16 Channels Default value - 7

SDI Audio Extractor Register Space

This section specifies the offset address, register name, and accessibility of each firmware addressable registers within the SDI Audio Extractor. User access to each register is from an offset to the base address.

Table 30: **Register Address Space - SDI Audio Extractor**

Offset	Name	Description
0x00	Module Control Register	Controls enabling and disabling of the IP
0x04	Soft Reset Register	Soft reset control for core register set and data path
0x08	Reserved	N/A
0x0C	Interrupt Enable Register	Interrupt enable register
0x10	Interrupt Status Register	Interrupt status register
0x14	Reserved	N/A
0x18	Audio Control Register	Audio output control
0x1C	Programmable Maximum Audio Channels (PMAC)	Register to overwrite Maximum Audio Channels set during core generation
0x20	Demux 1 Control Register	Selects the audio group for Demux 1 instance. Enabled when PMAC > 0.
0x24	Demux 2 Control Register	Selects the audio group for Demux 2 instance. Enabled when PMAC > 4.
0x28	Demux 3 Control Register	Selects the audio group for Demux 3 instance. Enabled when PMAC > 8.

Table 30: **Register Address Space - SDI Audio Extractor** *(cont'd)*

Offset	Name	Description
0x2C	Demux 4 Control Register	Selects the audio group for Demux 4 instance. Enabled when PMAC > 12.
0x30	Reserved	N/A
0x34	Reserved	N/A
0x38	Reserved	N/A
0x3C	Reserved	N/A
0x40	Group Presence Register	Conveys the presence of pre-embedded audio groups
0x44	Control Packet Status	Conveys the active channel and sample rates decoded from the control packet
0x48	Channel Status Regiser 0	Audio channel status bits 31 to 0
0x4C	Channel Status Register 1	Audio channel status bits 63 to 32
0x50	Channel Status Register 2	Audio channel status bits 95 to 64
0x54	Channel Status Register 3	Audio channel status bits 127 to 96
0x58	Channel Status Register 4	Audio channel status bits 159 to 128
0x5C	Channel Status Register 5	Audio channel status bits 191 to 160
0x60	Reserved	N/A
0xFC	GUI Parameters	Conveys the parameters chosen during core generation

Module Control Register (0x00)

Table 31: **Module Control Register - Audio Extractor**

Bit	Field Name	Access Type	Description
31:1	Reserved	Not applicable	Reserved Default value - 0
0	extract_enable	R/W	When set to 1, this bit enables the extraction of audio. This bit should be set after all other configuration is complete. Default value - 0

Soft Reset Register (0x04)

Table 32: **Soft Reset Register - Audio Extractor**

Bit	Field Name	Access Type	Description
31:2	Reserved	N/A	Reserved Default value - 0
1	soft_reset_core	R/W	When set to 1, this bit resets the entire design except for the core register set and interrupts. Default value - 0

Table 32: **Soft Reset Register - Audio Extractor** *(cont'd)*

Bit	Field Name	Access Type	Description
0	soft_reset_config	RW1C	When set to 1, this bit resets the core register set and the interrupts. Default value - 0

Interrupt Enable Register (0x0C)

Table 33: **Interrupt Enable Register - Audio Extractor**

Bit	Field Name	Access Type	Description
31:6	Reserved	N/A	Reserved Default value - 0
5	checksum_err_det	R/W	When set to 1, this bit check for the checksum errors on audio packets. Default value - 0
4	parity_err_det	R/W	When set to 1, this bit checks for the parity errors on audio samples. Default value - 0
3	smpl_fifo_overflow_det	R/W	When set to 1, this bit checks for the overflow of receive sample FIFO. Default value - 0
2	chan_status_change_det	R/W	When set to 1, this bit checks for the change in channel status value compared to previous channel status value. Default value - 0
1	ctrl_pkt_change_det	R/W	When set to 1, this bit checks for the change in incoming control packet contents compared to previous packets (sample rate, active channels). Default value - 0
0	aud_group_change_det	R/W	When set to 1, this bit checks for the change in the presence of audio groups in the incoming SDI stream. Default value - 0

Interrupt Status Register (0x10)

Table 34: **Interrupt Status Register - Audio Extractor**

Bit	Field Name	Access Type	Description
31:6	Reserved	N/A	Reserved Default value - 0
5	checksum_err	RW1C	When set to 1, this bit indicates the checksum errors on ancillary packets. Default value - 0
4	parity_err	RW1C	When set to 1, this bit indicates the parity errors on audio samples. Default value - 0
3	smpl_fifo_overflow	RW1C	When set to 1, this bit indates the overflow of receive sample FIFO. Default value - 0

Table 34: **Interrupt Status Register - Audio Extractor** *(cont'd)*

Bit	Field Name	Access Type	Description
2	chan_status_change	RW1C	When set to 1, this bit indicates the change in channel status value com-pared to previous channel status value. See Channel Status Registers in the SDI Audio Extractor Register Space section. Default value - 0
1	ctrl_pkt_change	RW1C	When set to 1, this bit indicates the change in control packet content compared to earlier packets (sample rate and active channels). See Group Presence Register (0x40) for more information. Default value - 0
0	aud_group_change	RW1C	When set to 1, this bit indicates the change in the presence of audio groups in the incoming SDI stream. See Group Presence Register (0x40) for more information. Default value - 0

Audio Control Register (0x18)

Table 35: **Audio Control Register - Audio Extractor**

Bit	Field Name	Access Type	Description
31:1	Reserved	N/A	Reserved Default value - 0
0	clk_phase	R/W	This bit controls the output data timing in HD mode. • 0 - Reserved. • 1 - Audio samples are output when extracted from the SDI stream without considering the clock phase information. Default value - 1

Programmable Maximum Audio Channels (0x1C)

Table 36: **Programmable Maximum Audio Channels - Audio Extractor**

Bit	Field Name	Access Type	Description
31:5	Reserved	N/A	Reserved Default value - 0
4:0	prog_max_audio_chan	R/W	This signal overwrites the Maximum Audio Channels set during core generation. Default value - 0

Demux 1 Control Register (0x20)

Table 37: **Demux 1 Control Register - Audio Extractor**

Bit	Field Name	Access Type	Description
31:6	Reserved	N/A	Reserved Default value - 0
5:2	mute_chan	R/W	Each bit when set to 1 overwrites the extracted data with mute data. • Bit [2] – Channel 1 of selected group • Bit [3] – Channel 2 of selected group • Bit [4] – Channel 3 of selected group • Bit [5] – Channel 4 of selected group Default value - 0
1:0	aud_group_sel	R/W	Selects the group number from which audio to be extracted. Extracted data is placed on AXI4-Stream interface with TID 0, 1, 2, and 3. • 0 - Group 1 • 1 - Group 2 • 2 - Group 3 • 3 - Group 4 Default value - 0

Demux 2 Control Register (0x24)

Table 38: **Demux 2 Control Register - Audio Extractor**

Bit	Field Name	Access Type	Description
31:6	Reserved	N/A	Reserved Default value - 0
5:2	mute_chan	R/W	Each bit when set to 1 overwrites the extracted data with mute data. • Bit [2] – Channel 1 of selected group • Bit [3] – Channel 2 of selected group • Bit [4] – Channel 3 of selected group • Bit [5] – Channel 4 of selected group Default value - 0

Table 38: **Demux 2 Control Register - Audio Extractor** *(cont'd)*

Bit	Field Name	Access Type	Description
1:0	aud_group_sel	R/W	Selects the group number from which audio to be extracted. Extracted data is placed on AXI4-Stream interface with TID 4, 5, 6, and 7. • 0 - Group 1 • 1 - Group 2 • 2 - Group 3 • 3 - Group 4 Default value - 0

Demux 3 Control Register (0x28)

Table 39: **Demux 3 Control Register - Audio Extractor**

Bit	Field Name	Access Type	Description
31:6	Reserved	N/A	Reserved Default value - 0
5:2	mute_chan	R/W	Each bit when set to 1 overwrites the extracted data with mute data. • Bit [2] – Channel 1 of selected group • Bit [3] – Channel 2 of selected group • Bit [4] – Channel 3 of selected group • Bit [5] – Channel 4 of selected group Default value - 0
1:0	aud_group_sel	R/W	Selects the group number from which audio to be extracted. Extracted data is placed on AXI4-Stream interface with TID 8, 9, 10, and 11. • 0 - Group 1 • 1 - Group 2 • 2 - Group 3 • 3 - Group 4 Default value - 0

Demux 4 Control Register (0x2C)

Table 40: **Demux 4 Control Register - Audio Extractor**

Bit	Field Name	Access Type	Description
31:6	Reserved	N/A	Reserved Default value - 0
5:2	mute_chan	R/W	Each bit when set to 1 overwrites the extracted data with mute data. • Bit [2] – Channel 1 of selected group • Bit [3] – Channel 2 of selected group • Bit [4] – Channel 3 of selected group • Bit [5] – Channel 4 of selected group Default value - 0
1:0	aud_group_sel	R/W	Selects the group number from which audio to be extracted. Extracted data is placed on AXI4-Stream interface with TID 12, 13, 14, and 15. • 0 - Group 1 • 1 - Group 2 • 2 - Group 3 • 3 - Group 4 Default value - 0

Group Presence Register (0x40)

Table 41: **Group Presence Register - Audio Extractor**

Bit	Field Name	Access Type	Description
31:4	Reserved	N/A	Reserved Default value - 0
3:0			Each bit when set to 1, indicates the detection of audio group on the incoming SDI stream. • Bit[0] - Group 1 present • Bit[1] - Group 2 present • Bit[2] - Group 3 present • Bit[3] - Group 4 present Default value - 0

Control Packet Status (0x44)

Table 42: **Control Packet Status - Audio Extractor**

Bit	Field Name	Access Type	Description
[31:28]	Reserved	N/A	Reserved Default value - 0
[27:12]	group_act_chan		Active channel field captured from the control packet of each audio group • Bit[15:12] - Group 1 • Bit[19:16] - Group 2 • Bit[23:20] - Group 3 • Bit[27:24] - Group 4 Default value - 0
[11:0]	group_smpl_rate		Sample rate field captured from the control packet of each audio group • Bit[2:0] - Group 1 • Bit[5:3] - Group 2 • Bit[8:6] - Group 3 • Bit[11:9] - Group 4 Default value - 0

Channel Status Register 0 (0x48)

Table 43: **Channel Status Register 0 - Audio Extractor**

Bit	Field Name	Access Type	Description
31:0	chan_status0	R	Audio channel status bits 31 to 0 Default value - 0

Channel Status Register 1 (0x4C)

Table 44: **Channel Status Register 1 - Audio Extractor**

Bit	Field Name	Access Type	Description
31:0	chan_status1	R	Audio channel status bits 63 to 32 Default value - 0

Channel Status Register 2 (0x50)

Table 45: **Channel Status Register 2 - Audio Extractor**

Bit	Field Name	Access Type	Description
31:0	chan_status 2	R	Audio channel status bits 95 to 64 Default value - 0

Channel Status Register 3 (0x54)

Table 46: **Channel Status Register 3 - Audio Extractor**

Bit	Field Name	Access Type	Description
31:0	chan_status 3	R	Audio channel status bits 127 to 96 Default value - 0

Channel Status Register 4 (0x58)

Table 47: **Channel Status Register 4 - Audio Extractor**

Bit	Field Name	Access Type	Description
31:0	chan_status 4	R	Audio channel status bits 159 to 128 Default value - 0

Channel Status Register 5 (0x5C)

Table 48: **Channel Status Register 5 - Audio Extractor**

Bit	Field Name	Access Type	Description
31:0	chan_status 5	R	Audio channel status bits 191 to 160 Default value - 0

GUI Parameters (0xFC)

Table 49: **GUI Parameters - Audio Extractor**

Bit	Field Name	Access Type	Description
31:9	Reserved	Not applicable	Reserved Default value - 0

Table 49: **GUI Parameters - Audio Extractor** *(cont'd)*

Bit	Field Name	Access Type	Description
8	chan_status_extract	R	This signal conveys the Channel Status option selected during core generation • 0 – Ignore channel status • 1 – Extract channel status Default value - 1
7	axi_lite	R	This signal conveys the Configuration interface selected during core generation • 0 - AXI4-Lite disabled • 1 - AXI4-Lite enabled Default value - 1
6	audio_function	R	This signal conveys the Audio Function selected during core generation • 0 - Embed • 1 - Extract Default value - 1
5:4	uhdsdi_standard	R	This signal conveys the SDI Standard selected during core generation • 0 - 3G SDI • 1 - 6G SDI • 2 - 12G SDI 8DS • 3 - 12G SDI 16DS Default value - 3
3:0	max_audio_channels	R	This signal conveys the Maximum Audio Channels selected during core generation • 0 - 2 Channels • 1 - 4 Channels • 2 - 6 Channels • 3 - 8 Channels • 4 - 10 Channels • 5 - 12 Channels • 6 - 14 Channels • 7 - 16 Channels Default value - 7

Designing with the Core

General Design Guidelines

This section contains examples of programming sequence and they are provided for reference with some use cases.

Soft Reset

Assert soft reset in the following scenarios.

- The signal `soft_reset_core` (Offset 0x4 - Bit 1) should be asserted when SDI mode or the video resolution of the incoming SDI interface is changed. This helps the core flush internal FIFO's and start afresh on the new video resolution.
- The signal `soft_reset_core` (Offset 0x4 - Bit 1) should be asserted before any of the registers need to be updated. For example, core should be to reset before switching from 2 channel embed/extract to 16 channel embed/extract by changing the PMAC value.

Programming Sequence

This section contains examples of programming sequence and they are provided as reference for some use cases. Some of the registers that are enabled based on the PMAC are:

- PMAC set to 2 or 4: 0x20 should be used to embed/extract up to 4 channels of audio
- PMAC set to 6 or 8: 0x20 and 0x24 should be used to embed/extract up to 8 channels of audio
- PMAC set to 10 or 12: 0x20, 0x24, 0x28 should be used to embed/extract up to 12 channels of audio
- PMAC set to 14 or 16: 0x20, 0x24, 0x28 and 0x2C should be used to embed/extract up to 16 channels of audio

SDI Audio Embedder - Use Cases

The following use cases are provided for the SDI Audio Embedder.

- Use case: Audio Embedder is generated with Maximum Audio Channels set to 16 and you want to embed 2 audio channels (48 KHz) onto group 3 in an SDI stream carrying 1080p30 video.
  - 0x04 - 0x0000_0002 [Soft Reset Core asserted to bring the design to a known state]
  - 0x04 - 0x0000_0000 [Soft Reset Core de-asserted]
  - 0x0C - 0x0000_0001 [Interrupt Enabled]
  - 0x14 - 0x0000_0024 [External line number selected and video mode selected as 1080p30]
  - 0x18 - 0x0000_0018 [Rate Control enabled, 24-bit audio for SD Mode and Sample Rate 48Khz]
  - 0x1C - 0x0000_0002 [Programmable Maximum Audio Channel is set to 2]
  - 0x20 - 0x0000_0002 [Insert channels 1-2 coming over AXI4-Stream onto Group 3]
  - 0x00 - 0x0000_0001 [Embed Enable]
- Use case: SDI Audio Embedder core is generated with Maximum Audio Channels set to 16 and you want to embed 16 audio channels (32 KHz) onto an SDI stream carrying 1080p60 video.
  - 0x04 - 0x0000_0002 [Soft Reset Core asserted to bring the design to a known state]
  - 0x04 - 0x0000_0000 [Soft Reset Core de-asserted]
  - 0x0C - 0x0000_0001 [Interrupt Enabled]
  - 0x14 - 0x0000_002D [External line number selected and video mode selected as 1080p60]
  - 0x18 - 0x0000_001A [Rate Control enabled, 24-bit audio for SD Mode and Sample Rate 32Khz]
  - 0x1C - 0x0000_0010 [Programmable Maximum Audio Channel count is set to 16]
  - 0x20 - 0x0000_0000 [Insert channels 1-4 coming over AXI4-Stream onto Group 1]
  - 0x24 - 0x0000_0001 [Insert channels 5-8 coming over AXI4-Stream onto Group 2]
  - 0x28 - 0x0000_0002 [Insert channels 9-12 coming over AXI4-Stream onto Group 3]
  - 0x2C - 0x0000_0003 [Insert channels 13-16 coming over AXI4-Stream onto Group 4]
  - 0x00 - 0x0000_0001 [Embed Enable]

SDI Audio Extractor - Use Cases

The following use cases are provided for the SDI Audio Extractor.

- Use case: Audio Extractor is generated with Maximum Audio Channels set to 16 and you want to extract 2 audio channels from group 4.
  - 0x04 - 0x0000_0002 [Soft Reset Core asserted to bring the design to a known state]
  - 0x04 - 0x0000_0000 [Soft Reset Core de-asserted]
  - 0x0C - 0x0000_003F [Interrupt Enabled]
  - 0x1C - 0x0000_0002 [Programmable Maximum Audio Channel count is set to 2]
  - 0x20 - 0x0000_0003 [Extract from Group 4]
  - 0x00 - 0x0000_0001 [Extract Enable]
- Use case: Audio Extractor is generated with Maximum Audio Channels set to 16 and you want to extract 16 audio channels.
  - 0x04 - 0x0000_0002 [Soft Reset Core asserted to bring the design to a known state]
  - 0x04 - 0x0000_0000 [Soft Reset Core de-asserted]
  - 0x0C - 0x0000_003F [Interrupt Enabled]
  - 0x1C - 0x0000_0010 [Programmable Maximum Audio Channel count is set to 16]
  - 0x20 - 0x0000_0000 [Extract from Group 1]
  - 0x24 - 0x0000_0001 [Extract from Group 2]
  - 0x28 - 0x0000_0002 [Extract from Group 3]
  - 0x2C - 0x0000_0003 [Extract from Group 4]
  - 0x00 - 0x0000_0001 [Extract Enable]

Clocking

The list of clocks in SDI Audio Embedder.

- **s_axi_aclk:** This is the processor domain clock. AXI4-Lite interface works on this clock.
- **s_axis_clk:** This is the AXI4-Stream interface clock. This should be greater than or equal to 512 times the audio sampling rate.

- **sdi_embed_clk:** This is the video domain clock. It is 74.25 MHz or 74.175 MHz during HD SDI, 148.5 MHz or 148.35 MHz during SD/3G/6G SDI and 297 MHz during 12G SDI mode. This is the same clock connected to `sdi_TX_clk` of the Xilinx UHD-SDI TX Subsystem.

The list of clocks in SDI Audio Extractor.

- **s_axi_aclk:** This is the processor domain clock. AXI4-Lite interface works on this clock.
- **m_axis_clk:** This is the AXI4-Stream interface clock. This should be greater than or equal to 512 times the audio sampling rate.
- **sdi_extract_clk :** This is the video domain clock. It is 74.25 MHz or 74.175 MHz during HD SDI, 148.5 MHz or 148.35 MHz during SD/3G/6G SDI and 297 MHz during 12G SDI mode. This is the same clock connected to `sdi_rx_clk` of the Xilinx UHD-SDI RX Subsystem.

Resets

The SDI Audio Embedder uses the following resets.

- `s_axi_aresetn`: This is Active-Low AXI4-Lite interface reset. This reset brings the core registers set and the interrupts to the default state.
- `s_axis_resetn`: This is an Active-Low AXI4-Stream interface reset. This resets the entire logic working on `s_axis_clk`
- `sdi_embed_reset`: This is an Active-High video domain reset. This resets the entire core except for the core register set and the interrupts.
- **Soft Reset:** Two soft resets are provided apart from the reset ports mentioned above.
  - Soft reset config resets the core register set and the interrupts
  - Soft reset core resets the internal FIFO's and the logic working on `s_axis_clk`

The SDI Audio Extractor uses the following resets.

- `s_axi_aresetn`: This is Active-Low AXI4-Lite interface reset. This reset brings the core registers set and the interrupts to the default state.
- `m_axis_resetn`: This is an Active-Low AXI4-Stream interface reset. This resets the entire logic working on `m_axis_clk`.
- `sdi_extract_reset`: This is an Active-High video domain reset. This resets the entire core except for the core register set and the interrupts.
- **Soft Reset:** Two soft resets are provided apart from these resets.
  - Soft reset config resets the core register set and the interrupts
  - Soft reset core resets the entire core except for the core register set and the interrupts.

Design Flow Steps

This section describes customizing and generating the core, constraining the core, and the simulation, synthesis and implementation steps that are specific to this IP core. More detailed information about the standard Vivado® design flows and the IP integrator can be found in the following Vivado Design Suite user guides:

- *Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator* (UG994)
- *Vivado Design Suite User Guide: Designing with IP* (UG896)
- *Vivado Design Suite User Guide: Getting Started* (UG910)
- *Vivado Design Suite User Guide: Logic Simulation* (UG900)

Customizing and Generating the Core

This section includes information about using Xilinx® tools to customize and generate the core in the Vivado® Design Suite.

If you are customizing and generating the core in the Vivado IP integrator, see the *Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator* (UG994) for detailed information. IP integrator might auto-compute certain configuration values when validating or generating the design. To check whether the values do change, see the description of the parameter in this chapter. To view the parameter value, run the `validate_bd_design` command in the Tcl console.

You can customize the IP for use in your design by specifying values for the various parameters associated with the IP core using the following steps:

1. Select the IP from the IP catalog.
2. Double-click the selected IP or select the Customize IP command from the toolbar or right-click menu.

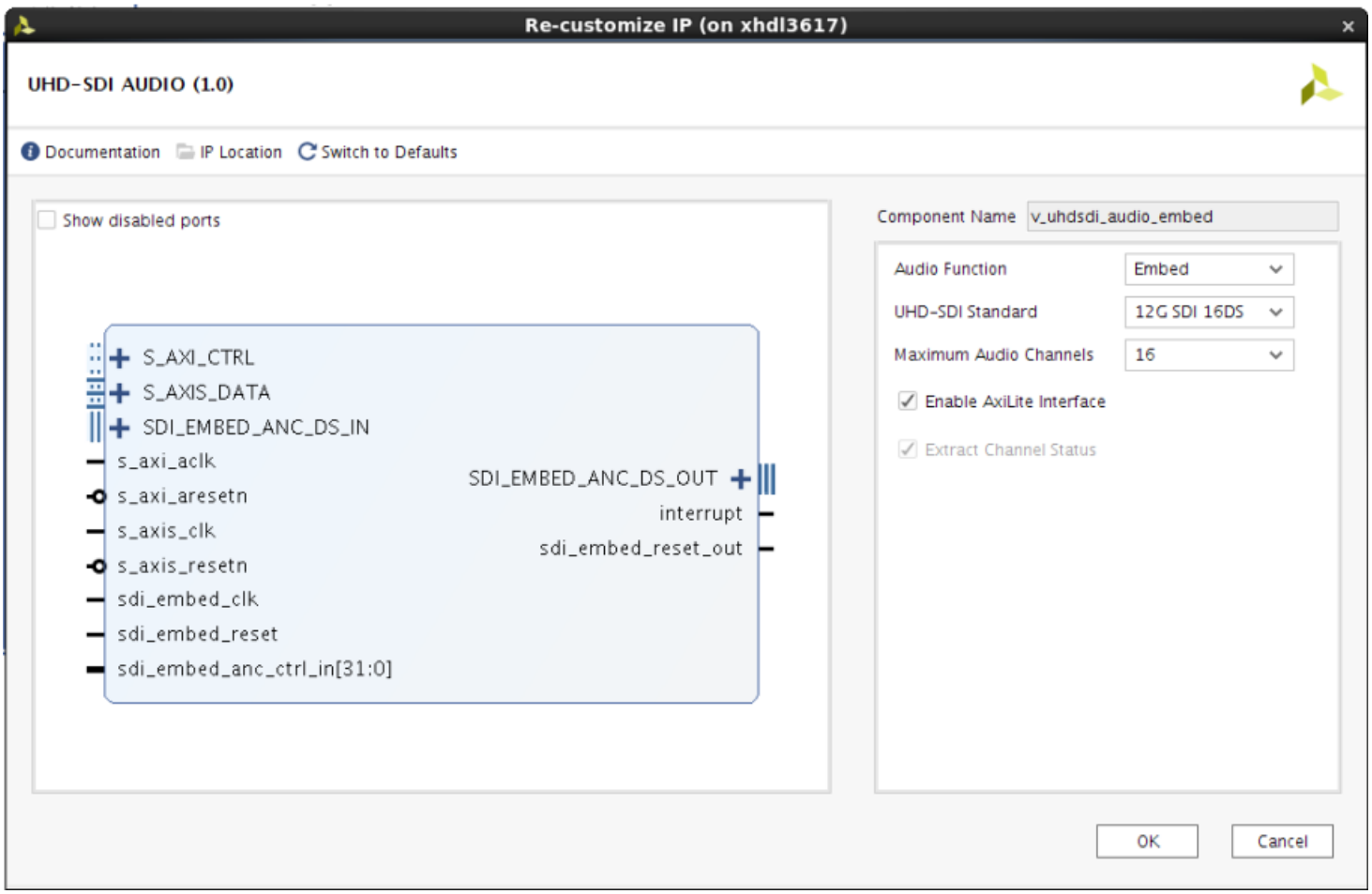
For details, see the *Vivado Design Suite User Guide: Designing with IP* (UG896) and the *Vivado Design Suite User Guide: Getting Started* (UG910).

Figures in this chapter are illustrations of the Vivado IDE. The layout depicted here might vary from the current version.

Configuration for Audio Embed Function

The following figure shows the Customize IP dialog box with information about customizing parameters for the SDI Audio Embedder.

Figure 11: **Re-customize IP**



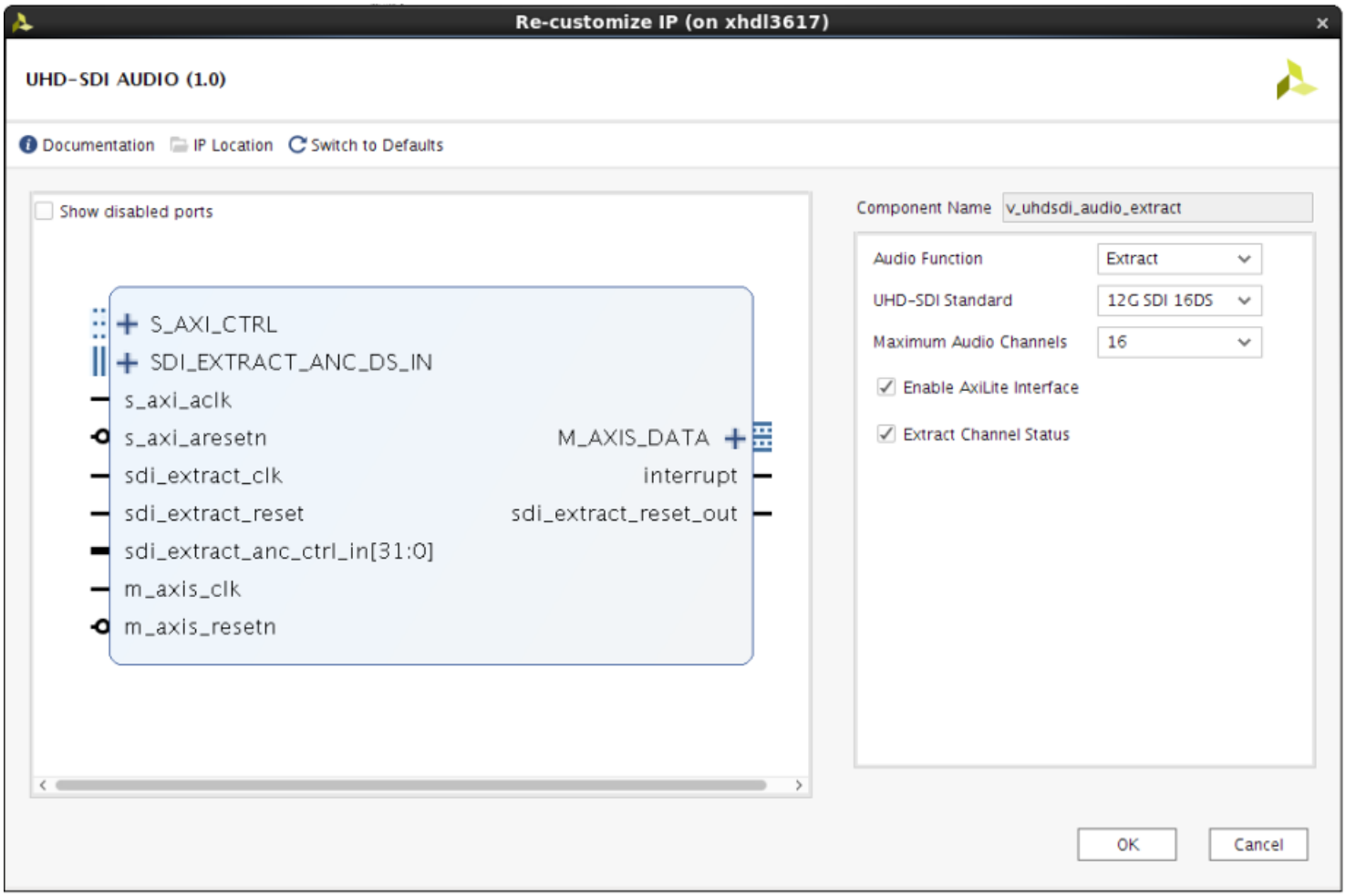
- **Component Name:** Enter a name for the core instance. The Component Name is the base name of the output files generated for this core. This example uses the name v_uhdsdi_audio_embed.
- **Audio Function:** Specifies the Audio Function. Available options:
  - Embed
  - Extract
- **UHD SDI Standard:** Specifies the SDI standard. Available options:
  - 3G SDI
  - 6G SDI

  - 12G SDI 8DS
  - 12G SDI 16DS
- **Maximum Audio Channels:** Specifies the Maximum Audio Channels that should be supported by this core. Available options:
  - 2
  - 4
  - 6
  - 8
  - 10
  - 12
  - 14
  - 16
- **Enable AXI4-Lite Interface:** when enabled, the AXI4-Lite interface is used for configuration. If it is not enabled, port based interface is chosen.

Configuration for Audio Extract Function

The following figure shows the Customize IP dialog box with information about customizing parameters for the SDI Audio Extractor.

Figure 12: **Re-customize IP**



- **Component Name:** Enter a name for the core instance. The Component Name is the base name of the output files generated for this core. This example uses the name v_uhdsdi_audio_embed.
- **Audio Function:** Specifies the Audio Function. Available options:
  - Embed
  - Extract
- **UHD SDI Standard:** Specifies the SDI standard. Available options:
  - 3G SDI

  - 6G SDI
  - 12G SDI 8DS
  - 12G SDI 16DS
- **Maximum Audio Channels:** Specifies the Maximum Audio Channels that should be supported by this core. Available options:
  - 2
  - 4
  - 6
  - 8
  - 10
  - 12
  - 14
  - 16
- **Extract Channel Status:** When enabled, a 192 bit channel status is extracted by the core.

User Parameters

The following table shows the relationship between the fields in the Vivado IDE and the user parameters (which can be viewed in the Tcl Console).

Table 50: **User Parameters**

Vivado IDE Parameter/Value[1]	User Parameter/Value	Default Value
Audio Function	C_AUDIO_FUNCTION	Embed
UHD-SDI Standard	C_LINE_RATE	12G SDI 16DS
Maximum Audio Channels	C_MAX_AUDIO_CHANNELS	16
Enable AxiLite Interface	C_INCLUDE_AXILITE	True
Extract Channel Status	C_EXTRACT_CHANNEL_STATUS	False

Notes:

1. Parameter values are listed in the table where the Vivado IDE parameter value differs from the user parameter value. Such values are shown in this table as indented below the associated parameter.

Output Generation

For details, see the *Vivado Design Suite User Guide: Designing with IP* (UG896).

Constraining the Core

Required Constraints

This section is not applicable for this IP core.

Device, Package, and Speed Grade Selections

This section is not applicable for this IP core.

Clock Frequencies

This section is not applicable for this IP core.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

This section is not applicable for this IP core.

Simulation

For comprehensive information about Vivado® simulation components, as well as information about using supported third-party tools, see the *Vivado Design Suite User Guide: Logic Simulation* (UG900).

Synthesis and Implementation

For details about synthesis and implementation, see the *Vivado Design Suite User Guide: Designing with IP* (UG896).

Example Design

Example design support is not available for the UHD-SDI Audio IP core. However, example design is available for SMPTE UHD-SDI RX Subsystem. As part of the example design for SMPTE UHD-SDI RX Subsystem demonstration, the UHD-SDI Audio IP core is used to embed or extract audio data. For more details on the options and features available, refer to the Example Design section of the *SMPTE UHD-SDI RX Subsystem Product Guide* (PG290).

Verification, Compliance, and Interoperability

The SDI Audio Embedder and Extractor has been verified using simulation and hardware testing. A highly parameterized transaction-based simulation test suite was used to verify the core.

The tests include:

- Different SDI modes and video resolutions
- Different audio sample rates
- Register read and write access

Hardware Testing

SDI Audio Embedder and Extractor has been tested with standard off-the-shelf SDI test equipment. The following table lists different video resolutions on which 16 channel 48 KHz audio embed and audio extract is validated.

Video Resolution	SDI Mode	SDI Source and Sink
720x486i59.94	SD-HDI	Phabrix SXE
720x576i50	SD-HDI	Phabrix SXE
1920x1080i47.95	HD-SDI	Omnitek 4K Toolbox
1920x1080i48	HD-SDI	Omnitek 4K Toolbox
1920x1080i50	HD-SDI	Omnitek 4K Toolbox
1920x1080i59.94	HD-SDI	Omnitek 4K Toolbox
1920x1080i60	HD-SDI	Omnitek 4K Toolbox
2048x1080i47.95	HD-SDI	Omnitek 4K Toolbox
2048x1080i48	HD-SDI	Omnitek 4K Toolbox
2048x1080i50	HD-SDI	Omnitek 4K Toolbox
2048x1080i59.94[1]	HD-SDI	Omnitek 4K Toolbox
2048x1080i60[1]	HD-SDI	Omnitek 4K Toolbox
1280x720p25	HD-SDI	Omnitek 4K Toolbox

Video Resolution	SDI Mode	SDI Source and Sink
1280x720p29.97	HD-SDI	Omnitek 4K Toolbox
1280x720p30	HD-SDI	Omnitek 4K Toolbox
1280x720p50	HD-SDI	Omnitek 4K Toolbox
1280x720p59.94	HD-SDI	Omnitek 4K Toolbox
1280x720p60	HD-SDI	Omnitek 4K Toolbox
1920x1080p23.98	HD-SDI	Omnitek 4K Toolbox
1920x1080p24	HD-SDI	Omnitek 4K Toolbox
1920x1080p25	HD-SDI	Omnitek 4K Toolbox
1920x1080p29.97	HD-SDI	Omnitek 4K Toolbox
1920x1080p30	HD-SDI	Omnitek 4K Toolbox
1920x1080sF23.98	HD-SDI	Omnitek 4K Toolbox
1920x1080sF24	HD-SDI	Omnitek 4K Toolbox
1920x1080sF25	HD-SDI	Omnitek 4K Toolbox
1920x1080sF29.97	HD-SDI	Omnitek 4K Toolbox
1920x1080sF30	HD-SDI	Omnitek 4K Toolbox
2048x1080p23.98	HD-SDI	Omnitek 4K Toolbox
2048x1080p24	HD-SDI	Omnitek 4K Toolbox
2048x1080p25	HD-SDI	Omnitek 4K Toolbox
2048x1080p29.97[1]	HD-SDI	Omnitek 4K Toolbox
2048x1080p30[1]	HD-SDI	Omnitek 4K Toolbox
2048x1080sF23.98	HD-SDI	Omnitek 4K Toolbox
2048x1080sF24	HD-SDI	Omnitek 4K Toolbox
2048x1080sF25	HD-SDI	Omnitek 4K Toolbox
2048x1080sF29.97[1]	HD-SDI	Omnitek 4K Toolbox
2048x1080sF30[1]	HD-SDI	Omnitek 4K Toolbox
1920x1080p47.95	3G-A	Omnitek 4K Toolbox
1920x1080p48	3G-A	Omnitek 4K Toolbox
1920x1080p50	3G-A	Omnitek 4K Toolbox
1920x1080p59.94	3G-A	Omnitek 4K Toolbox
1920x1080p60	3G-A	Omnitek 4K Toolbox
2048x1080p47.95	3G-A	Omnitek 4K Toolbox
2048x1080p48	3G-A	Omnitek 4K Toolbox
2048x1080p50	3G-A	Omnitek 4K Toolbox
2048x1080p59.94[1]	3G-A	Omnitek 4K Toolbox
2048x1080p60[1]	3G-A	Omnitek 4K Toolbox
1920x1080p47.95	3G-B DL	Omnitek 4K Toolbox
1920x1080p48	3G-B DL	Omnitek 4K Toolbox
1920x1080p50	3G-B DL	Omnitek 4K Toolbox
1920x1080p59.94	3G-B DL	Omnitek 4K Toolbox
1920x1080p60	3G-B DL	Omnitek 4K Toolbox

Video Resolution	SDI Mode	SDI Source and Sink
2048x1080p47.95	3G-B DL	Omnitek 4K Toolbox
2048x1080p48	3G-B DL	Omnitek 4K Toolbox
2048x1080p50	3G-B DL	Omnitek 4K Toolbox
2048x1080p59.94[1]	3G-B DL	Omnitek 4K Toolbox
2048x1080p60[1]	3G-B DL	Omnitek 4K Toolbox
3840x2160p23.98	6G-SDI	Omnitek 4K Toolbox
3840x2160p24	6G-SDI	Omnitek 4K Toolbox
3840x2160p25	6G-SDI	Omnitek 4K Toolbox
3840x2160p29.97	6G-SDI	Omnitek 4K Toolbox
3840x2160p30	6G-SDI	Omnitek 4K Toolbox
4096x2160p23.98	6G-SDI	Omnitek 4K Toolbox
4096x2160p24	6G-SDI	Omnitek 4K Toolbox
4096x2160p25	6G-SDI	Omnitek 4K Toolbox
4096x2160p29.97[1]	6G-SDI	Omnitek 4K Toolbox
4096x2160p30[1]	6G-SDI	Omnitek 4K Toolbox
3840x2160p47.95	12G-SDI	Omnitek 4K Toolbox
3840x2160p48	12G-SDI	Omnitek 4K Toolbox
3840x2160p50	12G-SDI	Omnitek 4K Toolbox
3840x2160p59.94	12G-SDI	Omnitek 4K Toolbox
3840x2160p60	12G-SDI	Omnitek 4K Toolbox
4096x2160p47.95	12G-SDI	Omnitek 4K Toolbox
4096x2160p48	12G-SDI	Omnitek 4K Toolbox
4096x2160p50	12G-SDI	Omnitek 4K Toolbox
4096x2160p59.94[1]	12G-SDI	Omnitek 4K Toolbox
4096x2160p60[1]	12G-SDI	Omnitek 4K Toolbox

Notes:

1. Only 8-channel audio embedding and extraction is tested in these modes. Due to a limitation in the blanking period available, a maximum of 8 audio channels per data stream can be embedded or extracted in 2048x1080p/i 29.97/30 Hz & 4096x2160p/i 29.97/30 Hz video resolutions.

Debugging

This appendix includes details about resources available on the Xilinx Support website and debugging tools.

If the IP requires a license key, the key must be verified. The Vivado® design tools have several license checkpoints for gating licensed IP through the flow. If the license check succeeds, the IP can continue generation. Otherwise, generation halts with error. License checkpoints are enforced by the following tools:

- Vivado Synthesis
- Vivado Implementation
- write_bitstream (Tcl command)

Note: IP license level is ignored at checkpoints. The test confirms a valid license exists. It does not check IP license level.

Finding Help on Xilinx.com

To help in the design and debug process when using the core, the Xilinx Support web page contains key resources such as product documentation, release notes, answer records, information about known issues, and links for obtaining further product support.

Documentation

This product guide is the main document associated with the core. This guide, along with documentation related to all products that aid in the design process, can be found on the Xilinx Support web page or by using the Xilinx® Documentation Navigator. Download the Xilinx Documentation Navigator from the Downloads page. For more information about this tool and the features available, open the online help after installation.

Answer Records

Answer Records include information about commonly encountered problems, helpful information on how to resolve these problems, and any known issues with a Xilinx product. Answer Records are created and maintained daily ensuring that users have access to the most accurate information available.

Answer Records for this core can be located by using the Search Support box on the main Xilinx support web page. To maximize your search results, use keywords such as:

- Product name
- Tool message(s)
- Summary of the issue encountered

A filter search is available after results are returned to further target the results.

Master Answer Record for the UHD SDI Audio Core

AR 70290.

Technical Support

Xilinx provides technical support in the Xilinx Support web page for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support if you do any of the following:

- Implement the solution in devices that are not defined in the documentation.
- Customize the solution beyond that allowed in the product documentation.
- Change any section of the design labeled DO NOT MODIFY.

To contact Xilinx Technical Support, navigate to the Xilinx Support web page.

Debug Tools

There are many tools available to address design issues. It is important to know which tools are useful for debugging various situations.

Vivado Design Suite Debug Feature

The Vivado® Design Suite debug feature inserts logic analyzer and virtual I/O cores directly into your design. The debug feature also allows you to set trigger conditions to capture application and integrated block port signals in hardware. Captured signals can then be analyzed. This feature in the Vivado IDE is used for logic debugging and validation of a design running in Xilinx® devices.

The Vivado logic analyzer is used to interact with the logic debug LogiCORE IP cores, including:

- ILA 2.0 (and later versions)
- VIO 2.0 (and later versions)

See the *Vivado Design Suite User Guide: Programming and Debugging* (UG908).

Hardware Debugging

General Checks

Perform the following general checks:

- Ensure that all the timing constraints for the core were met during implementation.
- Verify all clocks are connected and are with expected frequencies.
- Verify all resets are connected and are with expected polarities.
- Ensure that soft resets are de-asserted and core is enabled.
- Ensure that your programming sequence matches with the reference programming sequence provided in General Design Guidelines section.

Core Generation

Ensure that core is generated with expected settings (Audio function, SDI line rate, Maximum audio channels, Axi4-Lite enable) by reading the “GUI Parameters” register (Offset - 0xFC).

Programmable Audio Channels

Ensure that Programmable Maximum Audio Channels (PMAC) is non zero and is correctly set as per the requirement (Register Offset – 0x1C). PMAC should be an even number and is less than or equal to the Maximum Audio Channels set during core generation.

Audio Group Selection

Perform the following checks.

- If audio is embedded to or extracted from the wrong audio group, make sure that audio group is correctly configured (Register offset – 0x20, 0x24, 0x28, 0x2C).
- Ensure that no 2 instances of Audio Mux or Demux engines working on same audio group.

AXI4-Stream Slave Interface

Perform the following checks.

- Ensure that the audio samples are strictly distributed as per the audio sample rate.
- Ensure that audio channels are coming in strictly incremental order as specified in the AXI4-Stream Slave module description.

SDI Transmitter Ancillary Data Control

Perform the following checks.

- The Audio Embedder receives video data streams from SDI Transmitter, embeds audio and transmits the audio embedded video data streams to the SDI Transmitter core.
- The Xilinx SDI Transmitter has the provision to use the video data streams or audio embedded video data streams (ancillary data).
- If Audio Embedder is embedding the audio data and the audio data is not visible on the SDI link, ensure that the SDI Transmitter is configured to use the ancillary data path.

Core Status

After all the configuration is done and core enabled, if the Audio Embedder or Extractor is not working, ensure the core is not under reset by probing the `sdi_embed_reset_out` and the `sdi_extract_reset_out` signals.

Appendix B

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

Documentation Navigator and Design Hubs

Xilinx® Documentation Navigator provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open the Xilinx Documentation Navigator (DocNav):

- From the Vivado® IDE, select **Help → Documentation and Tutorials**.
- On Windows, select **Start → All Programs → Xilinx Design Tools → DocNav**.
- At the Linux command prompt, enter `docnav`.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In the Xilinx Documentation Navigator, click the **Design Hubs View** tab.
- On the Xilinx website, see the Design Hubs page.

***Note*:** For more information on Documentation Navigator, see the Documentation Navigator page on the Xilinx website.

References

These documents provide supplemental material useful with this product guide:

1. *Vivado Design Suite: AXI Reference Guide* (UG1037)
2. *Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator* (UG994)
3. *Vivado Design Suite User Guide: Designing with IP* (UG896)
4. *Vivado Design Suite User Guide: Getting Started* (UG910)
5. *Vivado Design Suite User Guide: Logic Simulation* (UG900)
6. *Vivado Design Suite User Guide: Programming and Debugging* (UG908)
7. *Xilinx® SMPTE UHD-SDI RX Subsystem Product Guide*(PG290)

Training Resources

1. Vivado Design Suite Hands-on Introductory Workshop
2. Vivado Design Suite Tool Flow

Revision Table

The following table shows the revision history for this document.

Date	Version	Revision
04/04/2018	1.0	Initial Xilinx release.

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