



Versal™ ACAP Premium Series Product Selection Guide



Industry's First Adaptive Compute Acceleration Platform (ACAP)

Versal™ Premium Series – Resources

		VP1102	VP1202	VP1402	VP1502	VP1552	VP1702	VP1802
Adaptable Engines	System Logic Cells (K)	1,575	1,969	2,233	3,763	3,837	5,558	7,352
	LUTs	719,872	900,224	1,020,928	1,720,448	1,753,984	2,540,672	3,360,896
	NoC Master / NoC Slave Ports	30	28	42	52	52	76	100
	Distributed RAM (Mb)	22	27	31	53	54	78	103
Memory	Total Block RAM (Mb)	49	47	70	89	89	132	174
	UltraRAM (Mb)	127	190	181	366	366	541	717
	Total PL Memory (Mb)	198	264	282	508	509	751	994
	DDR Memory Controllers	3	4	3	4	4	4	4
	DDR Bus Width	192	256	192	256	256	256	256
Intelligent Engines	DSP Engines	1,904	3,984	2,672	7,440	7,392	10,896	14,352
Scalar Engines	APU	Dual-core Arm® Cortex®-A72, 48KB/32KB L1 Cache w/ parity & ECC; 1MB L2 Cache w/ ECC						
	RPU	Dual-core Arm Cortex-R5F, 32KB/32KB L1 Cache, and 256KB TCM w/ECC						
	Memory	256KB On-Chip Memory w/ECC						
	Connectivity	Ethernet (x2); UART (x2); CAN-FD (x2); USB 2.0 (x1); SPI (x2); I2C (x2)						
Serial Transceivers	GTP Transceivers (32.75Gb/s)	8	28 ⁽¹⁾	8	28 ⁽¹⁾	68 ⁽¹⁾	28 ⁽¹⁾	28 ⁽¹⁾
	GTM Transceivers ⁽²⁾ (58G (112G))	64 (32)	20 (10)	96 (48)	60 (30)	20 (10)	100 (50)	140 (70)
Integrated Protocol IP	CCIX & PCIe® w/DMA (CPM5)	-	2 x Gen5x8, CCIX	-	2 x Gen5x8, CCIX	2 x Gen5x8, CCIX	2 x Gen5x8, CCIX	2 x Gen5x8, CCIX
	PCI Express®	2 x Gen5x4	2 x Gen5x4	2 x Gen5x4	2 x Gen5x4	8 x Gen5x4	2 x Gen5x4	2 x Gen5x4
	100G Multirate Ethernet MAC	6	2	6	4	4	6	8
	600G Ethernet MAC	4	1	8	3	1	5	7
	600G Interlaken	2	0	2	1	0	2	3
	400G High-Speed Crypto Engine	3	1	5	2	2	3	4

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Notes:

1. 16 GTYP transceivers are dedicated to the CPM5 for PCI Express use.
2. GTM transceivers can operate at data rates up to 112Gb/s by combining two transceivers together.

Versal™ Premium Series – Packaging

		VP1102	VP1202	VP1402	VP1502	VP1552	VP1702	VP1802
Package	Package Dimensions (mm)	Ball Pitch (mm)	XPIO DDR Only, XPIO DDR+PL HDIO, MIO GTYP, GTM (112G)					
VFVF1760 ⁽¹⁾	40x40	0.92	180, 306 22, 78 8, 40 (20)		180, 306 22, 78 8, 40 (20)			
VSVC2197 ⁽¹⁾	45x45	0.92		132, 516 0, 78 28, 20 (10)				
VSVA2785 ⁽²⁾	50x50	0.92	180, 306 44, 78 8, 64 (32)	132, 570 0, 78 28, 20 (10)	180, 306 44, 78 8, 80 (40)	132, 570 0, 78 28, 56 (28)	132, 570 0, 78 68, 16 (8)	
VSVA3340	55x55	0.92			180, 306 44, 78 8, 96 (48)	132, 354 0, 78 28, 60 (30)	132, 354 0, 78 68, 20 (10)	132, 354 0, 78 28, 88 (44)
LSVC4072	65x65	1.0					132, 570 0, 78 28, 100 (50)	132, 570 0, 78 28, 140 (70)

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- Notes:
- Some packages are footprint compatible with Versal Prime series devices.
 - VP1202, VP1502, and VP1552 in VSVA2785 support LPDDR4 in 486 I/O only.

Versal™ Premium Series – Figures of Merit

			VP1102	VP1202	VP1402	VP1502	VP1552	VP1702	VP1802
Adaptable Engines	Adaptable Engine Peak Perf – INT1	TOPs	753	941	1067	1799	1834	2656	3514
	Adaptable Engine Peak Perf – INT2	TOPs	345	431	489	824	840	1217	1610
	Adaptable Engine Peak Perf – INT4	TOPs	89	112	127	214	218	316	418
	Adaptable Engine Peak Perf – INT8	TOPs	23	29	33	55	56	81	107
	NoC Cross-sectional Bandwidth	Tb/s	1.7	2.2	1.7	2.2	2.2	2.2	2.2
Memory	Total Bandwidth - Block RAM	Tb/s	202	193	285	366	366	539	712
	Total Bandwidth - Ultra RAM	Tb/s	48	72	69	138	138	205	271
	Total SRAM Bandwidth	Tb/s	250	265	354	504	504	743	982
	DDR4 Memory Bandwidth	Gb/s	76.8	102.4	76.8	102.4	102.4	102.4	102.4
	LPDDR4 Memory Bandwidth	Gb/s	102.4	136.5	102.4	136.5	136.5	136.5	136.5
Intelligent Engines	DSP Engine Peak Perf – INT8	TOPs	13.1	27.5	18.4	51.3	51.0	75.2	99.0
	DSP Engine Peak Perf – INT24	TOPs	4.4	9.2	6.1	17.1	17.0	25.1	33.0
	DSP Engine Peak Perf – CINT18	Complex TOPs	1.9	3.9	2.6	7.3	7.3	10.7	14.1
	DSP Engine Peak Perf – FP32	TFLOPs	3.1	6.4	4.3	12.0	11.9	17.5	23.1
Scalar Engines	Arm® Cortex-A72 Performance	DMIPs	15980	15980	15980	15980	15980	15980	15980
	Arm Cortex-R5F Performance	DMIPs	2505	2505	2505	2505	2505	2505	2505
I/O	Transceiver Bandwidth	Tb/s	3.97	2.08	5.83	4.40	3.39	6.72	9.04
	Sensor I/O Bandwidth	Gb/s	979	1,824	979	1,824	1,824	1,824	1,824
Connectivity Throughput	PCIe Gen5 Throughput	GT/s	256	768	256	768	1536	768	768
	Interlaken Throughput	Gb/s	1200	0	1800	600	0	1200	1800
	Ethernet Throughput	Gb/s	3000	800	4400	2200	1000	3600	5000
	Cryptographic (AES-256) Throughput	Gb/s	1200	400	1600	800	800	1200	1600
Connectivity Ports	10G Ethernet Ports	#	24	8	32	16	16	24	32
	25G Ethernet Ports	#	24	8	32	16	16	24	32
	40G Ethernet Ports	#	6	2	8	4	4	6	8
	50G Ethernet Ports	#	12	4	16	8	8	12	16
	100G Ethernet Ports	#	30	8	44	22	10	36	50
	200G Ethernet Ports	#	12	3	18	9	3	15	21
	400G Ethernet Ports	#	4	1	6	3	1	5	7

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Versal™ ACAP Ordering Information



Device Name

Device Attributes

Package Definition

XC	V	C	1902	-1	M	S	E	V	S	V	D1760
Xilinx	Architecture	Series Name	Device Number	Speed Grade	Voltage	Static Screen	Temp Grade	Ball Pitch	Lid	RoHS6 Code ⁽²⁾	Footprint
XC: Commercial XA: Automotive XQ: Defense	Versal	E: AI Edge C: AI Core M: Prime P: Premium H: HBM	Digits 1-3: Value Identifier Digit 4: # of Primary Cores	-1: Slowest -2: Mid -3: Highest	L: Low (0.7V) M: Mid (0.80V) H: High (0.88V)	S: Standard L: Low Static	E: 0 to 110°C ⁽¹⁾ I: -40 to 110°C ⁽¹⁾ Q: -40 to +125°C M: -55 to +125°C	V: 0.92mm, w/LSC N: 0.92mm, no LSC S: 0.8mm L: 1.0mm	S: Lidless, w/Stiffener Ring F: Lidded B: Lidless, no Stiffener Ring H: Lidded Overhang I: Lidless, w/Stiffener Ring & Overhang	V: Pb-free Ball Q: Eutectic Ball R: Ruggedized, Eutectic Ball	

Note:

1. Operation at 110°C Tj is limited to 3% of the device lifetime and can occur sequentially or at regular intervals as long as the total time does not exceed 3% of device lifetime—except -1E and -3E (standard 0–100°C).
2. All packages have Pb-free bumps.