RF Data Converter Interface

User Guide

UG1309 (v1.3) December 23, 2020





Revision History

The following table shows the revision history for this document.

Section	Revision Summary					
12/23/2020 Version 1.3						
General updates	Updated throughout to add Gen 3 information and clarify content for the different devices (Gen 1, 2, and 3). Removed content that is not related to the GUI and is covered in other documentation.					
Chapter 1: Introduction	Added references to ZCU216 documentation. Updated Feature Support table with ZCU208 and ZCU216 information.					
Software Installation	Added Select Destination figure.					
Settings Menu Options	Revised Communication Interface figure.					
Clock Settings	Added clock information for Gen 3 devices.					
RF-DAC Output Settings—Gen 1 and 2	Added note and Gen 3 information.					
Tile PLL Settings	Added note.					
Converter Settings	Updated Converter Settings figure.					
RF-ADC Settings	Added Calibration Frozen and Attenuation functions.					
RF-DAC Settings	Added information for Gen 3.					
Clock Distribution (Gen 3)	Added new section.					
Interrupts	Added new section.					
FIFO Data	Added new section.					
Selecting the Hardware Target and Bitstream	Updated the overview figure.					
Configuring the Sample Clock	Updated configuring the sample clock figures. Removed Sample Clocks Configuration, Generating a Signal, Acquirir a Signal, ZCU111 and ZCU1275 Setup, and Bitstream Generation sections.					
RF Analyzer Tool Menu Options	Added new section.					
RF Analyzer Tool Tabs	Added new section.					
Appendix A: LVM and TDMS File Format	Renamed appendix. Customization and Testing and Loopback Test information removed. FFT Metrics and Appending Files information moved to appendices.					
08/16/2019	Version 1.2					
Working with the RF Analyzer	Added sub-topics to include detail about installation, generation, and acquisition.					
12/14/2018	Version 1.1					
Chapter 1: Introduction	Added information about supported features.					
File Menu Options	Added information about the Bitstream file menu option.					
Settings Menu Options	Updated information about the Communication and Analysis settings menu options.					
RF-DAC Output Settings—Gen 1 and 2	Updated the section and DAC Current Mode screen capture.					
Power Advantage Tool—Gen 1, 2, and 3	Added new section.					



Section	Revision Summary		
RF Evaluation Tool Tabs	Updated the MemType section and added information about the size limitation in the DDR mode.		
FFT Page	Added information about Zoom Tools.		
Chapter 3: RF Analyzer	Added new chapter.		
Appendix C: Appending Files	Added new section.		
10/19/2018	Version 1.0		
Initial release.	N/A		





Table of Contents

Revision History	2
Chapter 1: Introduction	5
Chapter 2: RF Evaluation Tool	7
Software Installation	7
RF Evaluation Tool Menu Options	
RF Evaluation Tool Tabs	13
Chapter 3: RF Analyzer	34
Overview	34
Working with the RF Analyzer	34
Installing the RF Analyzer	34
RF Analyzer Tool Menu Options	39
RF Analyzer Tool Tabs	44
Appendix A: LVM and TDMS File Format	58
LVM File Format	58
TDMS File Format	60
Appendix B: FFT Metrics	61
Appendix C: Appending Files	63
Appendix C: Appending Files RF-DAC Data Pattern	63
Appendix C: Appending Files RF-DAC Data Pattern Configuration and Preferences	63 63 64
Appendix C: Appending Files RF-DAC Data Pattern Configuration and Preferences Appendix D: Additional Resources and Legal Notices	63 63 64 65
Appendix C: Appending Files RF-DAC Data Pattern Configuration and Preferences Appendix D: Additional Resources and Legal Notices Xilinx Resources	63 63 64 65
Appendix C: Appending Files RF-DAC Data Pattern Configuration and Preferences Appendix D: Additional Resources and Legal Notices Xilinx Resources Documentation Navigator and Design Hubs	63 63 64 65 65
 Appendix C: Appending Files	63 63 64 65 65 65



Chapter 1

Introduction

This document describes the RF Data Converter graphical user interface (GUI) used to drive and analyze the Zynq[®] UltraScale+[™] RFSoC product family.

This general user interface is common to the RF Data Converter Evaluation Tool and the RF Analyzer Tool. It can be used to guide signal generation through RF-sampling digital-to-analog converters (RF-DACs), data capturing through RF-sampling analog-to-digital converters (RF-ADCs), and rapid data analysis using the fast Fourier transform (FFT) and other standard RF data converter metrics. This document primarily focuses on the usage of the GUI.

For the hardware evaluation board and reference design of the Zynq UltraScale+ RFSoC first generation, see the ZCU111 Evaluation Board User Guide (UG1271) and Zynq UltraScale+ RFSoC RF Data Converter Evaluation Tool (ZCU111) User Guide (UG1287). For the Zynq UltraScale+ RFSoC third generation, see the ZCU216 Evaluation Board User Guide (UG1390), Zynq UltraScale+ RFSoC ZCU208 and ZCU216 RF Data Converter Evaluation Tool User Guide (UG1433), and ZCU208 Evaluation Board User Guide (UG1410).

Use the Zynq UltraScale+ RFSoC Product Tables and Product Selection Guide (XMP105) to identify the specific devices that support the different generations of the Zynq UltraScale+ RFSoC family.

When this GUI is used as a component of the RF Analyzer, all board control functions, including onboard clock configuration, RF-DAC current mode control, and external interface configuration are not available. The clock scheme used with the RF Analyzer is controlled in the Vivado tools IP configuration.

The highlights of the RF Data Converter user interface are:

- Ability to control all RF-ADC and RF-DAC channels operating at the same time with a userfriendly graphical interface.
- Ability to configure RFDC clocking subsystem on targeted hardware.
- Direct API function access.
- Save and restore of configurations and preferences that enables quick settings.
- Synchronized data transmission and capturing enabled with multi-tile synchronization (MTS).
- Import and export of data waveform with LVM (ASCII) and TDMS (binary) file format.
- Data length of transmission and capturing of up to 64M samples (DDR mode).
- Enable single or multi-channel views in frequency and time domains for RF analog signals.



The following table compares the features that this software GUI supports with the Evaluation Tool and RF Analyzer.

Table 1: Feature Support

Feature	Evaluation Tool	RF Analyzer	
Communication interface	Ethernet	JTAG-UART	
Board support	ZCU111 ZCU208 ZCU216	Any Zynq UltraScale+ RFSoC device	
Sample memory	DDR memory and block RAM	Block RAM only	
External component support	External PLL, RF-DAC Power supply (on ZCU111)	None	
Multi-tile synchronization (MTS) support	Yes	Yes	
Multi-band support	Yes	Yes with pre-built bitstreams	
Tile clock forwarding	ZCU208 ZCU216	All devices greater or equal to third generation (ZU4x or greater)	
RFDC data stream import/export from/to file	Yes	Yes	
Configuration commands dump	Yes	Yes	
RFDC samples record options	On-chip or external DDR memory	On-chip only	



Chapter 2

RF Evaluation Tool

Software Installation

- 1. The Vivado[®] Design Suite might need to be installed on the host.
- 2. Run the installer supplied with the tool through to completion. This installer might request the LabVIEW run-time engine. If necessary, use this link to download the 32-bit version of the LabVIEW Run-time Engine 2018 SP1 Patch.

🕷 Setup - Xilinx RF Data Converter Evaluation User Interface 1.6.0 — 🛛 🛛 🗙
Select Destination Location Where should RF Data Converter Evaluation User Interface be installed?
Setup will install RF Data Converter Evaluation User Interface into the following folder.
To continue, click Next. If you would like to select a different folder, click Browse.
C:\Xilinx\RF_DC_Evaluation_UI Browse
At least 559.3 MB of free disk space is required.
Next > Cancel



🛃 Setup - RF Data Converter Evaluation User Interface	8	<u></u> -		×
Select Components				
Which components should be installed?				
Select the components you want to install; clear the c install. Click Next when you are ready to continue.	omponents y	ou do not v	want to	
Application			~	
	_	_		
	Ne	xt >	Can	cel

RF Evaluation Tool Menu Options

File Menu Options

- File → Load/Save configuration: Configuration covers all the displayed settings of the Zynq[®] UltraScale+[™] RFSoC such as, real or I/Q mode, mixer settings, and enable or bypass internal PLL. All these settings can be saved and restored. This feature enables quick configuration as well as configurations that can be shared with others. Configuration files are located in \Config\ directory, with the file extension of .cfg.
- File → Load/Save preferences: Preferences are the user-defined settings of the GUI. It includes tabs used for data generation, data capture, and user options in the GUI that are not linked to the device under test (DUT) configuration such as, mapping in the MultiView mode, number of samples, and tone frequency. You can save the preferred settings of GUI or restore any of them. Preferences files are located in \Config\ directory, with the file extension of .prf.
- File \rightarrow Hardware target: RF Analyzer only. Opens the bitstream download screen.
- File → Export ADC Data: This command exports the RF-ADC data captured of all the opened RF-ADC channels with LVM or TDMS file format (chosen in Settings → Data File Format). The default directory is \Data\ADC\.



• File \rightarrow Exit: Exit the software.

Edit Menu Options

• Edit: Standard Windows edit menu.

Settings Menu Options

• Settings → Communication: Displays the current communication interface. Ethernet is used for the RF Evaluation Tool.

Communication setting Interface Selection	s	×
	Ethernet	~
Int	erface Configuratio	n
IP Address	169.254.10.2 Ping response	e recieved
Control Port 808	31 Data Po	rt 8082
	Cancel	ОК

Figure 1: Communication Interface

 Settings → Dynamic Performances: Some RF-ADC metrics are based on the frequency range. On the RF-ADC FFT page, there is a marked-out calculation table, the SNR, ENOB, SFDRxH23, and FspurxH23 are calculated based on the Band of Interest set here. In loop mode, some metrics are calculated over a number of measurements that can be set under Averaging.



Communication		
Dynamic Performances Data File Format Data Folders	Board ZCU111	E XILINX.
	Package G1517	
	Processing System (PS)	
	Programmable Logic (PL)	
	RF Data Converter Subsystem : DAC	
DAC Tile 0 DAC 2 PL Master DAC 1 DAC 0	DAC Tile 1 0AC2 RL BAC1 BAC1 BAC2 BAC2 BAC2 BAC2 BAC2 BAC2 BAC2 BAC2	
	RF Data Converter Subsystem : ADC MTS @ Perver	
ADC Tile 0 ADC 23 PLL Master ADC 01	ADC Tile 1 ADC 31 PL ADC 01 ADC Tile 2 ADC 33 PL ADC 01 ADC Tile 3 ADC 33 PL ADC 01 ADC Tile 3 ADC 33 PL ADC 01 ADC Tile 3 ADC 33 PL ADC 01 ADC 01 ADC Tile 3 ADC 33 ADC 01 ADC 01 AD	

Figure 2: Band of Interest

• Settings → Data File Format: Indicate your preferred file format between the .lvm and .tdms formats. For the RF-ADC output, you can individually select whether Data or Metrics is exported.





 Settings → Data Folders: Select your preferred folders for the test vector of RF-DAC, saved data from RF-ADC, and onboard clocking frequency configuration files. By default, these are located in \Data\, with ADC, DAC, and Clocking as the respective folder names.



Window Menu Options

• Window → MultiView: The MultiView option makes it possible to view several of the RF-ADC or RF-DAC FFT diagrams on a single page with customized channels. Click Generate/Acquire All to update all the windows.



Figure 4: MultiView RF-ADC FFT

To display all the RF-ADC channel signals in the time domain, select the **ADC Time Domain** option. This feature is particularly useful in the MTS mode.



Figure 5: MultiView RF-ADC Time Domain



 Window → Commands log: This opens the commands log window where the history for all the commands can be seen, the API can be run, and feedback can be viewed. If an error occurs with the GUI, it appears on the command log. The command log window can also be used to create a dump file which lists out all the previously used commands. This can be useful in debugging if an error occurs with a sent command.

2 Zynq UltraScale+	RFSoC Evaluation So	oftware				- 🗆 X
File Edit Settings	Window Help					
Overview	Commands L	00				
	_					
		-				
Time	Exec (ms)	Query			Answer	^
15:07:56	302	GetQMCSettings 1 0 3		GetQMCSettings 1 0 3 0.000000 0.000000 0 0 0 0		
15:07:56	151	GetNyquistZone 1 0 3		GetNyquistZone 1 0 3 1		
15:07:57	252	GetInvSincFIR 0 3		GetInvSincFIR 0 3 0		
15:07:57	201	GetDecoderMode 0 3		GetDecoderMode 0 3 1		
15:07:57	151	GetInterpolationFactor 0 3		GetInterpolationFactor 0 3 1		
15:07:57	351	GetIPStatus		GetIPStatus 1 15 15 1 1 1 3 15 1 1 1 15 15 1 1 1 3 15 1 1 0 0 0 0 0 1 3 15 1 1 (0 0 0 0 1 3 15 1 1 807416096	
15:07:57	150	GetClockSource 1 1		GetClockSource 1 1 1		
15:07:58	302	GetBlockStatus 1 1 0		GetBlockStatus 1 1 0 4.000000 16 17 1 3 3		
15:07:58	200	DynamicPLLConfig 1 1 1 245.76000	0 4000.000000	DynamicPLLConfig 1 49 3		
15:07:58	201	GetPLLLockStatus 1 1		GetPLLLockStatus 1 1 2		
15:07:58	252	GetMixerSettings 1 1 0		GetMixerSettings 1 1 0 0.000000 0.000000 2 0 16 1 0		
15:07:59	301	GetQMCSettings 1 1 0		GetQMCSettings 1 1 0 0.000000 0.000000 0 0 0 0		
15:07:59	151	GetNyquistZone 1 1 0		GetNyquistZone 1 1 0 1		
15:07:59	203	GetInvSincFIR 1 0		GetInvSincFIR 1 0 0		
15:07:59	200	GetDecoderMode 10		GetDecoderMode 1 0 1		
15:07:59	202	GetInterpolationFactor 1 0		GetInterpolationFactor 1 0 1		
15:08:00	252	GetMixerSettings 1 1 1		GetMixerSettings 1 1 1 0.000000 0.000000 2 0 16 1 0		
15:08:00	253	GetQMCSettings 1 1 1		GetQMCSettings 1 1 1 0.000000 0.000000 0 0 0 0		
15:08:00	253	GetNyguistZone 1 1 1		GetNyquistZone 1 1 1 1		
15:08:00	151	GetInvSincFIR 1 1		GetInvSincFIR 1 1 0		
15:08:01	252	GetDecoderMode 11		GetDecoderMode 1 1 1		
15:08:01	201	GetInterpolationFactor 1 1		GetInterpolationFactor 1 1 1		
15:08:01	251	GetMixerSettings 1.1.2		GetMixerSettings 1 1 2 0.000000 0.000000 2 0 16 1 0		
15:08:01	252	GetOMCSettings 112		GetOMCSettings 1 1 2 0.000000 0.000000 0 0 0 0		
15:08:01	151	GetNyouistZone 112		GetNyouistZone 1121		
15:08:02	201	GetInvSincEIR 1.2		GetInvSincEIR 12.0		
15:08:02	250	GetDecoderMode 12		GetDecoderMode 1 2 1		
15:09:02	200	GetInternolationEactor 1.2		GetInternolationEactor 1.2.1		
15:09:02	250	GetMixerSettingr 1.1.3		GetMixerSettings 1.1.3.0.000000.0.000000.2.0.16.1.0		
15:08:02	250	GetOMCSettings 113		GetOMCSettings 1 1 3 0 000000 0 000000 0 0 0 0		
15:08:03	201	GethymuistZone 113		GetNequitZone 1131		
15:08:03	200	Gatter/SincElR 13		GetIns/SincElR 13.0		
15,00,03	200	GetDecoderMode 1.2		GetDesedeMede 1.2.1		
15/00/03	200	Catleters elation Factor 1.2		California a lation for the 1.2.1		
10:00:05	133	Getinterpolationractor 1.5		Getinterpolationractor 1.5.1		
						*
Dump			Command			Send
Board: ZCU111	Package: G1517	Device: ZU28DR	Communication OK		Modification pending. Press "Apply" to validate	

Figure 6: **Command Window**

• Window → Merge all windows: Opened tabs for DACs or ADCs can be moved to separate windows with a left-click and drag on the tab area as shown in the following figure. This command merges all the separate windows into one.

Figure 7: Create Separate Windows



• Window → Attach: Opened tabs can be moved to separate windows. This command merges back selected separate windows.



Help Menu Options

• Help → About: Provides general information about the RF Data Converter evaluation tool. Use this option to check the version, which is used when building the .lvm file.

RF Evaluation Tool Tabs

The Overview page is the home page of the RF Data Converter evaluation tool GUI. It displays the top framework of all the converters grouped by tile. This page is displayed upon start-up and cannot be closed.

Overview

Generation 1 and 2

In the overview tab, select **MemType** to choose the memory type, **BRAM** (on Zynq[®] UltraScale+[™] RFSoC) or **DDR** (on the ZCU111 evaluation board). The DDR is bigger in size than the block RAM.



Figure 8: Overview Page—Gen 1 and 2

Generation 3

In the overview tab, click on an DAC or ADC tile and then choose the memory type, **BRAM** (on Zynq[®] UltraScale+[™] RFSoC) or **DDR** (on the Gen 3 evaluation board). The DDR is bigger in size than the block RAM.



RF Data Converter	Evaluation User Interface (I Window Help	(FEvalTool v2.2)									
verview	ADC Tile 0	ADC Tile 0 - ADC 0									
		Board	I ZCU216					3	XILIN	JX.	
		Packa	ge G1517						ADC Tile 0		
		Processing	J System (PS)								
		Programma	ble Logic (PL)						Tile Status		
		RF Data Convert	ter Subsystem : DAC		MTS			Ava Power-on	ilable State Machine (Curre	ent State)	
DA Til 22	AC e 0 DAC 3 8 DAC 2	DAC Tile 1 DAC 3 229 DAC 2	DAC Tile 2 230 DAC 3 DAC 2	DAC Tile 3 DA 231 DA	iC 3			Pov	rered	V 15	
Ma	Ter DAC 1 DAC 0	DAC 1 DAC 0	DAC 1 DAC 0	PLL DA	IC 1			Clo	ck Detected		
c	lock Distribution								Memory Selection	1	
		RF Data Convert	er Subsystem : ADC		MTS			Memory	Type BRAM	~	
AD	ADC 3	ADC ADC 3	ADC ADC 3	ADC	DC 3	Power Settings			Sele	ect	
22 Ma	4 ADC 2 PLL ADC 1	225 ADC 2 PLL ADC 1	226 ADC 2 PLL ADC 1	227 AE PLL	C 2	Settings					
	IICK ADC 0	ADC 0	ADC 0		C 0		D Refresh	Apply	谷 Reset	Shutdown	Tile Settings
							S Aeresi	-thbill	A Neser	- unatdown	The settings

Figure 9: Overview Page—Gen 3

Clock Settings

There are different on-chip clock distribution architecture limitations in different RFSoC generations. The user guides for each board show which RF PLLs/tiles are driven from off-chip and which RF PLLs/tiles get clocks from the on-chip clock distribution system.

Gen 1 and 2: see the ZCU111 Evaluation Board User Guide (UG1271) for more information.

Gen 3: see the ZCU208 Evaluation Board User Guide (UG1410) or ZCU216 Evaluation Board User Guide (UG1390).

Gen 1 and 2 Predefined Mode

In the overview tab, select **Clock Settings** to open the onboard PLL GUI in the right panel. This GUI allows you to control and set the input and output frequencies for the PLLs that are integrated onto the ZCU111 evaluation board. In the Predefined mode, available frequencies are provided in the drop-down list for RF-ADC and RF-DAC. Choose your options and click **Apply**. The GUI programs the onboard RFPLLs. If your desired frequency does not appear in the predefined list, then you must use the advanced configuration mode to customize the sample rates.





	Board ZCU111			E XILINX
	Package G1517			OnboardPII
	Processing System (PS)			
				Onboard PLL
	Programmable Logic (PL)			Configuration Mode
	RE Data Converter Subsystem - DAC	MTS		Predefined Advanced
				PEE Clock 122 000 v MUz
DAC	DAC		DAC	U90
Tile 0 DAC 3	Tile 1		Output Mode	REDI 1 245 760 w h to a
PH	PIL		20 mA	U102 / ADC Tiles 0 + 1
Marter DAC 1	DAC 1		AVTT	REP11 2 245.760 Milling
DAC 0	DAC 0		2.5 V	102.406
				204.800 REPLL 3 ✓ 245.760
				409.600
	KF Data Converter Subsystem : ADC	MIS	Settings	737.280
ADC		ADC		1474.560 1966.080
Tile 0	Tile 1 Tile 2 ADC 31	Tile 3	Settings	2048.000
AUC 23	AUC 23	AUC 23		2457.600 2949.120
	Put Put	-u	Clocking Diagram	3072.000
	ADC 01 ADC 01	ADC 01		3194.880 3276.800
Master ADC 01				
ADC Tile 0 ADC 23	ADC Tile 1 ADC 23 PL ADC 01	ADC Tile 3 ADC 23 PLL ADC 01	Clock Settings	1966.000 2068.000 249.57.00 249.51.00 307.2.00 3194.800 375.600

Figure 10: Clock Settings Predefined—Gen 1 and 2

Gen 1 and Gen 2 Advanced Mode

The Advanced mode accepts the configuration file for the individual clock ICs on your clocking plug-in board. You can choose the .tcs file shipped along with this tool or generate your own configuration files using TICS Pro Software.

Click **Advanced** to select the desired clock configuration.



Figure 11: Onboard PLL Advanced



Gen 3

In the overview tab, select **Clock Settings** to open the onboard PLL GUI in the right panel. This GUI allows you to control and set the input and output frequencies for the PLLs mounted on the CLK104 (daughter board of the ZCU216 and ZCU208 boards). Choose your options and click **Apply**. The GUI programs the onboard RFPLLs.

	Board ZCU216		🔪 XILINX.
	Package G1517		OnboardPLL
	Processing System (PS)		Onboard PLL
	Programmable Logic (PL)		LMK KEF CIOCK
	RF Data Converter Subsystem : DAC MTS		LMX DAC RFPLL
M	DAC DAC DAC DAC Tile 0 DAC 2 Tile 1 DAC 3 DAC 2 Tile 1 DAC 2 DAC 7 Fil DAC 1 DAC 1 DAC 1 DAC 2 DAC 1 DAC 1 DAC 1 DAC 3 DAC 1 DAC 1 DAC 1		Clock 104 CikOut0 245,760 0.0007 For ADC FOutA 0.000 LMX FOut8 0.000
	Clock Distribution		ClkOut4 - 245.760 - 0.000 - Fosc DAC FOutA - 0.000 LMX Fourt8 - 0.000
	RF Data Converter Subsystem : ADC MTS		ClkOute DAC REFCLK
A Ti	ADC Tile 0 ADC3 ADC2 File 1 ADC3 ADC2 File 1 ADC3 ADC2 File 2 ADC3 ADC2 File 3 ADC3 File 3 ADC	 Power Settings Clock Settings 	CIROU12 - 245.760 - ADC REFCLK CIROU89 - 122.890 - PL CLK (MMCM Fin) CIROU89 - 7.680 - AMS SYSREF CIROU99 - 7.680 - PL SYSREF All values are

Figure 12: Onboard PLL —Gen 3

RF-DAC Output Settings—Gen 1 and 2

Note: In Gen 3, the variable output power (VOP) provides fine control for the DAC output. For more information, see *Zynq UltraScale+ RFSoC RF Data Converter LogiCORE IP Product Guide* (PG269).

RF-DAC output current settings are only available with the RF evaluation tool. In the overview tab, click the **Power Settings** button to open the RF-DAC output settings page in the right panel. Choose from the available 20 mA/2.5V and 32 mA/3.0V options. Power supply for this current mode control (DAC_AVTT) is programmable on the board through the power management unit (PMU). Click **Apply** to program the onboard PMU for either 2.5V or 3.0V, and switch to the corresponding RF-DAC output current mode.



	Board ZCU111				🐒 XII INX
	Package G1517				PowerManagement
	Processing System (PS)				DAC Output Settings
	Programmable Logic (PL)	PL Settin	195		Current / Voltage Mode 20 mA / 2.5 V
	RF Data Converter Subsystem : DAC	MTS			20 mA / 2.5 V 32 mA / 3.0 V
DAC Tile 0 PL Master DAC 1 DAC 0	DAC DAC 1 Tile 1 DAC 2 RL DAC 1 DAC 0			DAC tput Mode Current 20 mA AVTT 2.5 V	Launch Power Advantage Tool
	RF Data Converter Subsystem : ADC	MTS	6	Power Settings	
ADC Tile 0 ADC 23 PL Master ADC 01	ADC Tile 1 ADC 23 RL ADC 01	ADC Tile 3 ADC 23 PL ADC 01	8	Clock Settings Clocking Diagram	

Figure 13: RF-DAC Current Mode

Related Information

RF-DAC Settings

Power Advantage Tool—Gen 1, 2, and 3

The power advantage tool is integrated in this software to provide power related information for reference. This power advantage tool displays voltage, current, and power information for each rail that is monitored by the onboard power management unit. The power advantage tool communicates with the evaluation software through the JTAG interface. To retrieve the power information, connect the JTAG port to the host. For Gen 3, if the installation path of the evaluation tool is not standard, it must be changed in the .ini file to enable the power advantage tool.





		Board ZCU111				🐒 XILINX
		Package G1517				
	P	rocessing System (PS)				
	D ZynqusRowerTeel	esize Button		- 0)		DAC Output Settings
	ZYNA	Zynq Utracicale*	UFSoC Power Man	agement		Creaters / Anade Weeks 01 Jun / 53 A. (6)
-	Low Put Poses				DAG	ZynqUS Power Advantage Tool
Tile 0	Alter Alter	Piti Respectives D.P. Fall Power Domain		784.3 wW	Output Mode Current	Laarsch Power Advantage Tool
Master					20 mA	
				11275.4 wW	2.5 V	
_	Print Earl Prover Disease				do Power	
400	Logic Domain			10214.8 wW	10 ¹ Settings	
Tile 0	and the second se				Settingi	
Matter	ADC ON	ADC 01	ADC 01	ADC 01	Clocking Diagram	
					(i) Board	

Figure 14: Power Advantage Tool

Figure 15: Zynq UltraScale+ RFSoC Power Management

ZY	IltraSCALE+	Zynq UltraScale-	- RFSo	C Powe	er Mana	gement	
Low Power 85/0 ©100% R5/1	Preset	PS Temperature 0.0° Full Power Domain Vccrv2 Motriva Motriva	Voltage (V) 1.197 1.203 1.798	Current (mA) 605.0 43.0 9.5	Power (mW) 724.5 51.8 16.9	793.2 mW	Select Plot Rails System 1 Legend About
@100% @100% TCM	@100% @100% @100% GPU DDR	Low Power Domain	Voltage (V) 0.846 1.801	Current (mA) 1884.5 862.5	Power (mW) 1594.7 1553.4	3148.1 mW	
OCM PMU CSU Periph	Domain	Prog Logic Domain VecilyT VaD_Fare Marakec VecilyT_AMS Analog Rails DBC_AYTT	Voltage (V) 0.856 1.201 0.903 0.851 2.502	Current (mA) 4232.5 0.0 8.5 2086.5 213.5	Power (mW) 3624.0 0.0 7.6 1776.0 534.0	11278.6 mW	
Progr Logic	ammable O c Domain	DAC_AVCCAUX ADC_AVCC ADC_AVCCAUX DAC_AVCC	1.802 0.923 1.817 0.927	172.5 1502.0 1356.0 1266.0	310.8 1387.5 2464.5 1174.2		
②100% ④100% H 川 ²⁵	Options i ard ECC % / 25%, 0.85V, 2.5V	Total				15219.9 mW	



RF-ADC/RF-DAC Tile

In the overview tab, selecting any of the RF-ADC or RF-DAC tile opens the individual tile page as illustrated in the following figure. In this tab, you can reset, shut down, start up a tile, and also view the current tile status by clicking **Refresh**. When a tile is in operation, selecting **Tile settings** opens up the configuration tab for it. Refer to the *Zynq UltraScale+ RFSoC RF Data Converter LogiCORE IP Product Guide* (PG269) for more information on the commands and power up state machine status.





Tile PLL Settings

Note: See Clock Distribution (Gen 3) for clock and PLL settings in Gen 3.

For Gen 1 and 2, in the tile settings page, click on the **PLL** box to open the PLL settings in the right panel.





Figure 17: Clock Source—Gen 1 and 2

For Gen 3, to select clock sources and options for on-chip clock distribution, use the **Clock Distribution** button shown in the following figure.





Ensure that the input clock rate is correct for the internal PLL, enabled or bypassed. When bypassing the internal PLL, the input clock functions as a sampling clock of the converters in the tile, and is usually several GHz. When the internal PLL is enabled, ensure that the input frequency is within the range specified by the *Zynq UltraScale+ RFSoC Data Sheet: DC and AC Switching Characteristics* (DS926). A reference frequency can also be typed in when the internal PLL is disabled. This helps the GUI calculate the reference spurs on the FFT page.



Converter Settings

In each RF-ADC/RF-DAC tile, the available converter channels and associated internal function blocks are cascaded in the block diagram, and the text shows the current settings. Click any function block to open the config page in the right panel. FIFO and Crossbar have their own separate pages.



Figure 19: Converter Settings

RF-ADC Settings

 Calibration Mode: Selects between different calibration optimization schemes depending on the features of the input signals. Mode 1 is optimal for input frequencies F_{samp}/2(Nyquist) +/-10%. Otherwise, use Mode 2.





Figure 20: Calibration Mode

- **Nyquist Zone:** Choose the Nyquist zone in which the input signal located. This is related to interleaving calibration and must be indicated correctly. Zone 1 is for odd numbered zones and Zone 2 is for even numbered zones.
- Threshold Detection: Use this to set the embedded threshold detection parameter.
- Decimation Settings: Use this to select the decimation factor.

Note: If you select Off, you will not receive any data.

Xilinx[®] recommends that the same decimation factor is used for all data converters in the tile to avoid potential timing issues at the interface.

• **Calibration Frozen:** Use this to freeze the interleaving calibration for each channel. The green light indicates a frozen status. The freeze function freezes or unfreezes the interleaving calibrations. The disable pin function can disable the calibration freeze real-time port control.

The following functions are for Gen 3 only.

- Attenuation: Attenuation value of on-chip DSA in dB for each RF-ADC channel. The disable pin can disable the DSA pin control.
- Power Management: Use to power down or power up a single channel within a tile.

RF-DAC Settings

- **Decoder Mode:** Choose which performance to optimize: noise floor or linearity. Noise floor optimization must be selected for communication applications.
- **Nyquist Zone:** Choose which Nyquist zone the signal will be located in: Normal Mode for Nyquist zone one and Mix Mode for Nyquist zone two. See this link for more information.
- Interpolation Settings: Choose your interpolation factor. If you select Off, some digital blocks will be powered down and the outputs will not be active.



• **Inverse Sinc Settings:** Enabling Inverse Sinc compensates sinc roll-off at high frequencies. This function is only effective when the signal is located in Nyquist zone one.

The following functions are for Gen 3 only.

- **DataPath:** The drop-down box used to choose datapath modes. The four available modes are Full Nyquist DUC, IMR low pass, IMR high pass, and DUC bypass.
- **Current:** The VOP current value. This value is also displayed on the diagram of each channel.
- **Power Management:** Use to power down or power up a single channel within a tile.

Settings Common to RF-ADC and RF-DAC

- **Mixer Settings:** Xilinx recommends setting the Crossbar page first, and then set other parameters of the mixer and NCO because the mixer is bypassed in the real-to-real mode.
- QMC Settings: QMC module contains gain, phase, and DC-offset adjusting. These are used to compensate unmatched I and Q signal path when converters interface to external modulators or demodulators. DC offset takes effect with DC coupling only. Phase offset takes effect with complex mode only. Gain takes effect in all modes.
- **FIFO:** Show the FIFO clock rates and number of words on PL and converter side for information only.



Crossbar

Click the **Crossbar** button at the bottom of the converter settings page, or, alternatively, the **Crossbar** box in the left panel to display the crossbar page. This page determines the real or complex mode of the mixer and multi-bands operating mode. Complex mode activates a pair of channels to support both in-phase(I) and quadrature(Q) signal. Because of the complex mixer (and NCO) architecture, the real-to-complex (R2C) or complex-to-complex (C2C) mode is allowed, but complex-to-real (C2R) mode is not allowed. This means that there is no C2R mode available for RF-ADC and no R2C mode available for RF-DAC. Correct operating modes are ensured by this tool. In complex mode, even channels are always used for I signals, and odd channels are used for Q signals.



Figure 21: Crossbar



Multi-Bands

Multiple bands enable one RF-DAC or RF-ADC analog channel and share multiple DUC or DDC channels to transmit or receive the multi-band carrier signals. For RF-DAC, multiple baseband signals can be up-converted in separate DUC chains and then combined at the crossbar before being sent to the analog RF-DAC block.

In RF-ADC, the multi-band/carrier inputs from one RF-ADC are split into multiple DDC paths for down-conversion. The carriers from different bands are separated and located at low frequencies (in general at zero). In the multi-band operation, a converter is enabled on channel 0 (dual bands at channel 0 and 1) or channel 2 (dual bands at channel 2 and 3). Multi-bands operations support both real and complex output. All these configurations can be enabled at the crossbar page. The following figure illustrates the dual bands configuration of C2C and C2R.



Figure 22: Multi-Bands

FFT Page

Click **Acquisition** in the ADC settings page, or **Generation** in the DAC settings page, to open the FFT page. In the RF-DAC FFT page, the single tone and dual tone generator is embedded in the software. To generate a complex modulated signal, load a test vector file. There are variations of sub-menus in this page, including signal characteristics, customizing FFT plot, windowing function, test vector input, and output. When decimation or interpolation is enabled in the RF-ADC or RF-DAC data path, with a value more than 1 (bypass), Eff.Fs and Fs show different values in this table. Fs indicates the sampling frequency of observed RF-ADC or RF-DAC, Eff.Fs indicates the sampling frequency of original data stream (base band) after decimation or before interpolation. The X-axis (frequency) of the FFT plot reflects back the Eff.Fs. The following figure shows the RF-ADC FFT page.





Figure 23: RF-ADC FFT Page

The following figure shows the Zoom Tools on the FFT page. Use the default Zoom Tools or edit the axis range to directly configure the start and/or end values for best plot observation.



Figure 24: FFT Zoom Tool



Multi-Tile Synchronization

The multi-tile synchronization (MTS) feature enables multiple converter channels working with an aligned and deterministic latency across tiles and chips. MTS is supported as a standard feature with the RF evaluation tool. In the overview page, there is an MTS tab on the right corner of the ADC and DAC group. Click the **MTS** tab to open the function window.



Figure 25: MTS

The external clocking coming from the board must be set up according to the MTS rules. For more information, see the "Clock Settings" chapter in Zynq UltraScale+ RFSoC RF Data Converter LogiCORE IP Product Guide (PG269). To enable the MTS function, check **enable** \rightarrow **Apply**. This enables the internal clock scheme to support MTS. After MTS is enabled, select **Synchronise** to implement the alignment and display the measured latency of each tile. An offset value also shows how many T1 (period of sampling clock) offset have been applied to align the tiles. The error lamp lights up red if there are any errors during MTS.



Set	ttings Window Help						
	ADC Tile 0	DAC Tile 0	ClockDistribution				
			Board ZCU216				
			Package G1517				
		Proc	cessing System (PS)				DAC - Multi Tile Synchronisation
							Configuration
		Prog	rammable Logic (PL)				Tile Index 0 1 2 3
ſ		DE Data	Committee Colomation - DAC		MTC		MTS Enable
		KF Data	Converter Subsystem : DAC		MIS		Sync Array 🗹 🗹 🗹
	DAC	DAC	DAC	DAC			MMCM Input Freq. 491.520 MHz
	Tile 0 DAC 3	Tile 1 DA	C 3 Tile 2 DAC 3	Tile 3	DAC 3		Target Latency -1 🖨
	228 DAC 2	229 DA	230 DAC2	231	PU DAC 2		Statur
	Master DAC 1 DAC 0	DA	C 1 DAC 1 C 0 DAC 0		DAC 1 DAC 0		Error
	Clock Distribution						SysRef Enable Marker Delay 15
Ĩ		RF Data	Converter Subsystem : ADC		MTS		Offset Latency
ſ							Tile 0 0 48 All values are expressed in T1
	ADC	ADC	ADC	ADC	400.2	Settings	Tile 1 0 48 (1/Fs)
	Tile 0 ADC 2	Tile 1 AD	C2 Tile 2 ADC3	Tile 3 227	ADC 2		Tile 2 0 48
	PLL	PLL	PLL		PLL	Clock Settings	Getlen data
	Master ADC 1	AD AD	C1 ADC1		ADC 1 ADC 0		metal: info: DTC Scan T1
							metal: info: DAC0: 00000000000011222200000000000000111222000000
							Refresh Apply Synchronise NCO Reset

Figure 26: MTS Successful

Clock Distribution (Gen 3)

The Zynq UltraScale+ RFSoC Gen 3 supports on-chip clock distribution. For more information, see Zynq UltraScale+ RFSoC RF Data Converter LogiCORE IP Product Guide (PG269).

Click the **Clock Distribution** button in the overview page to display the page shown in the following figure.





Figure 27: Clock Distribution

Note: The settings on this page should comply with the limitations of the on-chip clock distribution system and PLL.

Each tile has four input fields and a check box for an in-tile PLL, as described here.

- Sample Clock (MHz): Select the desired sampling rate of converters, which can be generated by the in-tile PLL or a forwarded sampling clock from the source tile.
- PLL Checkbox: Enable or disable the PLL in this tile.
- **Reference Clock (MHz):** Enter the reference or a sampling clock frequency, can be from an external input or a forwarded clock from the source tile.

Note: This frequency can be a reference for the in-tile PLL or the frequency of the sampling clock if it is used directly.

- **Output Divider (M):** Shows the output divider of the on-chip PLL (incorrect for PLL disabled tile). This field is for reference only and not editable.
- **Source Tile:** Use the drop-down list to select which tile the clock (reference) comes from. Select the tile itself for the external clock input to this tile, or the source tile for a forwarded clock (reference or sampling clock). Select the tile itself for a source tile.
- **Distribute Clock:** Select options to distribute the clock (acting as source tile) and which clock is distributed:
 - 1. None: select to not distribute the clock.



- 2. Input clock: select to distribute the input clock from an external input. This clock can be a low-frequency reference clock or a high-frequency sampling clock.
- 3. PLL output clock: select to distribute the clock generated by the in-tile PLL.

An example configuration is shown in the following figure.



Figure 28: **Example Clock Distribution Configuration**

In this example, two external input clocks (both at 245.76 MHz) are fed to the ADC_Tile_226 and DAC_Tile_230, respectively. All desired RF-ADC clocks are 2457.6 MHz and desired RF-DAC clocks are 4915.2 MHz.

For the RF-ADC group, Tile_226 distributes its *PLL output clock* to other RF-ADC tiles. For the RF-DAC group, Tile_230 distributes its input reference to all other RF-DAC tiles.

All RF-DAC tiles enable their PLLs to generate the desired sampling clock at 4915.2 MHz.

When the Apply button is clicked, the GUI updates these configurations to the chip, restarts all tiles, reads back status, and updates the GUI. This might take a while and a percentage bar shows the progress.

The following figure shows the tile status based on the clock distribution configurations in this example.



	ClockDistribution								
		Boa	rd ZCU216				S XI	INX	
		Pack	age G1517						
		Processi	ng System (PS)						
		Programm	nable Logic (PL)						
		RF Data Conv	erter Subsystem : DAC		MTS				
DA Til 22 Ma	AC DAC 3 28 DAC 2 PL DAC 1 DAC 1 DAC 0	DAC Tile 1 DAC 3 229 DAC 2 PLL DAC 1 DAC 1	DAC Tile 2 230 PLL DAC 1 DAC 1 DAC 0	DAC Tile 3 231	DAC 3 DAC 2 LL DAC 1 DAC 0				
C	Clock Distribution								
		RF Data Conv	erter Subsystem : ADC		MTS				
AL Til 22 Ma	DC ADC 3 Ie 0 ADC 3 PL PL ADC 1 ADC 0	ADC Tile 1 ADC 3 225 PLL ADC 1 ADC 1 ADC 0	ADC Tile 2 ADC 3 226 ADC 2 FL ADC 1 ADC 0	ADC Tile 3 227	ADC 3 ADC 2 LL ADC 1 ADC 0	 Power Settings Clock Settings 			

Figure 29: Tile Status Based on Clock Distribution

For RF-ADC, only Tile 0 (Tile_226) PLL is enabled, and PLLs in other tiles are disabled. The green channel status shows they are in operation status because these tiles are forwarded the sampling clock from Tile 0. For RF-DAC, all PLLs are enabled because Tile 0 (Tile_230) forwarded its reference to other tiles. The status of RF-ADCs and RF-DACs reflect the settings in the Clock Distribution page in this example. The PLL status can also be checked in the PLL page for each tile. For Gen 3, the PLL page shows the status only and all the clock configurations rely on this Clock Distribution page, which is different from the PLL page in Gen 1 and Gen 2.

Interrupts

Click the **Interrupts** button to display the page shown in the following figure (this example is for RF-DAC).



€ RF Da	ta Converter Ev	aluation User Interface (RFE	valTool v2020.2-es1)										- 🗆 ×
File Edit	Settings Wi	ndow Help											
Overview		ADC Tile 0	ClockDistribution	DAC Tile 0	,						V/II IN	IV	
	FIFO Data	Interpolation	Mixer	rossbar	QMC Gain/Phase	Inverse Sinc		Real		DAC T	Ile 0 - DAC 0 - Ir	NX., Iterrupts	
	Real	1x	Bypass 		Disabled	Disabled	Enabled	→ VOUT_N VOP 32.00 mA	Return		Interrupts Status	4	
	FIFO Data Real	Interpolation 1x	Mixer Bypass 	rossbar	QMC Gain/Phase Disabled	Inverse Sinc Disabled	DAC 2 Enabled	Real → VOUT_P → VOUT_N VOP 32.00 mA		FIFO Over/Underflow FIFO Overflow FIFO Underflow FIFO Marginal Overflow FIFO Marginal Underflow		Overflow in Inverse Syr Over/Underflow in Mix Over/Underflow in Mix Scaler overflow IMR overflow	nc Filter ker (half I) ker (half Q)
										Determeth laters at		Overflex in January Co.	- Films (De d Nhus)
		DAC Tile 0					PLL	7864.320 MHz	V Over	flow in DAC Interpolation	Stage 0 I Stage 1 I	overnow in inverse sy	ie mei (end raya)
	FIFO Data	Interpolation	Mixer C Bypass	rossbar	QMC Gain/Phase	Inverse Sinc	DAC 1	Real	Over Over Over Over Over Over	flow in DAC Interpolation flow in DAC Interpolation flow in DAC Interpolation flow in DAC Interpolation	Stage 2 I State 0 Q State 1 Q State 2 Q		
	Real	1x			Disabled	Disabled	Enabled	VOP 32.00 mA	V Over	flow in DAC Interpolation flow in DAC Interpolation	Stage 3 I Stage 3 Q		
	FIFO Data	Interpolation	Mixer C Bypass	rossbar	QMC Gain/Phase	Inverse Sinc	DAC 0	VOUT_P	V Over	flow in QMC Offset			
	Real	1x			Disabled	Disabled	Enabled	VOP 32.00 mA	Select All	Unselect All	ට Refresh	Clear	Apply
Board: ZC	U216 Packa	ge: G1517 Device: ZU49	DRES Protocol: Ethen	net Design	: 2020.2		Communication	OK					

Figure 30: Interrupts Status Page

The check box at the beginning of each row enables or disables (masks) the corresponding interrupts status. Click the **Apply** button to apply the selected interrupts status.

The **Refresh** button reads back the current status and the green light shows which corresponding interrupt bit is set.

The **Clear** button attempts to clear all interrupt bits and read back the status.

RECOMMENDED: It is good practice to check the interrupts status and solve the root cause if an interrupt bit has been set before generating or receiving data. For example, the FIFO or datapath overflow can corrupt data and provide an incorrect result.

FIFO Data

Click **FIFO Data** in any RF-ADC or RF-DAC channel to see the clock relationship of the converter tile, PL interface, and related MMCM configuration.





Figure 31: **FIFO Data**

Note: The clock scheme is tile based, which means all converter channels in one tile share the same clock scheme.

Note: In an MTS enabled bitstream, all RF-ADC tiles share one MMCM module in ADC Tile-0. All RF-DAC tiles share one MMCM module in DAC Tile-0. Values in the FIFO Data page of other tiles are invalid.

The following values are configurable in the FIFO Data page.

- **FabCLKDiv:** In a non-MTS bitstream, the converter sampling clock (Fs, also called T1) is divided by 8 and then divided by FabCLKDiv. The output goes to the MMCM module as an input reference.
- **M**, **D**, and **ClkDiv:** In the MMCM module, the MMCM generates a read or write clock for the FIFO on the PL side, which is shown as F(PL) in the FIFO Data page. The following formula can be used to calculate the PL FIFO clock.

F(PL)=Fin*M/D/ClkDiv

Note: The VCO in the MMCM has a limited frequency range requirement. See Zynq UltraScale+ RFSoC Data Sheet: DC and AC Switching Characteristics (DS926) for the VCO frequency range for different devices.

The proper values for the FIFO related clock configurations are set automatically based on user configuration in the clock distribution page and converter configurations. Generally, these values do not need to be changed.



Chapter 3

RF Analyzer

Overview

The RF Analyzer provides an easy and fast way to evaluate the performance of RF-ADCs and RF-DACs in the Zynq[®] UltraScale+[™] RFSoC. The bitstream is independent of the evaluation board and external devices, thus the following board related configurations are not available in the GUI.

- Power settings
- External clock settings
- Programmable logic (PL) settings

Working with the RF Analyzer

The RF Analyzer requires that either the 2020.1 HW server (or later version) or the Vivado[®] Design Suite (2020.1 or later version) is installed on the host. Ensure that the external clocks are stable before downloading the bitstream based on the actual hardware design. The corresponding converter tiles might show an error if there are no valid clocks available when the converter IP starts up.

Note: When using the RF Analyzer with Xilinx[®] evaluation boards, the System Controller User Interface (SCUI) tool can be used to configure the onboard clocks. See the *ZCU111 System Controller – GUI Tutorial* (XTP517) for details.

Installing the RF Analyzer

- 1. Double-click Setup_RF_Analyzer_<version>.exe (you might have to right-click and select Run as Administrator).
- 2. Select the folder where the RF Analyzer is to be installed and then follow the instructions on the following screens.



- 11 - 1				
👸 Setup - RF Analyzer	_			\times
Select Destination Location Where should RF Analyzer be installed?			Q	
Setup will install RF Analyzer into the following folder.				
To continue, click Next. If you would like to select a different folder,	click	Brow	se.	
C:\Xilinx\RF_Analyzer		Brov	vse	
At least 145.7 MB of free disk space is required.				
Nex	t >		Can	icel

Setting the Vivado Path

When the RF Analyzer starts up for the first time, it looks for the Vivado Design Suite. If there is no Vivado Design Suite or HW server directory specified in the RF_Analyzer.ini, a window asking for the path of Vivado Design Suite pops open.

1. In the Vivado Directory Selection, browse to the folder where the Vivado Design Suite or HW server is installed.

8	Vivado Directory Selection	х
	Vivado Path	
	C:\Xilinx\Vivado\2020.1	
	Cancel OK	

2. Click OK. This directory is recorded in the RF_Analyzer.ini for further applications.

Selecting the Hardware Target and Bitstream

If you have set up the cable for JTAG access, you can use the RF Analyzer start screen to configure and work with the hardware target. This is the same communication method that is used by the Vivado tools.



Analyzer dit Settings Wind	dow Help	
re Target		E XILINX.
	Connect to: Local Server (target is on local machine)	
	Hardware JTAG Frequency	
	Type/Serial Number Status Sta	
	Bitstream Path	
	Bittream	
	Devices Devices ITAC HART Devices	

Figure 32: RF Analyzer Start Screen

- 1. In the Connect to: dialog box, select the connection type as Local or Remote. Click **Connect**.
- 2. In the Hardware dialog box, you can see the automatically detected cables and JTAG chain.
- 3. In the Bitstream Path dialog box select the bitstream. A pre-built bitstream for each supported part is available in the install folder under \Protocol\RF_Analyzer \bitstreams\. These bitstreams provide the maximum RF configuration flexibility. You can also use your own bitstream by customizing and generating the RF DC IP in the Vivado[®] Design Suite (see the Zynq UltraScale+ RFSoC RF Data Converter LogiCORE IP Product Guide (PG269) for information on generating the RF Data Converter IP core).



Hardware Target	
	Connect to: Local Server (target is on local machine)
	Hardware JTAG Frequency Type/Serial Number Status 15MHz
	HW-Z1-ZCU104/1280976b020A Freq: 15MHz xczu28dr Configured MicroBlaze ≠0 RF Analyzer
	< >
	Bitstream Path
	C:\Case\RF_Analyzer\work_191\GUI\RF_Analyzer\Protocol\RFAnalyzer\ bitstreams\RF_Analyzer_28DR_20mA.bit Download Bitstream Select Target >

After the bitstream download is complete, select MicroBlaze[™] as the target. The RF Analyzer sets up a connection with the Zynq[®] UltraScale+[™] RFSoC, and refreshes the status of the GUI. The following overview page shows up if there are no errors. Device information and the green communication OK bulb appears on the status bar at the bottom of the overview page. The active RF-ADC or RF-DAC tiles might be different based on your actual hardware configuration.





E RF Analyzer	RF Analyzer 1.9)		,—, 🗆 🕽
File Edit Setti	ngs Window Help		
Overview			E XILINX.
	Programmable Logic (PL)		
	RF Data Converter Subsystem : DAC	MTS	
	DAC DAC DAC DAC Tile 2 DAC DAC Tile 2 DAC Tile 2 DAC DAC Tile 2 DAC DAC Tile 2 DAC D	C DAC 3 3 DAC 3 1 DAC 2 PL DAC 1 DAC 0	
	Clock Distribution		
	RF Data Converter Subsystem : ADC	MTS	
	ADC ADC: ADC:	C	
l	Device: ZU40DR Protocol: JTAG-UART Design: rfdc.com v1 9	Communication OK	

Configuring the Sample Clock

The RF Analyzer acquires the absolute values of tile input clocks and sampling clocks from the IP configuration. Consequently, if the board clocks are different to the initial IP configuration, it is important to configure the sampling clocks before other operations.

w	E XILINX.
Programmable Logic (PL)	
RF Data Converter Subsystem : DAC MTS	
DAC DAC3 DAC4C3 DAC3 DAC4 DAC4 <t< th=""><th></th></t<>	
Clock Distribution	
RF Data Converter Subsystem : ADC MTS	
ADC ADC <td></td>	

1. Click Clock Distribution.





2. Select the PLL and configure the clocks based on the board setup.

See Zynq UltraScale+ RFSoC RF Data Converter LogiCORE IP Product Guide (PG269) for information on the permitted clocking configurations for your RFSoC device.

RF Analyzer Tool Menu Options

File Menu Options

- File → Load/Save configuration: Configuration covers all the displayed settings of the Zynq[®] UltraScale+[™] RFSoC such as, real or I/Q mode, mixer settings, and enable or bypass internal PLL. All these settings can be saved and restored. This feature enables quick configuration as well as configurations that can be shared with others. Configuration files are located in \Config\ directory, with the file extension of .cfg.
- File → Load/Save preferences: Preferences are the user-defined settings of the GUI. It includes tabs used for data generation, data capture, and user options in the GUI that are not linked to the device under test (DUT) configuration such as, mapping in the MultiView mode, number of samples, and tone frequency. You can save the preferred settings of GUI or restore any of them. Preferences files are located in \Config\ directory, with the file extension of .prf.
- File \rightarrow Hardware target: RF Analyzer only. Opens the bitstream download screen.



- File → Export ADC Data: This command exports the RF-ADC data captured of all the opened RF-ADC channels with LVM or TDMS file format (chosen in Settings → Data File Format). The default directory is \Data\ADC\.
- File \rightarrow Exit: Exit the software.

Edit Menu Options

• Edit: Standard Windows edit menu.

Settings Menu Options

• Settings → Communication: Displays the current communication interface. JTAG-UART is used for the RF Analyzer.

Interface Selection		
	JTAG-UART	\sim
Inter	face Configuration	
Host	localhost	
Port	9902	
Frequency	12 MHz 🗸	
	Cancel	OK

Figure 33: Communication Interface

 Settings → Dynamic Performances: Some RF-ADC metrics are based on the frequency range. On the RF-ADC FFT page, there is a marked-out calculation table, the SNR, ENOB, SFDRxH23, and FspurxH23 are calculated based on the Band of Interest set here. In loop mode, some metrics are calculated over a number of measurements that can be set under Averaging.



		E XILINX.
DAC DAC DAC Tile 0 DAC 2229 DAC 229 DAC 229 PL DAC 1 DAC 2 DAC 2 PL DAC 1 DAC 1 DAC 2	E Dynamic Performances Calculation X Band of Interest Stati Offset 100.000 (a) (MHz) Stop Offset 100.000 (a) (MHz) Averaging Nob Measurements 100 (a) (b) (b)	
Clock Distribution	Cancel OK	
RF Data Converter Subsystem : ADC		
ADC ADC3 Tile 0 ADC3 224 ADC2 PL ADC1 Matter ADC1 ADC00 ADC1	ADC Tile 3 ADC 3 227 ADC 2 File ADC 1 ADC 0	

Figure 34: Band of Interest

• Settings → Data File Format: Indicate your preferred file format between the .lvm and .tdms formats. For the RF-ADC output, you can individually select whether Data or Metrics is exported.



Figure 35: Data File Format

• Settings → Data Folders: Select your preferred folders for the test vector of RF-DAC, saved data from RF-ADC, and onboard clocking frequency configuration files. By default, these are located in \Data\, with ADC, DAC, and Clocking as the respective folder names.



Window Menu Options

Window → MultiView: The MultiView option makes it possible to view several of the RF-ADC or RF-DAC FFT diagrams on a single page with customized channels. Click Generate/Acquire All to update all the windows.



Figure 36: **MultiView RF-ADC FFT**

To display all the RF-ADC channel signals in the time domain, select the **ADC Time Domain** option.







Figure 37: MultiView RF-ADC Time Domain

• Window → Commands log: This opens the commands log window where the history for all the commands can be seen, the API can be run, and feedback can be viewed. If an error occurs with the GUI, it appears on the command log. The command log window can also be used to create a dump file which lists out all the previously used commands. This can be useful in debugging if an error occurs with a sent command.

🗜 RF Analyzer (RF A	Analyzer 1.91)							– 🗆 X
ile Edit Settings	Window Help							
Overview	Multiview A	DC FFT 1	DAC Tile 0	DAC Tile 0 - DAC 0	ADC Tile 0	Multiview ADC Time	Commands Log	
							-	
Time	Fue a (ma)		0					A
16-21-14	Exec (ms)	1 Catl a call fo	Query		Settle call Asm Sample			Answer
15,21,14	20	2 SetLocalMe	mSample 0.0.2.9102		SetLocalMemSample			
15:21:14	20	1 SetLocalMa	mSample 0.0.3.8192		SetLocalMemSample			
15:21:14	15	2 SetLocalMa	mSample 0.1.0.8192		SetLocalMemSample			
15:21:14	20	1 SetLocalMa	mSample 0 1 1 8192		SetLocalMemSample			
15:21:15	202	2 SetLocalMe	mSample 0 1 2 8192		SetLocalMemSample			
15:21:15	15	1 SetLocalMe	mSample 0 1 3 8192		SetLocalMemSample			
15:21:15	15	4 SetLocalMe	mSample 0.2.0.8192		SetLocalMemSample			
15:21:15	20	3 SetLocalMe	mSample 0 2 1 8192		SetLocalMemSample			
15:21:15	152	2 SetLocalMe	mSample 0 2 2 8192		SetLocalMemSample			
15:21:15	20	3 SetLocalMe	mSample 0 2 3 8192		SetLocalMemSample			
15:21:16	204	4 SetLocalMe	mSample 0 3 0 8192		SetLocalMemSample			
15:21:16	15	3 SetLocalMe	mSample 0 3 1 8192		SetLocalMemSample			
15:21:16	201	1 SetLocalMe	mSample 0 3 2 8192		SetLocalMemSample			
15:21:16	204	4 SetLocalMe	mSample 0 3 3 8192		SetLocalMemSample			
15:21:16	150	0 LocalMem	nfo 0		LocalMemInfo 0 E00000	0 4 16 16384 12 15 0		
15:21:16	15	3 LocalMem	Frigger 0 4 8192 0xFFFF		LocalMemTrigger			
15:21:17	(0 Acquisition			Acquisition 8192 0xE0008	1000		
15:21:17	(0 Acquisition			Acquisition 8192 0xE0010	000		
15:21:17	(0 Acquisition			Acquisition 8192 0xE0018	1000		
15:21:17	(0 Acquisition			Acquisition 8192 0xE0020	000		
15:21:18	(0 Acquisition			Acquisition 8192 0xE0028	000		
15:21:18	(0 Acquisition			Acquisition 8192 0xE0030	000		
15:21:18	(0 Acquisition			Acquisition 8192 0xE0038	000		
15:21:19	(0 Acquisition			Acquisition 8192 0xE0040	000		
15:21:19	(0 Acquisition			Acquisition 8192 0xE0048	000		
15:21:20	(0 Acquisition			Acquisition 8192 0xE0050	000		
15:21:20	(0 Acquisition			Acquisition 8192 0xE0058	000		
15:21:20	(0 Acquisition			Acquisition 8192 0xE0060	000		
15:21:21	(0 Acquisition			Acquisition 8192 0xE0068	000		
15:21:21	(0 Acquisition			Acquisition 8192 0xE0070	000		
15:21:21	(0 Acquisition			Acquisition 8192 0xE0078	000		
15:21:22	(0 Acquisition			Acquisition 8192 0xE0080	000		
15:21:22	367	7 GetLog			GetLog			
								×
Dump				Comman				Send
bump				commun				3010
		Device: 7140	ORES Protocol: ITAG-UA	RT Design: rfdc.com	v1.9	Communication OK		
		Device: 2049	THORE THORE THO THE	in pesigle nuc_com		communication OK		

Figure 38: Command Window



• Window → Merge all windows: Opened tabs for DACs or ADCs can be moved to separate windows with a left-click and drag on the tab area as shown in the following figure. This command merges all the separate windows into one.

Figure 39: Create Separate Windows



• Window → Attach: Opened tabs can be moved to separate windows. This command merges back selected separate windows.

Help Menu Options

• Help → About: Provides general information about the RF Data Converter evaluation tool. Use this option to check the version, which is used when building the .lvm file.

RF Analyzer Tool Tabs

The Overview page is the home page of the RF Data Converter analyzer tool GUI. It displays the top framework of all the converters grouped by tile. This page is displayed upon start-up and cannot be closed.

Overview

The overview page is similar to the RF Evaluation Tool but the memory type is not selectable because DDR (DRAM) storage is not supported.



Figure 40:	Overview	Page
------------	-----------------	------

RF Analyzer (RF Analyzer 1.9)	- 0
le Edit Settings Window Help	
vernerer Cread/buthbuthen	E XILINX.
Programmable Logic (PL) RF Data Converter Subwritem IDAC Mrs	Tile Status Available
DAC DAC DAC DAC Tite 0 MAC Tite 1 BAC 2 BAC 2 Za0 MAC Tite 2 BAC 2 Tite 3 BAC 2 NL NL NL BAC 2 BAC 3 BAC 2 BAC 3 BAC 3 </td <td>Power-on State Machine (Convert State) The Faced IS Clock Detected</td>	Power-on State Machine (Convert State) The Faced IS Clock Detected
Clock Distribution	
RF Data Converter Subsystem : ADC MTS	
ADC #6C3 Tite 0 #6C3 224 #6C1 225 #6C2 RL #6C1 Mater #6C1 #6C1 #6C3 Mater #6C1 #6C5 #6C5 #6C6 #6C5 #6C5 #6C5 #6C6 #6C5	
	🖸 Refresh Apply 🔆 Reset 🔳 Shutdown Tile Settings
Device: ZU49DR Protocol: JTAG-UART Design: rfdc_com_v1_9 Communication OK	

RF-ADC/RF-DAC Tile

In the overview tab, selecting any of the RF-ADC or RF-DAC tile opens the individual tile page as illustrated in the following figure. In this tab, you can reset, shut down, start up a tile, and also view the current tile status by clicking **Refresh**. When a tile is in operation, selecting **Tile settings** opens up the configuration tab for it. Refer to the *Zynq UltraScale+ RFSoC RF Data Converter LogiCORE IP Product Guide* (PG269) for more information on the commands and power up state machine status.







Tile PLL Settings

Click on PLL in the tab for a DAC or ADC to see a diagram that illustrates the PLL setup for that tile.



Figure 42: Tile PLL Settings

Converter Settings

In each RF-ADC/RF-DAC tile, the available converter channels and associated internal function blocks are cascaded in the block diagram, and the text shows the current settings. Click any function block to open the config page in the right panel. FIFO and Crossbar have their own separate pages.







RF-ADC Settings

 Calibration Mode: Selects between different calibration optimization schemes depending on the features of the input signals. Mode 1 is optimal for input frequencies F_{samp}/2(Nyquist) +/-10%. Otherwise, use Mode 2.



Figure 44: Calibration Mode

- **Nyquist Zone:** Choose the Nyquist zone in which the input signal is located. This is related to interleaving calibration and must be indicated correctly. Zone 1 is for odd numbered zones and Zone 2 is for even numbered zones.
- Threshold Detection: Use this to set the embedded threshold detection parameter.

Send Feedback



• **Decimation Settings:** Use this to select the decimation factor. Xilinx recommends using the same decimation factor for all data converters in the tile to avoid potential timing issues at the interface.

Note: Do not select Off or you will not receive any data.

• **Calibration Frozen:** Use this to freeze the interleaving calibration for each channel. The green light indicates a frozen status. The freeze function freezes or unfreezes the interleaving calibrations. The disable pin function can disable the calibration freeze real-time port control.

The following functions are for Gen 3 only.

- Attenuation: Attenuation value of on-chip DSA in dB for each RF-ADC channel. The disable pin can disable the DSA pin control.
- Power Management: Use to power down or power up a single channel within a tile.

RF-DAC Settings

- **Decoder Mode:** Choose which performance to optimize: noise floor or linearity. Noise floor optimization must be selected for communication applications.
- **Nyquist Zone:** Choose which Nyquist zone the signal will be located in: Normal Mode for Nyquist zone one and Mix Mode for Nyquist zone two. See this link for more information.
- Interpolation Settings: Choose your interpolation factor.

Note: If you select Off, some digital blocks will be powered down and the outputs will not be active.

• **Inverse Sinc Settings:** Enabling Inverse Sinc compensates sinc roll-off at high frequencies. This function is only effective when the signal is located in Nyquist zone one.

The following functions are for Gen 3 only.

- **DataPath:** The drop-down box used to choose datapath modes. The four available modes are Full Nyquist DUC, IMR low pass, IMR high pass, and DUC bypass.
- **Current:** The VOP current value. This value is also displayed on the diagram of each channel.
- **Power Management:** Use to power down or power up a single channel within a tile.

Settings in RF-ADC and RF-DAC

- **Mixer Settings:** Xilinx recommends setting the Crossbar page first, and then set other parameters of the mixer and NCO because the mixer is bypassed in the real-to-real mode.
- QMC Settings: QMC module contains gain, phase, and DC-offset adjusting. These are used to compensate unmatched I and Q signal path when converters interface to external modulators or demodulators. DC offset takes effect with DC coupling only. Phase offset takes effect with complex mode only. Gain takes effect in all modes.





• **FIFO:** Show the FIFO clock rates and number of words on PL and converter side for information only.

Crossbar

Click the **Crossbar** button at the bottom of the converter settings page, or, alternatively, the **Crossbar** box in the left panel to display the crossbar page. This page determines the real or complex mode of the mixer and multi-bands operating mode. Complex mode activates a pair of channels to support both in-phase(I) and quadrature(Q) signal. Because of the complex mixer (and NCO) architecture, the real-to-complex (R2C) or complex-to-complex (C2C) mode is allowed, but complex-to-real (C2R) mode is not allowed. This means that there is no C2R mode available for RF-ADC and no R2C mode available for RF-DAC. Correct operating modes are ensured by this tool. In complex mode, even channels are always used for I signals and odd channels are used for Q signals.



Figure 45: **Crossbar**



Multi-Bands

Multiple bands enable one RF-DAC or RF-ADC analog channel and share multiple DUC or DDC channels to transmit or receive the multi-band carrier signals. For RF-DAC, multiple baseband signals can be up-converted in separate DUC chains and then combined at the crossbar before being sent to the analog RF-DAC block.

In RF-ADC, the multi-band/carrier inputs from one RF-ADC are split into multiple DDC paths for down-conversion. The carriers from different bands are separated and located at low frequencies (in general at zero). In the multi-bands operation, a converter is enabled on channel 0 (dual bands at channel 0 and 1) or channel 2 (dual bands at channel 2 and 3). Multi-bands operations support both real and complex output. All these configurations can be enabled at the crossbar page. The following figure illustrates the dual bands configuration of C2C and C2R.



Figure 46: Multi-Bands

FFT Page

Click **Acquisition** in the ADC settings page, or **Generation** in the DAC settings page, to open the FFT page. In the RF-DAC FFT page, the single tone and dual tone generator is embedded in the software. To generate a complex modulated signal, load a test vector file. There are variations of sub-menus in this page, including signal characteristics, customizing FFT plot, windowing function, test vector input, and output. When decimation or interpolation is enabled in the RF-



ADC or RF-DAC data path, with a value more than 1 (bypass), Eff.Fs and Fs show different values in this table. Fs indicates the sampling frequency of observed RF-ADC or RF-DAC, Eff.Fs indicates the sampling frequency of original data stream (base band) after decimation or before interpolation. The X-axis (frequency) of the FFT plot reflects back the Eff.Fs. The following figure shows the RF-ADC FFT page.





The following figure shows the Zoom Tools on the FFT page. Use the default Zoom Tools or edit the axis range to directly configure the start and/or end values for best plot observation.





Figure 48: FFT Zoom Tool



Multi-Tile Synchronization

The multi-tile synchronization (MTS) feature enables multiple converter channels working with an aligned and deterministic latency across tiles and chips. MTS is only supported in the RF Analyzer with a custom bitstream.

Clock Distribution (Gen 3)

The Zynq UltraScale+ RFSoC Gen 3 supports on-chip clock distribution. For more information, see Zynq UltraScale+ RFSoC RF Data Converter LogiCORE IP Product Guide (PG269).

Click the **Clock Distribution** button in the overview page to display the page shown in the following figure.





Figure 49: Clock Distribution

Note: The settings on this page should comply with the limitations of the on-chip clock distribution system and PLL.

Each tile has four input fields and a check box for an in-tile PLL, as described here.

- Sample Clock (MHz): Select the desired sampling rate of converters, which can be generated by the in-tile PLL or a forwarded sampling clock from the source tile.
- PLL Checkbox: Enable or disable the PLL in this tile.
- **Reference Clock (MHz):** Enter the reference or a sampling clock, can be from an external input or a forwarded clock from the source tile.

Note: This frequency can be a reference for the in-tile PLL or the frequency of the sampling clock if it is used directly.

- **Output Divider (M):** Shows the output divider of the on-chip PLL (incorrect for PLL disabled tile). This field is for reference only and not editable.
- **Source Tile:** Use the drop-down list to select which tile the clock (reference) comes from. Select the tile itself for the external clock input to this tile, or the source tile for a forwarded clock (reference or sampling clock). Select the tile itself for a source tile.
- **Distribute Clock:** Select options to distribute the clock (acting as source tile) and which clock is distributed:
 - 1. None: select to not distribute the clock.



- 2. Input clock: select to distribute the input clock from an external input. This clock can be a low-frequency reference clock or a high-frequency sampling clock.
- 3. PLL output clock: select to distribute the clock generated by the in-tile PLL.

An example configuration is shown in the following figure.



Figure 50: Example Clock Distribution Configuration

In this example, two external input clocks (both at 245.76 MHz) are fed to the ADC_Tile_224 and DAC_Tile_228, respectively. All desired RF-ADC clocks are 2457.6 MHz and desired RF-DAC clocks are 4915.2 MHz.

For the RF-ADC group, Tile_224 distributes its *PLL output clock* to other RF-ADC tiles. For the RF-DAC group, Tile_228 distributes its input reference to all other RF-DAC tiles.

All RF-DAC tiles enable their PLLs to generate the desired sampling clock at 4915.2 MHz.

When the Apply button is clicked, the GUI updates these configurations to the chip, restarts all tiles, reads back status, and updates the GUI. This might take a while and a percentage bar shows the progress.

The following figure shows the tile status based on the clock distribution configurations in this example.



alyzer (RF Analyzer 1.91) Settings Window Help	
	E XILINX.
	DAC Tile 0
Programmable Logic (PL)	Tile Status
RF Data Converter Subsystem : DAC MTS	Available Power-on State Machine (Current State) Tile Ready
DAC Tile 0 DAC 3 Tile 1 DAC 3 Tile 2 DAC 3 DAC 4 23 DAC 3 DAC 3 DAC 4 23 DAC 3 DAC 4 DAC 4 23 DAC 4 DAC 4 DAC 4 23 DAC 4 DAC 4 DAC 4 23 DAC 4 DAC 4	Powered Clock Detected
Clock Distribution	
RF Data Converter Subsystem : ADC MTS	
ADC ADC <td></td>	
	Apply 🕸 Keset 🔳 Snutdown Tile Settin

Figure 51: Tile Status Based on Clock Distribution

For RF-ADC, only Tile 0 (Tile_224) PLL is enabled, and PLLs in other tiles are disabled. The green channel status shows they are in operation status because these tiles are forwarded the sampling clock from Tile 0. For RF-DAC, all PLLs are enabled because Tile 0 (Tile_228) forwarded its reference to other tiles. The status of RF-ADCs and RF-DACs reflect the settings in the Clock Distribution page in this example. The PLL status can also be checked in the PLL page for each tile. For Gen 3, the PLL page shows the status only and all the clock configurations rely on this Clock Distribution page, which is different from the PLL page in Gen 1 and Gen 2.

Interrupts

Click the **Interrupts** button to display the page shown in the following figure (this example is for RF-DAC).



c occurrys	window meip			2			
r	ADC Tile 0	ClockDistribution	DAC Tile 0	L			
FIFO E	Data Interpolation	Mixer Cro	ussbar QMC Gain/Phase	Inverse Sinc D4	Real	DAC Tile	0 - DAC 0 - Interrupts
Rea	al 1x	Bypass 	Disabled	Disabled	oled VOUT_N VOP 32.00 mA	Return	nterrunts Status
FIFO D	Data Interpolation	Mixer Cro Bypass 	ussbar QMC Gain/Phase Disabled	Inverse Sinc DA Disabled Enal	KC 2 VOUT_P VOUT_N VOP		Overflow in Inverse Sync Filter Over/Underflow in Mixer (half I) Over/Underflow in Mixer (half Q) Over/Underflow Scaler overflow Over/Underflow
					PLI 7954 220 MU-	Overflow in DAC Interrupt	2001
	DACINE				1004520 1112	Qverflow in DAC Interpolation St	ae 1
					P1	Overflow in DAC Internolation St.	ae 21
FIFO D	Data Interpolation	Mixer Cros	ssbar QMC Gain/Phase	Inverse Sinc DA	VOUT_P	Overflow in DAC Interpolation St. Overflow in DAC Interpolation St. Overflow in DAC Interpolation St.	te 0 Q te 1 Q
Rea	al 1x	Bypass 	Disabled	Disabled	vout_N vop 32.00 mA	Overflow in DAC Interpolation St. Overflow in DAC Interpolation St.	te 2 Q ge 3 I
						Overflow in DAC Interpolation St.	ge 3 Q
FIFO D	Data Interpolation	Mixer Cros	ssbar QMC	Inverse	Real	Image: Construction of the section of the s	
Day	al 1v	Bypass	Disabled	Disabled Enal			

Figure 52: Interrupts Status Page

The check box at the beginning of each row enables or disables (masks) the corresponding interrupts status. Click the **Apply** button to apply the selected interrupts status.

The **Refresh** button reads back the current status and the green light shows which corresponding interrupt bit is set.

The **Clear** button attempts to clear all interrupt bits and read back the status.

RECOMMENDED: It is good practice to check the interrupts status and solve the root cause if an interrupt bit has been set before generating or receiving data. For example, the FIFO or datapath overflow can corrupt data and provide an incorrect result.

FIFO Data

Click **FIFO Data** in any RF-ADC or RF-DAC channel to see the clock relationship of the converter tile, PL interface, and related MMCM configuration.





Figure 53: **FIFO Data**

Note: The clock scheme is tile based, which means all converter channels in one tile share the same clock scheme.

Note: In an MTS enabled bitstream, all RF-ADC tiles share one MMCM module in ADC Tile-0. All RF-DAC tiles share one MMCM module in DAC Tile-0. Values in the FIFO Data page of other tiles are invalid.

The following values are configurable in the FIFO Data page.

- **FabCLKDiv:** In a non-MTS bitstream, the converter sampling clock (Fs, also called T1) is divided by 8 and then divided by FabCLKDiv. The output goes to the MMCM module as an input reference.
- **M**, **D**, and **ClkDiv:** In the MMCM module, the MMCM generates a read or write clock for the FIFO on the PL side, which is shown as F(PL) in the FIFO Data page. The following formula can be used to calculate the PL FIFO clock.

F(PL)=Fin*M/D/ClkDiv

Note: The VCO in the MMCM has a limited frequency range requirement. See Zynq UltraScale+ RFSoC Data Sheet: DC and AC Switching Characteristics (DS926) for the VCO frequency range for different devices.

The proper values for the FIFO related clock configurations are set automatically based on user configuration in the clock distribution page and converter configurations. Generally, these values do not need to be changed.



Appendix A

LVM and TDMS File Format

LabVIEW Measurement (.lvm) is a text based file format. TDM Streaming (.tdms) is a stream based file format. For testing the Zynq[®] UltraScale+^m RFSoC with this evaluation software, Xilinx recommends the LVM file format for small pattern. For large pattern, such as a standard 4G/5G pattern, the TDMS file is recommended.

LVM File Format

The LabVIEW Measurement (.lvm) file is a native, text based file format of the LabVIEW software. This file format is used in this evaluation tool GUI for data input and output. The .lvm file contains a file header and column based data. Some items in the file header are required. An example .lvm file with the headers required by this evaluation tool GUI is shown in the following figure.



LabVIEW Measurement			
Writer_Version	2		
Reader_Version	2		
Separator	Tab		
Decimal_Separator			
Multi_Headings	No		
X_Columns	No		
Time_Pref	Relative		
Operator	xlnx		
Date	4/25/2018		
Time	36:46.7		
End_of_Header			
Start_Special			
Version	V1.0.0 Beta2		Help about
Fs(MHz)	2000		
End_Special			
Channels	2		I/Q data channel
Samples	4	4	Rows of data below
Date	4/25/2018	4/25/2018	
Time	36:46.7	36:46.7	
X_Dimension	Time	Time	
хо	0	0	
Delta_X	5.00E-10	5.00E-10	
End_of_Header			
X_Value	I_vector	Q_vector	Comment
	9298	-6573	
	11280	-6	
	9133	6436	
	3720	10422	

Figure 54: **LVM File Format**

For more information about the .lvm file format, see LabVIEW Measurement Files.



TDMS File Format

The TDMS file format targets the management and exchange of large and complex data sets. Unlike the text-based lvm format, the TDMS file is stream-based and thus, more difficult to generate and difficult to view in a simple text editor. National Instruments (NI) provides different tools such as a function library in MATLAB[®] and C/C++ that work with the TDMS file. NI also provides Excel add-ins for the TDMS file. The following figure shows a TDMS file open in Excel using the TDM Excel add-in.

C	D	E	F	G	H		J	K	L
Root Name	Title	Author	Date/Time	Groups	Description	datestring	Test_Module	Test_Name	Test_Operator
TR_M17_QT_42-1	Example data set	National Instruments	2017/02/08 04:56:53.000 PM	2		08.02.2017	17	M18-B4	Paul
1-		-							
Group	Channels	Description	Test_NoOfSensors	Test_Status					
QT_42-1_Lower	10	Dower boiler section	10	Fail					
QT_42-1_Upper	10	Upper boiler section	10	Pass					
OT 42-1 Lower									
Channel	Datatype	Unit	Length	Minimum	Maximum	Description	displaytype	Limit_High	Limit_Low
Temp A	DT DOUBLE	°C	250	20.93752875	27.5582237	Input: [1]/Temp A (1)	Numeric	50	20
Temp B	DT DOUBLE	°C	250	21.33752875	33.24760449	Input: [1]/Temp B (2)	Numeric	50	20
Temp C	DT DOUBLE	°C	250	21.13752875	28.33780719	Input: [1]/Temp C (3)	Numeric	50	20
Temp D	DT DOUBLE	°C	250	20.93752875	27.14689701	Input: [1]/Temp D (4)	Numeric	50	20
Temp E	DT DOUBLE	°C	250	21.33752875	28.61515167	Input: [1]/Temp E (5)	Numeric	50	20
Temp F	DT DOUBLE	°C	250	13.8902974	35.53946511	Input: [1]/Temp F (6)	Numeric	50	20
Temp G	DT DOUBLE	°C	250	21.01052651	45.09115071	Input: [1]/Temp G (7)	Numeric	50	20
Temp H	DT DOUBLE	°C	250	22.05368635	73.92498273	Input: [1]/Temp H (8)	Numeric	50	20
Temp I	DT DOUBLE	°C	250	21.03752875	27.39962727	Input: [1]/Temp (9)	Numeric	50	20
Temp J	DT DOUBLE	°C	250	21.53101107	74.87458339	Input: [1]/Temp J (10)	Numeric	50	20
Implicit	Start	Interval	Length						
Time	C) 2	250						
QT_42-1_Upper									
Channel	Datatype	Unit	Length	Minimum	Maximum	Description	displaytype	Limit_High	Limit_Low
Temp_A	DT_DOUBLE	°C	250	22.02478534	26.79858485	Input: [2]/Temp_A (11)	Numeric	50	20
Temp_B	DT_DOUBLE	°C	250	22.44478534	30.54130968	Input: [2]/Temp_B (12)	Numeric	50	20
Temp_C	DT_DOUBLE	°C	250	22.22478534	27.60212695	Input: [2]/Temp_C (13)	Numeric	50	20
Temp_D	DT_DOUBLE	°C	250	22.01478534	26.81686027	Input: [2]/Temp_D (14)	Numeric	50	20
Temp_E	DT_DOUBLE	°C	250	22.21977152	27.82849827	Input: [2]/Temp_E (15)	Numeric	50	20
Temp_F	DT_DOUBLE	°C	250	19.48462714	33.28898557	Input: [2]/Temp_F (16)	Numeric	50	20
Temp_G	DT_DOUBLE	°C	250	22.05831601	38.99275807	Input: [2]/Temp_G (17)	Numeric	50	20
Temp_H	DT_DOUBLE	°C	250	22.61210074	57.58257679	Input: [2]/Temp_H (18)	Numeric	50	20
Temp_I	DT_DOUBLE	°C	250	22.11478534	26.61582188	Input: [2]/Temp_I (19)	Numeric	50	20
Temp_J	DT_DOUBLE	°C	250	22.48210074	56.15038029	Input: [2]/Temp_J (20)	Numeric	50	20
Implicit	Start	Interval	Length						
Time	0	2	25	0					
	Root Name TR_M17_QT_42-1 Group QT_42-1_Lower QT_42-1_Lower QT_42-1_Upper Temp, A Temp, B Temp, C Temp, B Temp, B Temp, B Temp, I Temp, J Implicit Temp, B Temp, A Temp, G Temp, J Temp, B Temp, B Temp, C Temp, B Temp, C Temp, B Temp, C Temp, B Temp, C Temp, B Temp, F Temp, G Temp, C Temp, B Temp, C Temp, F Temp, G Temp, F Temp, G Temp, G Temp, I Temp, I Temp, J Implicit Temp, I	Root Name Title TR_M17_QT_42-1 Example data set Group Channels QT_42-1_Lower Channels QT_42-1_Loper 102 QT_42-1_Lower Datatype Channel Datatype Temp, A DT_DOUBLE Temp, B DT_DOUBLE Temp, C DT_DOUBLE Temp, F DT_DOUBLE Temp, G DT_DOUBLE Temp, G DT_DOUBLE Temp, G DT_DOUBLE Temp, G DT_DOUBLE Temp, J DT_DOUBLE Temp, J DT_DOUBLE Temp, A DT_DOUBLE Temp, G DT_DOUBLE Temp, J DT_DOUBLE Temp, A DT_DOUBLE Temp, A DT_DOUBLE Temp, B DT_DOUBLE Temp, B DT_DOUBLE Temp, C DT_DOUBLE Temp, C DT_DOUBLE Temp, B DT_DOUBLE Temp, C DT_DOUBLE Temp, C	Root Name Title Author TR_M17_QT_42-1 Example data set National Instruments Group Channels Description QT_42-1_Lower 10 Lower boiler section QT_42-1_Lower 10 Upper boiler section QT_42-1_Lower Unit Channel Datatype Unit Temp, A DT_DOUBLE °C Temp, B DT_DOUBLE °C Temp, C DT_DOUBLE °C Temp, F DT_DOUBLE °C Temp, F DT_DOUBLE °C Temp, F DT_DOUBLE °C Temp, G DT_DOUBLE °C Temp, J DT_DOUBLE °C Temp, J DT_DOUBLE °C Temp, J DT_DOUBLE °C Temp, J DT_DOUBLE °C Temp, B DT_DOUBLE °C Temp, A DT_DOUBLE °C Temp, B DT_DOUBLE °C Temp, B DT_DOUBLE °C <td< td=""><td>Root Name Title Author Date/Time TR_M17_QT_42-1 Example data set National Instruments 2017/02/08 04:56:53.000 PM Group Channels Description <i>Test_MoolSensors</i> QT_42-1_Lower 10 Lower boiler section 10 QT_42-1_Lower 10 Upper boiler section 10 QT_42-1_Lower 10 10 QT_42-1_Dover 10 Upper boiler section 10 QT_42-1_Dover 10 10 Temp, B DT_DOVBLE *C 250 Temp, F DT_DOVBLE *C 250 Temp, J DT_DOVBLE *C 250 Temp, J DT_DOVBLE *C 250 Temp, J DT_DOVBLE *C 250</td><td>Root Name Title Author Date/Time Groups Root Name Title Author Date/Time Groups Groups Channels Description 7est_Nat/2012/02/08 04:56:53.000 PM 2 Group Channels Description Test_Nat/2012/08 04:56:53.000 PM 2 Group Channels Description Test_Nat/2012/08 04:56:53.000 PM 2 QT_42-1 Lower 10 Uower boiler section 10 Pass QT_42-1 Lower Unit Length Minimum Temp, A DT_DOUBLE °C 250 21.3752875 Temp, B DT_DOUBLE °C 250 21.3752875 Temp, C DT_DOUBLE °C 250 21.3752875 Temp, F DT_DOUBLE °C 250 21.01052651 Temp, G DT_DOUBLE °C 250 21.01052651 Temp, J DT_DOUBLE °C 250 21.01052651 Temp, J DT_DOUBLE °C 250 21.03752875 <</td><td>Root Name Title Author Date/Time Groups Groups Description TR_M17_QT_42-1 Example data set National Instruments 201/702/08 04:56:53.000 PM 2 Description Group Channels Description <i>Test_NoO/Sensors Test_Status</i> Pail QT_42-1 Lower 10 Lower boiler section 10 Paas Maximum QT_42-1 Lower 10 Upper boiler section 10 Paas Maximum QT_42-1 Lower 10 Upter boiler section 10 Paas 27.5582237 QT_42-1 Lower C 250 20.3752875 27.589237 27.589237 Temp, B DT_DOUBLE *C 250 21.3752875 28.3780719 Temp, C DT_DOUBLE *C 250 21.3752875 27.14689701 Temp, F DT_DOUBLE *C 250 21.3752875 27.14689701 Temp, F DT_DOUBLE *C 250 21.03752875 27.14689701 Temp, G DT_DOUBLE <</td><td>Coot Name Title Author Date/Time Groups Description datestring Rot Name TR.M17_QT_42-1 Example data set National Instruments 2017/02/08 04:56:53.000 PM 2 Description 08.02.2017 Group Channels Description Test_MO/Sensors Test_Status 0 0 08.02.2017 Group Channels Description Test_MO/Sensors Test_Status 0 0 0 QT_42-1_Lower 10 Pass 0 Description Input: [1/Temp, A(1) Group D D_DOUBLE "C 250 21.33752875 27.5582237 Input: [1/Temp, A(1) Temp, B DT_DOUBLE "C 250 21.33752875 28.33780719 Input: [1/Temp, C(3) Temp, C DT_DOUBLE "C 250 21.33752875 28.35346511 Input: [1/Temp, E(3) Temp, F OT_DOUBLE "C 250 21.33752875 27.14689701 Input: [1/Temp, F(6) Temp, F OT_DOUBLE "C 250 21.00556855</td><td>Coot Name Title Author Date/Time Groups Description Test_Module RR_M17_QT_42-1 Example data set National Instruments 2017/02/08 04:56:53.000 PM 2 Description 08.02.2017 17 Group Channels Description Test_ModUle 7 7 7 7 Group Channels Description Test_ModUle 7 7 7 7 QT_42-1_Lower 10 Upper boiler section 10 Pass Description display/ppe QT_42-1_Lower 10 Pass 77.558275 32.34760449 input: [1/Temp_A(1) Numeric Temp, A DT_DOUBLE *C 250 21.33752875 28.33780719 input: [1/Temp_A(2) Numeric Temp, C DT_DOUBLE *C 250 21.33752875 28.35346511 input: [1/Temp_C (3) Numeric Temp, F OT_DOUBLE *C 250 21.39752875 27.35894511 input: [1/Temp_C (6) Numeric Temp, G DT_DOUBLE</td></td<> <td>C D E F Group Description datestring Test_Module R. Kn Group Channels Description 2017/02/08 04:56:53:000 PM 2 Description datestring datestring Test_Module Test</td>	Root Name Title Author Date/Time TR_M17_QT_42-1 Example data set National Instruments 2017/02/08 04:56:53.000 PM Group Channels Description <i>Test_MoolSensors</i> QT_42-1_Lower 10 Lower boiler section 10 QT_42-1_Lower 10 Upper boiler section 10 QT_42-1_Lower 10 10 QT_42-1_Dover 10 Upper boiler section 10 QT_42-1_Dover 10 10 Temp, B DT_DOVBLE *C 250 Temp, F DT_DOVBLE *C 250 Temp, J DT_DOVBLE *C 250 Temp, J DT_DOVBLE *C 250 Temp, J DT_DOVBLE *C 250	Root Name Title Author Date/Time Groups Root Name Title Author Date/Time Groups Groups Channels Description 7est_Nat/2012/02/08 04:56:53.000 PM 2 Group Channels Description Test_Nat/2012/08 04:56:53.000 PM 2 Group Channels Description Test_Nat/2012/08 04:56:53.000 PM 2 QT_42-1 Lower 10 Uower boiler section 10 Pass QT_42-1 Lower Unit Length Minimum Temp, A DT_DOUBLE °C 250 21.3752875 Temp, B DT_DOUBLE °C 250 21.3752875 Temp, C DT_DOUBLE °C 250 21.3752875 Temp, F DT_DOUBLE °C 250 21.01052651 Temp, G DT_DOUBLE °C 250 21.01052651 Temp, J DT_DOUBLE °C 250 21.01052651 Temp, J DT_DOUBLE °C 250 21.03752875 <	Root Name Title Author Date/Time Groups Groups Description TR_M17_QT_42-1 Example data set National Instruments 201/702/08 04:56:53.000 PM 2 Description Group Channels Description <i>Test_NoO/Sensors Test_Status</i> Pail QT_42-1 Lower 10 Lower boiler section 10 Paas Maximum QT_42-1 Lower 10 Upper boiler section 10 Paas Maximum QT_42-1 Lower 10 Upter boiler section 10 Paas 27.5582237 QT_42-1 Lower C 250 20.3752875 27.589237 27.589237 Temp, B DT_DOUBLE *C 250 21.3752875 28.3780719 Temp, C DT_DOUBLE *C 250 21.3752875 27.14689701 Temp, F DT_DOUBLE *C 250 21.3752875 27.14689701 Temp, F DT_DOUBLE *C 250 21.03752875 27.14689701 Temp, G DT_DOUBLE <	Coot Name Title Author Date/Time Groups Description datestring Rot Name TR.M17_QT_42-1 Example data set National Instruments 2017/02/08 04:56:53.000 PM 2 Description 08.02.2017 Group Channels Description Test_MO/Sensors Test_Status 0 0 08.02.2017 Group Channels Description Test_MO/Sensors Test_Status 0 0 0 QT_42-1_Lower 10 Pass 0 Description Input: [1/Temp, A(1) Group D D_DOUBLE "C 250 21.33752875 27.5582237 Input: [1/Temp, A(1) Temp, B DT_DOUBLE "C 250 21.33752875 28.33780719 Input: [1/Temp, C(3) Temp, C DT_DOUBLE "C 250 21.33752875 28.35346511 Input: [1/Temp, E(3) Temp, F OT_DOUBLE "C 250 21.33752875 27.14689701 Input: [1/Temp, F(6) Temp, F OT_DOUBLE "C 250 21.00556855	Coot Name Title Author Date/Time Groups Description Test_Module RR_M17_QT_42-1 Example data set National Instruments 2017/02/08 04:56:53.000 PM 2 Description 08.02.2017 17 Group Channels Description Test_ModUle 7 7 7 7 Group Channels Description Test_ModUle 7 7 7 7 QT_42-1_Lower 10 Upper boiler section 10 Pass Description display/ppe QT_42-1_Lower 10 Pass 77.558275 32.34760449 input: [1/Temp_A(1) Numeric Temp, A DT_DOUBLE *C 250 21.33752875 28.33780719 input: [1/Temp_A(2) Numeric Temp, C DT_DOUBLE *C 250 21.33752875 28.35346511 input: [1/Temp_C (3) Numeric Temp, F OT_DOUBLE *C 250 21.39752875 27.35894511 input: [1/Temp_C (6) Numeric Temp, G DT_DOUBLE	C D E F Group Description datestring Test_Module R. Kn Group Channels Description 2017/02/08 04:56:53:000 PM 2 Description datestring datestring Test_Module Test

Figure	55.	TDMS	File	Forma	ht
iguie	JJ.		I IIC	I UI IIIC	ιL

For additional details, see The NI TDMS File Format.



Appendix B

FFT Metrics

There are many converter metrics on the RF-ADC FFT page. These metrics are listed and defined as follows.

RF Data Converter E	valuation User Interface (TRD	beta v 1.0)								
Edit Settings V	Vindow Help	DAC Tile 1	ADC THE 1	Commande Log	DACTHAIL DAC 2	DAC THE O	ADC THE O			
erview	ADC IIIe 5	DACINET	ADC THE T	Commands Log	DAC THE T - DAC 2	DACINE	ADC THE U	ADC THE 0 - ADC 25	ADC THE 0 - ADC OF	
0- -5- -10- -15- -20- -25- -30- -35-	FundA	SFDR					Spectrum Maxhold Harmonics Interleave Offset Interleave Gain Fref Spurs Phase Noise Bins Harmonics Bins Visualization	F5 3194.8 Eff. F5 3194.8 CF 200.0 Samples 8	DC Tile 0 - ADC : Signal Type	23 Single-Tone
-40 - -45 -	SFDRxH2						Harmonics Interleaving Performances / Dynamic Performances	Dy	namic Performance Full Nyquist Zone	s A
4 -55-							ACLK Performances			
under -60 - -65 - -77 - -75 - -80 - -85 - -90 - -90 - -100 - -105 -	THE REAL PROPERTY OF THE PROPERTY OF THE REAL PROPE	Pipur Pipurt		tipoppin ^a nte ⁿ ter Activitation			Phase Noise Bins 12 ♥ Harmonics Bins 0 ♥ Search for fund. ♥ ♥ ✓ Hide cursors € Cursors Freg. Ampl. ● Hide cursors € ● Hide cursors € ● Hide cursors € ● Hide Science 9.6 ● Hide Science 9.6 ● Hide Science 9.6 ● Hide Science 9.25 ● Fref Spurs Science 9.25 ● Fref Spurs Science 9.26 ● Fref Spurs Science 9.26 ● Fref Spurs Science 9.26	FundA (dBFS SFDR (dBc) SFDR/t32(d Fspur (MH2) Fspur (MH2) THD (dBc) THD (dBc) SNDR (dBFS) SNDR (dBc) IM3 (dBc)	Value) -9.67 69.14 8c) 71.92 400.92 446.15 -67.34 1z) -151.80 59.80 0.00	10.52 10.52 58.91 61.65 374.18 412.95 -145.49 53.49 53.49 52.86 0.00
0 10	0 200 300	400 500 6	00 700 800 Frequency (MHz)	900 1000 1100	1200 1300 140	0 1500 1600	唐 贺 十		🗌 Loop	Acquire O

Figure 56: **RF-ADC FFT Metrics**

- dBFS: dBFS is the full scale of the RF-ADC expressed in dB, normalized to 0. The dBm value of 0 dBFS depends on the input impedance of the RF-ADC (100 Ω for Zynq[®] UltraScale+[™] RFSoC) and acceptable full scale input level (Vppd = 1V), for Zynq UltraScale+ RFSoC, 0 dBFS is 1 dBm.
- FundA: RMS power level of fund signal expressed in dBFS.
- **SFDR:** Spurious-free dynamic range (SFDR) expressed in dBc. SFDR is the ratio of the RMS value of the signal to the RMS value of the peak spurious spectral component for the analog input that produces the worst result.
- SFDRxH23: SFDR excludes the second and third harmonic distortion in dBc. The location of harmonic distortions are predictable and hence can be handled separately in application. Therefore, a separate SFDRxH23 is listed for reference.



- Fspur: The frequency location of the worst spur in MHz in the first Nyquist band.
- **FspurxH23:** The frequency location of the worst spur excludes the second and third harmonic distortion in MHz in the first Nyquist band.
- **THD:** Total harmonic distortion (THD) in dBc. THD is the ratio of the RMS signal energy to the RMS value of the sum of the first six harmonics.
- NSD: Noise spectrum density (NSD) in dBFS/Hz. NSD is the RMS noise power per Hz normalized to full scale in the first Nyquist band. The noise power in this software indicates total other power except the power of the found signal.
- **SNR:** Signal to noise ratio (SNR) in dB. SNR is the ratio of the RMS signal amplitude to the RMS value of the sum of all the spectral components except the first six harmonics and dc. The unit in dBFS indicates the signal here and refers to full scale of RF-ADC.
- **SNDR:** Signal to noise and distortion ratio (SNDR) expressed in dBc. SNDR is the ratio of the RMS signal amplitude to the RMS value of the sum of all spectral components except fund signal. It is similar to SNR, but includes all the harmonics.
- **IM3:** Third-order inter-modulation (IM3) distortion products expressed in dBc. IM3 used in dual-tone testing, indicates the ratio of RMS signal amplitude to the maximum RMS amplitude of $2F_2 \pm F_1$ or $2F_1 \pm F_2$.
- F_{ref} Spurs: Spurs generated by the input reference (the frequency of phase-frequencydetector) of the PLL, including its harmonics. When using an external PLL for clocking the Zynq UltraScale+ RFSoC directly, you must indicate the reference frequency in the PLL tab for this evaluation tool GUI to calculate the F_{ref} spurs. The RF-ADC is built with interleaving technology. Spurs of offset interleaving and gain/timing interleaving are listed on the RF-ADC FFT tab by choosing Interleaving Performances.
- Interleave Offset: The frequency location and amplitude of offset interleaving spurs.
- Interleave Gain: The frequency location and amplitude of gain/timing interleaving spurs.



Appendix C

Appending Files

RF-DAC Data Pattern

For ZCU111 (Gen 1) boards, data patterns with the TDMS or LVM file format are available for reference under $\Data\DAC$. The contents of these files can be easily identified from the file name. Here is an example of a file name,

IQ_1x_QAM256_RRC0p1_50M_BB491p52MHz_length_16M_-15dB.tdms.

This file name means that the data pattern is in IQ (complex) format, there is one QAM256 modulated carrier, the RRC roll-off coefficient is 0.1, carrier bandwidth is 50 MHz, data sampling rate is 491.52 MHz, data length is around 16M samples, carrier amplitude is –15 dBFS, and the file format is TDMS. Configure RF-DAC in IQ mode at the digital side, set the RF-DAC sampling clock at 3932.16 MSPS, set the interpolation factor as 8 (491.52M * 8 = 3932.16 MHz), then load this file from the RF-DAC FFT page, and you will see the correct carrier.

Note: For the ZCU111 board, the maximum number of samples that the BRAM can handle is 32K for IQ data and 64K for real data. For the ZCU208 and ZCU216 boards, the maximum number of samples that the BRAM can handle is 8K for IQ data and 16K for real data. Switch to the DDR mode (in Memory Type) for data sources if the number of samples is greater than this limitation.

The following figure illustrates the FFT plot of this carrier captured by RF-ADC with a loopback path. In this example, the RF-DAC is set in 32 mA/3V mode and some digital gain to increase carrier amplitude seen by the RF-ADC.







Figure 57: RF-DAC Test Pattern Example

Configuration and Preferences

Configurations (.cfg) and preferences (.prf) are available under \Config . Configurations and preferences are provided in pairs for easy evaluation. The major properties can be found from file name, for example,

RFDC_Example_BRAM_ADC_DAC_8X8_Loop_C2R_X8_3932P16M.efg. This configuration sets sampling frequencies of 3932.16 MHz for all eight RF-ADCs and RF-DACs with decimation and interpolation of 8× and the BRAM selected.



Appendix D

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

Documentation Navigator and Design Hubs

Xilinx[®] Documentation Navigator (DocNav) provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open DocNav:

- From the Vivado[®] IDE, select **Help → Documentation and Tutorials**.
- On Windows, select Start → All Programs → Xilinx Design Tools → DocNav.
- At the Linux command prompt, enter docnav.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In DocNav, click the **Design Hubs View** tab.
- On the Xilinx website, see the Design Hubs page.

Note: For more information on DocNav, see the Documentation Navigator page on the Xilinx website.

References

These documents provide supplemental material useful with this guide:



- 1. ZCU111 Evaluation Board User Guide (UG1271)
- 2. Zynq UltraScale+ RFSoC RF Data Converter Evaluation Tool (ZCU111) User Guide (UG1287)
- 3. LabVIEW Run-Time Engine 2017 SP1
- 4. Zynq UltraScale+ RFSoC RF Data Converter LogiCORE IP Product Guide (PG269)
- 5. Zynq UltraScale+ RFSoC Data Sheet: DC and AC Switching Characteristics (DS926)
- 6. ZCU111 System Controller GUI Tutorial (XTP517)
- 7. Texas Instruments Clocks and Synthesizers (TICS) Pro Software
- 8. LabVIEW Measurement Files
- 9. The NI TDMS File Format
- 10. Zynq UltraScale+ RFSoC Product Tables and Product Selection Guide (XMP105)
- 11. ZCU216 Evaluation Board User Guide (UG1390)
- 12. ZCU208 Evaluation Board User Guide (UG1410)
- 13. Zynq UltraScale+ RFSoC ZCU208 and ZCU216 RF Data Converter Evaluation Tool User Guide (UG1433)

Please Read: Important Legal Notices

The information disclosed to you hereunder (the "Materials") is provided solely for the selection and use of Xilinx products. To the maximum extent permitted by applicable law: (1) Materials are made available "AS IS" and with all faults, Xilinx hereby DISCLAIMS ALL WARRANTIES AND CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY, INCLUDING BUT NOT LIMITED TO WARRANTIES OF MERCHANTABILITY, NON-INFRINGEMENT, OR FITNESS FOR ANY PARTICULAR PURPOSE; and (2) Xilinx shall not be liable (whether in contract or tort, including negligence, or under any other theory of liability) for any loss or damage of any kind or nature related to, arising under, or in connection with, the Materials (including your use of the Materials), including for any direct, indirect, special, incidental, or consequential loss or damage (including loss of data, profits, goodwill, or any type of loss or damage suffered as a result of any action brought by a third party) even if such damage or loss was reasonably foreseeable or Xilinx had been advised of the possibility of the same. Xilinx assumes no obligation to correct any errors contained in the Materials or to notify you of updates to the Materials or to product specifications. You may not reproduce, modify, distribute, or publicly display the Materials without prior written consent. Certain products are subject to the terms and conditions of Xilinx's limited warranty, please refer to Xilinx's Terms of Sale which can be viewed at https://



www.xilinx.com/legal.htm#tos; IP cores may be subject to warranty and support terms contained in a license issued to you by Xilinx. Xilinx products are not designed or intended to be fail-safe or for use in any application requiring fail-safe performance; you assume sole risk and liability for use of Xilinx products in such critical applications, please refer to Xilinx's Terms of Sale which can be viewed at https://www.xilinx.com/legal.htm#tos.

Copyright

© Copyright 2018-2020 Xilinx, Inc. Xilinx, the Xilinx logo, Alveo, Artix, Kintex, Spartan, Versal, Virtex, Vivado, Zynq, and other designated brands included herein are trademarks of Xilinx in the United States and other countries. All other trademarks are the property of their respective owners.

