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Flexible Waveform Processing with the Xilinx Zynq-7000 Extensible Processing Platform

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Today's tactical and commercial Software Defined Radios must have the flexibility and processing power to support a growing number of wideband and broadband waveforms, including an extensive library of legacy waveforms. The secure Xilinx® Zynq™-7000 extensible processing platform (EPP) provides an ideal solution for these applications, not only because it features a high-performance processing system (PS) that leverages ARM® technology, but also because it provides a large programmable logic (PL) unit that supports Partial Reconfiguration and the Xilinx Isolation Design Flow (IDF)—all within a single device.

This white paper describes how the features of the Zynq-7000 Extensible Processing Platform (EPP) can provide a flexible waveform processing platform, using a Software Defined Radio example. Topics include a description of the Zynq-7000 architecture, how to use the Partial Reconfiguration and IDF capabilities of the PL to support various waveforms and reduce part count, and the power management features of the Zynq-7000 device.

Introduction

Figure 1 shows an example block diagram of a tactical SDR. The plain text (PT) portion of the radio (sometimes referred to as the "red" side because the information is unencrypted and can be classified) contains a General Purpose Processor (GPP) and "red" FPGA. The PT information is encrypted and transformed into Cipher Text (CT). The CT information is then processed by the "black" side. The black side (encrypted) of the radio contains a "black" FPGA, another GPP, and a FPGA for waveform processing (Modem FPGA). To ensure the security of the information, the PT and CT portions of the radio are isolated and separated to prevent an information leak of classified or sensitive information out of the system in plain text.

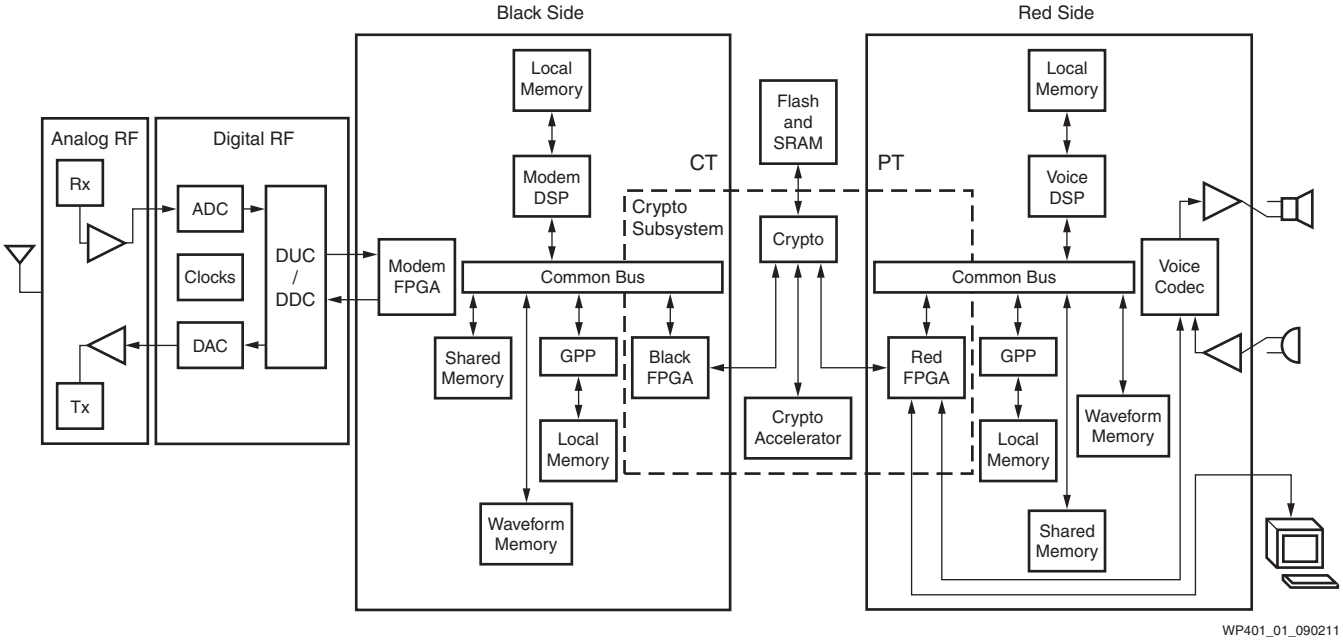

Figure 1: **Example SDR Block Diagram**

Therefore, a typical SDR implementation can use three different FPGAs as well as two separate GPPs, making the device count for these functions as high as five. The Modem FPGA must be sized appropriately to process all of the various waveforms supported by the radio because it is often required to have all the functions available simultaneously, even if only one is needed at a time. For example, processing the Soldier Radio Waveform (SRW) requires ~120K logic cells, 8 Mb of RAM, and 800 DSP slices. The Mobile User Objective System (MUOS) waveform requires >200K logic cells, 10 Mb of RAM, and 900 DSP slices, requiring the Modem FPGA to be quite large. Also, the red FPGA in the Crypto subsystem must also be large enough to contain all of the various cryptographic algorithms for the associated waveforms. The required number of devices, the amount of I/O signaling between the devices (which increases power dissipation), and the large logic density of the devices (which increases static current) make this is a non-optimal solution in terms of size, weight, power, and cost (SWAP-C).

With the Zynq-7000 EPP, the Modem FPGA, black FPGA, red FPGA, black GPP, and red GPP can all be combined into one device (see Figure 2). The Zynq-7000 EPP enables the combination and integration of these devices into a single device and provides a flexible, secure SDR solution that reduces SWAP-C.

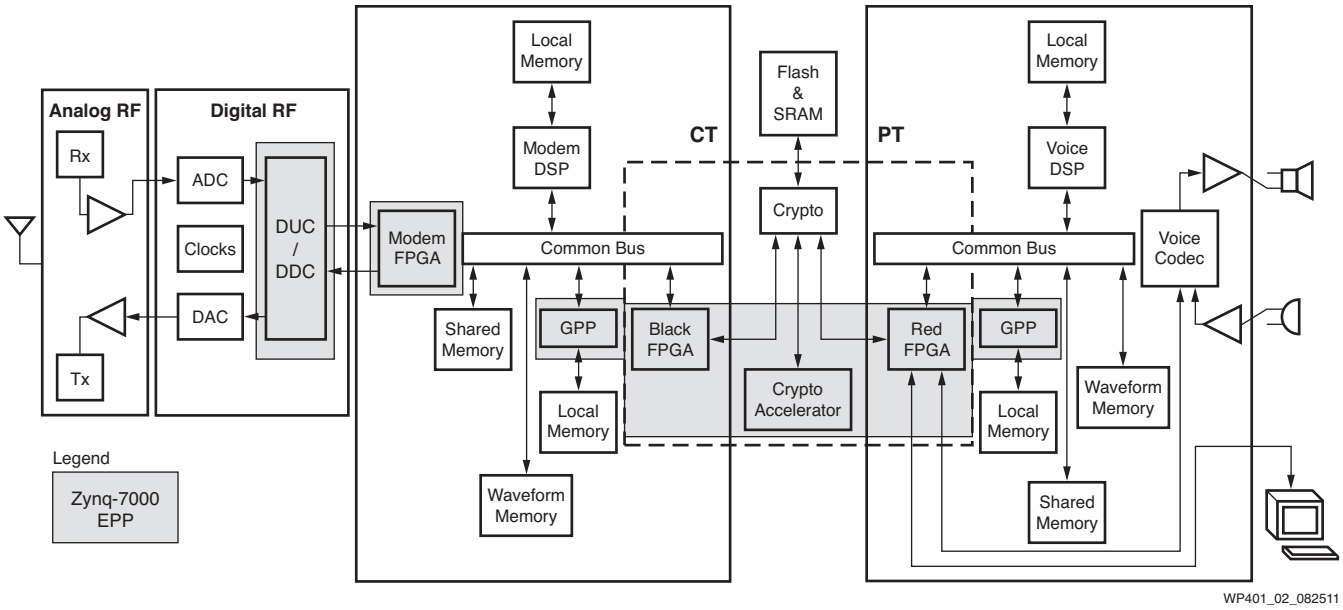

Figure 2: **Secure SDR with Zynq-7000 EPP**

Xilinx Zynq-7000 Extensible Processing Platform

The Zynq-7000 EPP combines an industry-standard ARM processor-based system with Xilinx 28 nm, low-power, high-performance programmable logic in a single device. The processing system (PS) provides dual ARM Cortex™-A9 processors, L1 and L2 cache, on-chip memory as well as a rich peripheral set sufficient for general purpose and/or waveform processing. The PL provides ample logic cells, configurable memory (dual-port RAM, FIFOs, shift registers, and block RAM), and hardware multipliers for DSP, which can be utilized for high-speed parallel processing of needed functions.

Processing System

The dual ARM Cortex-A9 processors each have 32 KB of instruction and data cache and 512 KB of shared L2 cache. Additionally, 256 KB of on-chip memory (OCM) is available to provide low-latency memory to both processors. Cache coherency is maintained by the Snoop Control Unit (SCU). Logic within the PL and the ARM Cortex-A9 processors can share memory, allowing fine-grained interaction between the processors and user logic. An Accelerator Coherency Port (ACP) is also provided to allow coherent sharing of information between the processor and the PL by enabling logic within the PL to access both the L2 cache and the OCM, though direct access to the OCM from the PL is also available. In addition, many industry-standard peripherals and memory interfaces are available to support general and waveform processing. See Figure 3.

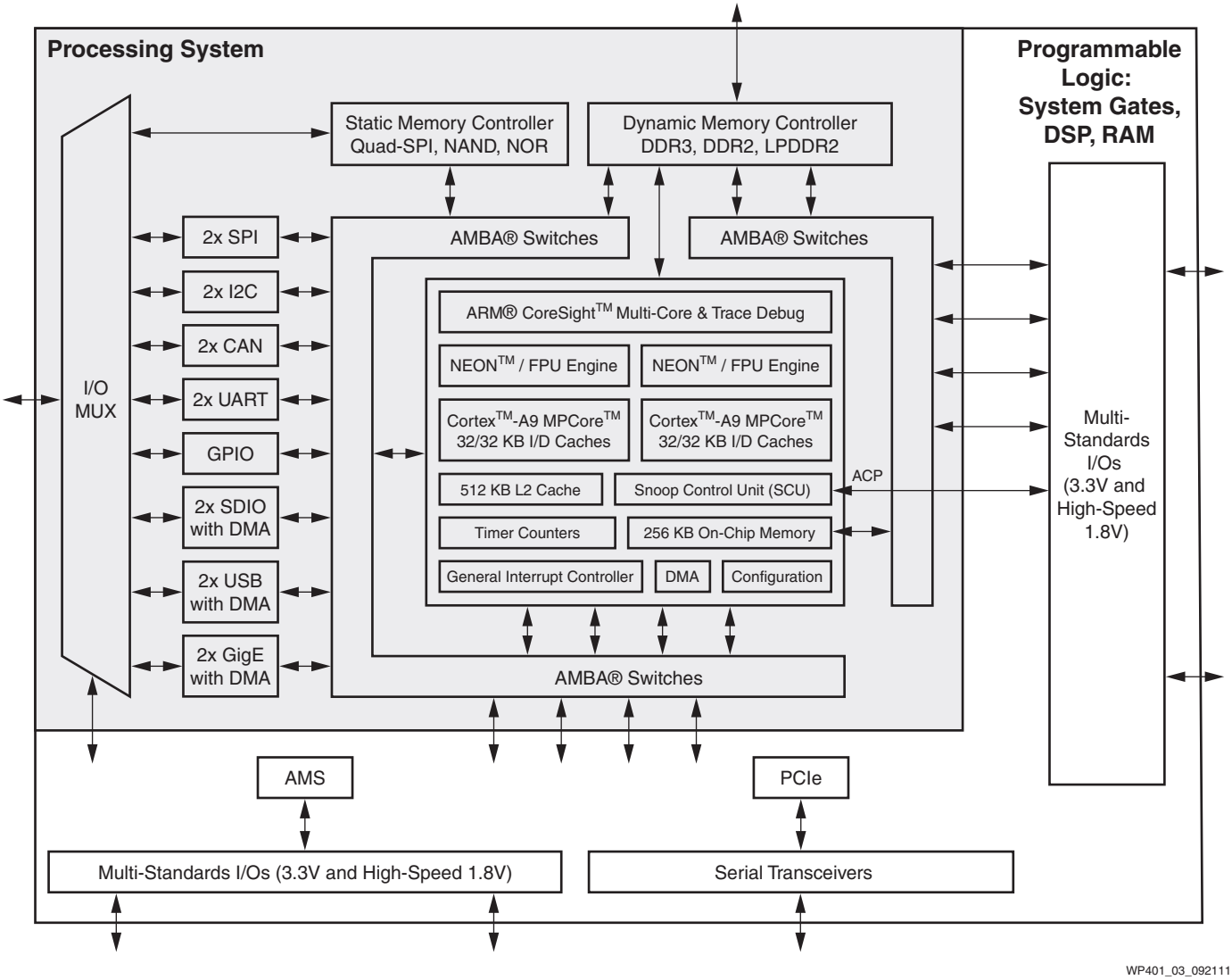

Figure 3: **Zynq-7000 Extensible Processing Platform Block Diagram**

Using the Zynq-7000 EPP PS for Secure Processing

The secure boot process and secure run-time environment provided by the Zynq EPP enables the dual ARM Cortex-A9 to replace both the red-side GPP and the black-side GPP for some applications.

Secure Boot and Configuration

Unlike many ASSPs, the Zynq-7000 EPP provides a Master Secure Boot Mode for configuration of secure, encrypted designs using the internal hardware AES decryption engine, and SHA-256 based authentication engine (HMAC) components within the PL. Security of the Zynq-7000 EPP is controlled through the secure boot sequence shown in Figure 4.

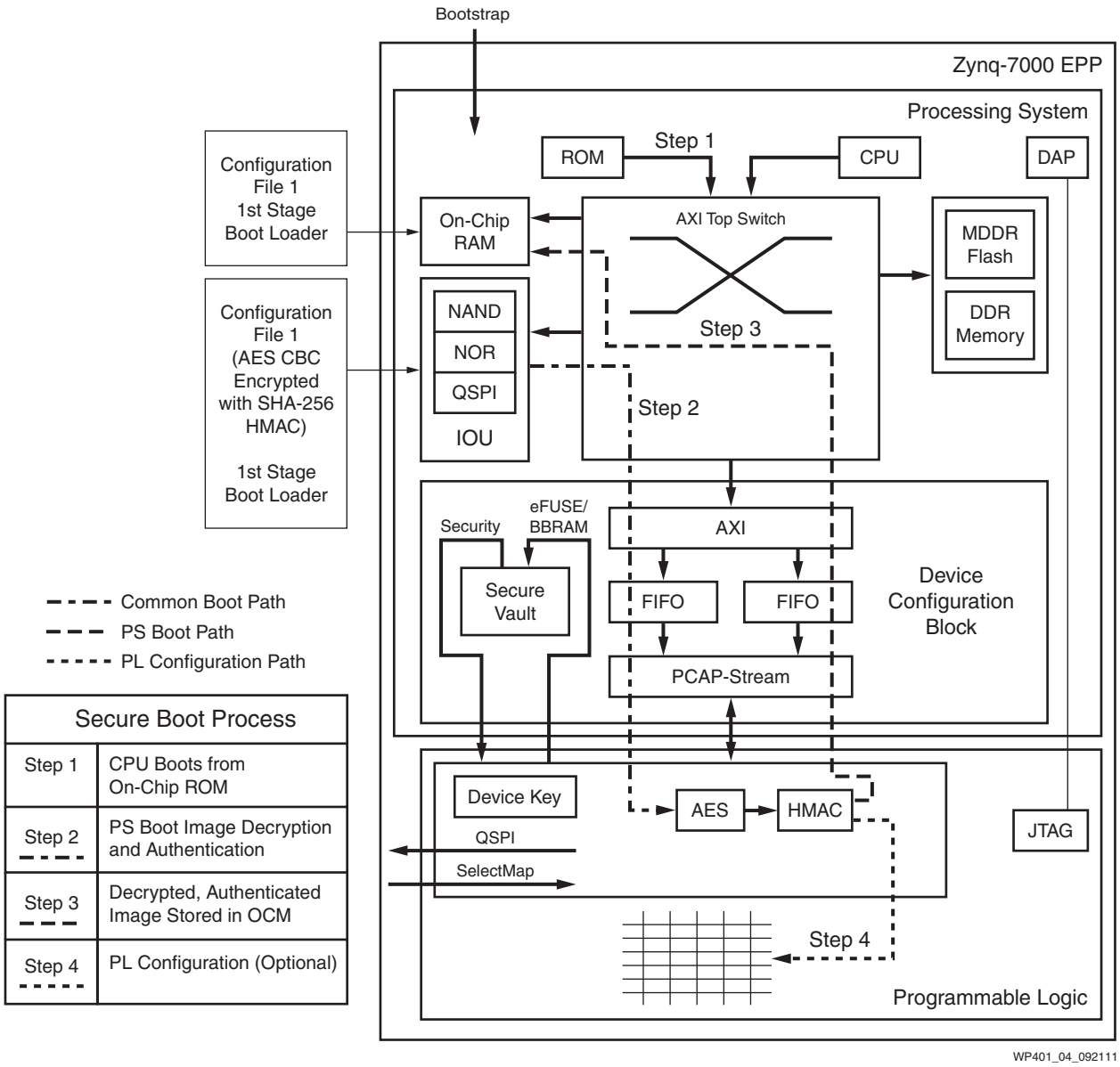

Figure 4: **Zynq-7000 EPP Secure Boot Process**

The master ARM Cortex-A9 processor boots first from the on-chip ROM (step 1). It then reads the PS boot image from the external boot device specified by the boot strap pins (step 2). In conjunction with step 2, the master ARM Cortex-A9 configures the device configuration block to push the PS master image through the hardened AES decrypt and HMAC authentication engines in the PL. The configuration logic loops back the decrypted, authenticated image immediately without internal buffering to be stored in On-Chip Memory within the PS (step 3). The master ARM Cortex-A9 processor polls the final authentication status from the configuration logic to ensure the image is properly authenticated. If it fails, the master ARM Cortex-A9 processor triggers a system secure reset. After the PS image has been successfully loaded, control is turned over to the First Stage Boot Loader (FSBL). Based on the user application, the FSBL can then either start processing, configure the PL (step 4), load additional software, or wait for further instruction from an external source.

Secure Run-Time Environment

The Zynq-7000 EPP provides a secure run time environment by incorporating ARM TrustZone technology throughout the device. TrustZone provides content protection by enabling software tasks to run in memory areas that are segregated, providing protection from unauthorized reading or writing. Eliminating access by other tasks creates and maintains a trusted processing environment. TrustZone is built into the dual ARM Cortex-A9 processors and each element within the PS. In addition, the AMBA TrustZone signals are extended into the PL to allow the development of trusted master and slave devices within the PL. Since complete, secure PL configuration support is provided, these user-developed master/slave devices can be completely trusted as is any other hardened block within the PS. When used with TrustZone software, the Zynq-7000 EPP's support of TrustZone can enable a secure system capable of handling keys, private data, and encrypted information.

Programmable Logic Unit

The PL unit within the Zynq-7000 EPP is built using Xilinx's 28 nm high-performance, low-power process technology. Four devices are available within the Zynq-7000 family, providing a range of PLs with logic cells from 28,000 to 235,000. The PL, like the other devices in the Xilinx 7 series family, provides configurable block RAM, programmable DSP functions, hardened Gen2 PCIe® (larger devices), and Agile Mixed Signal (AMS) technology. AMS technology provides dual 12-bit 1MSPS ADCs, dual independent track and hold amplifiers, on-chip voltage reference and thermal supply sensors, and external analog input channels.

As seen in Figure 2, the digital RF and the logic of the Modem, black, and red FPGAs can be combined and implemented in the PL of the Zynq-7000 EPP. The implementation of the digital RF, modem, and black/red FPGAs in the PL is possible through the use of Partial Reconfiguration and the IDF, not because of a large PL fabric.

Partial Reconfiguration

Partial Reconfiguration of the Zynq-7000 EPP PL takes the flexibility provided by normal FPGA technology a step further by allowing the modification of an operating design by reconfiguring portions of the PL to perform a different function. After the PL has been fully configured with a complete configuration file, partial configuration files can be downloaded to modify reconfigurable regions in the PL. The logic in the PL is divided into static logic and reconfigurable logic. The static logic remains functional and is completely unaffected by the loading of a partial configuration file. The reconfigurable logic is replaced by the contents of the partial configuration file. The downloading of partial configuration files is done without compromising the integrity of the applications running on those parts of the device not being reconfigured.

Partial Reconfiguration allows time multiplexing of different hardware functions dynamically on a single Zynq-7000 EPP. Time-independent functions can be identified, isolated, and implemented as reconfigurable modules and swapped in and out of a single device as needed. This reduces the need to have a Zynq-7000 EPP with programmable logic large enough for all of the required functions that are needed at different times. The PL now only has to be large enough for the largest function needed at any single time. SDR, by having mutually exclusive functionality, can directly benefit from this technology and see a dramatic improvement in flexibility, resource usage, and a reduction in static power.

The Zynq-7000 architecture further extends the flexibility of Partial Reconfiguration by allowing software running in the PS to reprogram portions of the PL via Partial Reconfiguration. For secure designs, since the PS and PL images are initially authenticated and control the loading of the partial reconfiguration file, the Partial Reconfiguration file can either be encrypted or unencrypted. So both the software processing algorithms and the corresponding programmable logic (to implement those algorithms) can be swapped in and out for different waveforms. See Figure 5.

Xilinx Isolation Design Flow

The IDF provides for multiple physically isolated/independent functions to be implemented within a single FPGA device, utilizing a fence of unused device components between each function. Each isolated function is separated by this fence, generating isolated regions within the device. The flow uses early floorplanning, modular design, modular synthesis, and adherence to a set of guidelines and considerations to guarantee isolation between desired functions. Once a design is implemented, the Xilinx Isolation Verification Tool (IVT) can be used to visualize the modules and fence, along with verifying that the design rules for isolation have been successfully implemented.

With the development of the IDF, red and black processing logic can reside on the same FPGA, allowing designers of the cryptographic portions of SDRs to realize the full capability of programmable logic. The IDF was developed to allow independent red and black functions to operate on a single device and to eliminate the requirement for separate red and black FPGAs. Examples of such single-chip applications include, but are not limited to, redundant data encryptors, resident red and black data, and functionality operating on multiple independent levels of security.

Waveform Processing Using the Zynq-7000 EPP

By defining each of the waveform processing blocks as reconfigurable logic, the PL within the Zynq-7000 EPP only has to be large enough to contain one waveform processing block at a time. The use of the IDF allows the encryption and decryption (red and black) processing logic to coexist within each waveform processing block. The use of Partial Reconfiguration allows different waveform processing blocks to be dynamically swapped in and out of the Zynq-7000 EPP PL under software control (see Figure 5). For certain radio applications, one of the ARM Cortex-A9 processors within the PS can perform the red GPP functions and the other ARM Cortex-A9 processor can perform the black GPP functions. This same SDR can also support future waveforms by developing the necessary software and waveform processing blocks to be swapped into the Zynq-7000 EPP's PS and PL as reconfigurable logic, extending the overall product life cycle of the SDR.

The Zynq-7000 EPP can reduce the device count for the example design shown in Figure 2 from five devices to a single device and provide flexibility to support future waveforms using the same hardware platform. Along with its power-saving features, the use of the Zynq-7000 EPP in an SDR can significantly improve the size, weight, power and cost (SWAP-C) of the system and provide a flexible, programmable platform. See Figure 5.

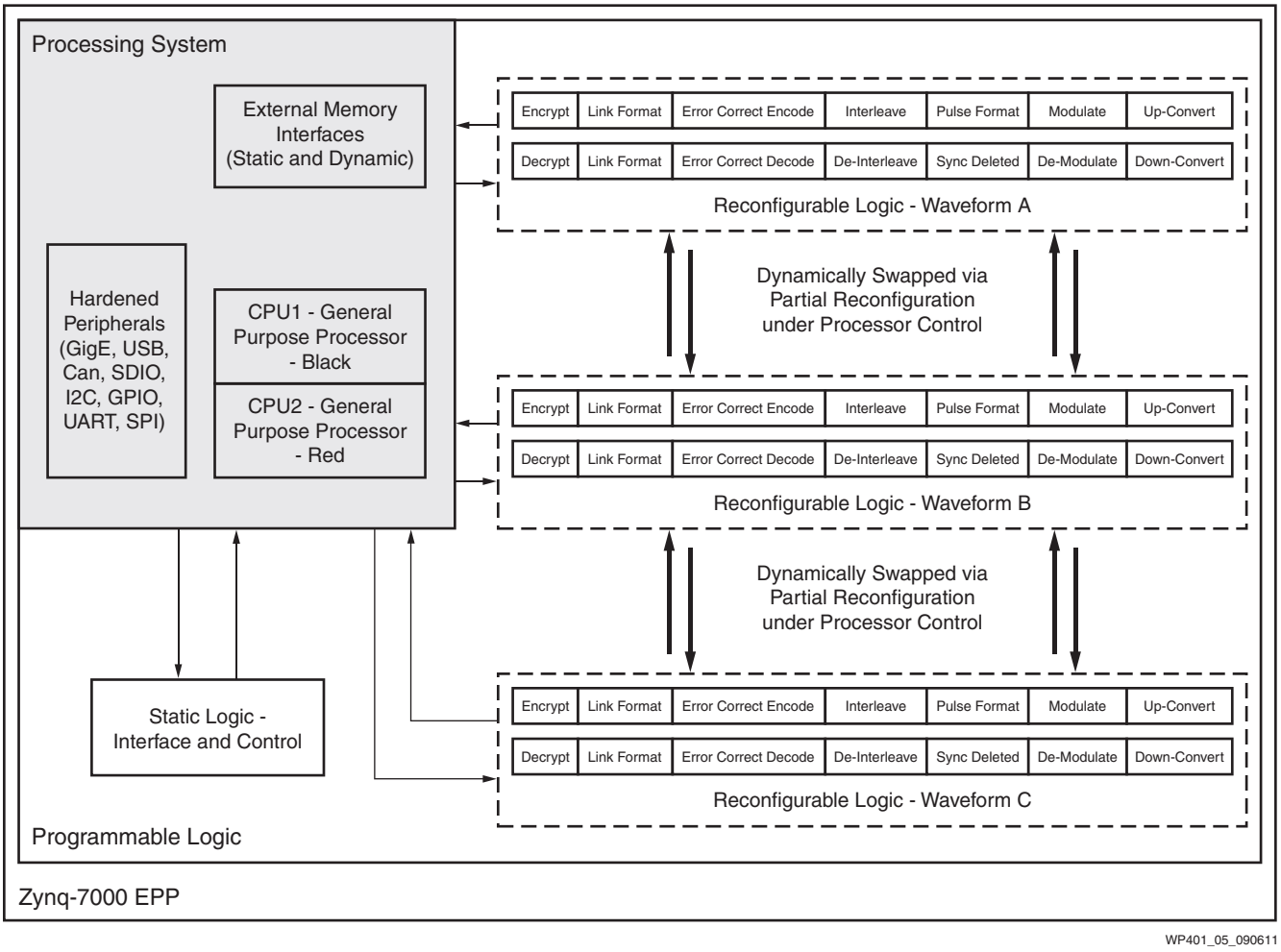

Figure 5: **Use of Zynq-7000 EPP Partial Reconfiguration and IDF to Support Multiple Waveforms**

Power Saving Features

Zynq-7000 EPP supports many features to lower the overall system power consumption, such as PS Power-on Only Mode, Sleep Mode, and Peripheral Independent Clock Domains. These features can be used to significantly reduce the dynamic power consumption of the device during idle periods.

PS Power-On Only Mode

The Zynq-7000 EPP's PS and PL are on two independent power rails, and each has its own dedicated power supply pins. It supports a PS power-on only mode but does not support a PL only mode. User software in the PS can turn the PL fabric power on/off at any point of time, which reduces the static power required. When the PS is powered off, it holds the PL in a permanent reset condition until the PS comes out of reset.

Sleep Mode

In sleep mode, a single ARM Cortex-A9 processor runs at ~10 MHz in Wake From Interrupt (WFI)/Wake From Exception (WFE) mode, interconnects are shut down, DDR is in self-refresh mode, all DDR termination is off, and PS peripherals are in clock-gating mode except for the selected wakeup device (CAN, Ethernet, or GPIO). The dynamic power consumption in sleep mode is only from a small part of the CPU circuit used to monitor the wakeup interrupt, SCU, and the wakeup peripheral device. The PL power can also be shut down in Sleep mode, resulting in further reductions in static power.

Independent Clock Domains

The Zynq-7000 EPP supports many clock domains, each with independent clock-gating control, which allows the user to shut down the clock domains that are not used in order to reduce dynamic power. Each of the peripherals within the PS (except the GPIO due to its small size and low speed) are on an independent clock domain, each with clock-gating control and can be turned off via software through the system-level control registers.

Conclusion

Continuing the tradition of secure integration, a single Xilinx Zynq-7000 EPP provides the processing power and logic formerly supplied by five or more separate devices for the processing and logic functions in tactical radios and commercial SDRs. The Zynq-7000 EPP provides the capability and flexibility to reuse the same logic resources to process various waveforms by dynamically redefining some or all of the logic functions within the PL, therefore enabling support of multiple waveforms and future waveforms. The reduction of several devices into one Zynq-7000 EPP can result in a significant reduction in overall size, weight, power, and cost (SWAP-C) of the SDR. Furthermore, the Zynq-7000 EPP provides several features that enable additional reductions in both static and dynamic power consumption, making it an ideal solution for a flexible, secure commercial or tactical SDR.

Additional Information

1. 1.Xilinx Zynq-7000 EPP Product Brief
   http://www.xilinx.com/publications/prod_mktg/zynq7000/Product-Brief.pdf
2. Xilinx 7 Series Product Brief
   http://www.xilinx.com/publications/prod_mktg/7-Series-Product-Brief.pdf
3. UG702, *Xilinx Partial Reconfiguration User Guide*

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
09/29/11	1.0	Initial Xilinx release.
03/06/12	1.0.1	Minor typographical edits.

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