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Reducing System BOM Cost with Xilinx's Cost-Optimized Portfolio

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Xilinx's Cost-Optimized Portfolio adds a new perspective to system cost analysis by offering many unique strategies for overall BOM cost reduction.

ABSTRACT

System designers are under enormous pressure to meet feature and performance requirements while managing down total project cost. Unlike development costs, system BOM cost typically scales with production quantity, making it an important area of focus for cost control.

A system's BOM comprises many interdependent component costs, meaning a holistic approach is required to ensure the lowest overall cost is achieved. Without looking at the big picture, system designers searching for cost optimization can unknowingly end up trapped in a local minimum cost point.

While cost optimization is a concern for nearly all systems, it is typically high volume applications that deal with exceptional cost pressure. Some examples of applications where cost is a significant factor include industrial motor control and vision systems, camera-based advanced driver assistance and autonomous driving systems, and portable systems including drones, medical equipment, and wireless communication systems.

Balancing the right features and cost-effectiveness, Xilinx offers an extensive Cost-Optimized Portfolio of products that delivers the best value for a breadth of applications. The portfolio features the Spartan®-6, Spartan-7, and Artix®-7 FPGAs with the MicroBlaze™ soft processor, as well as the Zynq®-7000S and Zynq-7000 SoCs.

Introduction

Total cost involves factors such as system BOM cost, field upgradeability, length of design cycles, and development of derivative products. This white paper focuses exclusively on the extraction of maximum value from the device selection to reduce system BOM cost. The device capabilities inherent in the Xilinx Cost-Optimized Portfolio offer system designers many holistic cost reduction opportunities. While methodically examining the cost of each device in a system is a worthy (and necessary) exercise, designers are best served by taking a holistic approach, examining the impact that device features might have on the design of the whole system, and hence on their effect upon the overall BOM cost.

It starts with an understanding of major cost drivers within a typical system's BOM, which include:

- Digital logic components (e.g., FPGAs, ASSPs)

- Processors (e.g., SoCs, CPUs, MPUs, DSPs)

- Mixed-signal and analog components (e.g., amplifiers, ADCs, DACs)

- Sensors (e.g., temperature, pressure, humidity)

- Power supplies and thermal management components

- Volatile and nonvolatile memory components

- Passive components (e.g., resistors, capacitors, inductors)

- Safety, security, and reliability components

- Protocol PHY components

- Clocking components

The mix and range of capabilities represented in the Cost-Optimized Portfolio canvas a majority of the low-cost application space, enabling system designers to select a best fit implementation technology with application-aligned features. As a result, integration is maximized and silicon overhead minimized, yielding a superior cost point. For complete consideration of system BOM cost, analysis must also include the cost of the printed circuit board (PCB) itself, including PCB layers, mechanical components, and connectors.

Cost-Optimized Portfolio Overview

The Xilinx® Cost-Optimized Portfolio delivers extremely high value to cost-sensitive applications across a broad range of computational and connectivity requirements. The multiple product families within the Cost-Optimized Portfolio ensure Xilinx can address diverse markets with aligned product features, minimizing the silicon overhead associated with a "one-size-fits-all" approach.

The Cost-Optimized Portfolio consists of the Spartan-6, Spartan-7, Artix-7, and Zynq-7000S and Zynq-7000 families, as shown in Figure 1. Spartan-6 FPGAs deliver I/O optimization with the highest I/O to logic cell ratio. Spartan-7 FPGAs provide silicon architecture improvements, access to next-generation development system software, and through the combination of these, a 2.5X improvement in performance per watt. With the same Spartan-7 FPGA silicon architecture, Artix-7 FPGAs expand connectivity through their robust transceiver technology while further extending

computational capability through higher available logic cell quantities. Zynq-7000S and Zynq-7000 AP SoCs are a fusion of the computational and connectivity strengths of Xilinx programmable logic technology with highly capable single- or dual-core ARM® Cortex™-A9 processing systems. These devices deliver system integration and optimization for SoC applications.

The Cost-Optimized Portfolio Backgrounder, available on the Xilinx website [Ref 1], provides an excellent overview of this recently assembled portfolio of Xilinx product families.
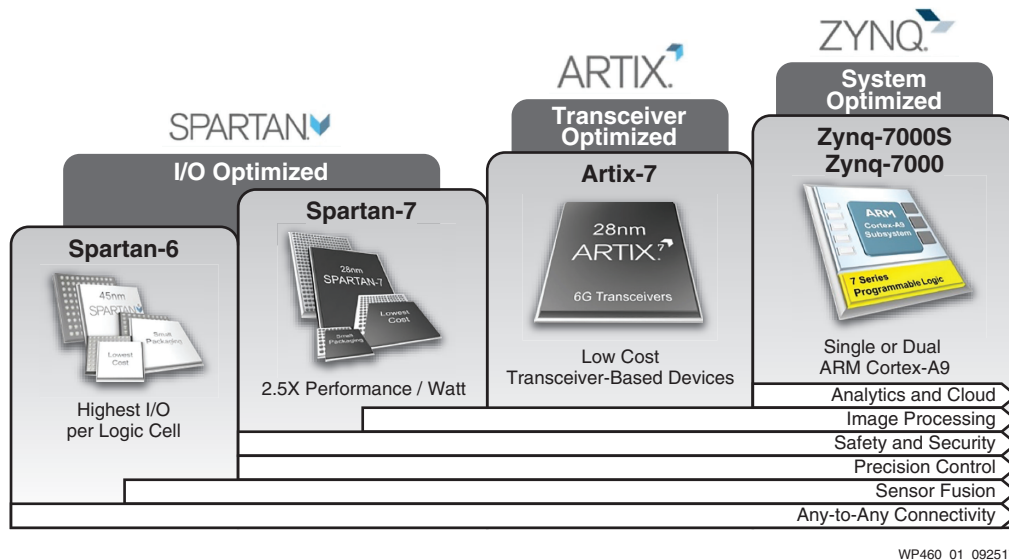

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Figure 1: **Xilinx's Cost-Optimized Portfolio Value**

The Spartan-6 family is the industry's low-cost leader and an ideal fit for simple to moderately complex bridging functions found in a range of applications. This includes such market segments as consumer, automotive infotainment, and industrial automation. In addition to the highest I/O to logic cell ratio, this device family offers small form-factor packaging and best-in-class logic performance that meets the power requirements for many cost-sensitive systems.

For FPGA applications that demand advanced functionality with increased opportunity for power or performance optimizations, the Spartan-7 family offers exceptional performance per watt. This family leads the industry in nearly every aspect of performance in a low-cost device, including logic fabric performance, memory interface bandwidth, and signal processing computational throughput.

The Artix-7 family is distinguished by its 7 series GTP transceivers, which are power optimized for consumer and commodity serial standards. With up to 16 GTP transceivers per device, and line rates up to 6.6Gb/s, the family offers the industry's smallest and fastest transceiver-based devices. Available in packages as small as 10mm x 10mm, Artix-7 devices are an ideal choice for bandwidth-intense applications that might otherwise require more costly solutions.

For applications that need complex control flows, protocol software stacks, intelligent management and analytics of hardware accelerators—or simply leading edge integration—the Zynq-7000S and Zynq-7000 family are ideal solutions. On a single chip, these devices bring together hardware, software, analog mixed signal, and connectivity capabilities, enabling a highly integrated solution at a cost point that cannot be matched by piece-wise assembly with separate

components at the board level. This, in turn, has downstream effects, reducing system power and maximizing performance. Zynq-7000S devices fuse Artix-7 FPGA fabric to a single-core ARM Cortex-A9 processing system, with Zynq-7000 devices raising the processing system performance bar through a dual-core processing system.

System designers are under enormous pressure to meet feature and performance requirements while managing down non-recurring development cost and system BOM cost. The Cost-Optimized Portfolio addresses a diverse range of needs, as shown in Figure 2. In Xilinx's product definition process, a large number of applications in a variety of markets was analyzed to evaluate total solutions, including silicon capability, firmware libraries, development tools and IP, and their corresponding impact on system BOM cost. Xilinx's focus is on delivering extremely capable solutions at the right price—inherently high value—while further enabling effective system BOM cost reduction.
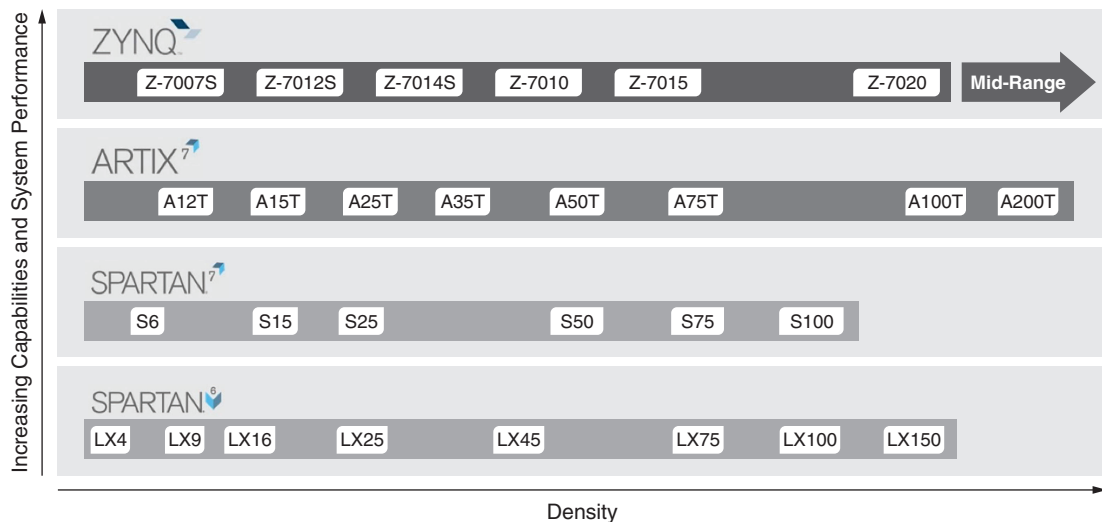
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Figure 2: **Cost-Optimized Portfolio by Logic Cell Density**

Bill of Materials Cost Reduction Strategies

Several elements impact and contribute to overall BOM cost in a system—i.e., the cost of the components and the board itself. Devices in the Xilinx Cost-Optimized Portfolio mitigate these costs by:

- Eliminating components through systems integration
- Reducing the cost of other components on the board through diverse functionality
- Minimizing PCB development and fabrication cost through best-in-class device packaging

Eliminating Components through System Integration

The advantage of a programmable device is not just customizable digital logic; it is, rather, the broad array of functions—in some cases, non-digital—available in today's technology. A system's high-value digital components can comprise processors, programmable logic, DSPs, ASSPs, or a combination of these; its non-digital components can include ADCs, sensors, and PHY interfaces, among others. Devices from Xilinx's Cost-Optimized Portfolio can integrate much of this functionality on a single chip.

High-density system integration like this not only lowers BOM cost, but because this process reduces board space and overall power consumption, it lowers the cost of the PCB itself, as well as the system's power and thermal management solutions.

Processor Integration

Many applications require a processor to simplify the interaction of the system with a wider network, with a human-machine interface (HMI), or with an observation-and-maintenance solution. In the past, systems needed to contain both programmable logic and a discrete processor to meet such requirements. However, Xilinx offers a range of processor-included solutions to meet a diverse set of application requirements. External processors are no longer needed.

MicroBlaze IP Core Processors

The MicroBlaze CPU is a highly configurable 32-bit microprocessor that has been optimized for Xilinx FPGAs. To help quickly deploy an application, preset configurations ("presets") have been defined that are similar to other familiar processor classes. If the design requires running bare-metal code, then the "Microcontroller" preset is suitable. If deterministic real-time processing capabilities running an RTOS are required, then the "Real-Time Processor" preset provides this capability. And finally if the full power of Linux is needed in the embedded system then the "Application Processor" preset is best suited for this use case.

Starting from these presets, if desired, it is possible to add or remove a variety of specific options to customize the processor to the specific needs of the application. The MicroBlaze processor meets requirements for many diverse applications in Industrial, Medical, Automotive, Consumer, and Communications markets, among others. The MicroBlaze processor can be used across all of Xilinx FPGAs and All Programmable (AP) SoC families. It is included at no cost with all editions of the Vivado® Tools.

Using Vivado tools' IP Integrator, a MicroBlaze processor can be expanded with IP from a catalog of driver-enabled peripherals such as PWMs, UARTs, serial interfaces, etc. Designers can leverage the no-cost, Eclipse-based Software Development Kit from Xilinx [Ref 29].

For detailed information and links to documentation, visit the MicroBlaze processor page on the Xilinx website [Ref 2].
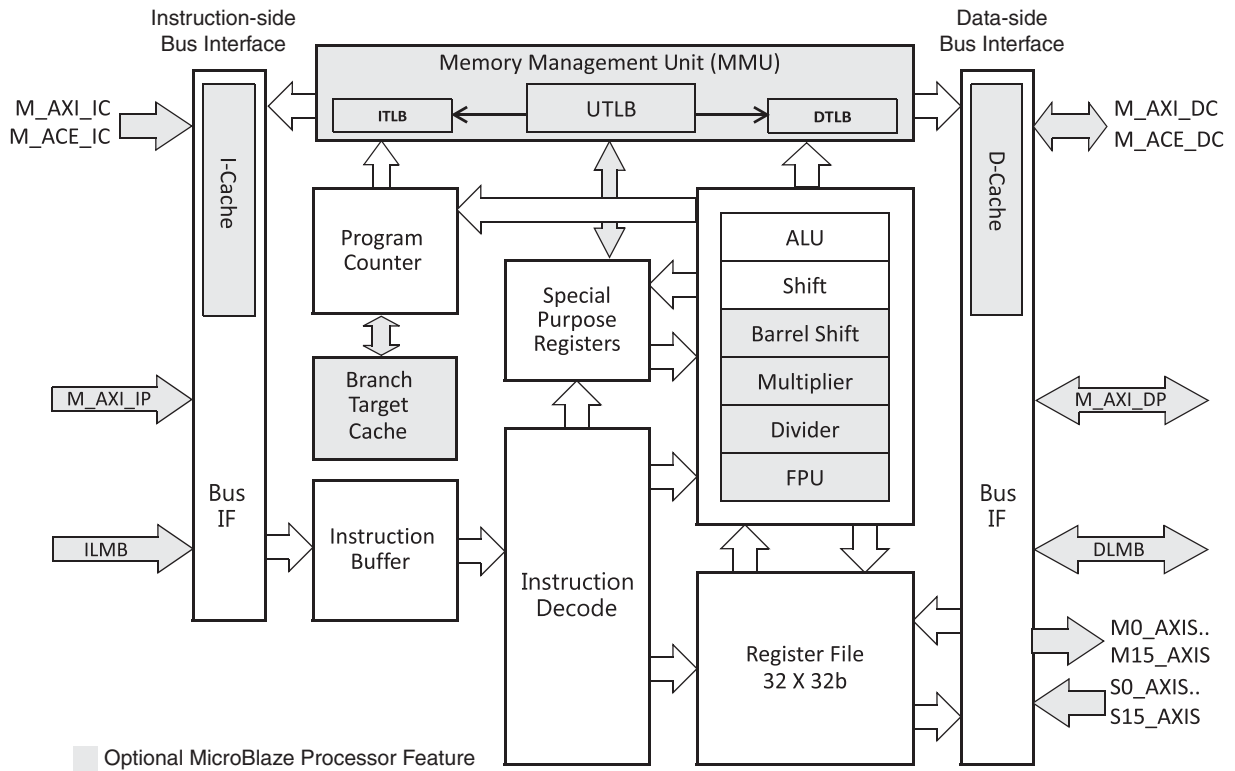
Figure 3: **MicroBlaze Soft Processor IP Block Diagram**

The variety of options available for configuring the MicroBlaze CPU enables highly customized processing solutions, including the possibility of extreme resource reduction yielding an implementation cost that can be less than 20 cents per processor. The core MicroBlaze processor presets include:

1. Microcontroller Preset

    a. Small 32-bit microprocessor for basic control applications

    b. 200MHz, 1.1DMIPS/MHz, 1000 LC

2. Real-Time Processor Preset

    a. More capable microprocessor suitable for RTOS applications

    b. 160MHz, 1.3DMIPS/MHz, 4500 LC

3. Applications Processor Preset

    a. Additional capability in support of Linux applications

    b. 120MHz, 1.4DMIPS/MHz, 6500 LC

Single- and Dual-Core ARM Cortex Processors

The Zynq-7000S and Zynq-7000 families offer even more in the way of processing options. Each device in these families contains a processor system, as shown in Figure 4. Both families leverage integrated implementations of the ARM Cortex-A9 microprocessor as single-core Zynq-7000S SoCs and dual-core Zynq-7000 SoCs. Processor clock frequencies up to 1GHz are available, and all devices enjoy extensive OS, middleware, and stack ecosystem availability.
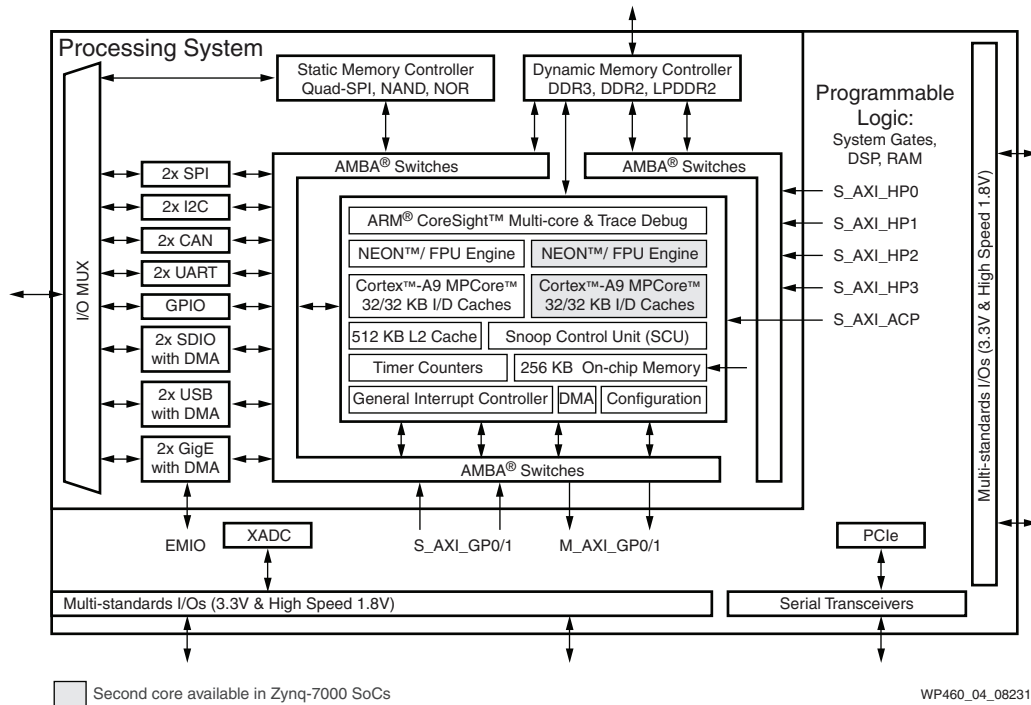
Figure 4: **1 GHz Dual-Core Hardened Implementation of the ARM Cortex-A9 MP Core Microprocessor**

This extensive array of processing options ensures that, in the vast majority of applications, no additional processor is required in the system, resulting in a significant BOM cost reduction. This also enables massive performance improvements due to the data transfer speeds that can be achieved between the on-chip processor and logic, as well as the hardware acceleration of processing and analytics functions that can be performed in the programmable logic space.

Mixed-Signal and Analog Components

Because mixed-signal and analog components (e.g., analog-to-digital converters, amplifiers) continue to be major contributors to a system's BOM, the 28 nm-based Spartan-7 (except 7S6 and 7S15), Artix-7, Zynq-7000S, and Zynq-7000 devices provide an integrated analog mixed signal block called the Xilinx Analog-to-Digital Converter (XADC) [Ref 3] containing:

- A dual 1 MSPS 12-bit analog-to-digital converter (ADC)
- Seventeen external voltage inputs
- On-chip temperature and supply sensors
- JTAG and zero-latency DRP interfaces

Not only can this block replace discrete ADC components—but when coupled with the signal processing resources of the FPGA or AP SoC, the XADC can simplify and reduce the costs of the entire AMS signal chain. For more information on this topic, see the Xilinx white paper *Efficient Implementation of Analog Signal Processing Functions in Xilinx All Programmable Devices* [Ref 4].

For applications like motion control, power conversion, and distributed control systems, the XADC can be used to directly replace discrete ADCs and cost-reduce or eliminate other elements in the main control path. This results in a highly integrated, high-performance, yet low-cost solution, similar to the motor control example shown in Figure 5.
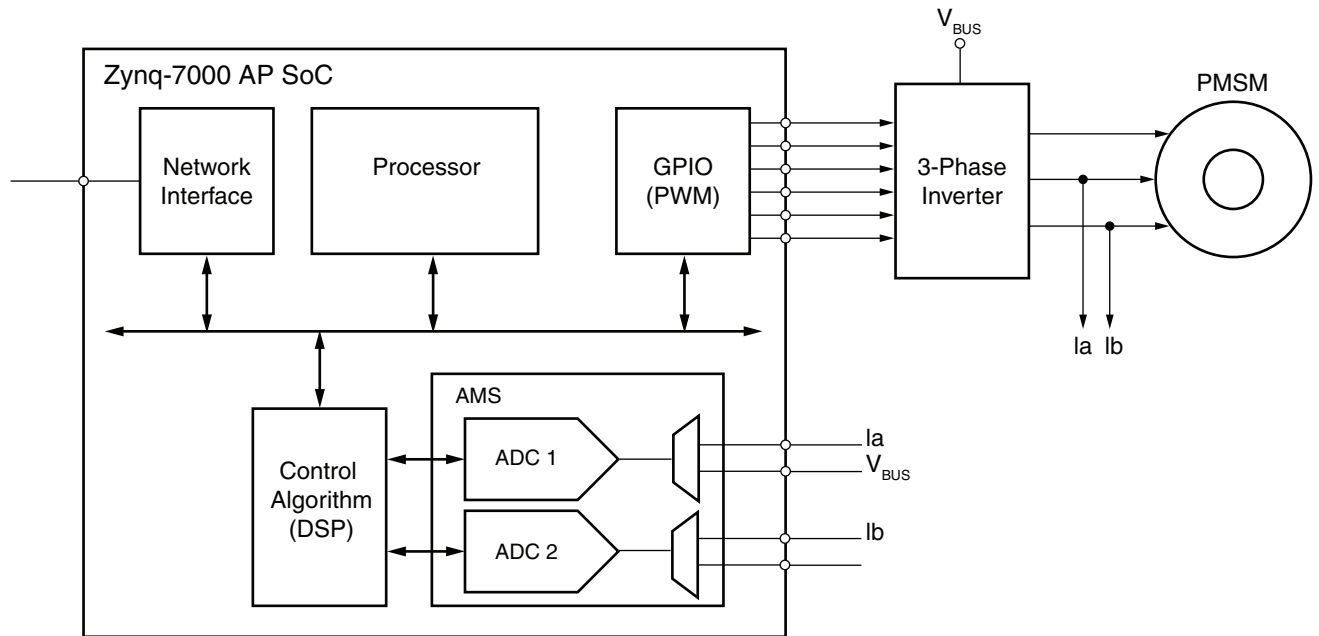
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Figure 5: **Integrated High-Performance Motor Control Solution**

For applications that demand high reliability, security, or functional safety, the XADC provides environmental monitoring capabilities, such as junction temperature and on-chip supply sensing, eliminating the need for external monitor solutions, while at the same time meeting industry standards such as IEC61508 and FIPS140-2.

PHY Integration

Given the growing array of interface standards and protocols, an external device (sometimes called a PHY) might be required to physically translate the electrical signals to a form that can be interfaced to an existing integrated circuit.

For a diverse number of protocols, Xilinx's Cost-Optimized Portfolio families offer interface support and IP to help remove the requirements for external components. For example, HDMI video IP (compliant up to HDMI 2.0) is available for all Artix-7, Zynq-7000S, and Zynq-7000 devices. This IP removes the requirement and associated cost of an external HDMI transmitter/receiver and replaces it with resistors on the receive side and simple drivers/level-shifters on the transmit side.

Other interfaces supported by the Cost-Optimized families include DisplayPort, XAUI, V-by-One, 3G-SDI, and JESD204B. For many of these protocols, multiple components are eliminated and overall system cost is reduced.

Clocking Integration

The simplicity of a single-clock fully synchronous design is appealing, but rarely practical. Factors that dictate the use of multiple clocks include selection of interface standards and protocols, design-level integration of multiple IPs, and system-level integration of components, which also need clock sources. The cost of discrete timing solutions, e.g., oscillators, clock generators, and clock buffers, quickly adds up.

All devices in the Cost-Optimized Portfolio support advanced clocking features, which represent an opportunity to pare down the need for discrete timing solutions. Approaches to seize these cost-down opportunities are:

1. Share clocks between design modules (removes redundant oscillators)

2. Generate clocks from a low frequency oscillator (reduces oscillator count and cost)

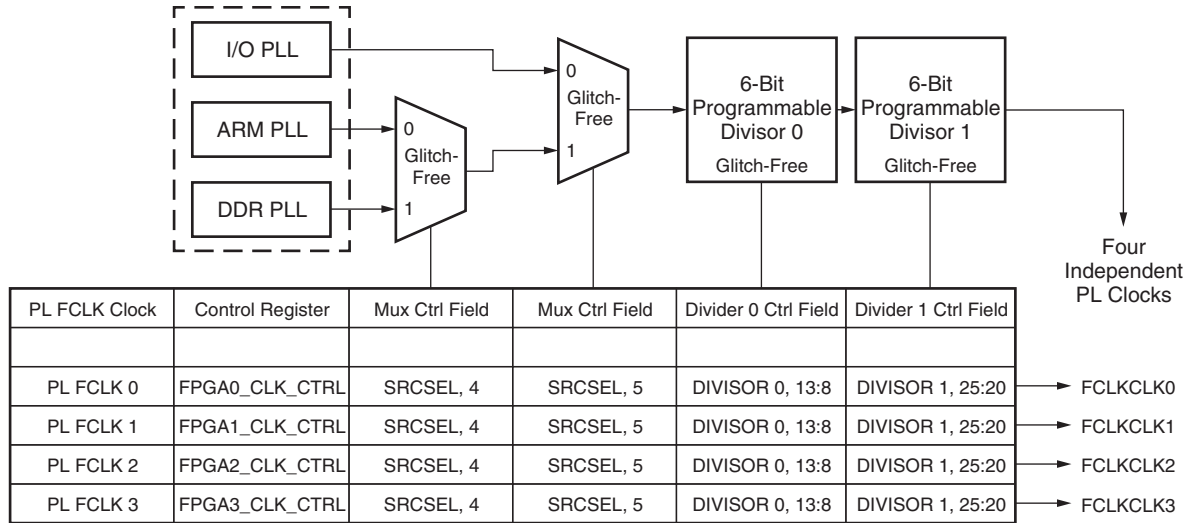3. Generate and distribute clocks for other components (minimize discrete timing solutions)

Although it seems obvious to share clocks between design modules, the required follow-through can sometimes pose a challenge. Many complex designs are assembled by stitching IP from various sources: reused legacy code from previous designs, proprietary IP from third parties, and IP from the Vivado® Design Suite IP catalog.

Xilinx recognizes this challenge and strives to demonstrate best practices in IP development. Many complex IP from the Vivado Design Suite have been architected under guidance of the Xilinx Shared Logic initiative. Shared logic is an IP feature that provides a flexible architecture that works both as a stand-alone IP and as a part of a larger design with one or more IP instances. This facilitates sharing clock input pins to remove redundant oscillators, internal clock buffers to consume fewer routing resources, and advanced clocking features to generate additional internal and external clocks. A sample of IP from the Vivado Design Suite that support clock sharing includes:

*   *Tri-Mode Ethernet MAC LogiCORE™ IP Product Guide* [Ref 5]

*   LogiCORE™ IP DDR3 SDRAM Interfaces per *Zynq-7000 AP SoC and 7 Series Devices Memory Interface Solutions v4.2* [Ref 6]

*   7 Series FPGAs Integrated Block for PCIe v3.3 *LogiCORE™ IP Product Guide* [Ref 7]

The lowest cost method to source the clocks that remain necessary is to generate them from a low-frequency oscillator, using advanced clocking features available in all Xilinx programmable devices. Xilinx provides the Clocking Wizard in the Vivado Design Suite for ease of use in configuring advanced clocking features. Although the names of these features vary based on device family, all of them are capable of frequency synthesis to generate new clock frequencies from their input clock. In many cases, a design does not require known a phase or frequency relationship between each of the generated clocks. When this is the case, it is advantageous for timing closure to apply false path constraints.

Zynq-7000 and Zynq-7000S AP SoCs provide additional options to generate clocks through the processing system PLLs. While the primary purpose of these PLLs is to support the processing system and its interfaces, the PLL outputs can be routed to four programmable divisors, yielding four independent clock signals into the programmable logic named FCLKCLK0 through FCLKCLK3. See Figure 6.

PL FCLK Clock	Control Register	Mux Ctrl Field	Mux Ctrl Field	Divider 0 Ctrl Field	Divider 1 Ctrl Field	
PL FCLK 0	FPGA0_CLK_CTRL	SRCSEL, 4	SRCSEL, 5	DIVISOR 0, 13:8	DIVISOR 1, 25:20	FCLKCLK0
PL FCLK 1	FPGA1_CLK_CTRL	SRCSEL, 4	SRCSEL, 5	DIVISOR 0, 13:8	DIVISOR 1, 25:20	FCLKCLK1
PL FCLK 2	FPGA2_CLK_CTRL	SRCSEL, 4	SRCSEL, 5	DIVISOR 0, 13:8	DIVISOR 1, 25:20	FCLKCLK2
PL FCLK 3	FPGA3_CLK_CTRL	SRCSEL, 4	SRCSEL, 5	DIVISOR 0, 13:8	DIVISOR 1, 25:20	FCLKCLK3

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Figure 6: **Signal Flow**

This example, borrowed from the Xilinx *Zynq-7000 All Programmable SoC Technical Reference Manual* [Ref 8], shows the signal flow and the registers associated with configuring it.

Given the advanced clocking features in all Xilinx programmable devices, it is possible to generate and distribute clocks for other components simply by routing a desired internal clock to one or more SelectIO™ interfaces. These interfaces support single-ended and differential signaling across a variety of signaling standards, enabling clock fanout buffering and voltage level translation without use of discrete timing solutions.

One of the most expensive discrete timing solutions is the voltage controlled crystal oscillator (VCXO) used in association with SerDes in applications such as broadcast video and networking. Under certain conditions, Zynq-7000 and Zynq-7000S AP SoCs and Artix-7 FPGAs can eliminate the need for external VCXOs. This novel solution is explained in detail in Xilinx application note XAPP589, *All Digital VCXO Replacement for Gigabit Transceiver Applications* [Ref 9]. At an estimated $10 to $15 per external VCXO, this represents a high-impact cost reduction.

Safety and Security Components

A growing number of applications are required to meet industry standards for security, functional safety, and reliability. As the world becomes more automated and interconnected, designers of automation equipment must ensure that their systems operate in a safe manner that cannot be interfered with, either by accident or by intentional adversaries.

Achieving the appropriate functional safety, security, and reliability standards is not a trivial task, and it is ultimately one that significantly impacts the BOM of the overall system. The most significant impact to BOM cost is the requirement for physical separation of certain functional blocks, resulting in expensive multi-chip solutions. For functional safety and high reliability, physical separation is required both for redundancy and for separation of safe and "not safe" functions. For security, physical separation is required to ensure separation of encrypted and unencrypted data.

Xilinx offers a unique Isolation Design Flow (IDF) tool (available for all Cost-Optimized Portfolio families) that can be used to guarantee physical separation of functions within a single device. This substantially reduces the number of components required on the board. The BOM cost savings made possible by IDF is illustrated by the single-chip solution for a software-defined radio (SDR) application shown in Figure 7. IDF is one of the key enablers of this design model because it allows encrypted and non-encrypted functions to share the same device.
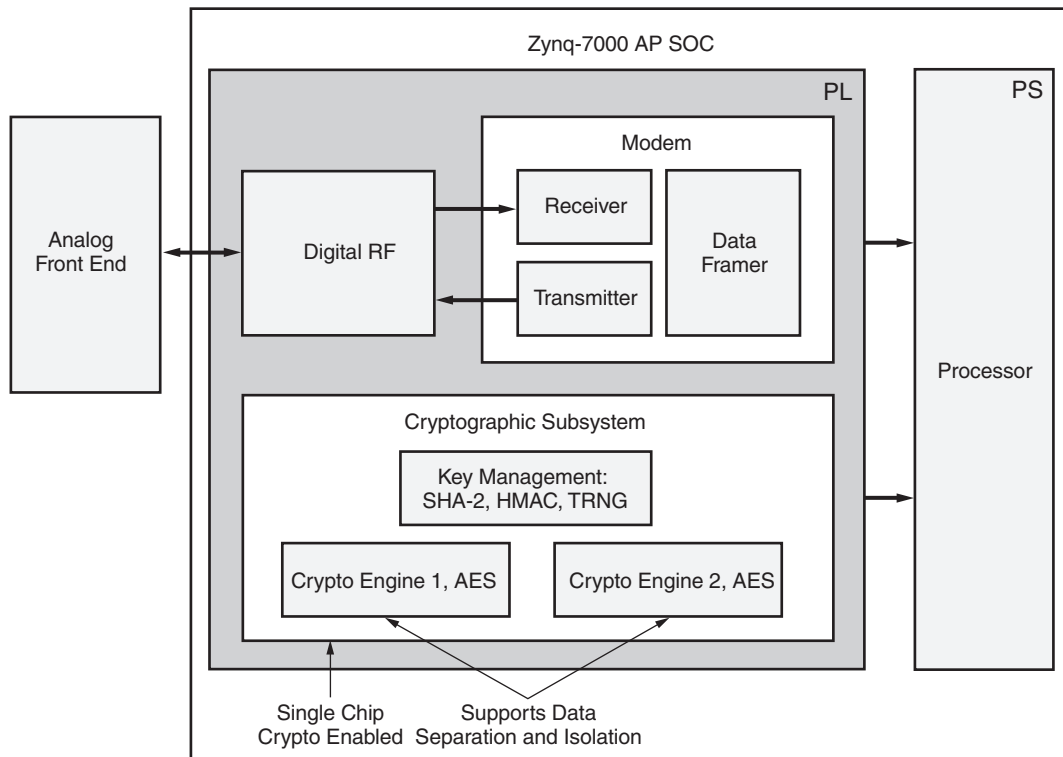
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Figure 7: **System Integration for Software-Defined Radio**

This tool has been approved for use by the National Security Agency of the United States in Type 1 Cryptographic Systems. IDF is also certified by TÜD SÜD as a "Software Tool for Safety Related Development" for ISO26262 and IEC61508, up to ASLID and SIL3 respectively. Additional details on IDF can be found in the Xilinx white paper *The Xilinx Isolation Design Flow for Fault-Tolerant Systems* [Ref 10] and in the Xilinx application note *Developing Secure and Reliable Single FPGA Designs with Xilinx 7 Series FPGAs or Zynq-7000 AP SoCs Using the Isolation Design Flow* [Ref 11].

Reducing Component Cost

Many components on the board make up the infrastructure that ensures the core system elements can perform to specification. Examples of these include components related to power delivery, thermal management, and both volatile and nonvolatile memory. The cost of these functions is often overlooked, resulting in higher BOM cost—and in lower system performance. However, careful FPGA or SoC selection can simplify these infrastructure requirements and provide the most cost-effective solutions.

Power and Thermal Management Components

Every device has unique power requirements (i.e., voltage levels, load currents, and number of rails), typically requiring a DC/DC conversion solution optimized for the device. The cost of such a power supply solution varies widely depending on a number of factors. The two main cost drivers that the integrated circuit device manufacturers can influence are:

- The number of unique power rails required by the device
- The amount of current sourced by each rail

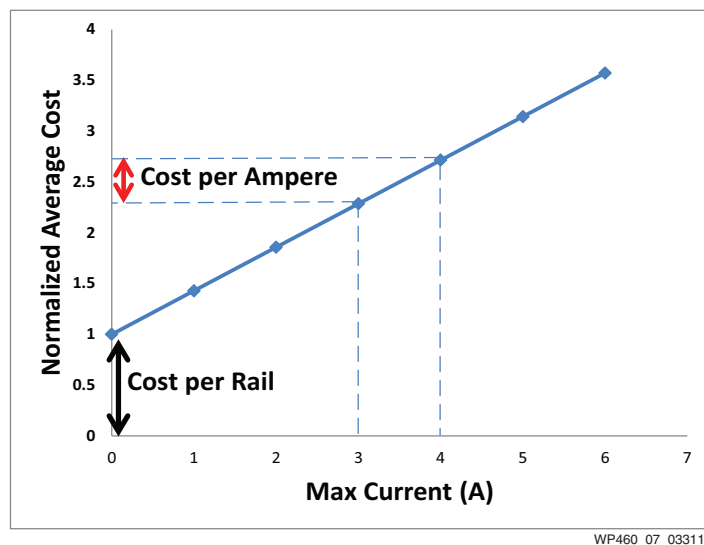The effect that these factors have on power supply solution costs is shown in Figure 8.

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Figure 8: **DC/DC Converter Cost**

Another key driver of power supply solution cost is the actual manufacturer/vendor and device chosen. Cost, efficiency, and PCB area requirements vary widely, so consideration needs to be given to finding the optimum solution for each system requirement.

Furthermore, the power dissipation of the system and the efficiency of the power conversion system directly impact thermal management requirements, which (depending on power dissipation needs) can range from nothing at all to an actively cooled system comprising large, expensive heat sinks and fans. In many instances (e.g., industrial motor control), expensive thermal management solutions are not an option for reasons of cost and reliability. Therefore, if a design cannot achieve certain power targets, it cannot proceed.

Number of Unique Power Rails

Integrated circuits typically require a number of unique power rails (e.g., 1.0V, 1.8V). Each of these rails requires a unique DC/DC converter. In some instances, different integrated circuits have the same requirements; therefore, the DC/DC converters can be shared between components. In the case of a programmable device, primary voltage requirements include those shown in Table 1.

Table 1: **Power Rail Requirements for a Typical Programmable Device**

Voltage Supply	Purpose
V_{CCINT}	Core logic (e.g., CLBs, DSP blocks)
V_{CCBRAM}	Block RAMs (normally shared with V_{CCINT})
V_{CCAUX}	Auxiliary logic (e.g., clock managers, configuration pins)
V_{CCO}	I/O banks
$MGTAV_{CC}$	Transceivers (analog)
$MGTAV_{TT}$	Transceiver termination circuits (analog)
$V_{CCINTPS}$	For processor subsystem (AP SoCs)

As illustrated in Figure 8, pricing of DC/DC converters has a fixed element, meaning that every unique rail in the system adds cost. Therefore, reducing the number of DC/DC converters on the board always has a reduction impact on the overall BOM cost. This is especially true when the current consumption of that rail is less than 2A, as the cost per rail dominates.

To help reduce the number of unique rails in the system, Xilinx minimizes the number of different rails required to power its devices. Where this is not possible, Xilinx uses rail voltages that are most likely to be already available in the system; alternatively, Xilinx strives to ensure that current requirements are low enough so that, in many instances, inexpensive linear regulators can be used.

This strategy was implemented in the Spartan-6 FPGA, whose power supply requirements are shown in Figure 9.

- For designers *not* using transceivers, only two rails are required, 1.1V and 2.5V:
  - In many instances, 2.5V is already being used in the system for other components; therefore, it can be shared.
  - In many other instances, the current requirement is so low that a low-cost linear regulator can be used to provide 2.5V power to the Spartan-6 device.
- If transceivers *are* to be used:
  - One additional 1.2V regulator is required. *Given the tight ripple requirements on $MGAV_{CC}$ and $MGAV_{TT}$, it is not recommended to share it with other components.*
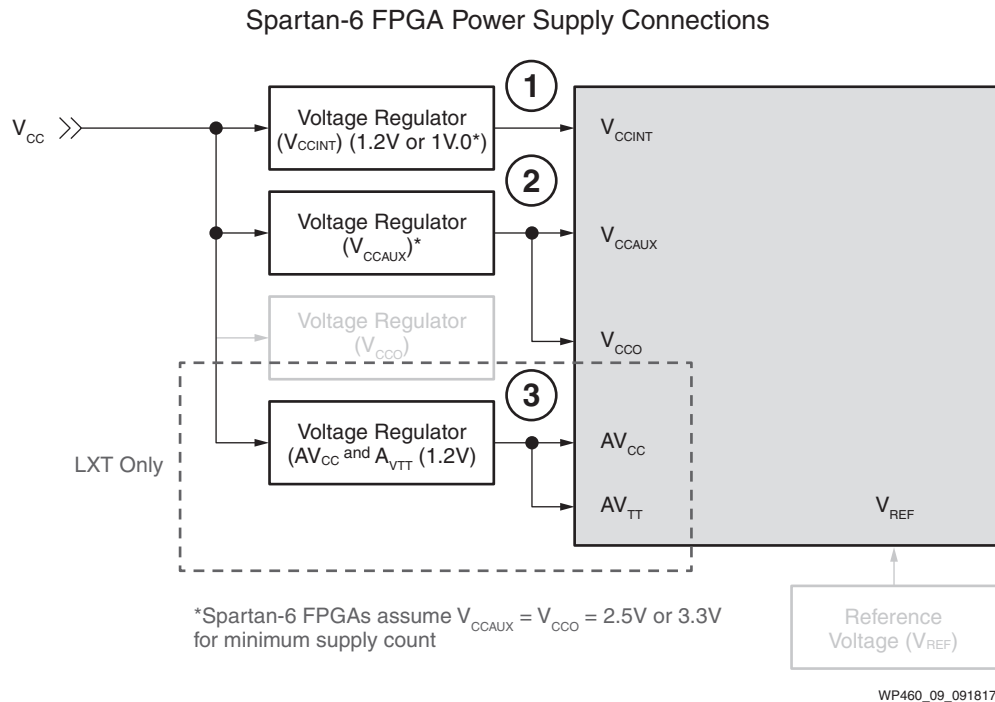
Spartan-6 FPGA Power Supply Connections

Figure 9: **Spartan-6 FPGA Power Supply Requirements**

In the case of Artix-7, Zynq-7000S, and Zynq-7000 devices—even for the lowest-power -1LI speed grade—the V_{CCINT} and V_{CCBRAM} voltages can be tied together and their voltage taken down to 0.95V. This eliminates the need for a unique voltage rail for V_{CCBRAM}.

Low Power Dissipation

Power is increasingly a key differentiator for the small-form-factor, high-performance space that requires tight thermal and power budgets. Through the combination of innovative product architectures and by leveraging the best foundry processes in the industry (such as the TSMC 28nm High Performance Low Power (HPL) process), Xilinx is able to deliver high performance with up to a 30% power savings, versus the nearest competitor, for all 28nm FPGA or AP SoCs. Refer to the Xilinx white paper *Lowering Power at 28nm with Xilinx 7 Series FPGAs* [Ref 12].

Architectural innovations include:

- Transceivers to granularly balance power and performance trade-offs
- Multi-mode I/O control to dynamically disable input and output buffers as needed during memory interface write, read, and idle states
- Intelligent clock gating of unused components
- Power binning and voltage scaling of screened parts for lower operating voltage

These power-saving features are shown in Figure 10.
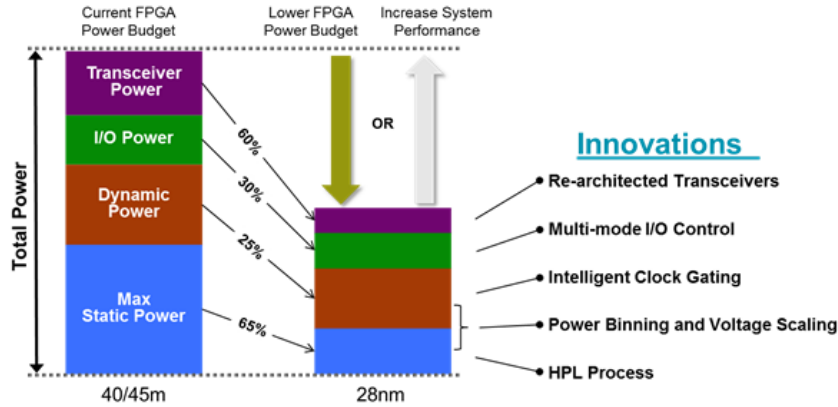
Figure 10: **Xilinx Power Reduction at 28nm v. Previous Generation**

While voltage scaling and the low-power device options are available for all Spartan-7, Artix-7, Kintex®-7, and Virtex®-7 FPGAs, as well as for Zynq-7000S and Zynq-7000 AP SoCs, cost-optimized devices in particular offer extensive voltage scaling options that reduce overall power by an additional 30% while retaining needed performance (see Figure 11 and Table 2).

This is made possible by the headroom (i.e., flexibility permitting performance and power trade-offs) gained with the 28nm HPL process. While normal operating voltage is 1.0V, low-end devices can offer a 0.95V option for -1 industrial speed grade (-1LI) devices while retaining identical performance.
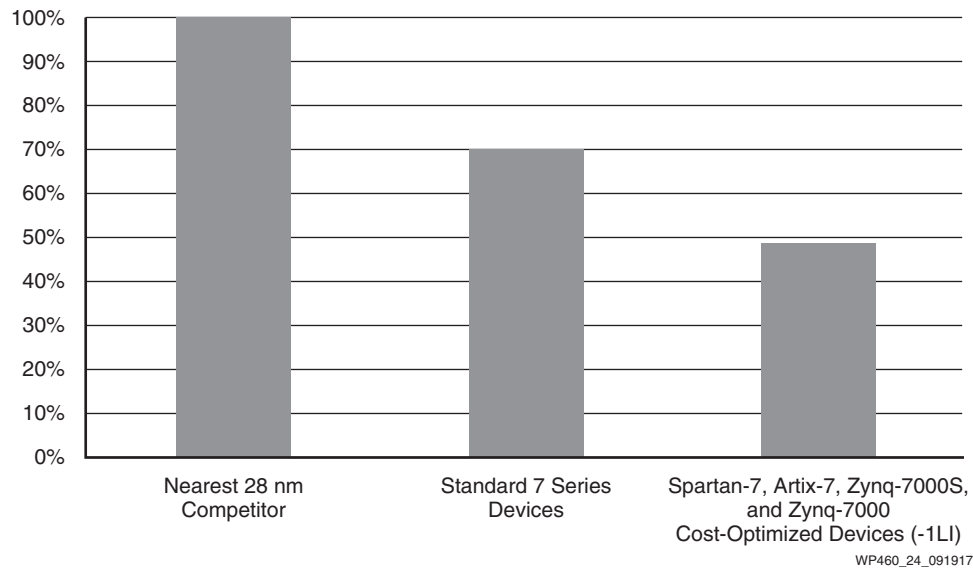
Figure 11: **Total Power Reduction with Voltage Scaling for Cost-Optimized Industrial-Grade Devices**

Table 2: **Additional ~20-30% Total Power Reduction with Voltage Scaling (-1LI)**

	V_{CCINT}[1]	Static Power Savings	Dynamic Power Savings
-1I, -2I	1.0V	0%	0%
Spartan-7 and Artix-7 -1LI	0.95V	50%	10%
Zynq-7000S and Zynq-7000 Cost-Optimized -1LI	0.95V	50%	10%
	1.0V[2]	45%	0%

Notes:

1. For Zynq-7000S and Zynq-7000 devices, voltage change is limited to programmable logic.
2. At 1.0V, one voltage rail can be used for both programmable logic and processor sub-system.

Given the dependency on DC/DC converter pricing for the amount of current being consumed by each power rail (see Figure 8), the substantial power savings offered by Xilinx devices reduces power supply cost.

In addition, the cost of the passive components (inductors, capacitors, etc.) required by the DC/DC converter vary greatly with their size, which in turn often tracks closely with the amount of current the device must be capable of handling. For example, using a power supply calculator [Ref 13] provided by one major vendor, the total cost of a 1.0V rail decreases 33% by reducing its maximum current rating from 3A to 2A. (In this example, the large cost differential is driven mainly by the cost of the inductor.)

Optimum Power Supply Solutions

The cost effectiveness of power supply solutions varies widely depending on the vendor and the specific device chosen. Xilinx partners with leading power supply vendors in the industry to meet diverse requirements at the most attractive price, with the smallest board area, and at maximal efficiency. In addition, given their broad view of complete system power requirements for various applications, power control vendors are in a unique position to be able to offer the best solutions.

The diverse range of use cases makes it difficult to create a one-size-fits-all solution. However, a number of highly integrated solutions offer compelling value for a vast array of end use cases. The Dialog DA9062 [Ref 14], Monolithic Power Systems MP5416 [Ref 15], Exar/MaxLinear XRP7714 [Ref 16], and Texas Instruments TPS65023 [Ref 17] are four such system power control devices that provide outstanding flexibility and performance while requiring minimal board space.

Solutions like these offer excellent value, as they provide a large number of rails that, in many instances, can provide a complete power supply solution for the entire system, not merely for the programmable device itself. In addition, they require only a small amount of board space and are routable on two layers. For more information on power delivery systems and solutions from Xilinx partners, go to https://www.xilinx.com/products/technology/power.html.

Configuration and Boot Memories

Programmable devices generally require nonvolatile storage, somewhere in the system, to hold the device programming information. This means system designers must factor in components to support the necessary storage.

Some programmable devices provide a limited amount of on-chip nonvolatile memory (NVM) for this purpose, but it forces use of older manufacturing process technologies to accommodate the needs of NVM fabrication. As a side effect, devices with on-chip NVM often cannot deliver the cost point, storage capacity, computational capability, or interface standards and rates, needed by many system designers.

Other programmable devices require use of proprietary companion NVM devices, forcing system designers into solutions that are often very expensive due to lack of competition.

Xilinx programmable devices hold their device programming information in SRAM, enabling use of advanced CMOS manufacturing process technologies. They can be programmed and re-programmed, in system, on demand, an unlimited number of times. With this SRAM-based architecture, Xilinx programmable devices are initialized when power is applied. For FPGAs, this initialization is named configuration, and for AP SoCs, this initialization is named boot. A variety of configuration or boot modes allow system designers to optimize for a desired figure of merit, including cost.

All devices in the Xilinx Cost-Optimized Portfolio support autonomous configuration or boot from commodity NVM devices, including serial NOR flash. Serial NOR flash, sometimes referred to as QSPI, based on its Quad I/O Serial Peripheral Interface, provides a component cost advantage in addition to PCB cost savings from a small footprint and simple interface. The Vivado Design Suite even enables convenient, no-cost, low volume R&D programming of several brands of serial NOR flash as listed in *Vivado Design Suite User Guide: Programming and Debugging* [Ref 18].

The range of interoperable serial NOR flash for boot or configuration is far wider than suggested in the user guide [Ref 18]. To capitalize on the full advantages of serial NOR flash as a commodity product, Xilinx recommends drawing from the list of serial NOR flash in the user guide [Ref 18] while basing the package selection on cross-vendor flexibility.

This approach facilitates seamless bring-up, prototyping, and development in a research and development environment, with a direct path to production. Additionally, it provides a framework to validate the possibility of additional cost reduction for production, by using pre-programmed interoperable serial NOR flash, in the same package but from other vendors, regardless of their inclusion in the user guide [Ref 18]. For the basic interoperability requirements of serial NOR flash with:

- Spartan-6 FPGAs, see *Spartan-6 FPGA Configuration User Guide* [Ref 19]

- Spartan-7 FPGAs and Artix-7 FPGAs, see *7 Series FPGAs Configuration User Guide* [Ref 20]

- Zynq-7000 and Zynq-7000S AP SoCs, see *Zynq-7000 All Programmable SoC Technical Reference Manual* [Ref 21]

Systems consisting specifically of FPGAs from the Xilinx Cost-Optimized Portfolio and other active components can provide opportunities to reduce cost by merging multiple NVMs into a single

shared NVM. This is accomplished by using one of the other active components to forward programming information from the NVM to the FPGAs in slave serial configuration mode. For more information on this approach, see Xilinx application note *Using a Microprocessor to Configure 7 Series FPGAs via Slave Serial or Slave SelectMAP Mode* [Ref 22].

Volatile Memory

Xilinx's cost-optimized devices contain a significant amount of integrated memory in the form of block RAM, distributed RAM, processor caches, and processing system on-chip memory (OCM). In many cases, the memory available within the device, either directly or via innovative methods [Ref 23], is sufficient for runtime code and data storage, therefore eliminating the need for off-chip dynamic memory devices like SDRAM. As a specific example, Zynq-7000S and Zynq-7000 devices have 512KB of L2 cache and 256KB of OCM into which code and data can be pre-loaded and locked. Depending on the configuration or boot mode, and system performance requirements, it can also be feasible to execute-in-place (XIP) directly from NVM.

However, a number of applications require additional external memory (e.g., frame buffering in video processing applications). System designers must factor in the cost of these external memories for the entire product life cycle. Xilinx supports DDR3 SDRAM across its complete Cost-Optimized Portfolio, including the Spartan-6 family. DDR3 is currently the lowest cost per Mb/s option, and is likely to continue to be for the foreseeable future [Ref 24].

Ensuring the Smallest, Lowest-Cost Programmable Device

High Utilization

One of the primary criteria when selecting a programmable solution is device density. Designers naturally want the smallest, lowest-cost device possible for their applications. Historically, the challenge with programmable solutions is maximizing utilization of logic resources for any given design without sacrificing performance. By nature of traditional architectures and implementation tools, imperfect design packing is inevitable, leading to significantly less than 100% utilization and potential performance degradation.

Starting with the 28nm families, Xilinx leveraged its next-generation design environment, the Vivado® Design Suite, to ensure maximum device utilization and performance from its silicon architectures. With the tool's hierarchical implementation and analytical engine, Xilinx cost-optimized 28 nm devices can deliver the following advantages over the competition:

- A full speed grade of performance improvement

- 20% better device utilization

The Vivado Design Suite realizes the potential of a device's programmable logic fabric and dedicated on-chip functional blocks through architecture and software integration to yield maximally efficient results. The speed grade and utilization improvements directly impact the cost of the device because smaller, lower-speed-grade devices can be used to perform the same task.

Partial Reconfiguration

Xilinx partial reconfiguration extends the inherent flexibility of the programmable logic by allowing specific regions of the device to be reprogrammed with new functionality while applications continue to run uninterrupted in other regions. In many designs, there can be a number of mutually exclusive functions. Partial reconfiguration can be used to configure the programmable logic with only the functions that are required at that particular instance in time. Examples of this are illustrated in the Xilinx application note *Partial Reconfiguration of a Hardware Accelerator on Zynq-7000 All Programmable SoC Devices* (ISE® tools) [Ref 25] and Xilinx user guide *Zynq-7000 All Programmable SoC ZC702 Base Targeted Reference Design* (Vivado tools) [Ref 26].

Partial reconfiguration offers unique benefits from a BOM cost perspective because it has the potential to substantially reduce the device density requirement and power consumption of the design. Machine vision and camera-based advanced driver assistance applications can time-multiplex stages of their video pipelines through cyclic partial reconfiguration to reduce cost. On-demand partial reconfiguration gives applications such as software defined radio the ability to support a library of current and yet-to-be-developed modulation standards—not only reducing cost but also increasing system value and longevity through field update capability.

Reducing Printed Circuit Board (PCB) Costs

In the absence of adequate care, attention, and planning, the cost of the PCB can become a significant part of the overall system cost. The key drivers for PCB cost are the number of layers required, the size of the board, the need for cutting-edge PCB technology like laser vias and fine trace widths, through-hole component use, and single vs. double-sided component assembly.

Reducing PCB Layers with Innovative Packaging Solutions

Innovative packaging in Xilinx's Cost-Optimized Portfolio products ensures that the lowest-cost PCB solution can be found. To support system designers, Xilinx provides guidance on common PCB routing scenarios such as in Xilinx white paper *DDR2/DDR3 Low-Cost PCB Design Guidelines for Artix-7 and Spartan-7 FPGAs* [Ref 27].

An excellent example of innovative packaging is the Artix-7 FPGA CPG236 package. The package itself is a 10x10mm, 0.5mm pitch BGA, with more than 100 usable I/Os. In general, routing to a 10x10mm, 0.5mm pitch BGA requires many PCB layers and the use of fine-geometry design rules. However, the innovative ball-grid pattern allows all of the balls to be routed on only two layers using standard spacing and via sizes. For Spartan-7 FPGAs, eight of the sixteen packages can be routed in four or fewer layers.

Board Area Reduction via System Integration

PCB costs are also substantially reduced by system integration, choice of an optimum power supply and distribution method, component size, and so forth—because they all affect the size of the PCB as well as the level of interconnect required. This can directly affect the number of PCB layers required, which in itself a huge cost factor.

BOM Cost Savings in End Applications

To further illustrate the system BOM cost savings possible in end applications with Xilinx's cost-optimized product families, a number of typical application examples have been analyzed from a system BOM cost perspective relative to competing implementations.

Sensor Interface with Artix-7 Devices

A range of end markets, e.g., industrial process control and in-service monitoring systems in large mechanical equipment, use FPGAs such as the Artix-7 XC7A35T device to aggregate and process sensor data and transmit critical information to a central host. The type of sensors used can vary widely depending on the application, but can include temperature, pressure, strain, position, and vibration sensors.

The block diagrams shown in Figure 12 illustrate how Artix-7 FPGAs provide integration advantages that drive system BOM cost reduction in sensor interface applications versus competing FPGAs.
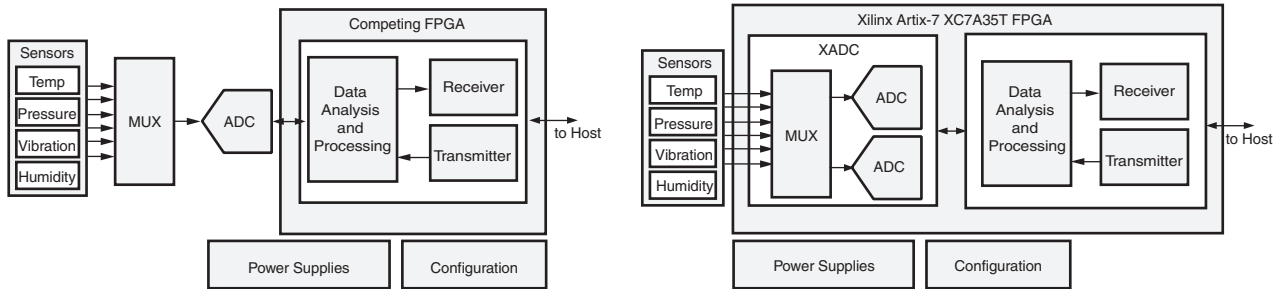
WP460_12_092017

Figure 12: **Sensor Interface, Competing FPGA vs. Artix-7 FPGA**

Figure 13 illustrates that the Xilinx Artix-7 FPGA solution provides a BOM cost saving of up to 30%, relative to the most comparable competitive FPGA. These savings are realized by leveraging the Artix-7 FPGA's lower-power, two-layer PCB routing that is made possible by its 10x10mm BGA connection technology. Additionally, the Artix-7 device works with inexpensive off-the-shelf configuration devices, and features a fully integrated, on-chip Xilinx analog-to-digital converter (XADC).
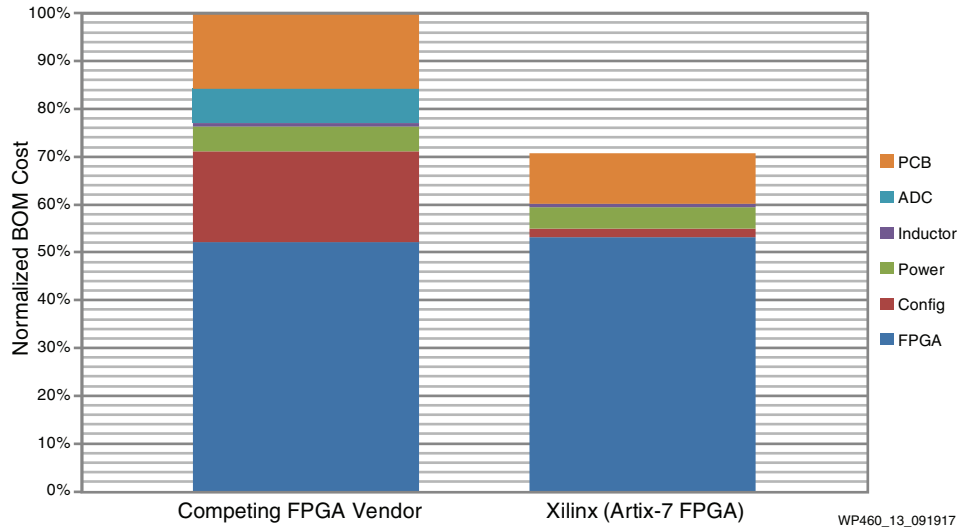
Figure 13: **Sensor Interface BOM Cost Savings**

Machine Vision with Spartan-7 Devices

Machine vision cameras are another common application niche for low-end FPGAs. Devices, such as the Spartan-7 XC7S50 FPGA, interface with an image sensor, perform complex image signal processing, implement custom IP, and transmit the recovered data to a central controller by way of various communications protocols.

Some competing FPGAs, especially those manufactured in larger process geometries like embedded 55nm, simply cannot perform the necessary processing required by this application. One resolution is to use an additional ASSP or DSP to perform the processing. However, a better option is a single, higher-performance device like a Spartan-7 FPGA. The block diagrams shown in Figure 14 illustrate how Spartan-7 FPGAs provide integration advantages driving system BOM cost reduction in machine vision applications versus competing solutions.
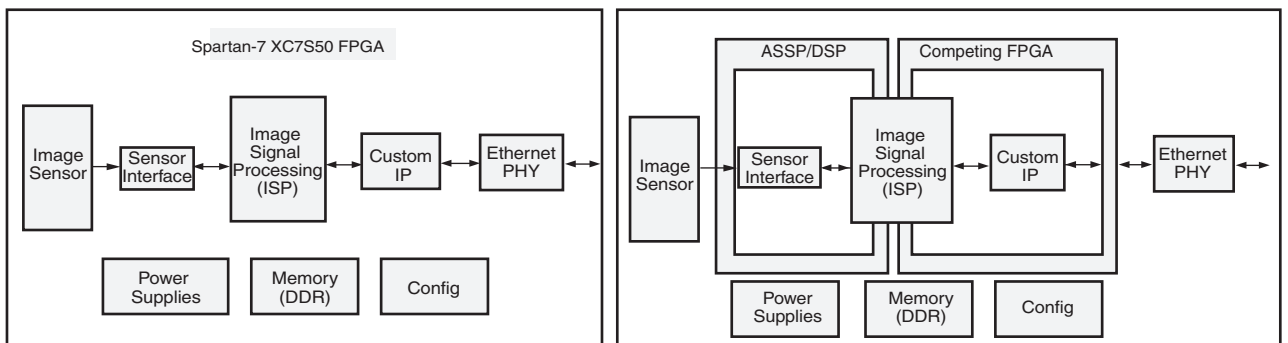
Figure 14: **Machine Vision with Spartan-7 FPGA**

As can be seen from Figure 15, highly significant BOM cost savings (up to 34%) can be realized by choosing the higher-performance Spartan-7 device, when compared to low-performance alternatives that require additional ASSP/DSP functionality to perform the complex image processing required of this application.
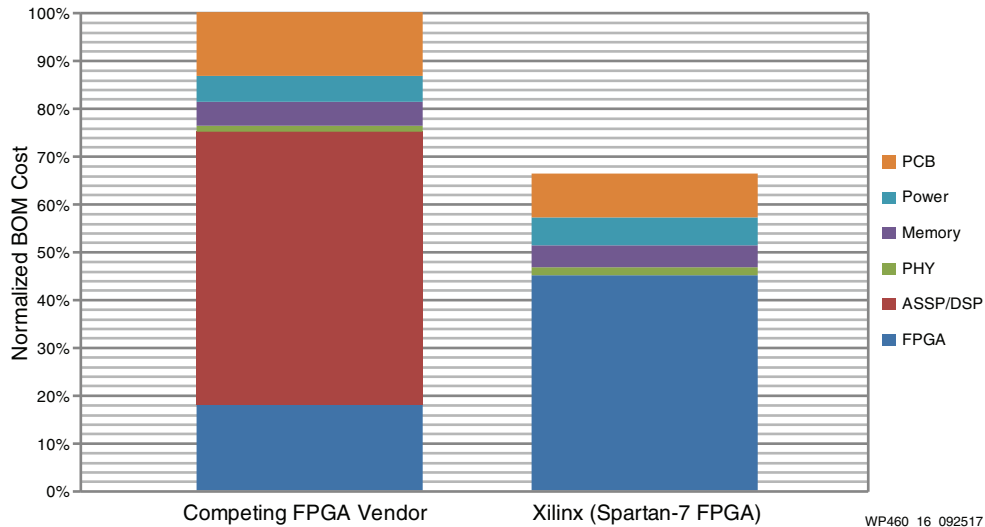
Figure 15: **Machine Vision BOM Cost Comparison**

Integrated Programmable Logic Controller (PLC) Using Zynq-7000 AP SoC

A common application for Xilinx Zynq-7000S and Zynq-7000 is for PLC, e.g., in a motion-control system. A typical block diagram is shown in Figure 16.
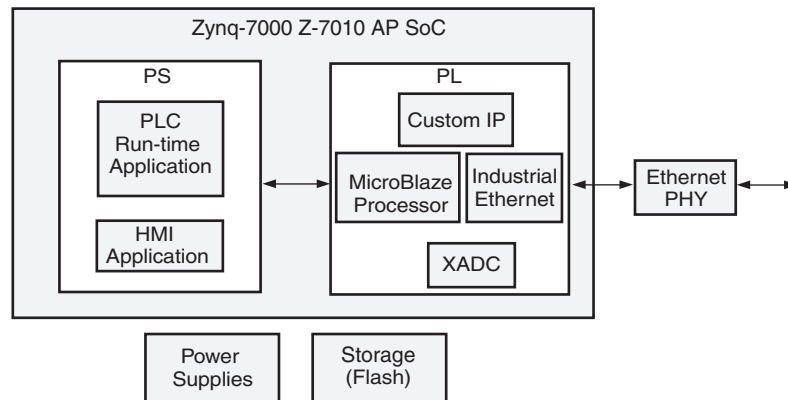
Figure 16: **Block Diagram of Motor Drive Using Zynq-7000 AP SoC**

Figure 17 shows that Xilinx is able to realize up to 23% BOM cost saving relative to its nearest competition for this PLC application. This saving is realized by leveraging the Zynq-7000 AP SoC's larger OCM capacity, as well as its XADC and PCB area savings.
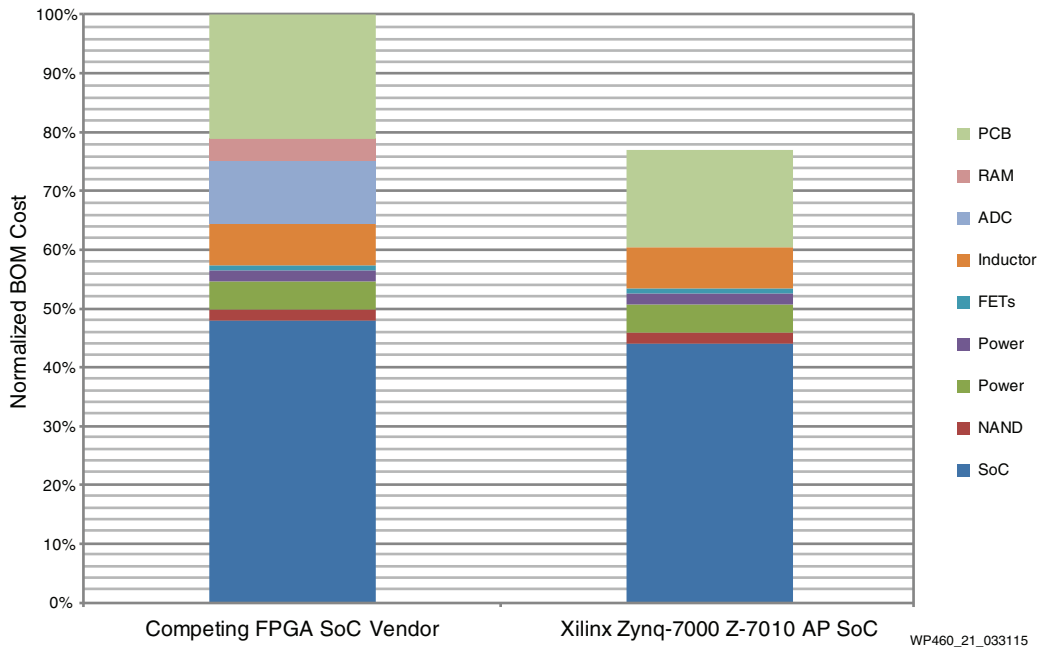
Figure 17: **Motor Drive BOM Cost Savings: Competitive SoC vs. Xilinx Zynq-7000 AP SoC**

Conclusion

When opting for a high-value component like an FPGA or AP SoC, designers must look beyond component unit cost to instead consider its overall impact on total BOM cost.

Xilinx's Cost-Optimized Portfolio solutions can impact cost savings across major system design categories, including processor elements and peripherals, power supplies, analog mixed signal components, safety and security components, memories, and PCB boards, among others. Enabled by four diverse families, the Xilinx Cost-Optimized Portfolio adds a new perspective to system cost analysis and offers unique solutions to overall system cost reduction.

For additional details on the Xilinx All Programmable Cost-Optimized Portfolio, visit the Xilinx website [Ref 28].

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28. Xilinx website, All Programmable Low-End Portfolio.

29. Xilinx website, Eclipse-based Software Development Kit

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
01/26/2018	1.2	Updated MicroBlaze IP Core Processors.
10/03/2017	1.1	Updated title; abstract; Introduction; Cost-Optimized Portfolio Overview; Figure 1; Figure 2; MicroBlaze IP Core Processors; Figure 4; Figure 6; Figure 8; Figure 10; Table 2; Optimum Power Supply Solutions; Configuration and Boot Memories; Volatile Memory; Partial Reconfiguration; Reducing PCB Layers with Innovative Packaging Solutions; Sensor Interface with Artix-7 Devices; Figure 11; Machine Vision with Spartan-7 Devices; Figure 14, and References. Added: Clocking Integration. Removed: Industrial Ethernet for Motor Control Using a Spartan-6 FPGA.
03/31/2015	1.0	Initial Xilinx release.

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