



WP465 (v1.0) November 20, 2015

Meeting Embedded HMI Requirements Using Zynq-7000 High-Performance All Programmable SoCs

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The Xilinx® Zynq®-7000 All Programmable SoC, running the Xylon graphics engine IP, accelerates product development and enables HMI designers to focus on their primary market differentiators.

ABSTRACT

Highly integrated SoCs using Zynq-7000 All Programmable SoC (AP SoC) technology can be complemented with a highly efficient, scalable human machine interface (HMI) solution for industrial, scientific, and medical applications. Together with Xilinx ecosystem partner Xylon, scalable differentiated platforms can be produced that provide superior HMI integration when compared to typical ASSP implementations.

The overall performance achievable by Zynq-7000 AP SoC-based HMI solutions is also examined and described.

Using Xilinx Zynq-7000 AP SoCs, this highly scalable integration of hardware, software, and system solutions allows HMI designers to produce a proven HMI solution at an accelerated pace while focusing on their primary mission: to produce optimally differentiated products that support a long marketplace lifetime.

Introduction

The Xilinx Zynq-7000 AP SoC is a powerful combination of programmable logic (PL) and a feature-rich dual-core ARM® Cortex™-A9 based processing system (PS) tightly integrated on a single device. It enables system designers to create more intelligent, more flexible, more highly integrated embedded systems. The Zynq-7000 AP SoC has applications in scientific, medical, industrial, and automotive systems, efficiently fulfilling both technical and business goals. Typical product lifetimes exceed ten years.

Hardware accelerator cores designed for specific applications can be implemented in the programmable logic (PL) section of the Zynq-7000 AP SoC. The custom software resident in the processing system (PS) runs this integrated PL hardware, which also offers a set of dedicated standard I/O peripherals. By offloading CPU-based tasks to hardware accelerators implemented in the PL, system designers can realize single-device SoC implementations that exceed the performance of existing competitive solutions. This ability provides a much higher level of integration and power savings.

From a business perspective, the Xilinx Zynq-7000 AP SoC provides a cost-effective technology platform offering many opportunities for increasing efficiency and reducing cost. Easily realized product differentiation and flexibility supports platform-based system designs that can be readily adapted to future changes and upgrades. In turn, this results in faster time to market, diminished risk of obsolescence, and a significant decrease in the overall cost of development over the product's lifetime.

Many embedded systems need an integrated visual HMI to display real-time information about the processes under PL control, providing high-level interactivity between the human operator and the machine. Development "from scratch" of a powerful, extensible PL-based graphics controller/accelerator is a daunting, time-consuming task; thus, a cost-effective, optimized HMI solution is highly advantageous for the Zynq-7000 AP SoC.

Pressure to create more differentiated products while shortening development time is driving designers to use off-the-shelf third-party IP cores and software. The Zynq-7000 AP SoC ecosystem provides proven software, hardware, and system solutions that greatly accelerate product development. This white paper explains how to use graphics logicBRICKS™ IP cores from Xilinx Alliance Program premier member Xylon to quickly design scalable, customizable HMIs that seamlessly integrate with the user's application implemented in the Zynq-7000 AP SoC.

By using pre-verified, quality-optimized graphics solutions that scale according to system needs and provide industry-standard software APIs, HMI designers can significantly shorten their design cycle and fully concentrate on their primary differentiators by leveraging the highly adaptable Zynq-7000 AP SoC platform to meet their needs.

Market Trends

An ever-growing number of industrial, scientific, and medical applications use graphical I/O HMIs. Here are just a few examples of products and processes that can benefit from incorporating this technology:

Products:

- Operator panels for highly productive Computer Numerical Control (CNC) machines
- Ultra-high resolution cameras and monitors in medical diagnostic applications
- Portable diagnostics devices
- Scientific measurement handhelds
- Industrial detection handhelds

Processes:

- Increased machinery processing speed
- Farm livestock management best practices that result in greater efficiency and less loss
- Sensing technologies requiring innovative, compute-intensive control algorithms
- Contactless video factory quality control (a [Smarter Vision](#) application)
- Sensor fusion applications (combining data from multiple sensors on a single I/O line)

In short, integrated HMI technology enables systems to include more intelligence, higher-precision control, and greater flexibility.

HMI is the main interface between the human operator and the embedded device under control. It must assure reliable real-time system control by handling the networking/interfacing with (a) diverse distributed intelligent controllers and sensors, and (b) with a visual interface that displays real-time information about the processes under real-time control. HMI also must enable an operator to reliably interact with the embedded system in intuitive ways, and to control it by using input devices (e.g., touch-screens, pushbuttons, or keyboards).

The graphics engine requirements for HMI are increasingly becoming more demanding. In the past, embedded system HMIs typically supported simple 2D graphics or no graphics at all. Gray-scale or blue-scale “color” schemes predominated, using high-contrast boundaries to signal alert conditions. Needless to say, it is difficult to effectively display large quantities of information on small LCD displays of this type.

Today, potential HMI operators are already accustomed to using interactive, high-density GUIs because of the explosive growth of smartphones and tablets that implement them. Low-resolution HMI displays are being replaced with full-color displays that can produce screen resolutions higher than full HD (1080p), and it is not uncommon to see Ultra HD (4K2K) or Super Hi-Vision (8K4K) monitors in medical diagnostics or surgery rooms and on factory floors. Additionally, many industrial and medical applications now require support for *multiple* displays, in an effort to preclude the operator inefficiencies associated with forcing the crowded display of too much disparate system information on one screen.

Legacy industrial and medical systems used to be designed to run either a proprietary, special-purpose operating system (OS), of which a great diversity existed at one time—or to run without any OS at all (“bare metal” hardware-based control). Modern HMI embedded systems run the most popular operating systems, like Microsoft Windows Embedded Compact, Linux, Android, or QNX. This evolution, in turn, has triggered a growing industry trend: multiple processors in Asymmetrical Multi-Processing (AMP) configuration, which combines bare metal or RTOS operational control (thus shortening control loops and maintaining control determinism) with a separated full OS dedicated to supporting advanced networking protocols and high-end HMI graphics.

Additionally, HMI technology is increasingly offering special features to support requirements such as live video streaming, voice and gesture recognition, mass storage interfacing, and multi-point touch screen interaction.

Design Challenges and Design Alternatives

Versatile and often mutually exclusive industrial and medical HMI requirements set challenges that design teams face more often now than ever before. More demanding intelligent features now require processing power that often exceeds the performance availability of traditionally used ASSP silicon devices. As a result, today’s embedded products must be designed with more flexible interfaces and more intuitive, visually appealing HMI functions. These requirements are in addition to the need to shrink the physical footprint, shorten the BOM, lower the consumption of power, and reduce cost.

Manufacturers of ASSPs for embedded HMI applications try to find an ideal balance of the processing system and peripherals, and to make SoCs with different mixes of processors, I/Os, bus interfaces, and hardware accelerators needed for a specific industrial or medical application. It is impossible to anticipate all future application requirements—and then fit the ASSP to conform to all of them. While having all necessary features in a single device would be too expensive and impractical for use across HMI product families, building new ASSPs for traditionally low-volume markets is also economically challenging and unfeasible.

Therefore, highly integrated modern HMI products are most likely to be multi-chip based platforms. The HMI ASSP provides the processing power, graphics engine, most common I/O peripherals, and a number of application-specific hardware accelerators such as DSP blocks. Then, one or more companion devices fill the functional “holes” on the ASSP. Customized chipsets that support the missing features and provide for some anticipated system expansion provide a certain level of flexibility—yet just *one* unanticipated, unsupported new requirement can exceed the flexibility margin and lead to a costly, time-consuming, full system redesign, refabrication, and revalidation.

Because ASSPs are fixed-featured, they allow for product differentiation only at the software level. To hedge against the innate limitations of ASSPs, a growing number of industrial, scientific, and medical HMI systems now incorporate *companion FPGAs* to provide insurance against unanticipated demand for more intelligence and feature flexibility. This is illustrated in [Figure 1](#).

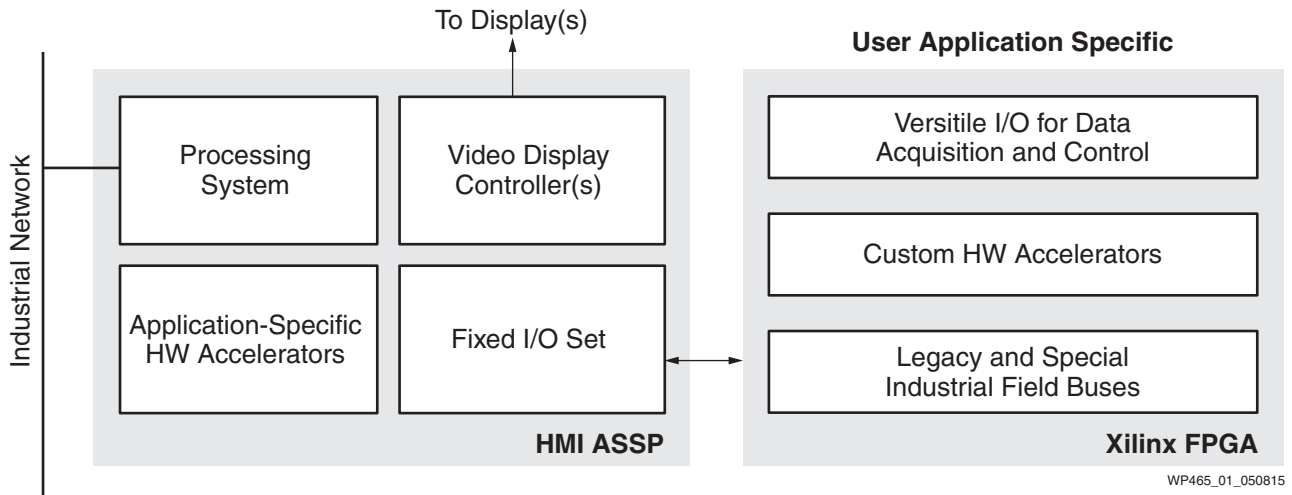


Figure 1: Embedded HMI Architecture with Xilinx Companion FPGA

Programmable FPGA I/Os allow for easy connection to vast numbers and types of sensors. These range from simple digital inputs and outputs to more complex industrial linear and angle positioning sensors, wireless devices, multiple video cameras and displays, and industrial field buses such as EtherCAT, PROFINET, EPL, SERCOS, and EtherNet/IP, among others.

Besides providing simple sensory data acquisition and interconnections, the companion FPGA significantly increases the computing power of the embedded HMI system, executing compute-intensive algorithms in carefully optimized FPGA logic hardware. Additionally, the companion FPGA can pre-process all the I/O data coming in from a large number of sensors before passing it to the ASSP in a format that it can process much more quickly. Adding these simple support functions can make a huge difference in the operational speed of the entire system.

The Xilinx Zynq-7000 All Programmable SoC family, with its combination of programmable logic and a feature-rich dual-core ARM Cortex-A9 based processing system, offers all the benefits of the ASSP+FPGA combination shown in Figure 1 and enables integration of all required HMI features into a single device, as shown in Figure 2.

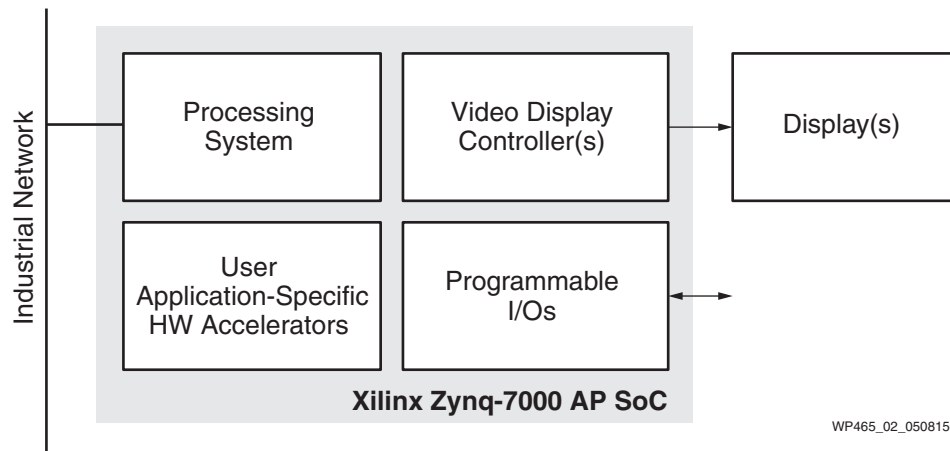


Figure 2: Xilinx Zynq-7000 AP SoC-Based Embedded HMI Architecture

Aside from the obvious influence on the system's BOM and the physical size, the tight on-chip integration of the processors with the programmable logic actually generates much higher synergy and outperforms ASSP+FPGA combinations in several ways.

Deeply embedded interfaces between the PS and the PL provide enormous bandwidths in comparison to any external chip-to-chip communications (buses). This can increase the system performance by boosting computing performance, decreasing latencies in data processing, and shortening the control loops. The Zynq-7000 AP SoC enables architectures that support precise system tasks partitioning between hardware and software. Removal of chip-to-chip buses generates significant power savings due to less radiated heat and the removal of power-hungry I/O connections. This reduces or eliminates EMI, making system design much easier and ultimately increasing system reliability.

Besides a large number of user programmable digital I/Os, the Zynq-7000 AP SoC incorporates analog mixed signal (AMS) general-purpose analog interfaces to support direct monitoring of analog inputs at a sample rate of 1MSPS. System-level housekeeping functions like power monitoring, thermal management, and control of the integrated resistive touch-screen are additional integration features for HMIs.

System designers can then differentiate their products in the market by implementing multiple specific hardware accelerators in the PL to support key features and to enable real-time control typically out of reach to any software-oriented controller. By changing only application-specific SoC parts and re-using large portions of the SoC design—the software code, graphics HMI, and networking—system designers can quickly design the whole line-up of HMI products for different applications as part of a common platform. Previously unseen options for this platform-based approach can shorten time to market and decrease non-recurring engineering (NRE) costs.

Depending on the application's complexity and the number of system tasks running on the processing system and hardware accelerators, the size and cost of the chosen Zynq-7000 AP SoC can be easily scaled up or down, due to assured pinout compatibility throughout the Zynq-7000 product family.

Many embedded HMI applications have lifetime requirements in excess of ten years. This could certainly cause competitive silicon component manufacturers to struggle to provide that much longevity in the face of the constantly escalating demand for the next generation of technology and features. System architects can be forced to create full redesigns midway through the life cycle of the product, which is enormously expensive and time-consuming. With Xilinx products like the Zynq-7000 AP SoC, however, the customer is choosing a solution with an *inherently long lifetime* because of the easy migration it provides to next-generation features and technology.

Integrating the Graphics Engine in the Zynq-7000 SoC

The primary drivers for use of the Xilinx Zynq-7000 AP SoC in HMI systems are application-specific hardware accelerators that leverage the capabilities of the industry's first All Programmable SoC, differentiating the HMI solution from others available on the market. The industrial HMI design example shown in [Figure 3](#) illustrates how easily system designers can integrate the powerful Xylon logicBRICKS graphics engine with custom-designed hardware accelerators.

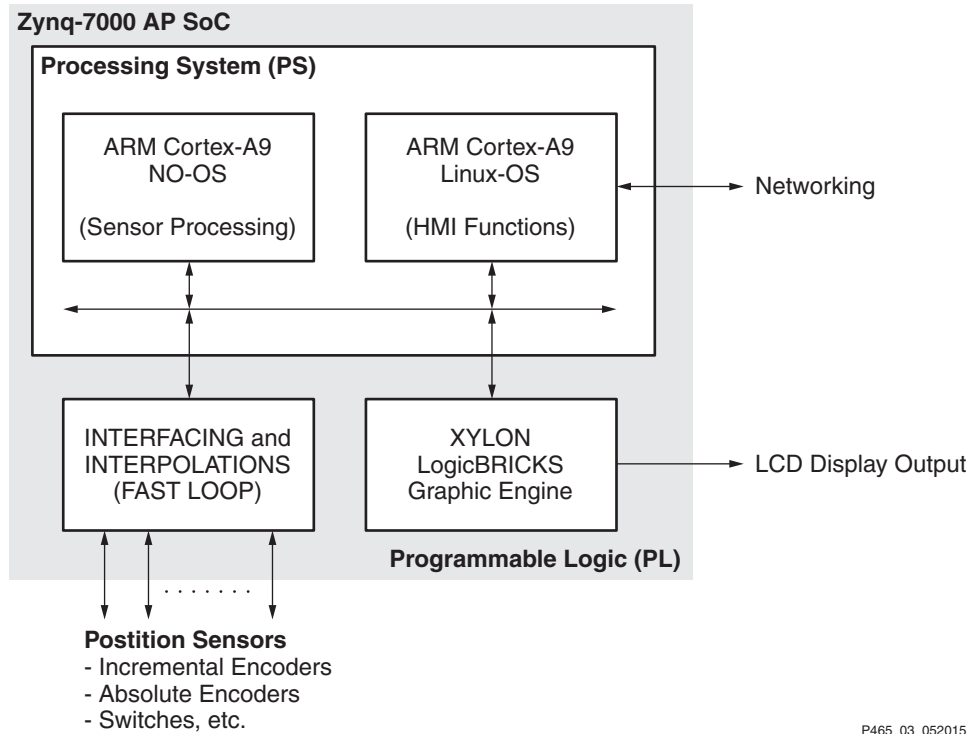


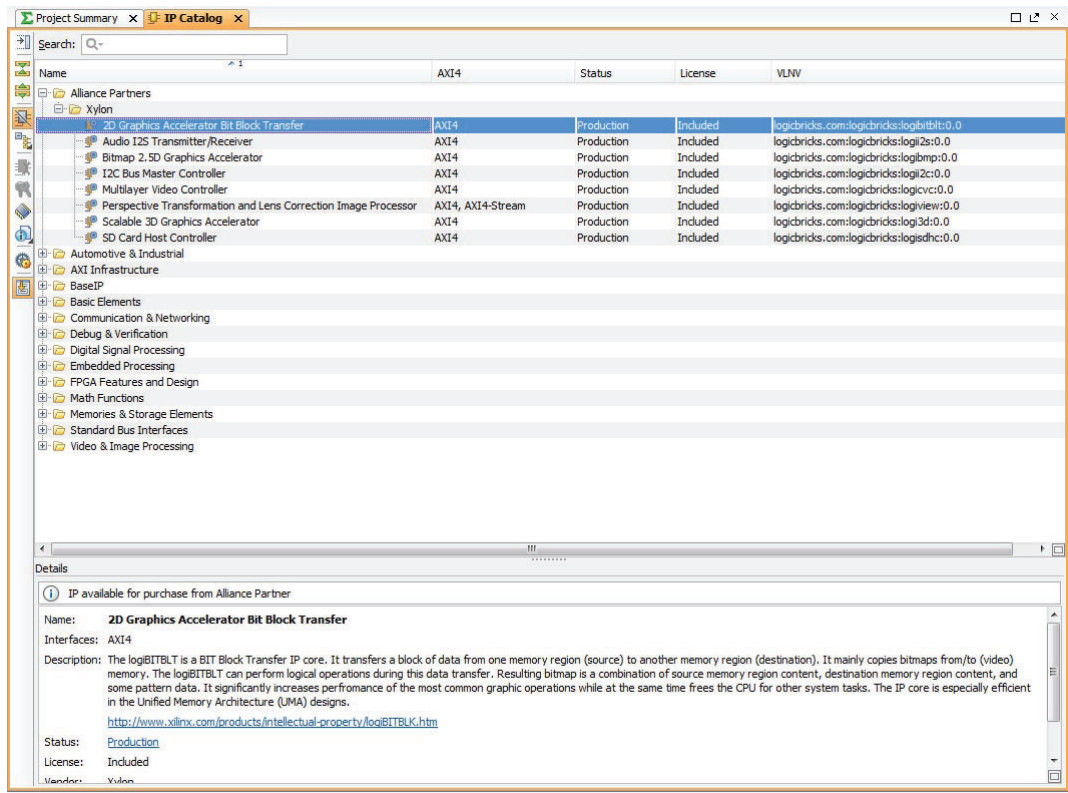
Figure 3: Example Industrial Application: High-Performance Digital Readout HMI

Digital readouts are required to interface with numerous positional sensors, e.g., linear encoders, incremental or absolute encoders, angle positioners, and digital switches, and to show measured values that allow the operator to control the device through a number of menus on the embedded LCD display. Today's highly efficient CNC machines incorporate actuators that move very quickly and precisely to assure required production speed and accuracy. The inputs from positioning sensors must be processed in very fast control loops that cannot be closed by software; the required speed and accuracy can be achieved only by customized hardware accelerators. This carefully designed hardware must capture sensor data and process it through various interpolation algorithms to determine the exact positions of a moving machine's actuators.

A long-term Xilinx Alliance Program premier member, Xylon offers a line-up of 2D and 3D graphics and video processing IP cores that can be quickly turned into fully customizable 2D and 3D graphics engines optimized for Xilinx All Programmable devices. Xylon's graphics IP cores are available in the IP library called logicBRICKS, and offer all key advantages that users require in IP cores. Pre-verified and validated logicBRICKS IP cores are packaged for Xilinx ISE® and Vivado® Design Suites (shown in Figure 4) and require no expertise beyond knowledge of general Xilinx tools. They can be used in the same ways as Xilinx LogiCORE™ and SmartCORE™ IP cores. This compatibility enables designers to implement graphics engines by one or more graphic logicBRICKS IP cores, in the shortest possible time and with the lowest risk.

Highly optimized and meticulously designed to give maximum performance in the smallest possible size, logicBRICKS IP blocks can be additionally tuned through tools configuration menus. Depending on the HMI graphics needs, designers can select only the needed graphic features, then downscale or upscale the graphics engine as needed. The design size can extend from that of a small, efficient display controller using a small fraction of the logic fabric available in the smallest

Zynq-7000 device (Z-7010), up to that of a full multi-layer HD display controller supporting complex 2D and 3D graphics operations.



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Figure 4: Xylon logicBRICKS IP Cores Viewed in the Xilinx Vivado IP Catalog

One of the most important criteria in selecting IP cores is software support. Xylon provides extensive software support of logicBRICKS IP cores that provide plug-and-play compatibility with popular operating systems, as well as in no-OS “bare-metal” designs. The provided software drivers and related middleware enable software designers to use a logicBRICKS graphics engine within familiar Xilinx design environments, requiring no knowledge about the underlying hardware.

Table 1 lists the software drivers, APIs, libraries, and application frameworks provided and supported by Xylon. Information about specific software drivers can be found at <http://www.logicbricks.com/Products/Software-Drivers.aspx>.

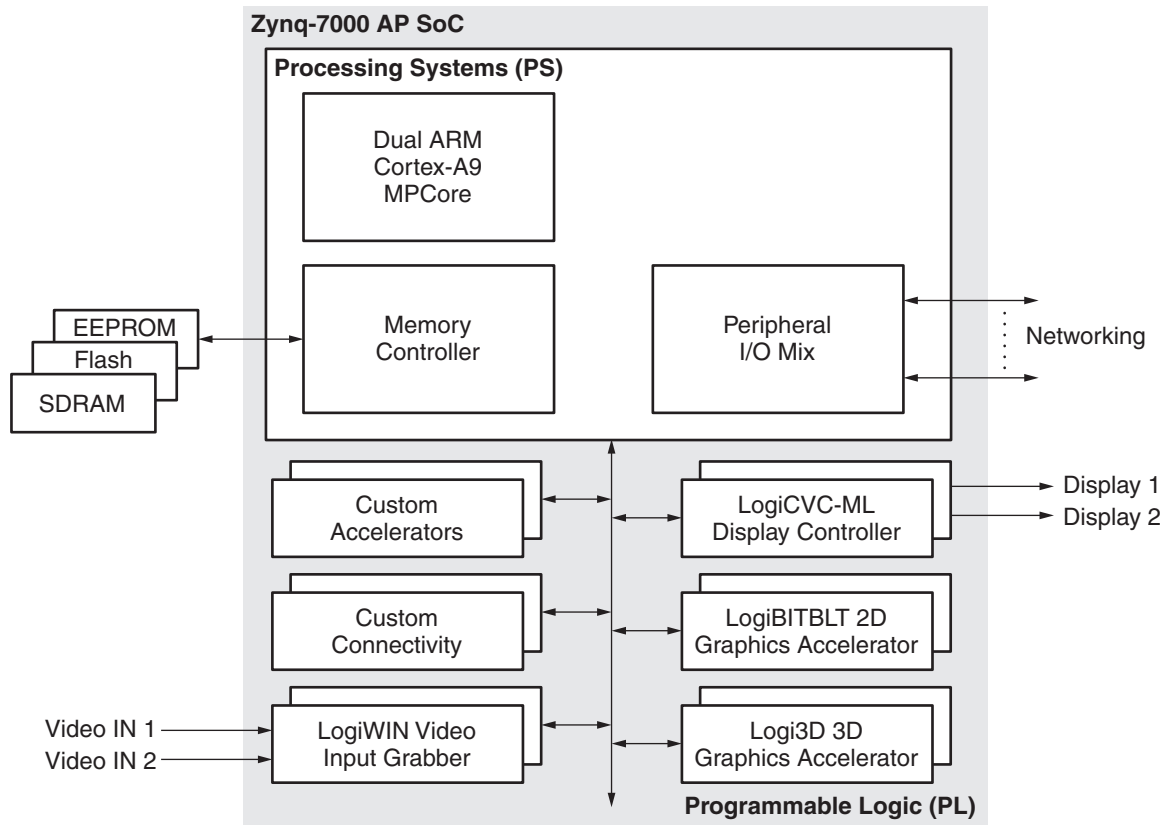
Table 1: logicBRICKS Software Provisions

Product	Supported OS	Software Type
Frame buffer	Linux 3.18, Android 2.3	Driver
Direct Rendering Manager (DRM)	Linux 3.18, Android 2.3	Driver
Direct Frame Buffer (DirectFB)	Linux	Library
OpenGL ES® 1.1	Linux 3.18, WEC 7/2013, Android	API
QNX Screen	QNX 6.5.0 SP1, 6.6.0	API
Windows display driver	WEC 7/2013	Driver
Windows GDI	WEC 7/2013	API
DirectX	WEC 7/2013	API
Qt 5.x, QtQuick 1.1	Linux 3.18, WEC 7/2013	Application framework

Xylon has production-deployed IP in many automotive, medical, and industrial products, attesting to the unsurpassed quality of the logicBRICKS IP cores being provided in these market segments. The Xylon quality management system has been independently audited since 2006, when the company achieved ISO9001 certification. This standard ensures that Xylon is continuously striving to satisfy and exceed customer quality expectations.

To assure smooth integration with the user's SoC design, and to remove foreseeable design obstacles, Xylon performs exhaustive hardware validation on hundreds, and in some cases thousands, of logicBRICKS IP core configurations. Along with a rich set of IP core deliverables that include documentation and maintenance, compatibility with new implementation tools and operating systems is assured. Xylon provides free reference designs created using evaluation logicBRICKS IP cores for the most popular Zynq-7000 AP SoC development kits. Seamless demo applications are available that can jump-start HMI development.

Anatomy of the logicBRICKS Graphics Engine



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Figure 5: Zynq-7000 SoC Based HMI with Extensible Xylon logicBRICKS Graphics Engine

Figure 5 illustrates the implementation of a Zynq-7000 AP SoC with an integrated logicBRICKS graphics engine.

A display controller is a must-have IP core that makes a minimal graphics engine configuration for any HMI application needing a display output. With a display controller-only graphics engine, the main processing system must draw (render) the complete graphics screen image by combining

multiple graphics objects in dedicated video buffers. These video buffers are usually implemented in off-chip memory due to the required memory footprint; for example, the HD 720p (1,280 x 720) resolution display requires 3.5MB of memory for a single video buffer. The smoothness of the graphics fully depends on the speed of the processing system that must calculate all graphic animations. The rendered graphics prepared in the video buffers must be formatted for the specific attached display and sent towards it by the display controller IP core.

Xylon's logiCVC-ML display controller IP core works with numerous different displays and interfaces. It supports up to five graphics layers with resolutions up to 8,192 x 8,192. The graphic layers are blended with no bandwidth needed from the processing system, which makes tasks like drawing cursors or showing a video stream overlaid by multiple overlapping menus very fast and efficient. Each graphics layer can be configured to support Pixel, Layer, or Color Look-Up Table (CLUT) blending. This IP core has an integrated DMA engine, which, in combination with the blending features and programmable size/positioning of each graphics layer, enables zero-copy of graphic objects from multiple video buffers and assures optimal use of the available memory bandwidth.

Rendering complex, high-resolution graphics requires very high usage of the processing system. This can cause an application's performance to bottleneck. To address this issue, HMI SoC designers can add Xylon's logiBITBLT Bit Block Transfer 2D Graphics Accelerator IP core for standard 2D graphics operations such as object copying/moving, bitmap flipping, up/down scaling, Porter-Duff image compositing, and others. The logiBITBLT IP core can significantly improve the graphics performance of the Zynq-7000 AP SoC-based HMI by offloading the ARM processors for other system tasks and speeding up graphics rendering, especially when the material includes large objects that do not fit in the processor cache or on-chip memories.

The impact of graphics acceleration on overall system performance can be illustrated by an example of a common blending operation between two graphics objects, such as overlapping transparent menu elements. To properly blend two overlapping graphics objects, either the processing system or the 2D graphics accelerator must (a) read the graphic object from the original video memory location; (b) read the second object stored at the destination video memory location; and (c) run logical operations to blend the two objects prior to final writing to the destination video memory location, where it appears as a blended graphics object.

Figure 6 shows the benchmarked graphic performance for the described graphic operation performed on the Xilinx ZC702 kit running Linux OS and the *QtPerf* application (designed for Qt graphic performance testing). The provided logicBRICKS software drivers enable software programmers to use the Qt cross-platform application framework in familiar ways, to design HMIs in the same way as with any SoC.

The same benchmark tests were run with the Zynq-7000 AP SoC configured to render graphics through the Linux frame buffer using no graphic acceleration, and then again with the logiBITBLT graphics accelerator supported by XylonQPA 2D acceleration plug-in for Qt5.x. The benchmark results shows that the Zynq-7000 SoC's PS can keep pace with the dedicated graphics accelerator while it is working with small-sized bitmaps, but the graphics operation occupies 100% of the single CPU's processing time. This is shown in Figure 6, presented as a 50% load on the processing system. The logiBITBLT IP core implements the dedicated logic for 2D graphics acceleration that delivers a 2X–3X performance improvement, significantly offloading the processing system when working with bigger bitmaps.

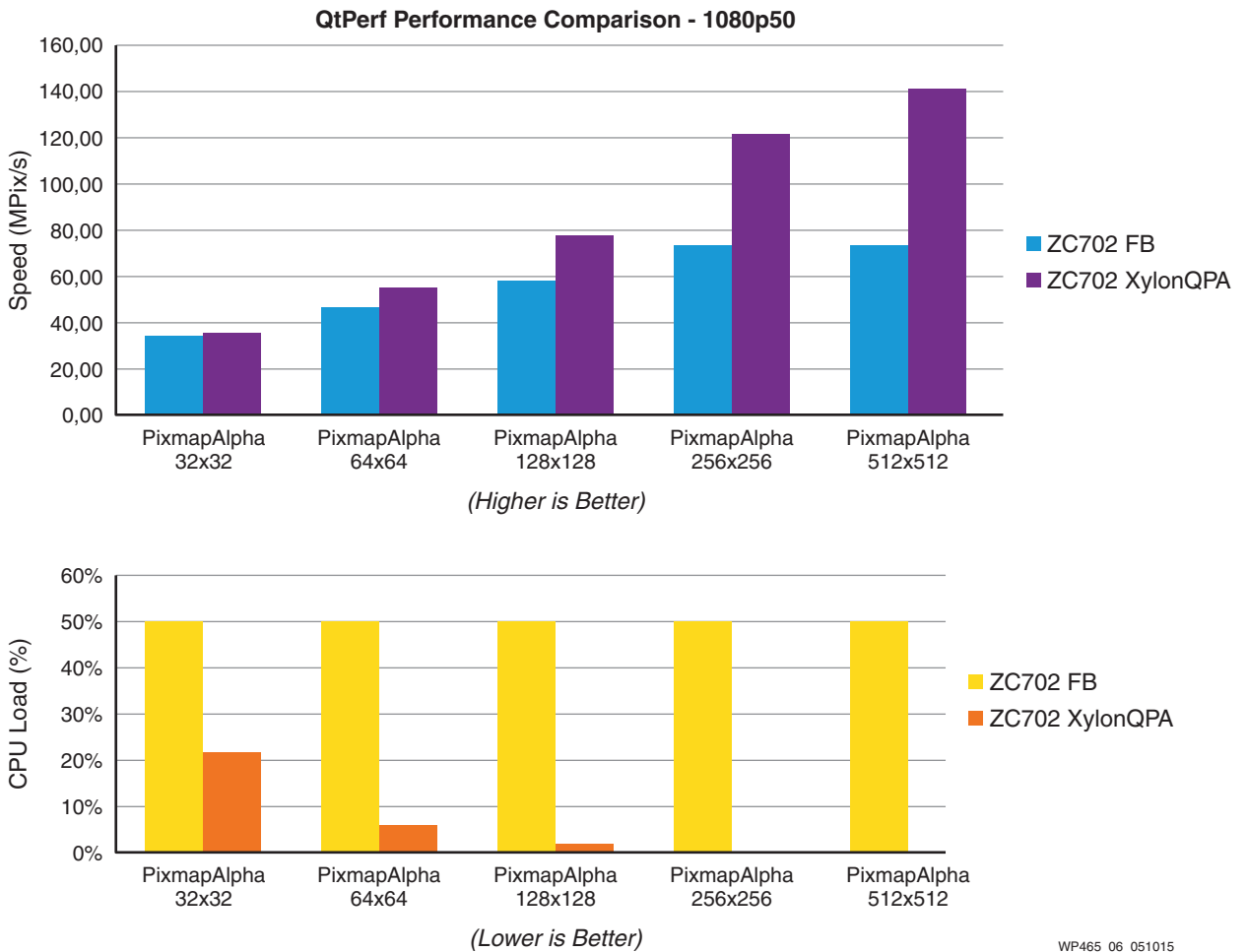


Figure 6: Impact of HW Accelerated Functions on Graphics Speed and CPU Load

QtPerf Test on Zynq ZC702 platform, where

ZC702 FB = frame buffer only

ZC702 XylonQPA = hardware acceleration implemented

Note: CPU time is higher on the 32 x 32 operation due to rapid back-to-back configuration of accelerator cores—i.e., the acceleration task happens very quickly.

Regardless of the size of the used graphics objects (bitmaps), the time required for logiBITBLT IP programming for each specific graphics operation is similar. The required CPU load can be as low as just a small percent of the time required for operations with larger bitmaps. Overall, the performance of real-life HMI applications depends on the overall SoC architecture, the software architecture, and the number and type of used graphics operations.

This video clip demonstrates the impact of the logiBITBLT graphics accelerator IP core on graphics performance (20X speed improvement) in the handheld measurement application based on the Zynq-7000 AP SoC running the Microsoft Windows Embedded Compact OS:

<http://www.logicbricks.com/logicBRICKS-IP-Library/Video-Galleries/logicBRICKS-2D-Graphics-Acceleration.aspx>

(Also available on YouTube at: <https://www.youtube.com/watch?v=ZabqKyWL6nc>).

With the integrated logicBRICKS graphic engine, the Xilinx Zynq-7000 AP SoC provides 2D graphic performance comparable with competing SoCs. Figure 7 shows the graphics performance benchmarked with the described software configuration running on the ZC702 board with the logicBRICKS 2D graphic accelerated engine and the Freescale i.MX6 based Mars development kit, which integrates an OpenGL ES 2.0 graphic engine. The logiBITBLT Bit Block Transfer 2D Graphics Accelerator IP core is optimized for bitmap graphics operations and provides software fallbacks for non-accelerated operations such as line drawing. The benchmark results show similar performance delivered by two benchmarked systems. Xylon can provide these benchmarks on request.

Note: Execution time is measured in seconds because the tests repeat each graphics operation thousands of times on multiple graphics objects.

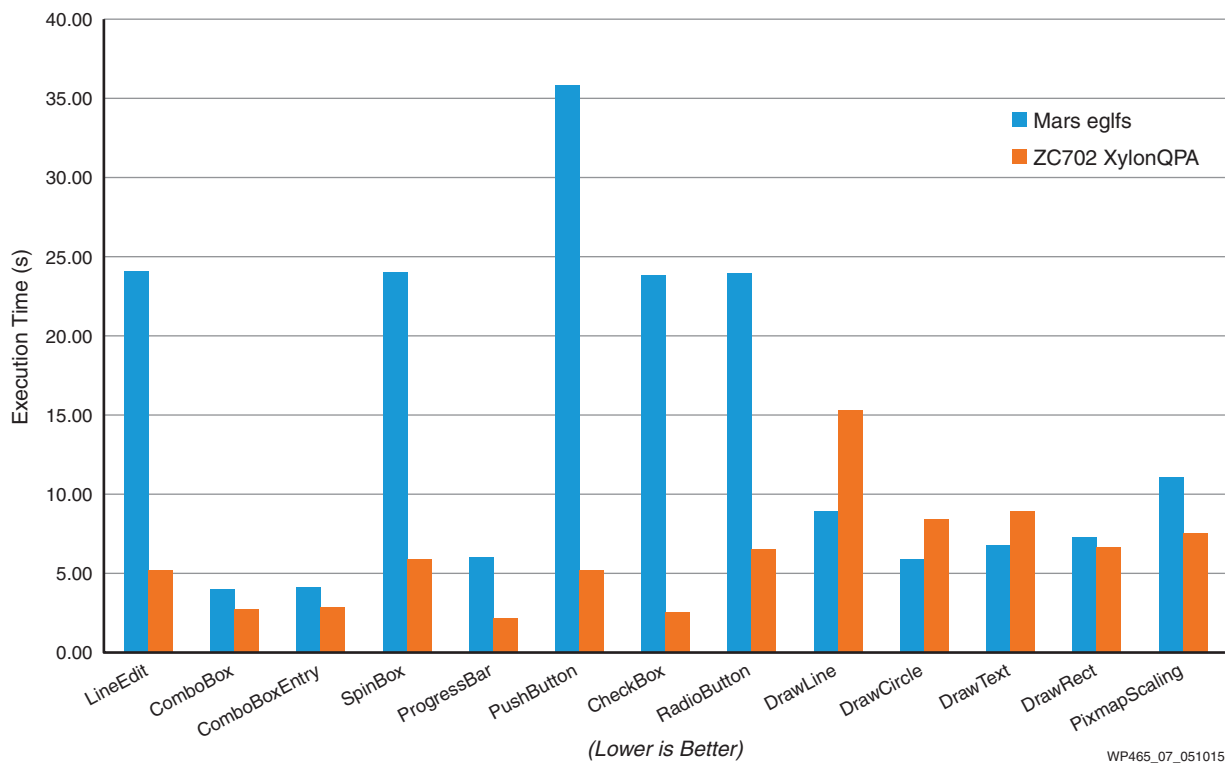


Figure 7: QtPerf Benchmark Results: ZC702 Evaluation Kit and i.MX6 MARS Evaluation Kit

More complex combinations can be designed using logicBRICKS IP cores. For example, it is possible to instantiate several display controller IP cores (see Figure 4) and to enable the Zynq-7000 AP SoC to simultaneously control two or more different type graphics displays showing completely different graphics. The described graphics engine can be further expanded by the logi3D Scalable 3D Graphics Accelerators IP core designed to support the OpenGL ES 1.1 API.

Besides the graphics controller logicBRICKS IP cores, Xylon also offers complementary video processing IP cores, such as the logiWIN Versatile Video Input IP core for frame grabbing applications and the logiISP Image Signal Processing (ISP) Pipeline IP cores for video quality enhancements. Combinations of graphics and video IP cores enable efficient single Zynq SoC implementations of low-latency, multi-channel video processing systems with an integrated graphic HMI, showing graphics menus overlaid on the streaming video and multiple video windows. More information about logicBRICKS IP cores can be found in the online IP catalog at: <http://www.logicbricks.com/Products/IP-Cores.aspx>

Getting Started with the logicBRICKS HMI

Xylon free pre-verified reference designs are developed for the Xilinx Zynq-7000 AP SoC ZC702 and ZC706 evaluation kits and the ZedBoard and MicroZed development kits from Avnet Electronics Marketing. These reference designs and development kits promise a quick start on graphic HMI development. The reference design deliverables include evaluation logicBRICKS IP cores and hardware design files prepared for the Xilinx Vivado Design Suite as well as the complete Linux OS image, IP cores software drivers, and documentation. The provided application-specific graphic demos include an industrial HMI example (Figure 3) designed by using the popular Qt application framework for GUI developments and the industrial Qt widgets library, avionics demo, 3D automotive demos, and several others.



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Figure 8: Screen Captures from Free Xylon Graphics HMI Demos

An industrial HMI demo video can be accessed at:

<http://youtu.be/qx3j8hVXfvM>

It can also be obtained from the Xylon website:

<http://www.logicbricks.com/logicBRICKS-IP-Library/Video-Galleries/logicBRICKS-Demos-Xilinx-ZC702-Video-Clip.aspx>

The logicBRICKS HMI can be evaluated with the following downloadable reference designs:

1. logiREF-ZGPU-ZC702 for the ZC702 kit:
<http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design/Graphics-for-Xilinx-Zynq-7000.aspx>
2. logiREF-ZGPU-ZC706 for the ZC706 kit:
<http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design/Graphics-for-Xilinx-Zynq-7000-ZC706.aspx>
3. logiREF-ZGPU-ZED for the ZedBoard kit:
<http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design/Graphics-for-Zynq-AP-SoC-ZedBoard.aspx>

To speed up development cycles, system designers can leverage the flexibility and scalability of logicBRICKS reference designs in several ways. Quick demoing on targeted hardware platforms is possible in minutes with the pre-compiled SD card image delivered in the installation package.

Hardware designers can customize the provided logicBRICKS reference designs to closely fit their requirements, enabling software designers to develop Linux and stand-alone applications for the product before the target hardware becomes available. The same reference designs can be also used with the Windows Embedded Compact Board Support Package (BSP) from Xilinx partner Adeneo Embedded. To learn more about using logicBRICKS with non-Linux operating systems, go to:

<http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design/OS-IP-Core-Support.aspx>

To obtain more information about logicBRICKS graphics IP and to download evaluation IP cores, go to:

- logiCVC-ML Compact Multilayer Video Controller:
<http://www.logicbricks.com/Products/logiCVC-ML.aspx>
- logiBITBLT Bit Block Transfer 2D Graphics Accelerator:
<http://www.logicbricks.com/Products/logiBITBLT.aspx>
- logi3D Scalable 3D Graphics Accelerator:
<http://www.logicbricks.com/Products/logi3D.aspx>

Conclusion

This white paper describes the benefits of using the Xilinx Zynq-7000 AP SoC as an enabler for new and upcoming industrial, scientific, and medical HMI systems. The key benefit for systems that require an HMI is the ability to implement differentiating application-specific hardware accelerators in the programmable logic and quickly upgrade it to a full SoC design with a high quality off-the-shelf graphics engine for display control. Such a platform enables the customer to achieve levels of differentiation, processing power, interfacing, and overall flexibility that surpass abilities of competing HMI ASSP products.

The Zynq-7000 All Programmable SoC ecosystem brings proven software, hardware, and system solutions to the market. The Xylon graphics engine solution described in this paper accelerates product development and enables HMI designers to concentrate on their primary differentiators.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
11/20/2015	1.0	Initial Xilinx release.

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