XQ Defense-Grade Portfolio Product Selection Guide

ZYNQ UltraSCALE+ KINTEX UltraSCALE+ VIRTEX UltraSCALE+ KINTEX UltraSCALE

ZYNQ KINTEX 7 VIRTEX 7 ARTIX 7

XQ Product Guide Contents and Fast Links

Defense-Grade SoC Portfolio and Comparison

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XQ SoC Product Documentation: Key Data Sheets

XQ FPGA Product Documentation: Key Data Sheets

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Defense-Grade SoC Portfolio and Comparison

	XQ Zynq®-7000 SoC Devices	XQ Zynq UltraScale+™ MPSoC EG Devices	XQ Zynq UltraScale+™ MPSoC EV Devices	XQ Zynq UltraScale+™ RFSoC DR Devices
Application Processor	**Dual**-core Arm® Cortex™-A9 MPCore™ up to **800MHz**	**Quad**-core Arm Cortex-A53 MPCore up to **1.33GHz**	**Quad**-core Arm Cortex-A53 MPCore up to **1.33GHz**	**Quad**-core Arm Cortex-A53 MPCore up to **1.33GHz**
Real-Time Processor	—	Dual-core Arm Cortex-R5F MPCore up to **533MHz**	Dual-core Arm Cortex-R5F MPCore up to **533MHz**	Dual-core Arm Cortex-R5F MPCore up to **533MHz**
GPU / VCU	—	Mali™-400 MP2 GPU	Mali™-400 MP2 GPU H.264 / H.265 (4x60fps)	—
High-Speed Analog	—	—	—	Available w/ SD-FEC, 14-bit DACs up to 10 Gs/s 14-bit ADCs up to 5 Gs/s
Programmable Logic	85K–444K Logic Cells 220–2,020 DSP Slices	154K–1,143K System Logic Cells 360–3,528 DSP Slices	256K–504K System Logic Cells 1,248–1,728 DSP Slices	930K System Logic Cells 4,272 DSP Slices
Other Key Features	• Tj up to –40°C to +125°C • Parity on cache and OCM • ECC on Block RAMs • Supports DDR3/2/3L, LPDDR2, 32b, or 16b w/ ECC • PCIe® Gen2 x8 • Up to 16X GTX 10.3Gb/s	• Tj up to –55°C to +125°C • Enhanced security plus available 256-bit PUF • ECC on all memories • Supports DDR4/3/3L, LPDDR4/3, 32/64b with ECC • Up to 5X PCIe Gen3x16 plus 1X PCIe Gen2 x4 • Up to 44X GTH 16.3Gb/s and up to 28X GTY 28.2Gb/s	• Tj up to –55°C to +125°C • Enhanced security plus available 256-bit PUF • ECC on all memories • Supports DDR4/3/3L, LPDDR4/3, 32/64b with ECC • Up to 2X PCIe Gen3x16 plus 1X PCIe Gen2 x4 • Up to 24X GTH 16.3Gb/s	• Tj up to –55°C to +125°C • Enhanced security plus available 256bit PUF • ECC on all memories • Supports DDR4/3/3L, LPDDR4/3, 32/64b with ECC • Up to 2X PCIe Gen4x8 plus 1X PCIe Gen2 x4 • Up to 16X GTY 28.2Gb/s

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XQ Zynq® UltraScale+™ RFSoCs: Block Diagram

Processing System

Application Processing Unit
Arm® Cortex™-A53
NEON™
Floating Point Unit
32KB I-Cache w/Parity
32KB D-Cache w/ECC
Memory Management Unit
Embedded Trace Macrocell
1 2 3 4
GIC-400
SCU
CCI/SMMU
1 MB L2 w/ECC

DDR Controller
DDR4/3/3L, LPDDR4/3 ECC Support
256 KB OCM with ECC

System Control
DMA, Timers, WDT, Resets, Clocking, Debug

High-Speed Connectivity
DisplayPort
USB 3.0
SATA 3.0
PCIe® Gen2
PS-GTR

Real-Time Processing Unit
Arm Cortex™-R5F
Vector Floating Point Unit
Memory Protection Unit
128KB TCM w/ECC
32KB I-Cache w/ECC
32KB D-Cache w/ECC
1 2
GIC

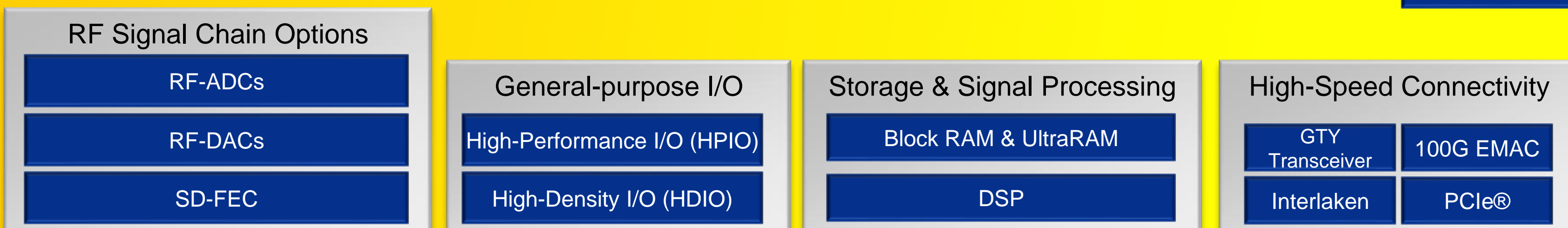
Security
Config, AES Decryption, Authentication, Secure Boot
TrustZone
Voltage/Temp Monitor

Platform Management Unit
Power
System Management

General Connectivity
GigE
CAN
UART
SPI
Quad SPI NOR
NAND
SD/eMMC

Programmable Logic

System Monitor



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XQ Zynq® UltraScale+™ RFSoCs

		Device Name	XQZU21DR	XQZU28DR	XQZU29DR	XQZU48DR	XQZU49DR
			Gen 1			Gen 3	
Processing System (PS)	Application Processor Unit	Processor Core	**Quad-core** ARM® Cortex™-A53 MPCore™ up to 1.33GHz				
		Memory w/ECC	L1 Cache 32KB I / D per core, L2 Cache 1MB, on-chip Memory 256KB				
	Real-Time Processor Unit	Processor Core	**Dual-core** Arm Cortex-R5F MPCore up to 533MHz				
		Memory w/ECC	L1 Cache 32KB I / D per core, Tightly Coupled Memory 128KB per core				
	External Memory	Dynamic Memory Interface	x32/x64: DDR4, LPDDR4, DDR3, DDR3L, LPDDR3 with ECC				
		Static Memory Interfaces	NAND, 2x Quad-SPI				
	Connectivity	High-Speed Connectivity	PCIe® Gen2 x4, 2x USB3.0, SATA 3.1, DisplayPort, 4x Tri-mode Gigabit Ethernet				
		General Connectivity	2xUSB 2.0, 2x SD/SDIO, 2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO				
	Integrated Block Functionality	Power Management	Full / Low / PL / Battery Power Domains				
		Security	RSA, AES, and SHA				
		AMS - System Monitor	10-bit, 1MS/s – Temperature and Voltage Monitor				
		PS to PL Interface	12 x 32/64/128b AXI Ports				
	RF Data Converter Subsystem	12-bit, 4GSPS RF-ADC w/DDC	–	8	–	–	–
		12-bit, 2GSPS RF-ADC w/DDC	–	–	16	–	–
		14-bit, 6.4GSPS RF-DAC w/DUC	–	8	16	–	–
		14-bit, 2.5GSPS RF-ADC w/DDC	–	–	–	–	16
		14-bit, 5GSPS RF-ADC w/DDC	–	–	–	8	–
		14-bit, 9.85GSPS[1] RF-DAC w/DUC	–	–	–	8	16
		SD-FEC	8	8	0	8	0
Programmable Logic (PL)	Programmable Functionality	System Logic Cells (K)	930	930	930	930	930
		CLB LUTs (K)	425	425	425	425	425
	Memory	Max. Distributed RAM (Mb)	13.0	13.0	13.0	13.0	13.0
		Total Block RAM (Mb)	38.0	38.0	38.0	38.0	38.0
		UltraRAM (Mb)	22.5	22.5	22.5	22.5	22.5
	Integrated IP	DSP Slices	4,272	4,272	4,272	4,272	4,272
		PCIe® Gen 3x16	2	2	2	–	–
		PCIe® Gen 3x16/Gen4 x8/CCIX	–	–	–	2	2
		150G Interlaken	1	1	1	1	1
		100G Ethernet MAC/PCS w/RS-FEC	2	2	2	2	2
		AMS - System Monitor	1	1	1	1	1
	Speed Grades	M-Temperature	-1	-1	-1	-1	-1
		I-Temperature	-1, -1L, -2	-1, -1L, -2	-1, -1L, -2	-1, -1L, -2, -2L	-1, -1L, -2, -2L

Notes:
1. For 10GSPS RF-DAC operation, contact your local Xilinx Sales Representative.

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XQ Zynq® UltraScale+™ RFSoCs: Packages

Device Name		XQZU21DR	XQZU28DR	XQZU29DR	XQZU48DR	XQZU49DR
			Gen 1		Gen 3	
Package Footprint	Package Dimensions (mm)	PSIO, HDIO, HPIO PS-GTR, GTY, RF-ADC, RF-DAC				
FFRD1156	35x35	214, 72, 208 4, 16, 0, 0				
FFRE1156	35x35		214, 48, 104 4, 8, 8, 8		214, 48, 104 4, 8, 8, 8	
FFRG1517	40x40		214, 48, 299 4, 16, 8, 8			
FSRG1517	40x40				214, 48, 299 4, 16, 8, 8	
FFRF1760	42.5x42.5			214, 96, 312 4, 16, 16, 16		
FSRF1760	42.5x42.5					214, 96, 312 4, 16, 16, 16

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XQ Zynq® UltraScale+™ RFSoC Ordering Information

M = Military (Tj = –55°C to +125°C)
I = Industrial (Tj = –40°C to +100°C)

Refer to Device Data Sheet Overview and Pinout Specifications for additional information.

Important: Verify all data in this document with the device data sheets found at www.xilinx.com

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XQ Zynq® UltraScale+™ MPSoCs: Block Diagram

Processing System

Application Processing Unit

Arm® Cortex™-A53
NEON™
Floating Point Unit
32KB I-Cache w/Parity
32KB D-Cache w/ECC
Memory Management Unit
Embedded Trace Macrocell
1 2 3 4
GIC-400
SCU
CCI/SMMU
1MB L2 w/ECC

Memory

DDR4/3/3L, LPDDR4/3 32/64 bit w/ECC
256KB OCM with ECC

Graphics Processing Unit ARM Mali™-400 MP2

Geometry Processor
Pixel Processor 1 2
Memory Management Unit
64KB L2 Cache

High-Speed Connectivity

DisplayPort v1.2a
USB 3.0
SATA 3.1
PCIe® 1.0 / 2.0
PS-GTR

Real-Time Processing Unit

Arm Cortex™-R5F
Vector Floating Point Unit
Memory Protection Unit
128KB TCM w/ECC
32KB I-Cache w/ECC
32KB D-Cache w/ECC
1 2
GIC

Platform Management Unit

System Management
Power Management
Functional Safety

Configuration and Security Unit

Config AES Decryption, Authentication, Secure Boot
Voltage/Temp Monitor
TrustZone

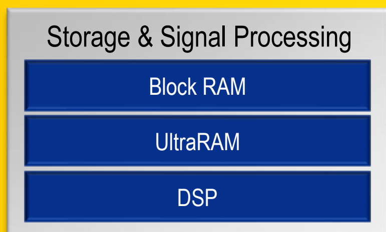
System Functions

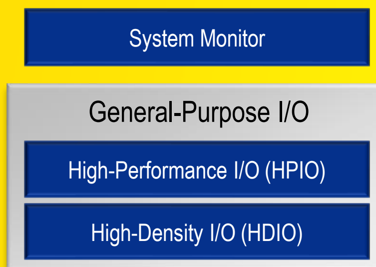
Multichannel DMA
Timers, WDT, Resets, Clocking & Debug

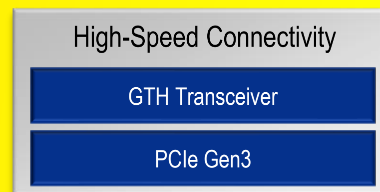
General Connectivity

GigE
USB 2.0
CAN
UART
SPI
Quad SPI NOR
NAND
SD/eMMC

Programmable Logic







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XQ Zynq® UltraScale+™ MPSoCs: Features

		Device Name	XQZU3EG	XQZU5EV	XQZU7EV	XQZU9EG	XQZU11EG	XQZU15EG	XQZU19EG
Processing System (PS)	Application Processor Unit	Processor Core	**Quad-core** Arm® Cortex™-A53 MPCore™ up to 1.33GHz						
		Memory w/ECC	L1 Cache 32KB I / D per core, L2 Cache 1MB, on-chip Memory 256KB						
	Real-Time Processor Unit	Processor Core	**Dual-core** ARM Cortex-R5F MPCore™ up to 533MHz						
		Memory w/ECC	L1 Cache 32KB I / D per core, Tightly Coupled Memory 128KB per core						
	Graphic & Video Acceleration	Graphics Processing Unit	Mali™-400 MP2 up to 600MHz						
		Memory	L2 Cache 64KB						
	External Memory	Dynamic Memory Interface	x32/x64: DDR4, LPDDR4, DDR3, DDR3L, LPDDR3 with ECC						
		Static Memory Interfaces	NAND, 2x Quad-SPI						
	Connectivity	High-Speed Connectivity	PCIe® Gen2 x4, 2x USB3.0, SATA 3.1, DisplayPort, 4x Tri-mode Gigabit Ethernet						
		General Connectivity	2xUSB 2.0, 2x SD/SDIO, 2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO						
	Integrated Block Functionality	Power Management	Full / Low / PL / Battery Power Domains						
		Security	RSA, AES, and SHA						
		AMS - System Monitor	10-bit, 1MSPS - Temperature, Voltage, and Current Monitor						
		PS to PL Interface	12 x 32/64/128b AXI Ports						
Programmable Logic (PL)	Programmable Functionality	System Logic Cells (K)	154	256	504	600	653	747	1,143
		CLB Flip-Flops (K)	141	234	461	548	597	682	1,045
		CLB LUTs (K)	71	117	230	274	299	341	523
	Memory	Max. Distributed RAM (Mb)	1.8	3.5	6.2	8.8	9.1	11.3	9.8
		Total Block RAM (Mb)	7.6	5.1	11.0	32.1	21.1	26.2	34.6
		UltraRAM (Mb)	-	18.0	27.0	-	22.5	31.5	36.0
	Clocking	Clock Management Tiles (CMTs)	3	4	8	4	8	4	11
	Integrated IP	DSP Slices	360	1,248	1,728	2,520	2,928	3,528	1,968
		Video Codec Unit (VCU)	-	1	1	-	-	-	-
		PCI Express® Gen 3x16	-	2	2	-	4	-	5
		150G Interlaken	-	-	-	-	1	-	4
		100G Ethernet MAC/PCS w/RS-FEC	-	-	-	-	2	-	4
		AMS - System Monitor	1	1	1	1	1	1	1
	Transceivers	GTH 16.3Gb/s Transceivers	-	16	24	24	32	24	44
		GTY 28.2Gb/s Transceivers	-	-	-	-	16	-	28
	Speed Grades	M-Temperature	-1						
		I-Temperature	-1 -1L -2						

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XQ Zynq® UltraScale+™ MPSoCs: Packages

Device Name		XQZU3EG	XQZU5EV	XQZU7EV	XQZU9EG	XQZU11EG	XQZU15EG	XQZU19EG
Pkg Footprint[2,3]	Dimensions (mm)	PSIO[1], HDIO, HPIO PS-GTR 6Gb/s, GTH 16.3Gb/s, GTY 28.2Gb/s						
SFRA484[4]	19x19	170, 24, 58 4, 0, 0						
SFRC784[4,5]	23x23	214, 96, 156 4, 0, 0	214, 96, 156 4, 4, 0					
FFRB900	31x31		214, 48, 156 4, 16, 0	214, 48, 156 4, 16, 0				
FFRC900	31x31				214, 48, 156 4, 16, 0		214, 48, 156 4, 16, 0	
FFRB1156	35x35				214, 120, 208 4, 24, 0		214, 120, 208 4, 24, 0	
FFRC1156	35x35			214, 48, 312 4, 20, 0		214, 48, 312 4, 20, 0		
FFRB1517	40x40							214, 72, 572 4, 16, 0
FFRC1760	42.5x42.5					214, 96, 416 4, 32, 16		214, 96, 416 4, 32, 16

Notes:
1. PS I/O is a combination of PS MIO and PS DDRIO.
2. Packages with the same last letter and number sequence, e.g., A484, are footprint compatible with all other UltraScale devices with the same sequence.
3. For full part number details, see the Ordering Information section in DS891, *Zynq UltraScale+ MPSoC Overview*.
4. These packages are only offered in 0.8mm ballpitch. All other packages are offered in 1.0mm ball pitch.
5. GTH transceivers in the C784 package support data rates up to 12.5Gb/s.

Important: Verify all data in this document with the device data sheets found at www.xilinx.com

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XQ Zynq® UltraScale+™ MPSoC Ordering Information

Footprint

XQ	ZU	#	EV	-1	F	F	R	A	####	M
Xilinx Defense-grade	Zynq UltraScale +	Value Index	SoC Type CG: Dual APU Dual RPU EG: Quad APU Dual RPU Single GPU EV: Quad APU Dual RPU Single GPU Single VCU	Speed Grade -1: Slowest -L1: Low Power -2: Mid -3: Fastest	F: Flip-chip w/ 1.0mm Ball Pitch S: Flip-chip w/ 0.8mm Ball Pitch	F: Lid B: Lidless	R: Ruggedized Package Q: Sn/Pb balls Pb-free inside	Package Designator	Package Pin Count	Temperature Grade (M, I)

M = Military (Tj = –55°C to +125°C)
I = Industrial (Tj = –40°C to +100°C)

Refer to Device Data Sheet Overview and Pinout Specifications for additional information.

Important: Verify all data in this document with the device data sheets found at www.xilinx.com

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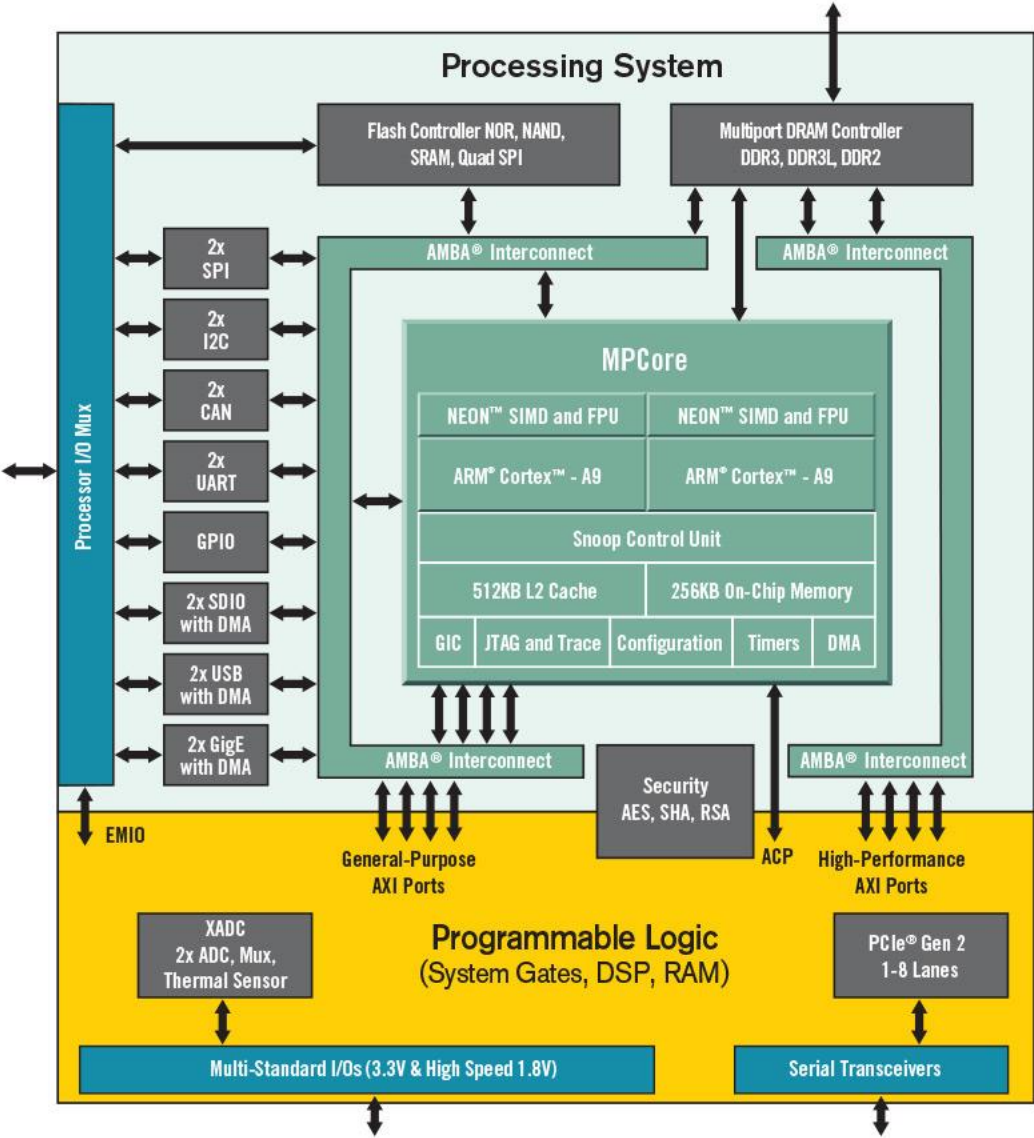
XQ Zynq®-7000 SoCs: Block Diagram



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XQ Zynq®-7000 SoCs: Features

	Device Name	XQ7Z020	XQ7Z030	XQ7Z045	XQ7Z100
Processing System (PS)	Processor Core	Dual-Core Arm Cortex-A9 MPCore Up to 766MHz	Dual-Core ARM Cortex-A9 MPCore Up to 800MHz		
	Processor Extensions	NEON™ SIMD Engine and Single/Double Precision Floating Point Unit per processor			
	L1 Cache	32KB Instruction, 32KB Data per processor			
	L2 Cache	512KB			
	On-Chip Memory	256KB			
	External Memory Support	DDR3, DDR3L, DDR2, LPDDR2			
	External Static Memory Support	2x Quad-SPI, NAND, NOR			
	DMA Channels	8 (4 dedicated to PL)			
	Peripherals	2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO			
	Peripherals w/ built-in DMA	2x USB 2.0 (OTG), 2x Tri-mode Gigabit Ethernet, 2x SD/SDIO			
	Security[1]	RSA Authentication of First Stage Boot Loader, AES and SHA 256b Decryption and Authentication for Secure Boot			
	PS to PL Interface	2x AXI 32b Master, 2x AXI 32b Slave, 4x AXI 64b/32b Memory, AXI 64b ACP, 16 Interrupts			
Programmable Logic (PL)	7 Series PL Equivalent	Artix®-7	Kintex®-7	Kintex®-7	Kintex®-7
	Logic Cells	85K	125K	350K	444K
	Look-Up Tables (LUTs)	53,200	78,600	218,600	277,400
	Flip-Flops	106,400	157,200	437,200	554,800
	Total Block RAM (# 36Kb Blocks)	4.9Mb (140)	9.3Mb (265)	19.2Mb (545)	26.5Mb (755)
	DSP Slices	220	400	900	2,020
	PCI Express®	—	Gen2 x4	Gen2 x8	Gen2 x8
	Analog Mixed Signal (AMS) / XADC	2x 12 bit, MSPS ADCs with up to 17 Differential Inputs			
	Security[1]	AES & SHA 256b Decryption & Authentication for Secure Programmable Logic Config			
	Speed Grades: Q-Temperature	-1	-1		–
	Speed Grades: I-Temperature	-1, -2, -1L	-1, -2, -2L		-1, -2, -2L

Notes:
1. Security block is shared by the Processing System and the Programmable Logic.

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XQ Zynq®-7000 SoCs: Packages

Device Name		XQZ7020	XQZ7030	XQZ7045	XQZ7100
Package Footprint[1]	Dimensions (mm)	HRIO, HPIO PSIO[2], GTP 6.2Gb/s	HRIO, HPIO PSIO[2], GTX 10.3Gb/s		
CL400	17x17	125, 0 128, 0			
CL484	19x19	200, 0 128, 0			
RB484	23x23		100, 63 128, 4		
RF676[1]	27x27		100, 150 128, 4	100, 150 128, 8	
RFG676[1]	27x27			100, 150 128, 8	
RF900	31x31			212, 150 128, 16	212, 150 128, 16
RF1156	35x35				250, 150 128, 16

Notes:
1. Devices in the same package are footprint compatible. FBG676 and FFG676 are also footprint compatible.
2. PS I/O count does not include dedicated DDR calibration pins.
3. PS DDR and PS MIO pin count is limited by package size. See DS190, *Zynq-7000 All Programmable SoC Overview* for details.

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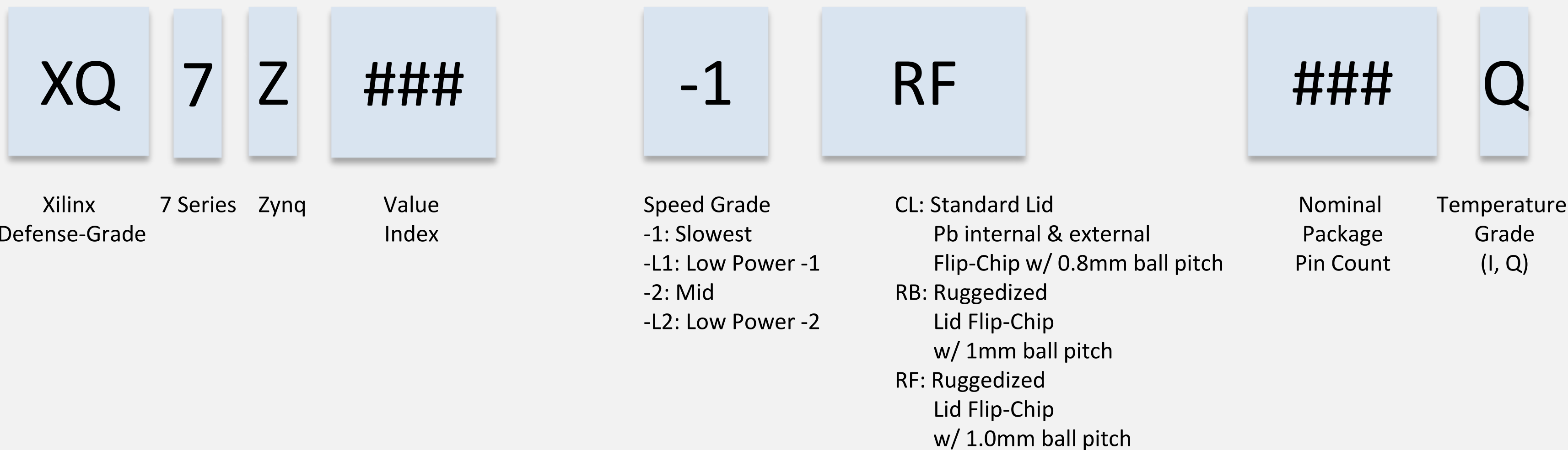
XQ Zynq®-7000 SoC Ordering Information



Q = Automotive (Tj = –40°C to +125°C)
I = Industrial (Tj = –40°C to +100°C)

Refer to Device Data Sheet Overview and Pinout Specifications for additional information.

Important: Verify all data in this document with the device data sheets found at www.xilinx.com

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Defense-Grade FPGA Portfolio and Comparison

	XQ Kintex UltraScale	XQ Kintex UltraScale+	XQ Virtex UltraScale+
Programmable Logic	530K–1,451K System Logic Cells 1,920–5,520 DSP Slices	475K–1,143K System Logic Cells 1,824–1,968 DSP Slices	862K–2,835K System Logic Cells 2,280–9,216 DSP Slices
Other Key Features	• Tj up to –55°C to +125°C • ECC on memories • Up to 6X PCIe® Gen3x8 • Up to 64X GTH/Y 16.3Gb/s	• Tj up to –55°C to +125°C • ECC on memories • Up to 5X PCIe Gen3x16 • Up to 32X GTH 16.3Gb/s and up to 24X GTY 28.2Gb/s	• Tj up to –55°C to +125°C • ECC on memories • Up to 4X PCIe Gen3x16 • Up to 96X GTY 28.2Gb/s

	XQ Artix-7	XQ Kintex-7	XQ Virtex-7
Programmable Logic	52K–215K Logic Cells 120–740 DSP Slices	326K–406K Logic Cells 840–1,540 DSP Slices	583K–979K Logic Cells 1,120–3,600 DSP Slices
Other Key Features	• Tj up to –55°C to +125°C • ECC on memories • Up to 1X PCIe Gen2x4 • Up to 8X GTP 6.6Gb/s	• Tj up to –55°C to +125°C • ECC on memories • Up to 1X PCIe Gen2x8 • Up to 16X GTX 10.3Gb/s	• Tj up to –55°C to +125°C • ECC on memories • Up to 3X PCIe Gen3x8 • Up to 48X GTH 11.3Gb/s

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XQ Virtex® and Kintex® UltraScale+™ FPGAs

	Device Name	XQKU5P	XQKU15P	XQVU3P	XQVU7P	XQVU11P
Logic	System Logic Cells (K)	475	1,143	862	1,724	2,835
	CLB Flip-Flops (K)	434	1,045	788	1,576	2,592
	CLB LUTs (K)	217	523	394	788	1,296
Memory	Max. Distributed RAM (Mb)	6.1	9.8	12.0	24.1	36.2
	Total Block RAM (Mb)	16.9	34.6	25.3	50.6	70.9
	UltraRAM (Mb)	18.0	36.0	90.0	180.0	270.0
Clocking	Clock Mgmt Tiles (CMTs)	4	11	10	20	12
Integrated IP	DSP Slices	1,824	1,968	2,280	4,560	9,216
	Peak INT8 DSP (TOPs)	–	–	7.1	14.2	28.7
	PCIe® Gen3 x16	1	5	2	4	3
	150G Interlaken	0	4	3	6	6
	100G Ethernet w/RS-FEC	1	4	3	6	9
I/O	Max. Single-Ended HD I/Os	96	96	–	–	–
	Max. Single-Ended HP I/Os	208	468	520	832	416
	GTH 16.3Gb/s Transceivers	0	32	–	–	–
	GTY 28.2Gb/s Transceivers	16	24	40	76	96
Speed Grades	M-Temperature	-1	-1	-1	–	–
	I-Temperature	-1 -1L -2	-1 -1L -2	-1 -2	-1 -2	-1 -2
Package Footprint[2][5]	Dimensions (mm)	HDIO, HPIO, GTH 16.3Gb/s, GTY 28.2Gb/s		HPIO, GTY 28.2Gb/s		
SFRB784[3]	23x23[4]	96, 208, 0, 16				
FFRB676	27x27	72, 208, 0, 16				
FRA1156[3]	35x35		48, 468, 20, 8			
FFRE1517	40x40		96, 416, 32, 24			
FFRC1517	40x40			520, 40		
FLRA2104	47.5x47.5				832, 52	
FLRB2104	47.5x47.5				702, 76	
FLRC2104	47.5x47.5					416, 96

Notes:

1. Maximum achievable performance is device and package dependent; consult the associated data sheet for details.
2. For full part number details, see the Ordering Information section in DS895, XQ *UltraScale Architecture* Overview.
3. GTY transceiver line rates are package limited: B784 to 12.5 Gb/s, and A1156 to 16.3 Gb/s. Refer to data sheet for details.
4. The B784 package is only offered in 0.8mm ball pitch. All other packages are 1.0mm ball pitch.
5. Packages with the same package footprint designator, e.g., A2104, are footprint compatible within XC and XQ UltraScale and UltraScale+ (footprint is underlined).

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XQ Kintex® UltraScale™ FPGAs

	Device Name	XQKU040	XQKU060	XQKU095	XQKU115
Logic Resources	System Logic Cells (K)	530	726	1,176	1,451
	CLB Flip-Flops	484,800	663,360	1,075,200	1,326,720
	CLB LUTs	242,400	331,680	537,600	663,360
Memory Resources	Maximum Distributed RAM (Kb)	7,050	9,180	4,800	18,360
	Block RAM/FIFO w/ECC (36Kb each)	600	1,080	1,680	2,160
	Block RAM/FIFO (18Kb each)	1,200	2,160	3,360	4,320
	Total Block RAM (Mb)	21.1	38.0	59.1	75.9
Clock Resources	CMT (1 MMCM, 2 PLLs)	10	12	16	24
	I/O DLL	40	48	64	64
I/O Resources	Maximum Single-Ended HP I/Os	416	416	468	624
	Maximum Single-Ended HR I/Os	104	104	52	104
Integrated IP Resources	DSP Slices	1,920	2,760	768	5,520
	System Monitor	1	1	1	2
	PCIe® Gen1/2/3	3	3	4	6
	Interlaken	0	0	2	0
	100G Ethernet	0	0	2	0
	16.3Gb/s Transceivers (GTH/GTY)	20	28	28[1]	64
Speed Grades	M-Temperature	-1	-1	-1	–
	I-Temperature	-1 -1L -2	-1 -1L -2	-1 -2	-1 -1L -2

Package Footprint[2, 3, 4, 5]	Package Dimensions (mm)	HRIO, HPIO, GTH/GTY			
		XQKU040	XQKU060	XQKU095	XQKU115
RBA676[6]	27x27	104, 208, 16			
RFA1156	35x35	104, 416, 20	104, 416, 28	52, 468, 28	
RLD1517	40x40				104, 234, 64
RLF1924	45x45				104, 624, 64

Notes:
1. GTY transceivers in KU095 devices support data rates up to 16.3Gb/s.
2. Packages with the same package footprint designator, e.g., A2104, are footprint compatible within XC and XQ UltraScale and UltraScale+ (footprint is underlined).
3. Maximum achievable performance is device and package dependent; consult the associated data sheet for details.
4. For full part number details, see the Ordering Information section in DS895, XQ *UltraScale Architecture* Overview.
5. See UG575, *UltraScale Architecture Packaging and Pinouts User Guide* for more information.
6. GTH transceivers in A676 packages support data rates up to 12.5Gb/s.

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XQ UltraScale™ Architecture FPGA Migration Table

UltraScale and UltraScale+ families provide footprint compatibility to enable users to migrate designs from one device or family to another.
Any two packages with the same footprint identifier code are footprint compatible, irrespective of being XQ or XC.

Pkg	mm	Kintex® UltraScale™							Kintex UltraScale+™						Virtex® UltraScale							Virtex UltraScale+					
		KU025	KU035	KU040	KU060	KU085	KU095	KU115	KU3P	KU5P	KU9P	KU11P	KU13P	KU15P	VU065	VU080	VU095	VU125	VU160	VU190	VU440	VU3P	VU5P	VU7P	VU9P	VU11P	VU13P
A784	23		XC	XC																							
B784	23								XC	XQ																	
A676	27		XC	XQ					XC	XC																	
B676	27								XC	XQ																	
A900	31		XC	XC																							
D900	31								XC	XC		XC															
E900	31										XC		XC														
A1156	35	XC	XC	XQ	XQ		XQ					XC		XQ													
A1517	40				XC	XC		XC																			
C1517	40						XC								XC	XC	XC					XQ					
D1517	40							XQ								XC	XC	XC									
E1517	40											XC		XQ													
A1760	42.5													XC													
B1760	42.5					XC	XC	XC								XC	XC	XC									
E1760	42.5													XC													
D1924	45							XC																			
F1924	45					XC		XQ																		XC	
A2104	47.5[1]							XC								XC	XC	XC					XC	XQ	XC		XC
B2104	47.5[1]						XC	XC								XC	XC	XC	XC	XC			XC	XQ	XC	XC	XC
C2104	47.5[1]																XC	XC	XC	XC			XC	XC	XC	XQ	XC
D2104	47.5[1]																								XC	XC	XC
B2377	50																				XC						
A2577	52.5																			XC					XC	XC	XC
A2892	55																				XC						

Legend
- XC Device
- XQ Device[2]
- Migration Path

Notes:
1.The body size of the VU13P device in the A2104, B2104, C2104, and D2104 packages is 52.5mm. These packages are footprint compatible with the corresponding 47.5mm body size packages. See UG583, *UltraScale Architecture PCB Design User Guide* for important migration details.
2. XQ devices in this table represent the XQ ruggedized package devices. Every XQ ruggedized device has an equivalent XC device.

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UltraScale™ Architecture FPGA Ordering Information

KINTEX UltraSCALE

XQ	K	U	###	-1	RF	A	####	M
Xilinx Defense-Grade	K: Kintex	UltraScale	Value Index	Speed Grade -1: Slowest -L1: Low Power -1 -2 = Mid	RB: Ruggedized Lid Flip-Chip w/ 0.8mm ball pitch RF: Ruggedized Lid Flip-Chip w/ 1.0mm ball pitch RL: Ruggedized SSI Lid Flip-Chip w/ 1.0mm ball pitch	Footprint Alpha	Package Pin Count	Temperature Grade (I, M)

Footprint: A ####

M = Military (Tj = –55°C to +125°C)
I = Industrial (Tj = –40°C to +100°C)

KINTEX UltraSCALE+ VIRTEX UltraSCALE+

XQ	V	U	#	P	-1	F	L	R	A	#	M
Xilinx Defense-Grade	V: Virtex K: Kintex	UltraScale	Value Index	P: Denotes UltraScale+	Speed Grade -1 = Slowest -L1 = Low Power -2 = Mid -L2 = Low Power -3 = Fastest	F: Flip-Chip w/ 1.0mm ball pitch S: Flip-Chip w/ 0.8mm ball pitch	F: Lid L: Lid SSI B: Lidless S: Lidless SSI Stiffener H: Lid Overhang SSI I: Lidless Overhang SSI Stiffener	R: Ruggedized Package Q: Sn/Pb balls Pb-free inside	Footprint Alpha	Package Pin Count	Temperature Grade (I, M)

Footprint: A #

M = Military (Tj = –55°C to +125°C)
I = Industrial (Tj = –40°C to +100°C)

Refer to Device Data Sheet Overview and Pinout Specifications for additional information.

Important: Verify all data in this document with the device data sheets found at www.xilinx.com

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XQ Virtex®-7 FPGAs

	Device Name	XQ7V585T	XQ7VX330T	XQ7VX485T	XQ7VX690T	XQ7VX980T
Logic Resources	Slices	91,050	51,000	75,900	108,300	153,000
	Logic Cells	582,720	326,400	485,760	693,120	979,200
	CLB Flip-Flops	728,400	408,000	607,200	866,400	1,224,000
Memory Resources	Maximum Distributed RAM (Kb)	6,938	4,388	8,175	10,888	13,838
	Block RAM/FIFO w/ ECC (36 Kb each)	795	750	1,030	1,470	1,500
	Total Block RAM (Kb)	28,620	27,000	37,080	52,920	54,000
Clocking	CMTs (1 MMCM + 1 PLL)	18	14	14	20	18
I/O Resources	Maximum Single-Ended I/O	850	700	700	1,000	900
	Maximum Differential I/O Pairs	408	336	336	480	432
Integrated IP Resources	DSP Slices	1,260	1,120	2,800	3,600	3,600
	PCIe® Gen2[2]	3	—	4	—	—
	PCIe Gen3	—	2	—	3	3
	Analog Mixed Signal (AMS) / XADC	1	1	1	1	1
	Configuration AES / HMAC Blocks	1	1	1	1	1
	GTX Transceivers (10.3 Gb/s Max Rate)[3]	36	—	28	—	—
	GTH Transceivers (11.3 Gb/s Max Rate)[4]	—	28	—	48	24
Speed Grades	M-Temperature	-1	-1	-1	—	—
	I-Temperature	-1, -2	-1, -2	-1, -2	-1, -2	-1
	E-Temperature	-2L	-2L	-2L	-2L	-2L

Package[1][5]	Dimensions (mm)	**Available User I/O:** HRIO, HPIO, GTX 10.3Gb/s, GTH 11.3Gb/s				
RF1157	35 x 35	0, 600, 20, 0	0, 600, 0, 20		0, 600, 0, 20	
RF1158	35 x 35				0, 350, 0, 48	
RF1761	42.5 x 42.5	100, 750, 36, 0	50, 650, 0, 28	0, 700, 28, 0	0, 850, 0, 36	
RF1930	45 x 45			0, 700, 24, 0	0, 1000, 0, 24	0, 900, 0, 24

Notes:
1. See DS185, *Defense-Grade 7 Series FPGAs Overview,* for package details. Other packages available with leaded external balls, see DS180 *7 Series FPGAs Overview* for XC package details.
2. Hard block supports PCI Express Base 2.1 specification at Gen1 and Gen2 data rates. Gen3 supported with soft IP.
3. 10.3125 Gb/s support in -2 speed grade.
4. 11.3 Gb/s support in -2 speed grade.
5. RF#### packages are pin compatible with FF#### packages, for same/equivalent ####; see product pinout specifications for details about compatibility.

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XQ Kintex®-7 FPGAs

	Device Name	XQ7K325T	XQ7K410T
Logic Resources	Slices	50,950	63,550
	Logic Cells	326,080	406,720
	CLB Flip-Flops	407,600	508,400
Memory Resources	Maximum Distributed RAM (Kb)	4,000	5,663
	Block RAM/FIFO w/ ECC (36 Kb each)	445	795
	Total Block RAM (Kb)	16,020	28,620
Clock Resources	CMTs (1 MMCM + 1 PLL)	10	10
I/O Resources	Maximum Single-Ended I/O	500	500
	Maximum Differential I/O Pairs	240	240
Integrated IP Resources	DSP48 Slices	840	1,540
	PCIe® Gen2[2]	1	1
	Analog Mixed Signal (AMS) / XADC	1	1
	Configuration AES / HMAC Blocks	1	1
	GTX Transceivers (10.3 Gb/s Max Rate)	16	16
Speed Grades	M-Temperature	-1, -1L	-1
	I-Temperature	-1, -2, -2L	-1, -2, -2L
	E-Temperature	-2L	-2L

	Package[1]	Dimensions (mm)	**Available User I/O**: HRIO, HPIO, GTX 10.3Gb/s	
	RF676[3]	27 x 27	250, 150, 8	250, 150, 8
	RF900[3]	31 x 31	350, 150, 16	350, 150, 16

Notes:
1. See DS185, *Defense-Grade 7 Series FPGAs Overview,* for package details.
2. Hard block supports PCI Express Base 2.1 specification at Gen1 and Gen2 data rates. Gen3 supported with soft IP.
3. RF676 is footprint compatible with FFG676, and RF900 is footprint compatible with FFG900.

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XQ Artix®-7 FPGAs

	Device Name	XQ7A50T	XQ7A100T	XQ7A200T
Logic Resources	Logic Cells	52,160	101,440	215,360
	Slices	8,150	15,850	33,650
	CLB Flip-Flops	65,200	126,800	269,200
Memory Resources	Maximum Distributed RAM (Kb)	600	1,188	2,888
	Block RAM/FIFO w/ ECC (36 Kb each)	75	135	365
	Total Block RAM (Kb)	2,700	4,860	13,140
Clock Resources	CMTs (1 MMCM + 1 PLL)	5	6	10
I/O Resources	Maximum Single-Ended I/O	250	300	500
	Maximum Differential I/O Pairs	120	144	240
Embedded Hard IP Resources	DSP Slices	120	240	740
	PCIe® Gen2[1]	1	1	1
	Analog Mixed Signal (AMS) / XADC	1	1	1
	Configuration AES / HMAC Blocks	1	1	1
	GTP Transceivers (6.6 Gb/s Max Rate)[2]	4	8	8
Speed Grades	M-Temperature	-1	-1	-1
	I-Temperature	-1, -1L, -2	-1, -1L, -2	-1, -1L, -2

	Package[3]	Dimensions (mm)		**Available User I/O**: HRIO, GTP 6.6Gb/s	
	CS324[4][7]	15 x 15		210, 0	
	CS325[4][7]	15 x 15	150, 4		
	RS484[4][7]	19 x 19			285, 4
	FG484[5]	23 x 23	250, 4	285, 4	
	RB484[5]	23 x 23			285, 4
	RB676[6]	27 x 27			400, 8

Notes:

1. Supports PCI Express Base 2.1 specification at Gen1 and Gen2 data rates.
2. Represents the maximum number of transceivers available. Note that the majority of devices are available without transceivers. See the Package section of this table for details.
3. Other packages are available with leaded external balls, see DS180 *7 Series FPGAs Overview* for XC package details.
4. Devices in CS324 are footprint compatible with CSG324, similarly CS325 is compatible with CSG325, and RS484 is compatible with SBG484.
5. Devices in FGG484, FBG484, FG484, and RB484 are footprint compatible.
6. Devices in FGG676, FBG676, and RB676 are footprint compatible.
7. Devices in CS324, CS325, and RS484 packages are 0.8mm ball pitch, all others are 1mm ball pitch.

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7 Series FPGA Ordering Information

For footprint compatibility see XQ datasheet

XQ	7	V	###	-1	RF	###	M
Xilinx Defense-Grade	7 Series	A: Artix K: Kintex V: Virtex	Value Index	Speed Grade -1: Slowest -L1: Low Power -1 -2: Mid -L2: Low Power -2	CS: Standard Lid Pb internal & external Wire-bond Chip-Scale w/ 0.8mm ball pitch FG: Standard Lid Pb internal & external (for XQ) Flip-Chip w/ 1mm ball pitch RB: Ruggedized Lid Flip-Chip w/ 1mm ball pitch RS: Ruggedized Lid Flip-Chip w/ 0.8mm ball pitch RF: Ruggedized Lid Flip-Chip w/ 1.0mm ball pitch	Nominal Package Pin Count	Temperature Grade (M, I, E)

M = Military (Tj = –55°C to +125°C)
I = Industrial (Tj = –40°C to +100°C)
E = Extended (Tj = 0°C to +100°C)

Refer to Device Data Sheet Overview and Pinout Specifications for additional information.

Important: Verify all data in this document with the device data sheets found at www.xilinx.com

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Reference Links for XQ Zynq® SoC Devices

DS895, *XQ UltraScale™ Architecture Overview*

DS925, *Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching Characteristics*

DS926, *Zynq UltraScale+ RFSoC Data Sheet: DC and AC Switching Characteristics*

UG1075, *Zynq UltraScale+ MPSoC and RFSoC Packaging and Pinouts Product Specification*

UG1085, *Zynq UltraScale+ MPSoC and RFSoC Technical Reference Manual*

DS196, *XQ Zynq®-7000 AP SoC Data Sheet: Overview*

DS187, *Zynq®-7000 AP SoC (XQ7Z020) Data Sheet: DC and AC Switching Characteristics*

DS191, *Zynq®-7000 AP SoC (XQ7Z030, XQ7Z045, XQ7Z100) Data Sheet: DC and AC Switching Characteristics*

UG865, *Zynq®-7000 AP SoC Packaging and Pinouts Product Specification*

UG585, *Zynq®-7000 AP SoC Technical Reference Manual*

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Reference Links for XQ FPGA Devices

DS895, *XQ UltraScale™ Architecture Overview*

DS923, *Virtex UltraScale+ FPGAs Data Sheet: DC and AC Switching Characteristics*

DS922, *Kintex UltraScale+ FPGAs Data Sheet: DC and AC Switching Characteristics*

DS893, *Virtex UltraScale FPGAs Data Sheet: DC and AC Switching Characteristics*

DS892, *Kintex UltraScale FPGAs Data Sheet: DC and AC Switching Characteristics*

UG575, *UltraScale and UltraScale+ FPGAs Packaging and Pinouts Product Specification*

DS185, *XQ 7 Series FPGA Data Sheet: Overview*

DS183, *Virtex-7 FPGAs Data Sheet: DC and AC Switching Characteristics*

DS182, *Kintex-7 FPGAs Data Sheet: DC and AC Switching Characteristics*

DS181, *Artix-7 FPGAs Data Sheet: DC and AC Switching Characteristics*

UG475, *7 Series FPGAs Packaging and Pinouts Product Specification*

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