PRESERVATION OF PLACE AND ROUTE.
FUNCTIONAL AND PHYSICAL ISOLATION.
DYNAMIC RECONFIGURATION.
FULLY ROUTED PARTIAL BITSTREAM.

R² FLOWS: ENABLING SAFE AND RELIABLE SOC SOLUTIONS FOR CERTIFIABLE APPLICATIONS

R² Flows: Reusable and Reliable Design Flows

- Reduce system cost and NRE
- Reduce risk and certification burden
- Enhance system functionality and availability
- Based on 4th generation fail-safe heritage

R² Flows include:

- Partitioning and Preservation
- Isolation Design Flow
- Dynamic Partial Reconfiguration
- Qualified Bitstream Flow

R² Flows are:

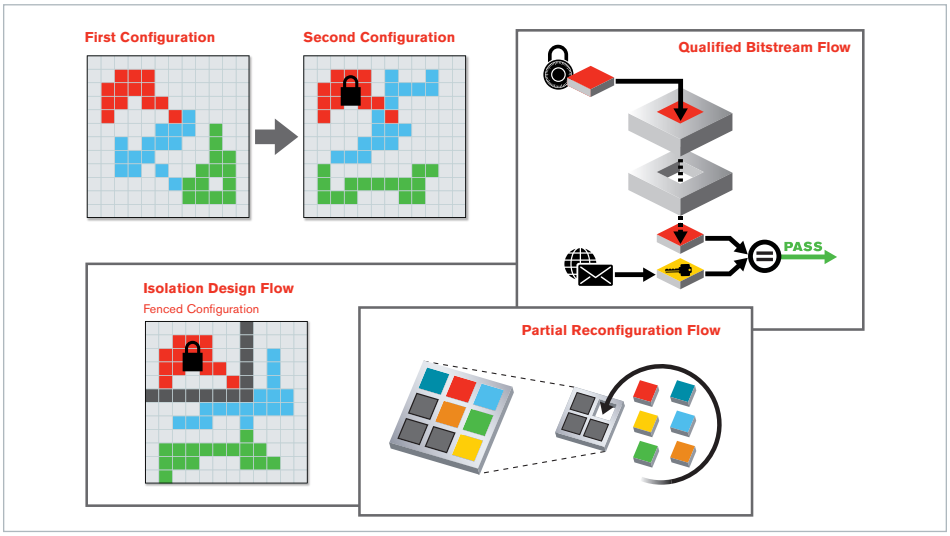
- Suitable for hi-rel applications such as avionics, automotive, industrial, medical
- Enabling complex SoC FPGA designs targeted for safe and reliable applications
- Supporting of IP reuse with reduced certification or verification burden
- Ideally suited for Xilinx's 7 series devices with scalable optimized architecture

Xilinx R² Flows are built on the foundation of design partitioning and preservation of placement and routing. These flows leverage Xilinx's extensive expertise and heritage in secure military applications.

Isolation Design Flow is a direct result of heritage work in Single Chip Cryptographic Milcom radio designs which rely on separation of red-side and black-side processing for assurance of data integrity within a single device. Similarly the Qualified Bitstream Flow is based on the core capabilities that enable delivery of a fully placed and routed partial bitstream, the Security Monitor IP Core. The fundamental enabling technology in Xilinx FPGA silicon and design environments allow us to support these flows as well as Dynamic Partial Reconfiguration.

R² Flows enable advanced, safe, and reliable SoC FPGA applications. They are suited for certifiable applications including avionics, automotive, industrial, and medical.

R² FLOWS



Four independent yet related design flows built on a common foundation. Mix and match the flows to meet system goals.

XILINX
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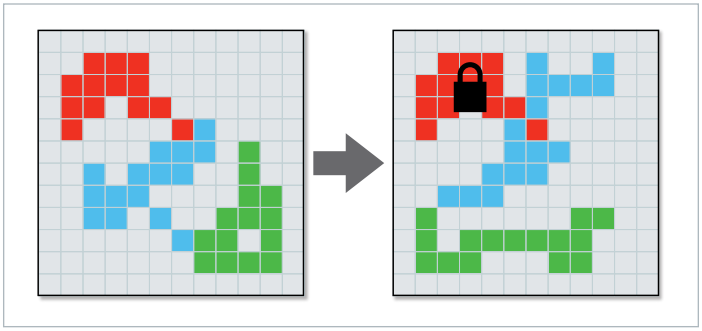
Partitioning and Preservation

Locked and preserved placement and routing for specified functional blocks. Example: Three functions implemented via a hierarchical design are placed an routed. One function, the red, uses preservation to retain its exact placement and routing. In rerouted design the other two functions can use all unutilized resources. The verified behavior of locked, red, function remains unchanged. The precise placement, and thus performance, is unchanged.

Based on the design rules, using existing tool flow, this flow reduces NRE for engineering changes, and it forms the foundation for other R^2 flows.

FIRST AND SECOND CONFIGURATIONS



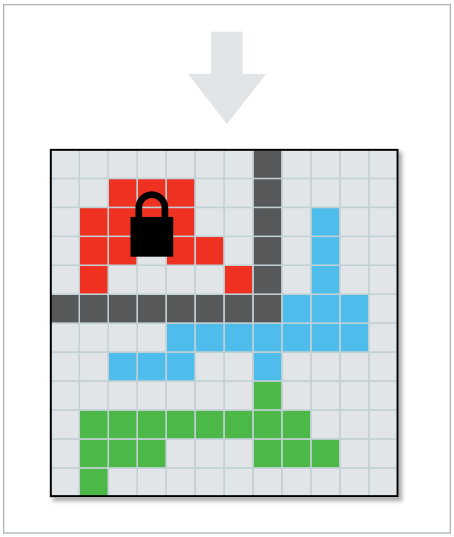
Isolation Design Flow

Supporting enhanced verification and mixed-level certification in a single device. Isolation Design Flow adds verifiable physical isolation, to partitioning and preservation.

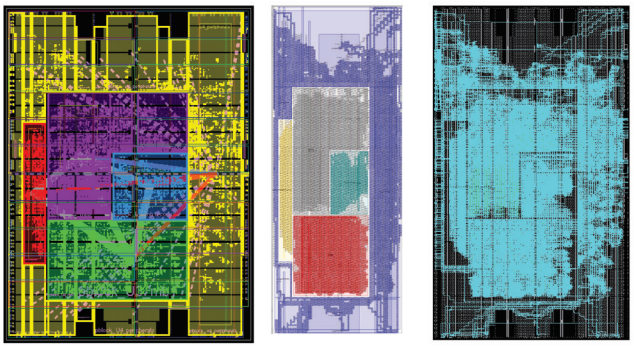
Approved for secure cryptographic systems that require information assurance.

- Utilizing a justifiable/certifiable design flow
- Leveraging an independent Isolation Verification Tool (IVT)
- Ensuring physical and functional isolation

ISOLATED CONFIGURATION



IDF DESIGN ITERATIONS



IDF XAPP584 design shown in Floorplaner, SVG, and FPGA Editor post implementation.

A commercial systems reference design, XAPP584, gives a tutorial; implementing a lockstep soft core MicroBlaze(tm) processor design with adherence to IDF design rules and walking through the full flow to verification using IVT.

Achieve:

- Isolation of critical and non-critical functions
- Reduction of common cause failure modes
- Separation of test and debug logic
- Enhanced verification capability
- Reduced NRE for design modifications

Well suited for:

- Avionics applications requiring DO-254
- Industrial systems requiring IEC 61508
- Other certifiable systems requiring functional safety and robust design

DYNAMIC PARTIAL RECONFIGURATION

Dynamic Partial Reconfiguration enables dynamically adaptive applications with on-the-fly/real-time reprogramming of hardware during operation.

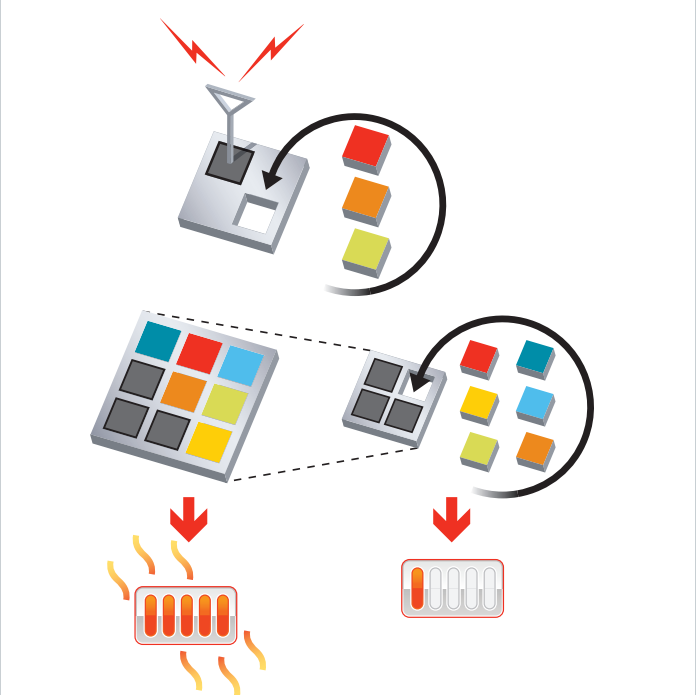
Allow multiple algorithms to run in a single hardware platform. Adapt functionality for a given operational scenario. Leverage a time multiplexed hardware implementation.

Achieve:

- Higher performance
- Lower cost
- Increased power efficiency

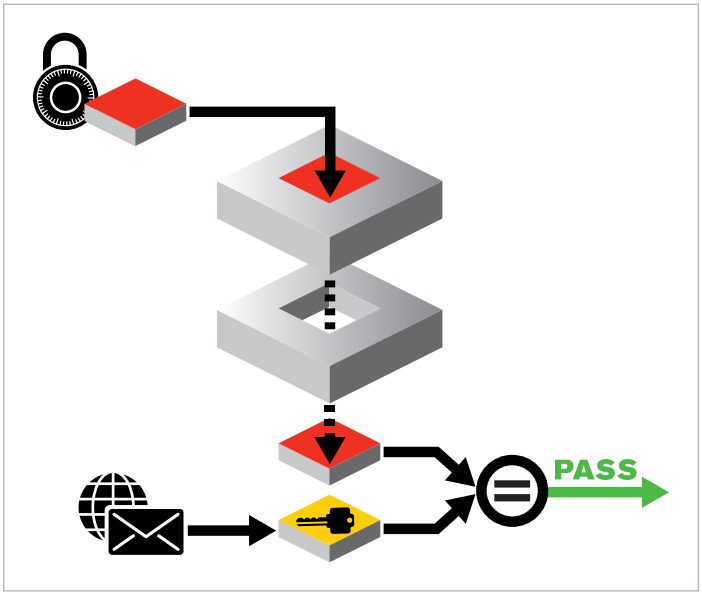
Well suited for:

- Software Defined Radio
- Imaging and Video systems
- Sensor Payloads
- Adaptive systems
- Self-healing applications
- Hardware muli-tasking



Swappable algorithms can enable smaller device sizes and reduced power.

QUALIFIED BITSTREAM FLOW



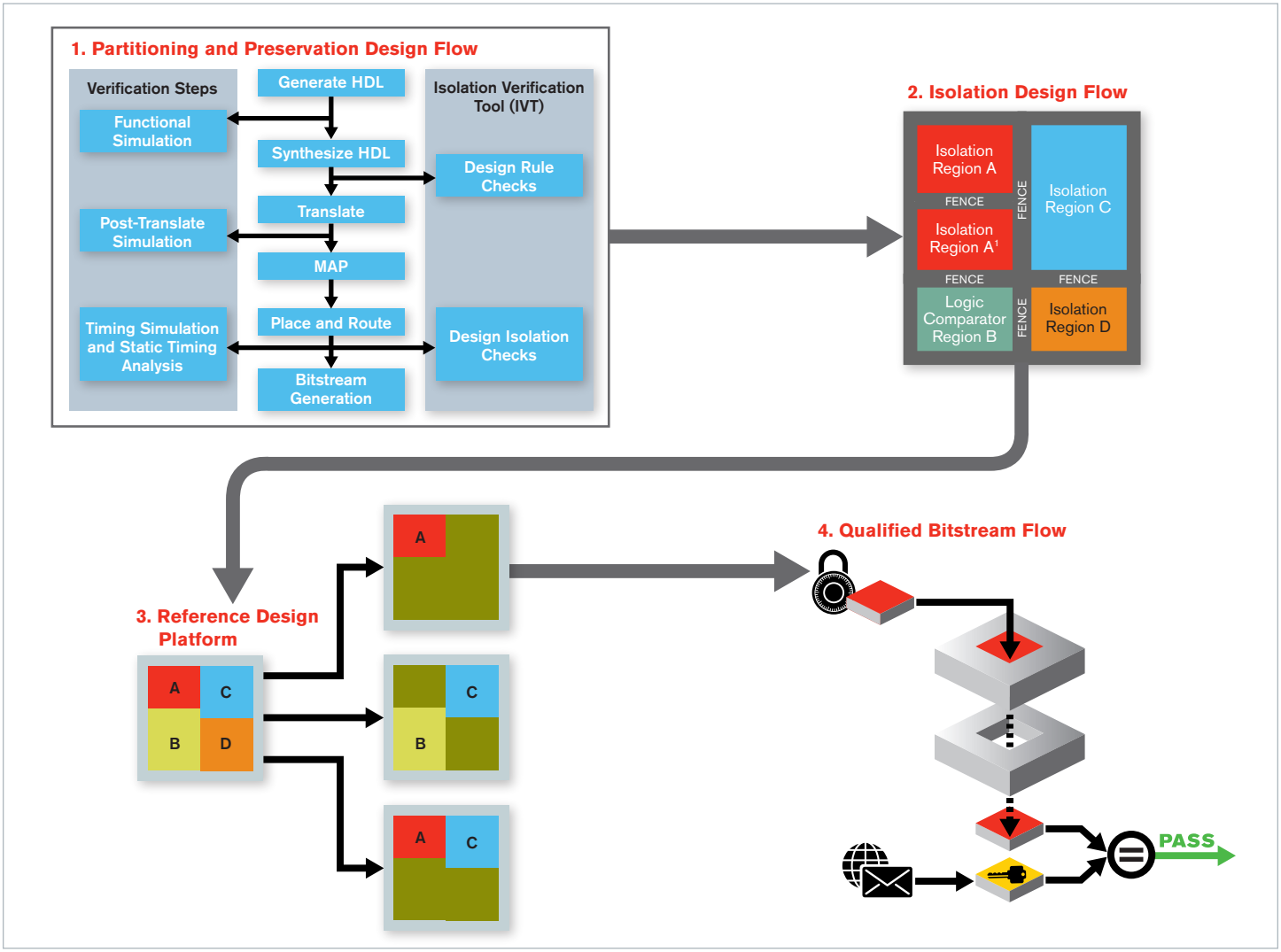
Qualified bitstream can be inserted in design and later extracted for comparison against golden source.

Qualified Bitstream Flow is a newly emerging advanced flow that allows for reuse of fully placed routed partial bitstreams. Security Monitor is the first and only IP core in world to be delivered as a fully placed and routed IP. With significant heritage Xilinx is now expanding the capability to other IP core and customer uses.

The flow follows design floor planning rules to allow insertion of partial bitstreams. IP solutions may be generated and verified to the bitstream level. After integration and fully building the final device bitstream, the partial bitstream can still be verified against the golden verified source, irrespective of design flow versions.

QBF is the ultimate reusable IP solution, with an unmatched degree of integrity and security.

R² DESIGN FLOW



Begin building advanced, efficient, cost-effective, scalable, certifiable SoC applications today.

Take the NEXT STEP

For documentation and more information about R² Flows, and for information regarding DO-254 and SEU Mitigation, visit the avionics site, and avionics developers site, accessible at: **www.xilinx.com/avionics/**

For information regarding licensing of Isolation Design Flow (IDF), or Dynamic Partial Reconfiguration, consult a local Xilinx sales rep.

For interests in the Qualified Bitstream Flow (QBF), please email **avionics@xilinx.com**

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