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Understanding the CoolRunner-II Timing Model

Summary

This document describes the CoolRunner™-II timing model. Understanding the CoolRunner-II timing model is essential to creating a CPLD design that meets the desired timing requirements.

Introduction

CPLD designers often require an understanding of the device timing model to compare design specific timing requirements. CPLD designers can use the CoolRunner-II timing model to create a design that fits required timing requirements and compare design critical paths. Designers can use the timing model to create equations of time delays for each logic path in a design. This document will describe the CoolRunner-II timing model in detail and provide examples for using this timing model.

A brief overview of the CoolRunner-II architecture as it pertains to the timing model will be described in the following section.

CoolRunner-II Architecture

The CoolRunner-II architecture consists of function blocks that are interconnected by a routing matrix called the Advanced Interconnect Matrix (AIM). Each function block contains a Programmable Logic Array (PLA) and 16 macrocells. A total of eight global signals are multiplexed with eight I/O pins and include three clocks, four output enables, and one set/reset signal. The CoolRunner-II architecture allows these global signals to be driven by internal logic. Figure 1 illustrates a block diagram of the CoolRunner-II architecture.

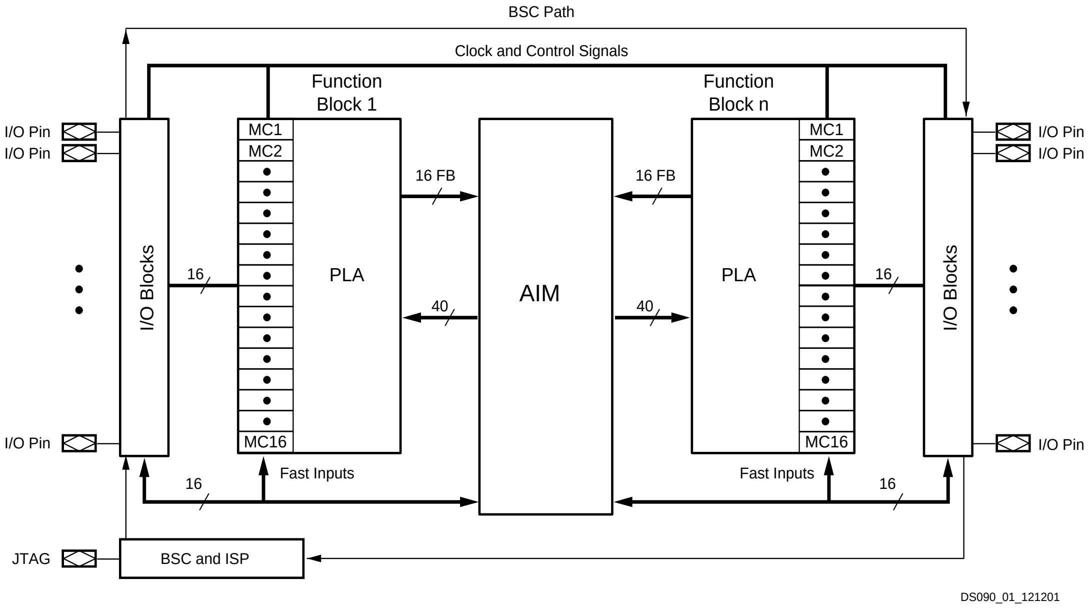

Figure 1: **CoolRunner-II Architecture**

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The function block product term and sum term array is a pure PLA (programmable AND array, programmable OR array). Each PLA has 40 inputs from the AIM (true and complement) and contains 56 unique product terms. Product terms can be used as macrocell clocks, control terms (reset, preset, asychronous clock, clock enable, or output enable), or as needed as logic by the macrocells in the function block.

Of the function block product terms, four are available as control terms. The control terms, CTC, CTR, CTS, and CTE, can be a macrocell clock, reset, preset, or output enable. In addition to these function block control terms, each macrocell has three dedicated product terms available as additional control terms, local to that macrocell. PTA can be used as the macrocell reset or preset, PTB for the macrocell output enable, and PTC for the clock enable or product term clock. Note that if these product terms are not needed as control terms, they are available for other logic. Figure 2 illustrates the CoolRunner-II macrocell.

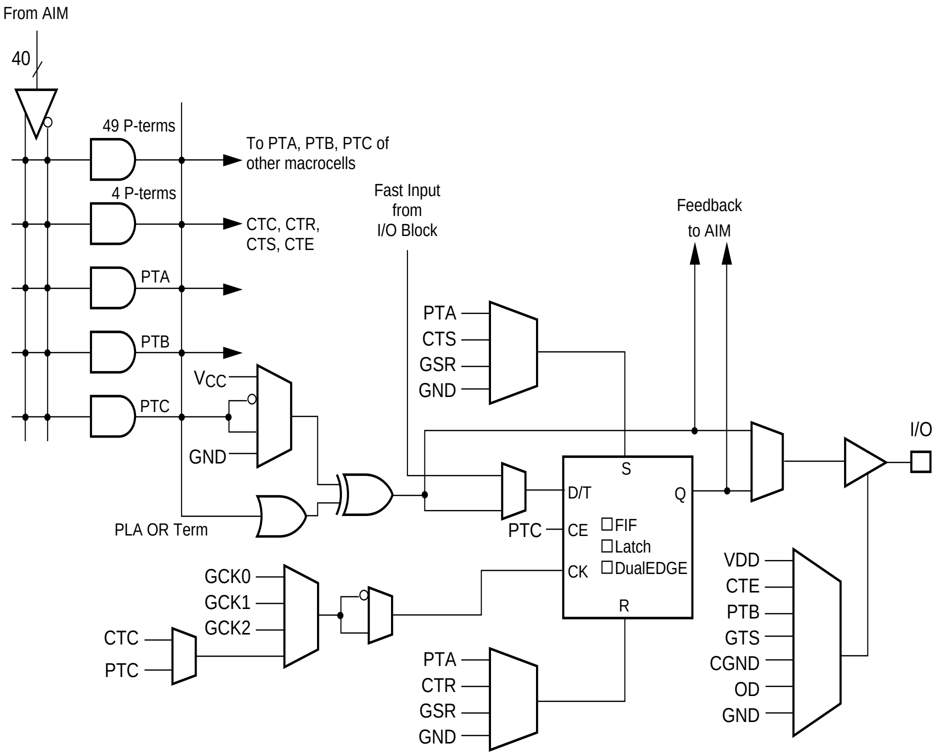

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Figure 2: **CoolRunner-II Macrocell**

Timing Model

Overview

External signals enter at the pins and are delivered through the I/O block to the AIM. From the AIM, they are dispatched to the various function blocks (FBs). As the signals enter the FBs, they incur incremental time delays depending on how the signals are used within the FB. For example, all logic signals must pass through the AND array where product terms are created and a time delay is incurred as the signal progresses. The number of product terms in a logic equation will impact the time delay encountered on the signal. With the CoolRunner-II architecture, each macrocell has a fast path that contains one product term, PTC (see Figure 2), in a logic equation. With this path, the OR term is bypassed and fed directly into the macrocell register. Logic equations with two or more product terms must enter the OR term and will therefore encounter an additional time delay.

There are additional timing requirements such as setup and clock-to-output times involved when passing signals through a flip-flop. The macrocell output is either directed to the I/O block and pin, or are fed back into the AIM switch matrix for additional logic operations.

Design timing can be manually analyzed as separate signals, each having unique timing parameters that are easily calculated. However, the Xilinx development tools provide a detailed timing report that tallies and summarizes all paths specified by the designer. The timing report is based on the model described here and is a convenient text based mechanism for isolating and displaying timing relationships.

Description

The timing model, shown in Figure 3, is used by the Xilinx development software which provides complete fitting for the CoolRunner-II family as well as timing models for simulation and detailed static timing reports.

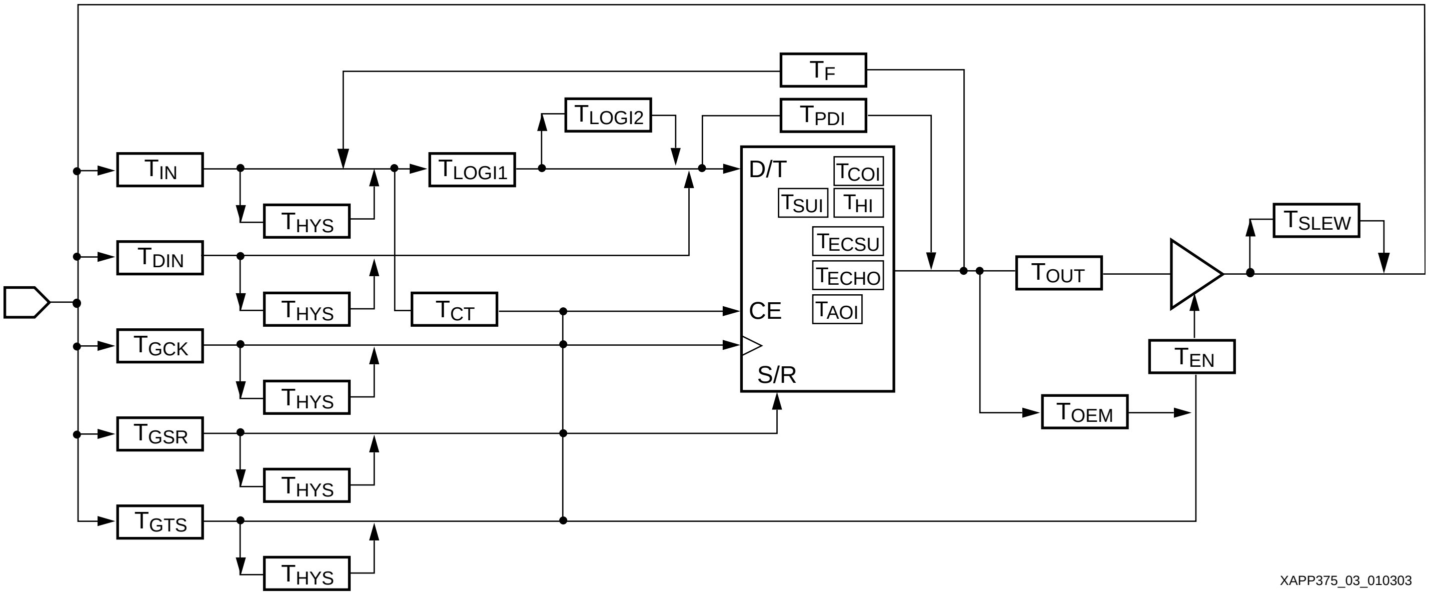


Figure 3: **CoolRunner-II Timing Model**

The timing model shown in Figure 3 represents the CoolRunner-II macrocell with additional time delays included to account for the AIM switch matrix and I/O buffers. As signals progress through a CoolRunner-II device, they encounter some of these delays which are tallied to arrive at a cumulative time delay for that signal. Table 1 provides a detailed definition of each parameter contained in Figure 3. The exact values for each device can be obtained from the specific data sheets.

Table 1: **CoolRunner-II Internal Timing Parameters**

Parameter	Description
Buffer Delays	
T_{IN}	Input buffer delay (see Table 2)
T_{DIN}	Direct input buffer delay (input registers) (see Table 2)
T_{GCK}	Global clock buffer delay (see Table 2)
T_{GSR}	Global set/reset buffer delay (see Table 2)
T_{GTS}	Global tristate buffer delay (see Table 2)
T_{OUT}	Output buffer delay (see Table 2)
T_{EN}	Output buffer enable/disable delay
Product Term Delays	
T_{CT}	Control term delay (single P-term or FB control term)

Table 1: **CoolRunner-II Internal Timing Parameters *(Continued)***

Parameter	Description
T_{LOGI1}	Internal logic delay (single P-term)
T_{LOGI2}	Multiple P-term delay adder
Internal Register and Combinatorial Delays	
T_{PDI}	Macrocell input to output valid
T_{SUI}	Macrocell register setup time
T_{HI}	Macrocell register hold time
T_{ECSU}	Macrocell register clock enable setup time
T_{ECHO}	Macrocell register clock enable hold time
T_{COI}	Macrocell register clock to output delay
T_{AOI}	Macrocell register set/reset to output delay
Feedback Delays	
T_F	AIM delay
T_{OEM}	Macrocell to global output enable delay
Time Delays	
T_{HYS}	Hysteresis time delay (see Table 2)
T_{SLEW}	Slew rate limited delay (see Table 2)

Table 2 illustrates various timing parameters associated with the available I/O standards on CoolRunner-II devices. Note that the SSTL and HSTL standards are only available on 128 macrocell and larger CoolRunner-II CPLDs. Values for the parameters shown in Table 2 are available in the specific product data sheet. Note that values shown in Table 2 are timing delay adders.

Table 2: **I/O Standard Related Timing Parameters**

Parameter	Description
1.5V I/O	
T_{IN15}	Input buffer adder for T_{IN}, T_{DIN}, T_{GCK}, T_{GSR}, and T_{GTS}
T_{HYS15}	Input hysteresis input adder for T_{IN}, T_{FIN}, T_{GCK}, T_{GSR}, and T_{GTS}
T_{OUT15}	Output delay adder
T_{SLEW15}	Output slew adder
1.8V LVCMOS	
T_{IN18}	Input buffer adder for T_{IN}, T_{DIN}, T_{GCK}, T_{GSR}, and T_{GTS}
T_{HYS18}	Input hysteresis input adder for T_{IN}, T_{FIN}, T_{GCK}, T_{GSR}, and T_{GTS}
T_{OUT18}	Output delay adder
T_{SLEW18}	Output slew adder
2.5V LVCMOS	
T_{IN25}	Input buffer adder for T_{IN}, T_{DIN}, T_{GCK}, T_{GSR}, and T_{GTS}
T_{HYS25}	Input hysteresis input adder for T_{IN}, T_{FIN}, T_{GCK}, T_{GSR}, and T_{GTS}
T_{OUT25}	Output delay adder

Table 2: **I/O Standard Related Timing Parameters *(Continued)***

Parameter	Description
T_{SLEW25}	Output slew adder
3.3V LVTTL/LVCMOS	
T_{IN33}	Input buffer adder for T_{IN}, T_{DIN}, T_{GCK}, T_{GSR}, and T_{GTS}
T_{HYS33}	Input hysteresis input adder for T_{IN}, T_{FIN}, T_{GCK}, T_{GSR}, and T_{GTS}
T_{OUT33}	Output delay adder
T_{SLEW33}	Output slew adder
SSTL2-I	
T_{INSS2}	Input buffer adder for T_{IN}, T_{DIN}, T_{GCK}, T_{GSR}, and T_{GTS}
T_{OUTSS2}	Output delay adder
SSTL3-I	
T_{INSS3}	Input buffer adder for T_{IN}, T_{DIN}, T_{GCK}, T_{GSR}, and T_{GTS}
T_{OUTSS3}	Output delay adder
HSTL-I	
T_{INHS1}	Input buffer adder for T_{IN}, T_{DIN}, T_{GCK}, T_{GSR}, and T_{GTS}
T_{OUTHS1}	Output delay adder

External Timing Parameters

Table 3 shows how key external timing parameters are derived from the internal timing parameters.

Table 3: **Expressions for External Timing Parameters**

Parameter	Description	Equation
T_{PD1}	Propagation delay time (single P-term)	$T_{IN} + T_{LOGI1} + T_{PDI} + T_{OUT}$
T_{PD2}	Propagation delay time (OR array)	$T_{IN} + T_{LOGI1} + T_{LOGI2} + T_{PDI} + T_{OUT}$
T_{SUD}	Direct input register setup time	$T_{DIN} + T_{SUI} - T_{GCK}$
T_{SU1}	Setup time (single P-term)	$T_{IN} + T_{LOGI1} + T_{SUI} - T_{GCK}$
T_{SU2}	Setup time (OR array)	$T_{IN} + T_{LOGI1} + T_{LOGI2} + T_{SUI} - T_{GCK}$
T_{HD}	Direct input register hold time	$T_{GCK} + T_{HI} - T_{DIN}$(1)
T_H	Hold time	$T_{GCK} + T_{HI} - T_{IN} - T_{LOGI1}$(1)
T_{CO}	Clock to output (global synchronous clock pin)	$T_{GCK} + T_{COI} + T_{OUT}$
T_{CYCLE1}	Minimum clock period (single P-term)	$T_{COI} + T_F + T_{LOGI1} + T_{SUI}$
T_{CYCLE2}	Minimum clock period (OR array)	$T_{COI} + T_F + T_{LOGI1} + T_{LOGI2} + T_{SUI}$
$f_{SYSTEM1}$	Maximum system frequency (single P-term)	$1/T_{CYCLE1}$
$f_{SYSTEM2}$	Maximum system frequency (OR array)	$1/T_{CYCLE2}$
f_{EXT1}	Maximum external frequency (single P-term)	$1/(T_{SU1} + T_{CO})$
f_{EXT2}	Maximum external frequency (OR array)	$1/(T_{SU2} + T_{CO})$
f_{TOGGLE}	Maximum register toggle frequency	$1/(2 * T_{CW})$
T_{PSUD}	Direct input register P-term clock setup time	$T_{DIN} + T_{SUI} - T_{IN} - T_{CT}$

Table 3: **Expressions for External Timing Parameters *(Continued)***

Parameter	Description	Equation
T_{PSU1}	P-term clock setup time (single P-term)	$T_{IN} + T_{LOGI1} + T_{SUI} - T_{IN} - T_{CT}$
T_{PSU2}	P-term clock setup time (OR array)	$T_{IN} + T_{LOGI1} + T_{LOGI2} + T_{SUI} - T_{IN} - T_{CT}$
T_{PHD}	Direct input register P-term clock hold time	$T_{IN} + T_{CT} + T_{HI} - T_{DIN}$ + skew
T_{PH}	P-term clock hold	$T_{IN} + T_{CT} + T_{HI} - T_{IN} - T_{LOGI1}$(1)
T_{PCO}	P-term clock to output	$T_{IN} + T_{CT} + T_{COI} + T_{OUT}$
T_{OE}/T_{OD}	Global OE to output enabled/disabled	$T_{GTS} + T_{EN}$
T_{POE}/T_{POD}	P-term OE to output enabled/disabled	$T_{IN} + T_{CT} + T_{EN}$
T_{MOE}/T_{MOD}	Macrocell driven OE to output enabled/disabled	$T_{GCK} + T_{COI} + T_{OEM} + T_{EN}$
T_{PAO}	P-term set/reset to output set/reset	$T_{IN} + T_{CT} + T_{AOI} + T_{OUT}$
T_{AO}	Global set/reset to output set/reset	$T_{GSR} + T_{AOI} + T_{OUT}$
T_{SUEC}	Register clock enable setup time	$T_{IN} + T_{CT} + T_{ECSU} - T_{GCK}$
T_{HEC}	Register clock enable hold time	$T_{GCK} + T_{ECHO} - T_{IN} - T_{CT}$
T_{CW}	Global clock pulse width (high or low)	Please see product data sheet
T_{PCW}	P-term clock pulse width (high or low)	Please see product data sheet
T_{DGSU}	Input setup required before DataGate latch assertion	Please see product data sheet
T_{DGH}	Input hold relative to DataGate latch assertion	Please see product data sheet
T_{DGR}	DataGate recovery to new data relative to data input pin	Please see product data sheet
T_{DGW}	DataGate high pulse width	Please see product data sheet
T_{CDRSU}	Setup time of CDRST before negative going GCK2	Please see product data sheet
T_{CDRH}	Hold time of CDRST after negative going GCK2	Please see product data sheet

Notes:

1. All CoolRunner-II devices guarantee a zero hold time, even though the equations shown here may create a negative hold time value.

Please note that these times will change if multiple feedback passes (internal nodes) are used.

The following sections provide a few examples of how the device timing is calculated. These calculations are automatically done for the user by software development tools but examples are provided here to help the user better understand how the software calculates device timing. Please note these examples do not cover every possible case.

Combinatorial Timing Examples

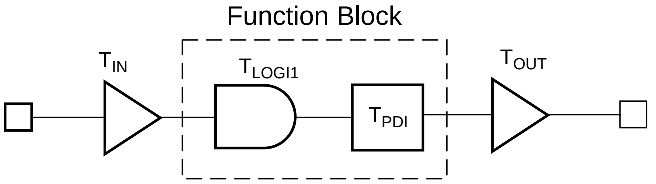
This section provides various combinatorial timing examples. The examples provided here include propogation delay with a single P-term, multiple P-terms, and multiple levels of logic.

One combinatorial timing example is propagation delay, or T_{PD}. CoolRunner-II T_{PD} is seperated into two individual timing parameters, T_{PD1} and T_{PD2}. T_{PD1} is calculated based on a single P-term path in the PLA structure. T_{PD2} is calculated based on more than one P-term existing in the data path.

Single Product Term Propogation Delay

The CoolRunner-II architecture provides a fast path T_{PD} with a single product term logic equation. With a single P-term logic equation, the OR term can be bypassed, and the P-term is fed directly in the macrocell using PTC (see Figure 2).

T_{PD1} is calculated as the sum of the input buffer time delay (T_{IN}), the single P-term logic time delay (T_{LOGI1}), the bypass path of the macrocell (T_{PDI}), and the output buffer time delay (T_{OUT}), as shown in Figure 4. Note that the input buffer delay is combined with the AIM time delay since the entering signal passes through the AIM switch matrix.



$$T_{PD1} = T_{IN} + T_{LOGI1} + T_{PDI} + T_{OUT}$$

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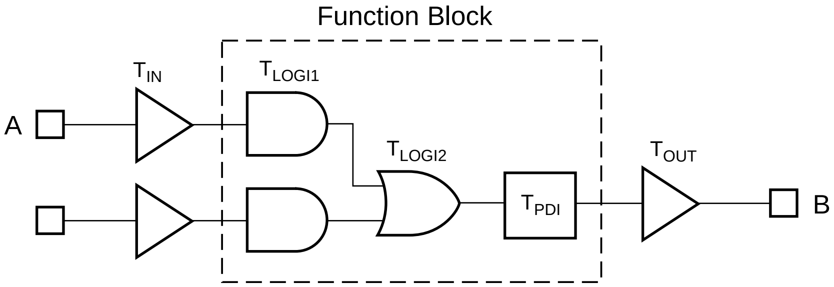
Figure 4: **T_{PD1} with a Single Product Term**

Multiple Product Term Propogation Delay

Figure 5 illustrates a variation to the simple T_{PD1} example with the addition of more product terms. The time delay from input A is slightly altered with T_{PD2}, which accounts for additional product terms. T_{PD2} is the same independent of the number of product terms, ranging from 2 to 56.



$$T_{PD2} = T_{A \rightarrow B} = T_{IN} + T_{LOGI1} + T_{LOGI2} + T_{PDI} + T_{OUT}$$

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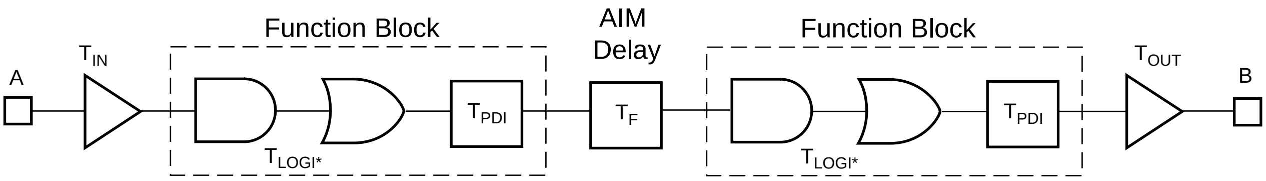
Figure 5: **T_{PD2} with 2 to 56 Product Terms**

Multiple Logic Level Propogation Delay

If combinational data requires multiple passes of logic, T_{PD} will increase accordingly. Figure 6 illustrates the case where T_{PD} is calcuated based on cascaded levels of logic. In this case, there is a single pass through the input buffer, a pass through the function block logic, a pass through the feedback path, an additional pass through the function block logic, and the output buffer.



$$T_{PD} = T_{A \rightarrow B} = T_{IN} + T_{LOGI*} + T_{PDI} + T_F + T_{LOGI*} + T_{PDI} + T_{OUT}$$

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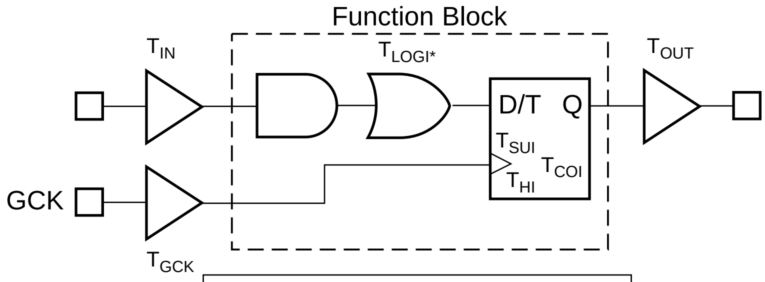
Figure 6: **T_{PD} with 2 Levels of Logic**

Note: $T_{LOGI*} = T_{LOGI1}$ if a single P-term is used, and $T_{LOGI*} = T_{LOGI1} + T_{LOGI2}$ if 2 to 56 P-terms are used.

Registered Timing Examples

Simple Registered Path

A simple registered timing example is shown in Figure 7. Figure 7 illustrates a macrocell flip-flop with a CoolRunner-II global synchronous clock signal, GCK. The equations for T_{SU}, T_{CO}, and T_H are valid for this arrangement. In this example, the equations for T_{SU}, T_{CO}, and T_H are not for fast input register or any special clocking features, ie. divider or doubler. The equations shown in Figure 7 are closely related to T_{SU1}/T_{SU2}, T_{CO}, and T_H described in Table 3.



$$T_{SU} = T_{IN} + T_{LOGI*} + T_{SUI} - T_{GCK}$$

$$T_{CO} = T_{GCK} + T_{COI} + T_{OUT}$$

$$T_H = T_{GCK} + T_{HI} - T_{IN} - T_{LOGI*}$$

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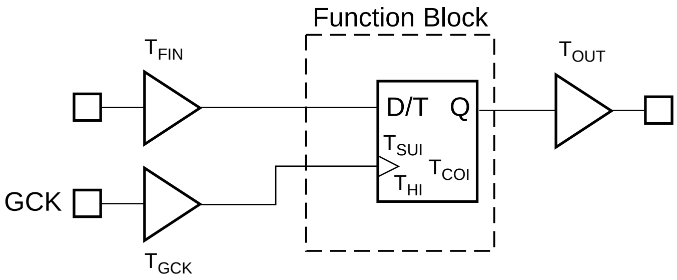
Figure 7: **Simple Registered Path**

Direct Input Register

Figure 8 illustrates the CoolRunner-II direct input register architecture feature. Direct input registers allow a designer to capture data from a high speed external bus with minimal T_{SU}. The equations shown in Figure 8 are closely related to T_{SUD}, T_{CO}, and T_{HD} described in Table 3.



$$T_{SU} = T_{FIN} + T_{SUI} - T_{GCK}$$

$$T_{CO} = T_{GCK} + T_{COI} + T_F + T_{LOGI*} + T_{OUT}$$

$$T_H = T_{GCK} + T_{HI} - T_{FIN}$$

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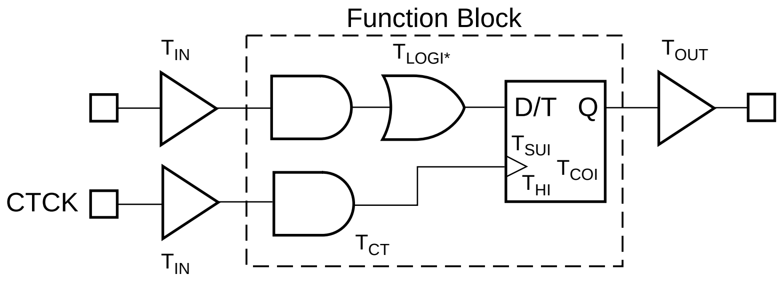
Figure 8: **Direct Input Register Path**

Product Term Clocking

Another architectural feature available in CoolRunner-II is product term register clocking. Product terms clocks available in each CoolRunner-II macrocell include, CTC and PTC shown in Figure 2. PTC is dedicated to each macrocell, while CTC is shared among macrocells within a function block. Figure 9 illustrates the timing parameters for product term clocking on a single flip-flop. This implementation is similar to Figure 7 except the clock source is now a product/control term. The timing parameters, T_{PSU}, T_{PCO}, and T_{PH} shown in Figure 9 are closely related to the equations for T_{PSU1}/T_{PSU2}, T_{PCO}, and T_{PH} described in Table 3.



$$\boxed{T_{PSU} = T_{IN} + T_{LOGI*} + T_{SUI} - T_{IN} - T_{CT}}$$

$$\boxed{T_{PCO} = T_{IN} + T_{CT} + T_{COI} + T_{OUT}}$$

$$\boxed{T_{PH} = T_{IN} + T_{CT} + T_{HI} - T_{IN} - T_{LOGI*}}$$

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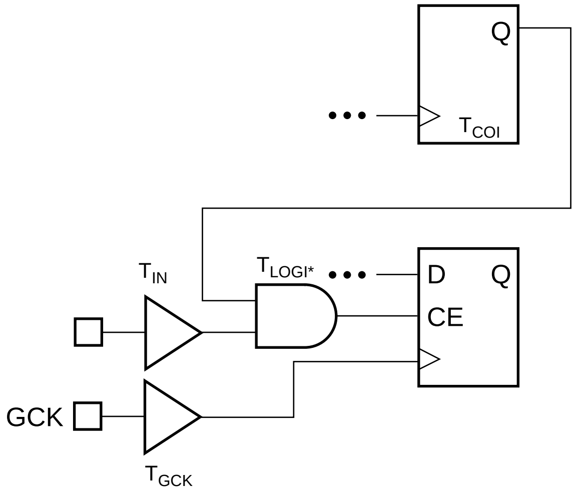
Figure 9: **Product Term Clocking**

Register Clock Enable

CoolRunner-II CPLDs provide true clock enables at each flip-flop as shown in Figure 10. Each macrocell has one dedicated clock enable, PTC. The clock enable has both setup (T_{SUEC}) and hold (T_{HEC}) timing parameters. The T_{SUEC} and T_{HEC} equations shown in Figure 10 are closely related to T_{SUEC} and T_{HEC} shown in Table 3.



$$\boxed{T_{SUEC} = T_{IN} + T_{LOGI*} + T_{ECSU} - T_{GCK}}$$

$$\boxed{T_{HEC} = T_{GCK} + T_{ECHO} - T_{IN} - T_{LOGI*}}$$

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Figure 10: **Clock Enable Timing Parameters**

Registered Logic with Multiple Levels

Figure 11 illustrates multiple levels of logic clocked by the global clock, GCK. The calculation for maximum system frequency is shown in Figure 11. Maximum system frequency is determined by the time delay of one flip-flop output to the next flip-flip input. As shown in

Figure 11, f_{SYSTEM} is determined by the first flip-flop output, T_{CO}, the AIM feedback delay, T_F, the delay through the PLA, T_{LOGI*}, and the register setup time, T_{SUI}.

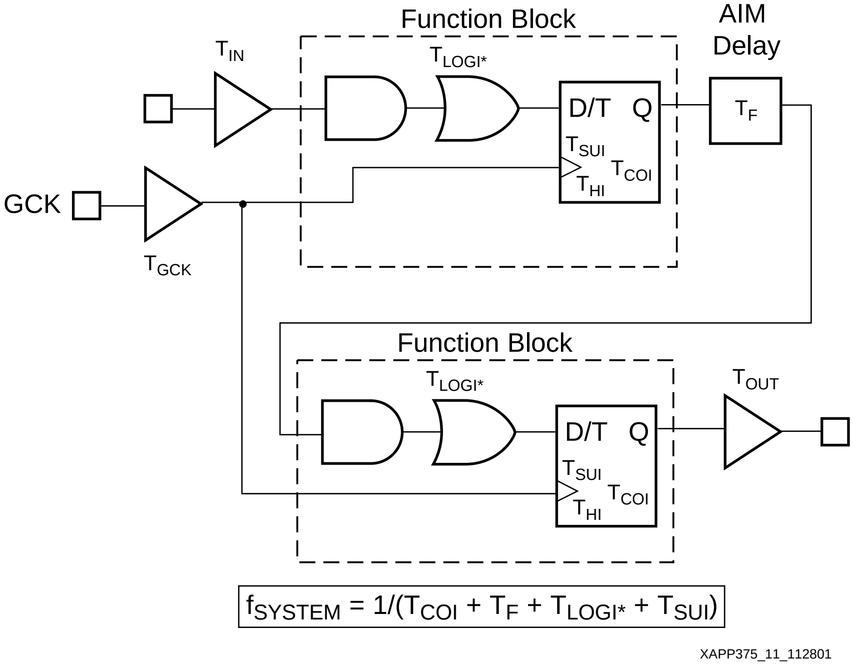

Figure 11: **Multiple Logic Levels**

I/O Related Timing Examples

Global Output Enable

Output enable timing can be calculated for both the CoolRunner-II global output enable, GTS and product term driven OE control. The timing delay from the CoolRunner-II global output enable, GTS to enabling or disabling the output is shown in Figure 12.

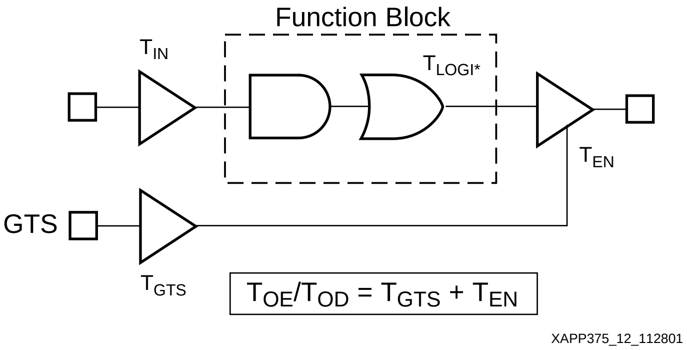

Figure 12: **Global Output Enable Timing**

Product Term Output Enable

For product output enable control, each macrocell has one dedicated OE and one function block OE control shown in Figure 2. The timing parameters when using one of these product term driven output enables is shown in Figure 13.

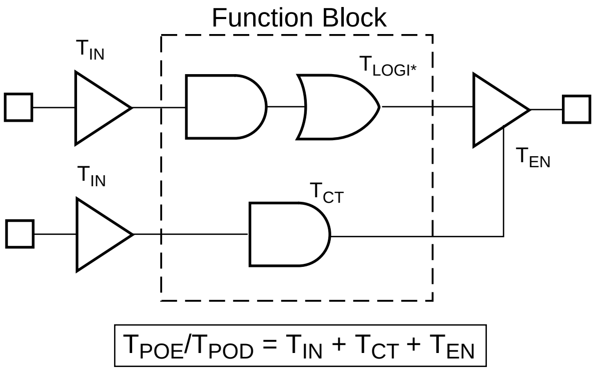

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Figure 13: **Product Term Output Enable Timing**

Macrocell Driven Output Enable

The CoolRunner-II architecture also allows a macrocell to drive the global output enable. The macrocell output can be routed to one of the four available global output enables, GTS[3:0]. Figure 14 illustrates this case and the associated T_{MOE}/T_{MOD} timing parameters. Note the lower function block drawing is for the data output.

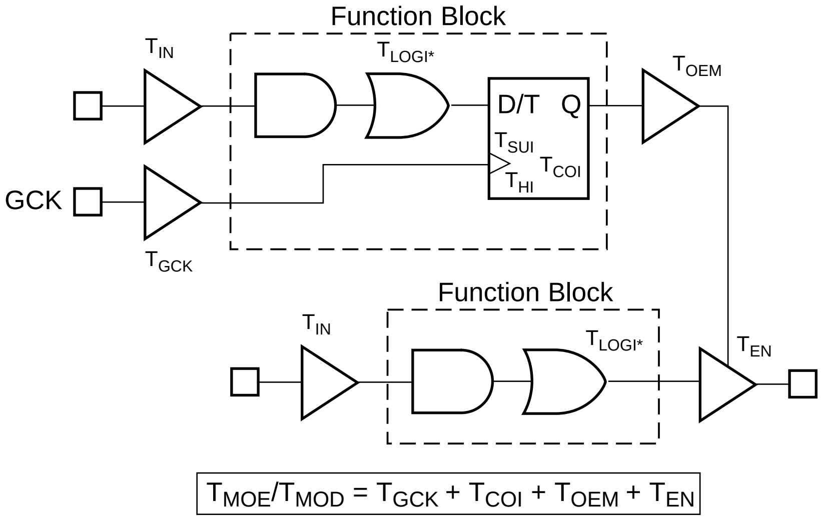

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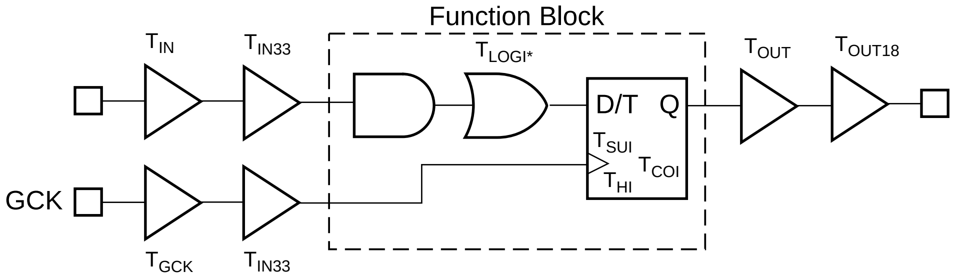
Figure 14: **Macrocell Driven Ouput Enable Timing**

I/O Standard Timing

Figure 15 illustrates a registered timing example using multiple I/O standards. This example utilizes 3.3V LVCMOS tolerant inputs and drives 1.8V LVCMOS outputs. Note the addition of the 3.3V LVCMOS timing delay, T_{IN33} on both the data and GCK inputs. Also note the addition of the 1.8V LVCMOS output delay adder, T_{OUT18}. The associated T_{SU}, T_{CO} and T_H timing parameters are shown in Figure 15.



$$\boxed{T_{SU} = T_{IN} + T_{IN33} + T_{LOGI*} + T_{SUI} - T_{GCK} - T_{IN33}}$$

$$\boxed{T_{CO} = T_{GCK} + T_{IN33} + T_{COI} + T_{OUT} + T_{OUT18}}$$

$$\boxed{T_H = T_{GCK} + T_{IN33} + T_{HI} - T_{IN} - T_{IN33} - T_{LOGI*}}$$

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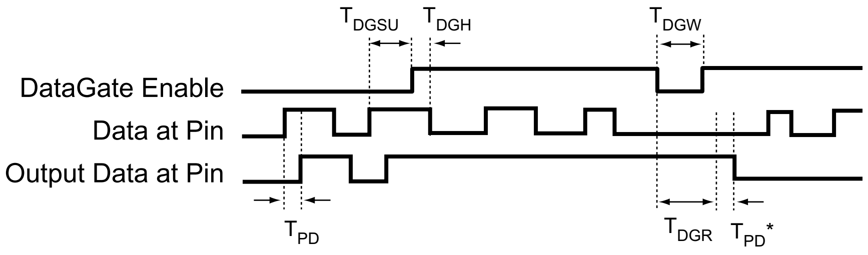
Figure 15: **I/O Standard Timing Example**

DataGate Characteristics

For more information on using DataGate in CoolRunner-II devices, refer to the family data sheet found on **http://www.xilinx.com**.

Figure 16 illustrates the timing requirements when using DataGate. A description of each timing parameter can be found in Table 3, page 5. The timing parameter, T_{DGR}, is referred to as the DataGate latch recovery time. T_{DGR} represents the recovery time of the DataGate latch output with respect to the DataGate enable input, DGE. The delay, T_{PD}*, shown in Figure 16 illustrates the delay incurred from the DataGate latch output to the pin output data.



$$\boxed{T_{PD}^{*} = T_{LOGI*} + T_{PDI} + T_{OUT}}$$

$$\boxed{T_{PD} \text{ (from deasserted DGE)} = T_{DGR} + T_{LOGI*} + T_{PDI} + T_{OUT}}$$

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Figure 16: **DataGate Timing Requirements**

Clock Divider Reset Characteristics

The clock divider reset signal, CDRST, is available for use with the global clock divider in CoolRunner-II devices. The CDRST is an active high reset signal for the clock divider circuit on GCK2. The CDRST signal is asserted low (disable reset condition) and is recognized by the clock divider on the next falling edge of the incoming clock, GCK2. Once this condition is met, the output of the clock divider will toggle at the specified frequency.

Figure 17 illustrates the setup and hold time requirements with using the clock divider reset, CDRST, on CoolRunner-II devices.

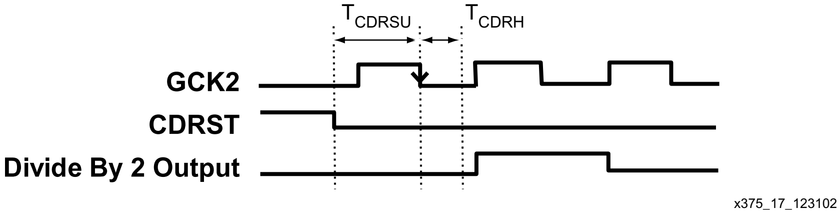

Figure 17: **CDRST Timing Requirements**

These examples should start to illustrate how timing parameters are calcuated from the Xilinx software tools. When calculating register hold times, skew should also be accounted in the equation. Other timing delays, such as T_{SLEW} are easily added to the output timing requirements.

Conclusion

Studying the CoolRunner-II timing model should provide a basic understanding of how timing parameters are calculated. Understanding the timing model allows designers to maximize system performance in any CoolRunner-II CPLD design.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
12/19/01	1.0	Initial Xilinx release.
02/04/02	1.1	Changes made to Table 3, page 5. Removed T_{SUEC1} and T_{HEC1} timing parameters. Renamed T_{SUEC2} to T_{SUEC} and T_{HEC2} to T_{HEC}. Modified T_{SUEC} and T_{HEC} equations. Modified T_{PH1} equation.
06/03/02	1.2	Changes made to Table 3, page 5. Renamed T_{SU1} to T_{SUF}. Added T_{SU1} parameter. Renamed T_{CYCLE} to T_{CYCLE2}. Added T_{CYCLE1} parameter. Renamed F_{SYSTEM} to $T_{SYSTEM2}$. Added $F_{SYSTEM1}$ parameter. Renamed F_{EXT} to F_{EXT2}. Added F_{EXT1} parameter. Renamed T_{PSU1} to T_{PSUF}. Added T_{PSU1} parameter. Added F_{TOGGLE} timing parameter. Renamed T_{H1} to T_{HF}. Renamed T_{H2} to T_H. Renamed T_{PH1} to T_{PHF}. Renamed T_{PH2} to T_{PH}.
01/3/03	1.3	Added 1.5V I/O timing parameters in Table 2, page 4. Added DataGate timing parameters and illustration. Added clock divider reset timing parameters and illustration. Changed all references from "Fast Input Register" to "Direct Input Register". Changes made to Table 3, page 5. Renamed T_{FIN} to T_{DIN}. Renamed T_{SUF} to T_{SUD}. Renamed T_{HF} to T_{HD}. Renamed T_{PSUF} to T_{PSUD}. Renamed T_{PHF} to T_{PHD}.
02/11/03	1.4	Updated Figure 16 T_{DGW} specification.
2/28/03	1.5	Removed timing parameters T_{CDIV} and T_{RAI}.