# Versal ACAP Packaging and Pinouts

## *Architecture Manual*

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# Revision History

The following table shows the revision history for this document.

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# Overview

## Introduction to Versal ACAP

Versal™ adaptive compute acceleration platforms (ACAPs) combine Scalar Engines, Adaptable Engines, and Intelligent Engines with leading-edge memory and interfacing technologies to deliver powerful heterogeneous acceleration for any application. Most importantly, Versal ACAP hardware and software are targeted for programming and optimization by data scientists and software and hardware developers. Versal ACAPs are enabled by a host of tools, software, libraries, IP, middleware, and frameworks to enable all industry-standard design flows.

Built on the TSMC 7 nm FinFET process technology, the Versal portfolio is the first platform to combine software programmability and domain-specific hardware acceleration with the adaptability necessary to meet today's rapid pace of innovation. The portfolio includes six series of devices uniquely architected to deliver scalability and AI inference capabilities for a host of applications across different markets—from cloud—to networking—to wireless communications—to edge computing and endpoints.

The Versal architecture combines different engine types with a wealth of connectivity and communication capability and a network on chip (NoC) to enable seamless memory-mapped access to the full height and width of the device. Intelligent Engines are SIMD VLIW AI Engines for adaptive inference and advanced signal processing compute, and DSP Engines for fixed point, floating point, and complex MAC operations. Adaptable Engines are a combination of programmable logic blocks and memory, architected for high-compute density. Scalar Engines, including Arm® Cortex™-A72 and Cortex-R5F processors, allow for intensive compute tasks.

The Versal AI Core series delivers breakthrough AI inference acceleration with AI Engines that deliver over 100x greater compute performance than current server-class of CPUs. This series is designed for a breadth of applications, including cloud for dynamic workloads and network for massive bandwidth, all while delivering advanced safety and security features. AI and data scientists, as well as software and hardware developers, can all take advantage of the high-compute density to accelerate the performance of any application.

The Versal Prime series is the foundation and the mid-range of the Versal platform, serving the broadest range of uses across multiple markets. These applications include 100G to 200G networking equipment, network and storage acceleration in the Data Center, communications test equipment, broadcast, and aerospace & defense. The series integrates mainstream 58G transceivers and optimized I/O and DDR connectivity, achieving low-latency acceleration and performance across diverse workloads.

The Versal Premium series provides breakthrough heterogeneous integration, very high-performance compute, connectivity, and security in an adaptable platform with a minimized power and area footprint. The series is designed to exceed the demands of high-bandwidth, compute-intensive applications in wired communications, data center, test & measurement, and other applications. Versal Premium series ACAPs include 112G PAM4 transceivers and integrated blocks for 600G Ethernet, 600G Interlaken, PCI Express® Gen5, and high-speed cryptography.

The Versal architecture documentation suite is available at: https://www.xilinx.com/versal.

## Navigating Content by Design Process

Xilinx® documentation is organized around a set of standard design processes to help you find relevant content for your current development task. This document covers the following design processes:

- **System and Solution Planning:** Identifying the components, performance, I/O, and data transfer requirements at a system level. Includes application mapping for the solution to PS, PL, and AI Engine. Topics in this document that apply to this design process include:
  - Device/Package Combinations
  - Footprint Compatibility between Packages
  - Chapter 2: Die Level Bank Numbering and Device Diagrams
- **Board System Design:** Designing a PCB through schematics and board layout. Also involves power, thermal, and signal integrity considerations. Topics in this document that apply to this design process include:
  - Chapter 1: Overview describes the architecture, package resources, and footprint compatibility between packages.
  - Device Diagrams Overview, Chapter 3: Package Files, and Chapter 4: Device Diagrams describes the package pinouts in textual and graphical format.
  - Chapter 5: Mechanical Drawings includes the physical dimensions for each package.
  - Chapter 6: Package Marking and Chapter 7: Packing and Shipping.
  - Chapter 8: Soldering Guidelines, Chapter 9: Recommended PCB Design Rules for BGA, and Chapter 10: Edge Bonding Guidelines provide PCB implementation information.

- Chapter 11: Thermal Specifications, Chapter 12: Thermal Management Strategy, Chapter 13: Heat Sink Guidelines for Bare-die VB Packages, and Chapter 14: Mechanical and Thermal Design Guidelines for Lidless Flip-chip Packages include guidelines for overall thermal management.

# Package and Pinout Overview

This section describes the packages and pinouts for various organic flip-chip 0.80 mm, 0.92 mm, and 1.00 mm pitch BGA packages.

**IMPORTANT!** *All standard packages are lead-free (signified by an additional V in the package name). All devices supported in a particular package are footprint compatible. Each device is split into I/O banks to allow for flexibility in the choice of I/O standards. See the Versal ACAP SelectIO Resources Architecture Manual (AM010).*

The flip-chip assembly materials for the Versal devices are manufactured using ultra-low alpha (ULA) materials defined as <0.002 cph/cm$^2$ or materials that emit less than 0.002 alpha-particles per square centimeter per hour.

**IMPORTANT!** *All packages are available with eutectic BGA balls. To order these packages, the device type starts with an XQ vs. XC or XA, and the Pb-free signifier in the package name is Q.*

# Device/Package Combinations

The following table shows the size and BGA pitch of the Versal device packages. All packages are available with eutectic BGA balls. For these packages, the Pb-free signifier in the package name is a Q.

*Table 1:* **Package Specifications**

| Packages | Description | Package Specifications | | | |
|---|---|---|---|---|---|
| | | **Package Type** | **Pitch (mm)** | **Size (mm)** | **LSC Ball Grid Size (balls)** |
| SFVB625 | Super-fine pitch with forged lid | BGA | 0.8 | 21 × 21 | – |
| VBVA1024 | Fine pitch bare-die | | 0.92 | 31 × 31 | 4 × 4 |
| VFVB1024 | Fine pitch with forged lid | | | 31 × 31 | 4 × 4 |
| VFVB1369 | Fine pitch with forged lid | | | 35 × 35 | 5 × 5 |
| VSVE1369 | Fine pitch lidless with stiffener ring | | | 35 × 35 | 5 × 5 |
| VSVA1596 | Fine pitch lidless with stiffener ring | | | 37.5 × 37.5 | 5 × 5 |
| VIVA1596 | Overhang fine pitch lidless with stiffener ring | | | 40 × 40 | 6 × 6 |
| VFVA1760 | Fine pitch with forged lid | | | 40 × 40 | 6 × 6 |
| VFVC1760 | Fine pitch with forged lid | | | 40 × 40 | 6 × 6 |
| VSVD1760 | Fine pitch lidless with stiffener ring | | | 40 × 40 | 6 × 6 |
| VSVA2197 | Fine pitch lidless with stiffener ring | | | 45 × 45 | 7 × 7 |
| VSVA2785 | Fine pitch lidless with stiffener ring | | | 50 × 50 | 9 × 9 |

**IMPORTANT!** *Packages with land-side capacitors (LSC) include a region of the BGA matrix where the BGA balls are replaced with capacitors. The LSC Ball Grid Size column in Table 1 describes the size of the LSC region in terms of the number of BGA balls replaced by capacitors. Therefore, packages with LSCs have fewer balls than the package name implies (for example, the VSVA2197 has 7 x 7 = 49 fewer balls than the implied 2197 balls).*

# Gigabit Transceiver Channels by Device/Package

The following table lists the quantity of gigabit transceiver channels for the Versal devices. There is one set of MGTRXP, MGTRXN, MGTTXP, and MGTTXN pins for the GTY or GTM channels in all devices. All packages are available with eutectic BGA balls where the device type is XQ and the Pb-free signifier in the package name is a Q.

*Table 2:* **Serial Transceiver Channels (GTY and GTM) by Device/Package**

| Device | Package | GTY Channels | GTM Channels |
|---|---|---|---|
| VM1102 | SFVB625 | 4 | 0 |
| VC1352 | VBVA1024 | 8 | 0 |
| VC1502 | | 8 | 0 |

*Table 2:* **Serial Transceiver Channels (GTY and GTM) by Device/Package** *(cont'd)*

| Device | Package | GTY Channels | GTM Channels |
|---|---|---|---|
| VM1102 | VFVB1024 | 12 | 0 |
| VM1302 | | 16 | 0 |
| VM1402 | | 16 | 0 |
| VM1302 | VFVB1369 | 24 | 0 |
| VM1402 | | 24 | 0 |
| VM1502 | | 16 | 0 |
| VM1302 | VFVF1369 | 8 | 0 |
| VM1402 | | 8 | 0 |
| VC1352 | VSVE1369 | 8 | 0 |
| VC1702 | | 24 | 0 |
| VC1502 | VSVG1369 | 24 | 0 |
| VC1502 | VSVA1596 | 32 | 0 |
| VC1702 | | 16 | 0 |
| VC1802 | VIVA1596 | 32 | 0 |
| VC1902 | | 32 | 0 |
| VM1302 | VFVA1760 | 24 | 0 |
| VM1402 | | 24 | 0 |
| VM2602 | | 8 | 24 |
| VM1502 | VFVC1760 | 44 | 0 |
| VM1802 | | 44 | 0 |
| VM2602 | | 8 | 40 |
| VM2902 | | 8 | 40 |
| VM1802 | VSVD1760 | 24 | 0 |
| VC1802 | VSVD1760 | 24 | 0 |
| VC1902 | | 24 | 0 |
| VM1802 | VSVA2197 | 44 | 0 |
| VM2502 | | 16 | 16 |
| VC1502 | VSVA2197 | 44 | 0 |
| VC1802 | | 44 | 0 |
| VC1902 | | 44 | 0 |

# Differences from Previous Generations

This section lists the differences from previous generations of the packaging and pinout specifications.

- In addition to 0.8 mm and 1.0 mm BGA ball pitch, Versal ACAP packages have 0.92 mm BGA ball pitch, signified by a package code beginning with a V.
- Some packages include land-side capacitor (LSC) technology (decoupling capacitors on the bottom side of the package, adjacent to the BGA balls). LSC array dimensions for each package are found in Chapter 5: Mechanical Drawings.
- Hardware blocks bonded to package pins have been added with Versal™ ACAPs, including XPIO, PMCMIO, and LPDMIO banks.
- I/Os in some banks on the left and right edges of the XPIO rows do not have direct access to all I/O logic resources and can only be used for DDR memory controller (DDRMC) applications.
- VRP pins, previously found in each HPIO bank, are replaced with a single IO_VR pin for each row of XPIO banks.
- $V_{CCO}$ voltage range for XPIO banks is 1.0V to 1.5V instead of the 1.0V to 1.8V range for HPIO banks in previous generations.
- Device diagrams showing package pinout (previously separated into I/O diagrams and power/dedicated/multifunction diagrams, are combined into a single diagram for Versal ACAP packages.
- Package marking found on previous device generations is replaced with a 2D bar code.

# User I/O Pins by Device Package

The following table lists the number of available PMC and LPD multiplexed I/Os (MIO), 3.3V-capable high-density (HD), and 1.5V-capable high-performance (XP) I/Os and the number of HD or XP differential I/O for each device/package combination. All packages are available with eutectic BGA balls where the device type is XQ and the Pb-free signifier in the package name is a Q.

*Table 3:* **Available I/O Pins by Device/Package**

| Device | Package | MIO | Total User I/O | | Differential I/O | |
|---|---|---|---|---|---|---|
| | | | XPIO | HDIO | XPIO | HDIO |
| VC1352 | VBVA1024 | 78 | 378 | 22 | 189 | 11 |
| | VSVE1369 | 78 | 378 | 44 | 189 | 22 |

*Table 3:* **Available I/O Pins by Device/Package** *(cont'd)*

| Device | Package | MIO | Total User I/O | | Differential I/O | |
|---|---|---|---|---|---|---|
| | | | XPIO | HDIO | XPIO | HDIO |
| VC1502 | VBVA1024 | 78 | 378 | 22 | 189 | 11 |
| | VSVG1369 | 78 | 378 | 44 | 189 | 22 |
| | VSVA1596 | 78 | 378 | 44 | 189 | 22 |
| | VSVA2197 | 78 | 378 | 44 | 189 | 22 |
| VC1702 | VSVE1369 | 78 | 378 | 44 | 189 | 22 |
| | VSVA1596 | 78 | 378 | 44 | 189 | 22 |
| VC1802 | VIVA1596 | 78 | 378 | 44 | 189 | 22 |
| | VSVD1760 | 78 | 648 | 0 | 324 | 0 |
| | VSVA2197 | 78 | 648 | 44 | 324 | 22 |
| VC1902 | VIVA1596 | 78 | 378 | 44 | 189 | 22 |
| | VSVD1760 | 78 | 648 | 0 | 324 | 0 |
| | VSVA2197 | 78 | 648 | 44 | 324 | 22 |
| VM1102 | SFVB625 | 78 | 216 | 22 | 108 | 11 |
| | VFVB1024 | 78 | 216 | 22 | 108 | 11 |
| VM1302 | VFVB1024 | 78 | 216 | 22 | 108 | 11 |
| | VFVB1369 | 78 | 216 | 22 | 108 | 11 |
| | VFVF1369 | 78 | 324 | 22 | 162 | 11 |
| | VFVA1760 | 78 | 432 | 22 | 216 | 11 |
| VM1402 | VFVB1024 | 78 | 324 | 22 | 162 | 11 |
| | VFVB1369 | 78 | 324 | 22 | 162 | 11 |
| | VFVF1369 | 78 | 648 | 22 | 324 | 11 |
| | VFVA1760 | 78 | 648 | 22 | 324 | 11 |
| VM1502 | VFVB1369 | 78 | 378 | 44 | 189 | 44 |
| | VFVC1760 | 78 | 378 | 44 | 189 | 44 |
| VM1802 | VFVC1760 | 78 | 378 | 44 | 189 | 44 |
| | VSVD1760 | 78 | 648 | 0 | 324 | 0 |
| | VSVA2197 | 78 | 648 | 44 | 324 | 22 |
| VM2502 | VSVA2197 | 78 | 648 | 22 | 324 | 11 |
| VM2602 | VFVA1760 | 78 | 756 | 0 | 378 | 0 |
| | VFVC1760 | 78 | 378 | 0 | 189 | 0 |
| VM2902 | VFVC1760 | 78 | 378 | 22 | 189 | 11 |

**Notes:**

1. The maximum user I/O numbers do not include the GT serial transceiver pins.

# Pin Definitions

The following tables list the pin definitions.

## SelectIO Pin Definitions

*Table 4:* **SelectIO Pin Definitions**

| Pin Name | Direction | Description |
|---|---|---|
| IO | Bidirectional | Pin name consists of:<br>L[1 to 24][P or N]: Differential pair number with P (positive) and N (negative)<br>N[0 to 8]P[0 to 5]: XPHY nibble number and pin number within the nibble (NIBBLESLICE number)<br>M[0 to number of triplets]P[0 to 161]: Triplet number and pin within the triplet<br>[bank number]: Bank number<br>The XP IOB block provides resources to enable high-speed interfaces between the programmable logic (PL) and the system outside the device. The XP IOB resources are designed to accommodate the signaling needs for high-speed memory and chip-to-chip interfaces that are powered between 1.0V and 1.5V. The XP IOB provides internal termination, internal reference generation, support for a diverse set of I/O standards, driver emphasis, and receiver equalization. These features allow the XP IOB to integrate with a diverse range of systems.<br>High-density (HD) I/O banks are resources designed to support I/O standards with voltages ranging from 1.8V to 3.3V. HD I/Os support single ended and pseudo-differential I/O bidirectional signaling operating at data rates of up to 400 Mb/s. Limited support for true differential inputs (with external termination) is also available to support LVDS and LVPECL clock inputs. HD I/O banks contain interface logic (HD IOL) that includes registers, a DPLL, and static delay lines to support asynchronous, system synchronous, and clock-based source synchronous interfaces. |
| GC/HDGC | Bidirectional | Global clock (GC) inputs provide dedicated, high-speed access to the internal global and regional clock resources. GC inputs use dedicated routing and must be used for clock inputs where the timing of various clocking features is imperative. General-purpose I/O with local interconnects must not be used for clock signals. |
| IO_VR | N/A | This pin is for the DCI voltage reference resistor, one per bank row: IO_VR_700 and IO_VR_800. Tie to VCCO_700 and VCCO_800, respectively, with a reference resistor. |

## Power Pin Definitions

*Table 5:* **Power Pin Definitions**

| Pin Name | Direction | Description |
|---|---|---|
| VCCINT | N/A | Power-supply pins for the programmable logic, AI Engines, and CPM |
| VCCAUX | N/A | Power-supply pins for the auxiliary circuits |
| VCC_IO | N/A | Power-supply pins for the HDIO and XPIO banks |
| VCCO (XPIO or HDIO) | N/A | Power-supply pins for the output drivers (per bank) |

*Table 5:* **Power Pin Definitions** *(cont'd)*

| Pin Name | Direction | Description |
|---|---|---|
| VCCO_500 | N/A | PMC MIO bank 0 power supply |
| VCCO_501 | N/A | PMC MIO bank 1 power supply |
| VCCO_502 | N/A | LPD MIO bank power supply |
| VCCO_503 | N/A | PMC dedicated I/O bank power supply |
| VCCAUX_PMC | N/A | Auxiliary power-supply pin for the PMC |
| VCC_PSFP | N/A | Power-supply for the PS full-power domain |
| VCC_PSLP | N/A | Power-supply for the PS low-power domain |
| VCC_PMC | N/A | Auxiliary power-supply pins for the PMC |
| VCC_SOC | N/A | Power supply pins for NoC, NPI, and the DDR |
| VCC_RAM | N/A | Power-supply pins for the RAM, UltraRAM, and clocking network |
| VCC_BATT | N/A | Battery supply voltage |
| VCC_FUSE | N/A | Power-supply pins for eFUSE programming |
| VCCAUX_SMON | N/A | Analog supply pin for the ADC and other analog circuits in the SYSMON |
| GND_SMON | N/A | Ground reference pin for the ADC and other analog circuits in the SYSMON |
| GND | N/A | Ground |
| RSVDGND | N/A | Reserved pin. Tie to GND. |
| NC | N/A | Reserved pin. Leave floating |

# PMCMIO, LPDMIO, PMCDIO Pin Definitions

*Table 6:* **PMCMIO, LPDMIO, PMCDIO Pin Definitions**

| Pin Name | Direction | Description |
|---|---|---|
| PMC_MIO[0 to 51] | Bidirectional | Platform management controller (PMC) multiplexed I/O (MIO) |
| LPD_MIO[0 to 25] | Bidirectional | Low-power domain (LPD) MIO |
| MODE[0 to 3] | Input | The MIO MODE selection pins are used to select the boot mode of the device. The value of these pins is captured on the rising edge of POR_B. |
| ERROR_OUT | Output | The ERROR_OUT pin is open drain with a weak internal pull-up. An external pull-up is recommended. ERROR_OUT is 3-stated and pulled High when an error occurs in the device. |
| RTC_PADO | Output | Real-time clock (RTC) crystal output |
| RTC_PADI | Input | RTC crystal input |
| PUDC_B | Input | The pull-up during configuration (PUDC_B) pin is used to select the behavior of the XPIO or HDIO during configuration. If the PUDC_B pin is High, then the XPIO and HDIO are put into tristate mode. If the PUDC_B is Low, then internal pull-ups at each XPIO and HDIO are enabled. The PUDC_B pin does not affect the PS or PMC I/O during boot and configuration. |
| DONE | Bidirectional | The DONE pin is open drain with a weak internal pull-up resistor. An external pull-up is recommended. DONE is tristated and pulled High when the boot sequence is complete. |
| REF_CLK | Input/Output | The reference clock is required for all boot modes. The REF_CLK is also the input clock to the PMC PLL and is required for the slave boot interface software register access. |

*Table 6:* **PMCMIO, LPDMIO, PMCDIO Pin Definitions** *(cont'd)*

| Pin Name | Direction | Description |
|---|---|---|
| POR_B | Input | Active-Low POR_B pin is the global power-on reset for the Versal device. It must remain asserted Low until power is fully applied to at least the VCC_PMC, VCCAUX_PMC, and VCCO_503. When the reset is released, the PMC begins the initialization and boot process. |
| TCK | Input | JTAG test clock |
| TDI | Input | JTAG test data input |
| TDO | Output | JTAG test data output |
| TMS | Input | JTAG test mode select |

# GTY Transceiver Quad Pin Definitions

*Table 7:* **GTY Transceiver Quad Pin Definitions**

| Pin Name | Direction | Description |
|---|---|---|
| GTY_RXP, GTY_RXN | Input | GTY_RXP and GTY_RXN are the differential input pairs for each of the receivers in the GTY transceiver Quad |
| GTY_TXP, GTY_TXN | Output | GTY_TXP and GTY_TXN are the differential output pairs for each of the transmitters in the GTY transceiver Quad |
| GTY_REFCLKP, GTY_REFCLKN | Input | Configured as either reference clock input pins or as RX recovered clock output pins for the GTY transceiver Quad |
| GTY_AVTTRCAL | Input (Pad) | Bias current supply for the termination resistor calibration circuit |
| GTY_RREF | Input (Pad) | Calibration resistor input pin for the termination resistor calibration circuit |
| GTY_AVCC | Input (Pad) | GTY_AVCC is the analog supply for the internal analog circuits of the GTY transceiver Quad tile. This includes the analog circuits for the PLLs, transmitters, and receivers. Most packages have multiple groups of power supply connections in the package for GTY_AVCC.<br>Refer to the package pin definitions to identify in which power supply group a specific GTY transceiver Quad is located.<br>The nominal voltage is $0.88V_{DC}$. |
| GTY_AVTT | Input (Pad) | GTY_AVTT is the analog supply for the transmitter and receiver termination circuits of the GTY transceiver Quad tile. Most packages have multiple groups of power supply connections in the package for GTY_AVTT.<br>Refer to the package pin definitions to identify in which power supply group a specific GTY transceiver Quad is located.<br>The nominal voltage is $1.2V_{DC}$. |
| GTY_AVCCAUX | Input (Pad) | GTY_VCCAUX is the analog LCPLL voltage supply for the transceivers. Most packages have multiple groups of power supply connections in the package for GTY_AVCCAUX.<br>Refer to the package pin definitions to identify in which power supply group a specific GTY transceiver Quad is located.<br>The nominal voltage is $1.8V_{DC}$. |

## SYSMON Pin Definitions

*Table 8:* **SYSMON Pin Definitions**

| Pin Name | Direction | Description |
|---|---|---|
| VREFP | N/A | This pin can be tied to an external 1.024V accurate reference IC for best performance of the ADC. This pin should be connected to GND_SMON if an external reference is not supplied. |
| VREFN | N/A | This pin should be tied to the ground pin of an external 1.024V accurate reference IC for best performance of the ADC. This pin should always be connected to GND_SMON even if an external reference is not supplied. |
| VP | Input | This is the positive input terminal of the dedicated differential analog input channel (VP/VN). When not used, tie to GND_SMON. |
| VN | Input | This is the negative input terminal of the dedicated differential analog input channel (VP/VN). When not used, tie to GND_SMON. |

# Footprint Compatibility between Packages

Versal devices are footprint compatible only with other Versal devices with the same numerical portion of the package name and the same preceding single character alphabetic designator. For example, the VM1802-VSVD1760 is footprint compatible with the VC1902-VSVD1760, because the 1760 is preceded with a *D* in both package names, but not footprint compatible with the VM1802-VFVC1760. Also, the VC1502-VSVA1596 is footprint compatible with the VC1902-VIVA1596, regardless of a difference in package dimensions, because the 1596 is preceded by an *A* in both package names. Pins that are available in one device but are not available in another device are labeled as NC in the package file of the other device.

**IMPORTANT!** *Footprint compatibility does not necessarily imply that all pins will function in the same manner for different devices in a package.*

The following table shows the footprint compatible devices available for each package. See the *Versal Architecture and Product Data Sheet: Overview* (DS950) for specific package letter code options. All packages are available with eutectic BGA balls. For these packages, the device type is XQ and the Pb-free signifier in the package name is a Q.

*Table 9:* **Footprint Compatibility**

| Packages | Footprint Compatible Devices | | |
|---|---|---|---|
| SFVB625 | VM1102 | | |
| VBVA1024 | VC1352 | VC1502 | |
| VFVB1024 | VM1102 | VM1302 | VM1402 |
| VFVB1369 | VM1302 | VM1402 | VM1502 |
| VSVE1369 | VC1352 | VC1702 | |

*Table 9:* **Footprint Compatibility** *(cont'd)*

| Packages | Footprint Compatible Devices | | | | |
|---|---|---|---|---|---|
| VFVF1369 | VM1302 | VM1402 | | | |
| VSVG1369 | VC1502 | | | | |
| VSVA1596<br>VIVA1596[1] | VC1502 | VC1702 | VC1802 | VC1902 | |
| VFVA1760 | VM1302 | VM1402 | VM2602 | | |
| VFVC1760 | VM1502 | VM1802 | VM2602 | VM2902 | |
| VSVD1760 | VM1802 | VC1802 | VC1902 | | |
| VSVA2197 | VM1802 | VM2502 | VC1502 | VC1802 | VC1902 |

**Notes:**

1. While footprint compatible, the body size for the VIVA1596 is 40 mm x 40 mm, which is larger than the 37.5 mm x 37.5 mm body size for the VSVA1596 package.

Many Versal devices that are footprint compatible in a package have different I/O bank and transceiver quad numbers connected to the same package pins. Due to these differences, when migrating between devices in a specific package, the type of bank (HD vs. XP) or quad (GTY, GTYP, or GTM), whether a bank is connected or NC at the package pins, and where the bank or quad is located on the die must be taken into consideration. The following tables show how the banks and transceiver quads are numbered between devices in each package. For all grouped-together footprint-compatible packages, the bank and quad numbers in the same column (indicated by the letters A through Z) for each device are connected to the same package pins. For example, in the VSVA2197 packages, quad 202 for the VM2502 is connected to the same pins as quad 203 for the VM1802, VC1502, VC1802, and VC1902. For a visual representation of all of this information, see Figure 1: Example Device Diagram.

**Related Information**

I/O Bank Footprint Compatibility between Packages
Transceiver Footprint Compatibility between Packages

# I/O Bank Footprint Compatibility between Packages

*Table 10:* **I/O Bank Migration**

| Package | Device | A | B | C | D | E | F | G | H | I | J | K | L | M-U | AA | AB | AC | AD | AE | AF | AG | AH | AI-AU | Unbonded I/O Banks |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SFVB625 | VM1102 | 700 | 701 | 702 | 703 | | | | | | | | | | 304 | | | | | | | | | |
| VBVA1024 | VC1352 | 700 | 701 | 702 | 703 | 704 | 705 | 706 | | | | | | | 604 | | | | | | | | | 302, 204, 203, 202, 201, 200 |
| VBVA1024 | VC1502 | 700 | 701 | 702 | 703 | 704 | 705 | 706 | | | | | | | 406 | | | | | | | | | 306 |
| VFVB1024 | VM1102 | 700 | 701 | 702 | 703 | | | | | | | | | | 304 | | | | | | | | | |
| VFVB1024 | VM1302 | 700 | 701 | 702 | 703 | | | | | | | | | | 306 | 307 | | | | | | | | 800, 801, 802, 803, 804, 704, 805, 705 |
| VFVB1024 | VM1402 | 700 | 701 | 702 | 703 | 704 | 705 | | | | | | | | 306 | 307 | | | | | | | | 800, 801, 802, 803, 804, 805 |
| VFVB1369 | VM1302 | 700 | 701 | 702 | 703 | | | | | | | | | | 306 | 307 | | | | | | | | 800, 801, 802, 803, 804, 704, 805, 705 |
| VFVB1369 | VM1502 | 700 | 701 | 702 | 703 | 704 | 705 | 706 | | | | | | | 406 | 306 | | | | | | | | |
| VFVB1369 | VM1402 | 700 | 701 | 702 | | 703 | 704 | 705 | | | | | | | 306 | 307 | | | | | | | | 800, 801, 802, 803, 804, 805 |
| VSVE1369 | VC1352 | 700 | 701 | 702 | 703 | 704 | 705 | 706 | | | | | | | 604 | 302 | | | | | | | | 204, 203, 202, 201, 200 |
| VSVE1369 | VC1702 | 700 | 701 | 702 | 703 | 704 | 705 | 706 | | | | | | | 608 | 302 | | | | | | | | 208, 207, 206, 205, 204, 203, 202, 201, 200 |
| VIVA1596 | VC1802 | 700 | 701 | 702 | 703 | 706 | 707 | 708 | | | | | | | 406 | 306 | | | | | | | | 704, 705, 709, 710, 711 |

*Table 10:* **I/O Bank Migration** *(cont'd)*

| Package | Device | A | B | C | D | E | F | G | H | I | J | K | L | M-U | AA | AB | AC | AD | AE | AF | AG | AH | AI-AU | Unbonded I/O Banks |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| VIVA1596 | VC1902 | 700 | 701 | 702 | 703 | 706 | 707 | 708 | | | | | | | 406 | 306 | | | | | | | | 704, 705, 709, 710, 711 |
| VSVA1596 | VC1502 | 700 | 701 | 702 | 703 | 704 | 705 | 706 | | | | | | | 406 | 306 | | | | | | | | |
| VSVA1596 | VC1702 | 700 | 701 | 702 | 703 | 704 | 705 | 706 | | | | | | | 608 | 302 | | | | | | | | 208, 207, 206, 205, 204, 203, 202, 201, 200 |
| VFVA1760 | VM1302 | 700 | 701 | 702 | 703 | | | | | | | | | | 800 | 801 | 802 | 803 | | | 307 | 306 | | 804, 704, 805, 705 |
| VFVA1760 | VM1402 | 700 | 701 | 702 | 703 | 704 | 705 | | | | | | | | 800 | 801 | 802 | 803 | 804 | 805 | 307 | 306 | | |
| VFVA1760 | VM2602 | 700 | 701 | 702 | 703 | 704 | 705 | 706 | 707 | | | | | | 800 | 801 | 802 | 803 | 804 | 805 | | | | 806, 807, 808, 708 |
| VFVC1760 | VM1502 | 700 | 701 | 702 | | | | | | | | | | | 704 | 705 | 706 | 703 | 306 | 406 | | | | |
| VFVC1760 | VM1802 | 700 | 701 | 702 | | | | | | | | | | | 703 | 704 | 705 | 706 | 306 | 406 | | | | 707, 708, 709, 710, 711 |
| VFVC1760 | VM2602 | 700 | 701 | 702 | | | | | | | | | | | 703 | 704 | 705 | 706 | | | | | | 800, 801, 802, 803, 804, 805, 806, 807, 707, 808, 708 |
| VFVC1760 | VM2902 | 700 | 701 | 702 | | | | | | | | | | | 703 | 704 | 705 | 706 | | 412 | | | | 800, 801, 802, 803, 804, 805, 806, 807, 707, 808, 708 |
| VSVD1760 | VM1802 | 700 | 701 | 702 | 703 | 704 | 705 | 706 | 707 | 708 | 709 | 710 | 711 | | | | | | | | | | | 306, 406 |
| VSVD1760 | VC1802 | 700 | 701 | 702 | 703 | 704 | 705 | 706 | 707 | 708 | 709 | 710 | 711 | | | | | | | | | | | 306, 406 |
| VSVD1760 | VC1902 | 700 | 701 | 702 | 703 | 704 | 705 | 706 | 707 | 708 | 709 | 710 | 711 | | | | | | | | | | | 306, 406 |
| VSVA2197 | VM2502 | 700 | 701 | 702 | 703 | 704 | 705 | 706 | 707 | 708 | 709 | 710 | 711 | | | 406 | | | | | | | | 712 |

*Table 10:* **I/O Bank Migration** *(cont'd)*

| Package | Device | A | B | C | D | E | F | G | H | I | J | K | L | M-U | AA | AB | AC | AD | AE | AF | AG | AH | AI-AU | Unbonded I/O Banks |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| VSVA2197 | VM1802 | 700 | 701 | 702 | 703 | 704 | 705 | 706 | 707 | 708 | 709 | 710 | 711 | | 306 | 406 | | | | | | | | |
| VSVA2197 | VC1502 | 700 | 701 | 702 | 703 | | | 704 | 705 | 706 | | | | | 306 | 406 | | | | | | | | |
| VSVA2197 | VC1802 | 700 | 701 | 702 | 703 | 704 | 705 | 706 | 707 | 708 | 709 | 710 | 711 | | 306 | 406 | | | | | | | | |
| VSVA2197 | VC1902 | 700 | 701 | 702 | 703 | 704 | 705 | 706 | 707 | 708 | 709 | 710 | 711 | | 306 | 406 | | | | | | | | |

# Transceiver Footprint Compatibility between Packages

*Table 11:* **Transceiver Migration – Left Side (GTM Quads are Shaded)**

| Package | Device | CA | CB | CC | CD | CE | CF | CG | CH | CI | CJ | CK | CL | CM | CN | CO | CP | CQ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SFVB625 | XCVM1102 | L | | | | | | | | | | | | | | | | |
| | | 103 | | | | | | | | | | | | | | | | |
| VBVA1024 | XCVC1352 | L | L | | | | | | | | | | | | | | | |
| | | 103 | 104 | | | | | | | | | | | | | | | |
| VBVA1024 | XCVC1502 | L | L | | | | | | | | | | | | | | | |
| | | 103 | 104 | | | | | | | | | | | | | | | |
| VFVB1024 | XCVM1102 | L | L | L | | | | | | | | | | | | | | |
| | | 102 | 103 | 104 | | | | | | | | | | | | | | |
| VFVB1024 | XCVM1302 | L | L | L | L | | | | | | | | | | | | | |
| | | 102 | 103 | 104 | 105 | | | | | | | | | | | | | |
| VFVB1024 | XCVM1402 | L | L | L | L | | | | | | | | | | | | | |
| | | 102 | 103 | 104 | 105 | | | | | | | | | | | | | |
| VFVB1369 | XCVM1302 | LS | LS | LS | LS | | LN | LN | | | | | | | | | | |
| | | 102 | 103 | 104 | 105 | | 106 | 107 | | | | | | | | | | |
| VFVB1369 | XCVM1502 | LS | LS | LS | LS | | | | | | | | | | | | | |
| | | 103 | 104 | 105 | 106 | | | | | | | | | | | | | |
| VFVB1369 | XCVM1402 | LS | LS | LS | LS | | LN | LN | | | | | | | | | | |
| | | 102 | 103 | 104 | 105 | | 106 | 107 | | | | | | | | | | |
| VSVE1369 | XCVC1352 | L | L | | | | | | | | | | | | | | | |
| | | 103 | 104 | | | | | | | | | | | | | | | |
| VSVE1369 | XCVC1702 | L | L | L | L | L | L | | | | | | | | | | | |
| | | 103 | 104 | 105 | 106 | 107 | 108 | | | | | | | | | | | |
| VIVA1596 | XCVC1802 | L | L | L | L | | | | | | | | | | | | | |
| | | 103 | 104 | 105 | 106 | | | | | | | | | | | | | |
| VIVA1596 | XCVC1902 | L | L | L | L | | | | | | | | | | | | | |
| | | 103 | 104 | 105 | 106 | | | | | | | | | | | | | |

*Table 11:* **Transceiver Migration – Left Side (GTM Quads are Shaded)** *(cont'd)*

| Package | Device | CA | CB | CC | CD | CE | CF | CG | CH | CI | CJ | CK | CL | CM | CN | CO | CP | CQ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| VSVA1596 | XCVC1502 | L | L | L | L | | | | | | | | | | | | | |
| | | 103 | 104 | 105 | 106 | | | | | | | | | | | | | |
| VSVA1596 | XCVC1702 | L | L | L | L | | | | | | | | | | | | | |
| | | 103 | 104 | 105 | 106 | | | | | | | | | | | | | |
| VFVA1760 | XCVM1302 | L | L | L | L | L | L | | | | | | | | | | | |
| | | 102 | 103 | 104 | 105 | 106 | 107 | | | | | | | | | | | |
| VFVA1760 | XCVM1402 | L | L | L | L | L | L | | | | | | | | | | | |
| | | 102 | 103 | 104 | 105 | 106 | 107 | | | | | | | | | | | |
| VFVA1760 | XCVM2602 | L | L | L | L | L | L | | | | | | | | | | | |
| | | 102 | 103 | 104 | 105 | 106 | 107 | | | | | | | | | | | |
| VFVC1760 | XCVM1502 | L | L | L | L | | | | | | | | | | | | | |
| | | 103 | 104 | 105 | 106 | | | | | | | | | | | | | |
| VFVC1760 | XCVM1802 | L | L | L | L | | | | | | | | | | | | | |
| | | 103 | 104 | 105 | 106 | | | | | | | | | | | | | |
| VFVC1760 | XCVM2602 | L | L | L | L | L | L | | | | | | | | | | | |
| | | 102 | 103 | 104 | 105 | 106 | 107 | | | | | | | | | | | |
| VFVC1760 | XCVM2902 | L | L | L | L | L | L | | | | | | | | | | | |
| | | 102 | 103 | 104 | 105 | 106 | 107 | | | | | | | | | | | |
| VSVD1760 | XCVM1802 | L | L | L | L | | | | | | | | | | | | | |
| | | 103 | 104 | 105 | 106 | | | | | | | | | | | | | |
| VSVD1760 | XCVC1802 | L | L | L | L | | | | | | | | | | | | | |
| | | 103 | 104 | 105 | 106 | | | | | | | | | | | | | |
| VSVD1760 | XCVC1902 | L | L | L | L | | | | | | | | | | | | | |
| | | 103 | 104 | 105 | 106 | | | | | | | | | | | | | |
| VSVA2197 | XCVM2502 | L | L | L | L | | | | | | | | | | | | | |
| | | 102 | 103 | 104 | 105 | | | | | | | | | | | | | |
| VSVA2197 | XCVM1802 | L | L | L | L | | | | | | | | | | | | | |
| | | 103 | 104 | 105 | 106 | | | | | | | | | | | | | |

*Table 11:* **Transceiver Migration – Left Side (GTM Quads are Shaded)** *(cont'd)*

| Package | Device | CA | CB | CC | CD | CE | CF | CG | CH | CI | CJ | CK | CL | CM | CN | CO | CP | CQ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| VSVA2197 | XCVC1502 | L | L | L | L | | | | | | | | | | | | | |
| | | 103 | 104 | 105 | 106 | | | | | | | | | | | | | |
| VSVA2197 | XCVC1802 | L | L | L | L | | | | | | | | | | | | | |
| | | 103 | 104 | 105 | 106 | | | | | | | | | | | | | |
| VSVA2197 | XCVC1902 | L | L | L | L | | | | | | | | | | | | | |
| | | 103 | 104 | 105 | 106 | | | | | | | | | | | | | |

*Table 12:* **Transceiver Migration – Right Side (GTM Duals are Shaded)**

| Package | Device | BA | BB | BC | BD | BE | BF | BG | BH | BI | BJ | BK | BL | BM | BN | BO | BP | BQ | BR | BS | BT | BU | BV | BW | BX | BY |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SFVB625 | XCVM1102 | | | | | | | | | | | | | | | | | | | | | | | | | |
| VBVA1024 | XCVC1352 | | | | | | | | | | | | | | | | | | | | | | | | | |
| VBVA1024 | XCVC1502 | | | | | | | | | | | | | | | | | | | | | | | | | |
| VFVB1024 | XCVM1102 | | | | | | | | | | | | | | | | | | | | | | | | | |
| VFVB1024 | XCVM1302 | | | | | | | | | | | | | | | | | | | | | | | | | |
| VFVB1024 | XCVM1402 | | | | | | | | | | | | | | | | | | | | | | | | | |
| VFVB1369 | XCVM1302 | | | | | | | | | | | | | | | | | | | | | | | | | |
| VFVB1369 | XCVM1502 | | | | | | | | | | | | | | | | | | | | | | | | | |
| VFVB1369 | XCVM1402 | | | | | | | | | | | | | | | | | | | | | | | | | |
| VSVE1369 | XCVC1352 | | | | | | | | | | | | | | | | | | | | | | | | | |
| VSVE1369 | XCVC1702 | | | | | | | | | | | | | | | | | | | | | | | | | |
| VIVA1596 | XCVC1802 | R | R | R | R | | | | | | | | | | | | | | | | | | | | | |
| | | 202 | 203 | 204 | 205 | | | | | | | | | | | | | | | | | | | | | |
| VIVA1596 | XCVC1902 | R | R | R | R | | | | | | | | | | | | | | | | | | | | | |
| | | 202 | 203 | 204 | 205 | | | | | | | | | | | | | | | | | | | | | |
| VSVA1596 | XCVC1502 | R | R | R | R | | | | | | | | | | | | | | | | | | | | | |
| | | 202 | 203 | 204 | 205 | | | | | | | | | | | | | | | | | | | | | |
| VSVA1596 | XCVC1702 | | | | | | | | | | | | | | | | | | | | | | | | | |
| VFVA1760 | XCVM1302 | | | | | | | | | | | | | | | | | | | | | | | | | |
| VFVA1760 | XCVM1402 | | | | | | | | | | | | | | | | | | | | | | | | | |
| VFVA1760 | XCVM2602 | | | | | | | | | | | | | | | | | | | | | | | | | |
| VFVC1760 | XCVM1502 | RS | RS | RS | RS | RN | RN | RN | | | | | | | | | | | | | | | | | | |
| | | 200 | 201 | 202 | 203 | 204 | 205 | 206 | | | | | | | | | | | | | | | | | | |
| VFVC1760 | XCVM1802 | RS | RS | RS | RS | RN | RN | RN | | | | | | | | | | | | | | | | | | |
| | | 200 | 201 | 202 | 203 | 204 | 205 | 206 | | | | | | | | | | | | | | | | | | |
| VFVC1760 | XCVM2602 | RS | RS | RS | RS | RN | RN | RN | RN | | | | | | | | | | | | | | | | | |
| | | 200 | 201 | 202 | 203 | 204 | 205 | 206 | 207 | | | | | | | | | | | | | | | | | |
| VFVC1760 | XCVM2902 | RS | RS | RS | RS | RN | RN | RN | RN | | | | | | | | | | | | | | | | | |
| | | 200 | 201 | 202 | 203 | 204 | 205 | 206 | 207 | | | | | | | | | | | | | | | | | |

*Table 12:* **Transceiver Migration – Right Side (GTM Duals are Shaded)** *(cont'd)*

| Package | Device | BA | BB | BC | BD | BE | BF | BG | BH | BI | BJ | BK | BL | BM | BN | BO | BP | BQ | BR | BS | BT | BU | BV | BW | BX | BY |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| VSVD1760 | XCVM1802 | R | R |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  | 203 | 204 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| VSVD1760 | XCVC1802 | R | R |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  | 203 | 204 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| VSVD1760 | XCVC1902 | R | R |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  | 203 | 204 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| VSVA2197 | XCVM2502 |  |  |  | R | R | R | R |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  | 202 | 203 | 204 | 205 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| VSVA2197 | XCVM1802 | R | R | R | R | R | R | R |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  | 200 | 201 | 202 | 203 | 204 | 205 | 206 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| VSVA2197 | XCVC1502 | R | R | R | R | R | R | R |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  | 200 | 201 | 202 | 203 | 204 | 205 | 206 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| VSVA2197 | XCVC1802 | R | R | R | R | R | R | R |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  | 200 | 201 | 202 | 203 | 204 | 205 | 206 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| VSVA2197 | XCVC1902 | R | R | R | R | R | R | R |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  | 200 | 201 | 202 | 203 | 204 | 205 | 206 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

*Table 13:* **Transceiver Migration – Unbonded Banks**

| Package | Device | Unbonded Banks |
|---|---|---|
| SFVB625 | XCVM1102 | 104, 102 |
| VBVA1024 | XCVC1352 | |
| VBVA1024 | XCVC1502 | 106, 105, 206, 205, 204, 203, 202, 201, 200 |
| VFVB1024 | XCVM1102 | |
| VFVB1024 | XCVM1302 | 107, 106 |
| VFVB1024 | XCVM1402 | 107, 106 |
| VFVB1369 | XCVM1302 | |
| VFVB1369 | XCVM1502 | 206, 205, 204, 203, 202, 201, 200 |
| VFVB1369 | XCVM1402 | |
| VSVE1369 | XCVC1352 | |
| VSVE1369 | XCVC1702 | |
| VIVA1596 | XCVC1802 | 206, 201, 200 |
| VIVA1596 | XCVC1902 | 206, 201, 200 |
| VSVA1596 | XCVC1502 | 206, 201, 200 |
| VSVA1596 | XCVC1702 | 108, 107 |
| VFVA1760 | XCVM1302 | |
| VFVA1760 | XCVM1402 | |
| VFVA1760 | XCVM2602 | 207, 206, 205, 204, 203, 202, 201, 200 |
| VFVC1760 | XCVM1502 | |
| VFVC1760 | XCVM1802 | |
| VFVC1760 | XCVM2602 | |
| VFVC1760 | XCVM2902 | 112, 111, 110, 109, 108, 212, 211, 210, 209, 208 |
| VSVD1760 | XCVM1802 | 206, 205, 202, 201, 200 |
| VSVD1760 | XCVC1802 | 206, 205, 202, 201, 200 |
| VSVD1760 | XCVC1902 | 206, 205, 202, 201, 200 |
| VSVA2197 | XCVM2502 | 106, 206, 201, 200 |
| VSVA2197 | XCVM1802 | |

*Table 13:* **Transceiver Migration – Unbonded Banks** *(cont'd)*

| Package | Device | Unbonded Banks |
|---|---|---|
| VSVA2197 | XCVC1502 | |
| VSVA2197 | XCVC1902 | |

# Die Level Bank Numbering and Device Diagrams

## Die Level Bank Numbering Overview

#### Banking and Clocking Summary

For each device, not all banks are bonded out in every package.

#### GTY and GTM Columns

- One GT Quad = Four transceivers = Four GTYE5_QUAD or GTME5_QUAD primitives.
- Not all GT Quads are bonded out in every package.
- Also shown are quads labeled with RCAL. This specifies the location of the RCAL masters for each device. With respect to the package, the RCAL masters are located on the same package pin for each package, regardless of the device.
- The XY coordinates shown in each quad correspond to the transceiver channel number found in the pin names for that quad (as shown in the next section).
- An alphabetic designator is shown in each quad. Each letter corresponds to the columns in the tables in the Transceiver Footprint Compatibility between Packages section.
- The power supply group is shown in brackets [ ] for each quad.

#### I/O Banks

- Each user XPIO bank has a total of 54 I/Os that can be used as differential (27 differential pairs) or single-ended I/Os. All 54 pads of a bank are not always bonded out to pins.
- A limited number of XPIO banks have fewer than 54 SelectIO pins. These banks are labeled as partial.
- Each user HDIO bank has a total of 22 I/Os that can be used as pseudo-differential (11 differential pairs) or single-ended I/Os.
- Adjacent to each bank is a physical layer (PHY) containing clock buffers and clock management resources

- XPIO banks are arranged in rows on the north and south of the device with adjacent PHY and clock management resources.
- XPIO banks are separated into groups of 1, 2, or 3 banks that signify how to group them when used for DDR memory controller applications.
- I/Os in some banks on the left and right edges of the XPIO rows do not have direct access to all I/O logic resources and can only be used for DDR memory controller (DDRMC) applications. These I/Os are specified in the following device diagrams, where each XPIO bank is designated by a Y (DDRMC only) or a N (access to all I/O logic resources) for each nibble (nine nibbles per bank and six I/Os per nibble). This is also specified in the *DDRMC Only* column of the Chapter 3: Package Files.
- Global clock (GC) pins in *DDRMC Only* nibbles include full access to clock management resources.
- HDIO banks are arranged in columns and separated into rows that are pitch-matched with adjacent PHY, clock management resources, and GT blocks.
- An alphabetic designator is shown in each bank. Each letter corresponds to the columns in Table 10.

### Clocking

- Each XPIO bank has four pairs of global clock (GC) inputs for four differential or four single-ended clock inputs. Single-ended clock inputs should be connected to the P-side of the differential pair.
- Each HDIO bank has two global clock (HDGC) inputs for two single-ended clock inputs, a pseudo-differential pair or a true-differential pair for a limited selection of I/O standards.
- Clock signals are distributed through global buffers driving routing and distribution networks to reach any clock region, I/O, or GTY transceivers.
- Global clock inputs can connect to MMCMs and PLLs within the XPIO bank or adjacent clock management resources

### Processor Blocks

- PMC MIO pins are in banks 500 and 501
- LPD MIO pins are in bank 502
- PMC dedicated pins are in bank 503

### PCIe, CPM, Interlaken, and 100GE Integrated Blocks

- **PCIe:** Integrated block for PCIe®. The PCIe blocks with an additional (Tandem) label support tandem configuration.
- **CPM:** CCIX and PCIe® processor sub-system module
- **ILKN:** Interlaken block

- **MRMAC:** 100G Ethernet block

# Device Diagrams Overview

The following figure shows an example diagram with a brief explanation for each component.

*Figure 1:* **Example Device Diagram**

| | | | |
|---|---|---|---|
| GTY Quad 106<br>X0Y6<br>CD [L] | HDIO<br>Bank 306<br>AA | HDIO<br>Bank 406<br>AB | GTY Quad 206<br>X1Y6<br>BG [R] |
| GTY Quad 105<br>X0Y5<br>CC [L] (RCAL) | PCIE<br>X0Y2 | PCIE<br>X1Y2 | GTY Quad 205<br>X1Y5<br>BF [R] |
| GTY Quad 104<br>X0Y4<br>CB [L] (RCAL) | PCIE<br>X0Y1 | MRMAC<br>X0Y3 | GTY Quad 204<br>X1Y4<br>BE [R] |
| GTY Quad 103<br>X0Y3<br>CA [L] | CPM4 | MRMAC<br>X0Y2 | GTY Quad 203<br>X1Y3<br>BD [R] (RCAL) |
| CPM4 | CPM4 | PCIE<br>X1Y0 | GTY Quad 202<br>X1Y2<br>BC [R] (RCAL) |
| LPDMIO<br>Bank 502 | PMCDIO<br>Bank 503 | MRMAC<br>X0Y1 | GTY Quad 201<br>X1Y1<br>BB [R] |
| PMCMIO/PMCDIO<br>Bank 500 | PMCMIO<br>Bank 501 | MRMAC<br>X0Y0 | GTY Quad 200<br>X1Y0<br>BA [R] |

| | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | XPIO<br>Bank 700<br>A | XPIO<br>Bank 701<br>B | XPIO<br>Bank 702<br>C | XPIO<br>Bank 703<br>D | XPIO<br>Bank 704<br>E | XPIO<br>Bank 705<br>F | XPIO<br>Bank 706<br>G | XPIO<br>Bank 707<br>H | XPIO<br>Bank 708<br>I | XPIO<br>Bank 709<br>J | XPIO<br>Bank 710<br>K | XPIO<br>Bank 711<br>L |
| DDRMC Only (by nibble): | YYYYYYYYY | YYYYYYYYY | YYYYNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | YYYYYYYYY |



The figures in this chapter show a die view of each device followed by a view with respect to each available package. The available resources by device and package are detailed in the *Versal Architecture and Product Data Sheet: Overview* (DS950).

# VC1802 Bank Diagram Overview

*Figure 2:* **VC1802 Banks**

| | | | |
|---|---|---|---|
| GTY Quad 106<br>X0Y6 | HDIO<br>Bank 306 | HDIO<br>Bank 406 | GTY Quad 206<br>X1Y6 |
| GTY Quad 105<br>X0Y5<br>(RCAL) | PCIE<br>X0Y2 | PCIE<br>X1Y2 | GTY Quad 205<br>X1Y5 |
| GTY Quad 104<br>X0Y4<br>(RCAL) | PCIE<br>X0Y1 | MRMAC<br>X0Y3 | GTY Quad 204<br>X1Y4 |
| GTY Quad 103<br>X0Y3 | CPM4 | MRMAC<br>X0Y2 | GTY Quad 203<br>X1Y3<br>(RCAL) |
| CPM4 | CPM4 | PCIE<br>X1Y0 | GTY Quad 202<br>X1Y2<br>(RCAL) |
| LPDMIO<br>Bank 502 | PMCDIO<br>Bank 503 | MRMAC<br>X0Y1 | GTY Quad 201<br>X1Y1 |
| PMCMIO/PMCDIO<br>Bank 500 | PMCMIO<br>Bank 501 | MRMAC<br>X0Y0 | GTY Quad 200<br>X1Y0 |

| | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | XPIO<br>Bank 700 | XPIO<br>Bank 701 | XPIO<br>Bank 702 | XPIO<br>Bank 703 | XPIO<br>Bank 704 | XPIO<br>Bank 705 | XPIO<br>Bank 706 | XPIO<br>Bank 707 | XPIO<br>Bank 708 | XPIO<br>Bank 709 | XPIO<br>Bank 710 | XPIO<br>Bank 711 |
| DDRMC Only (by nibble): | YYYYYYYYY | YYYYYYYYY | YYYYNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | YYYYYYYYY |

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# Bank Diagram by Package for VC1802

*Figure 3:* **VC1802 Banks in VIVA1596 Package**

| | | | |
|---|---|---|---|
| GTY Quad 106<br>X0Y6<br>CD [L] | HDIO<br>Bank 306<br>AB | HDIO<br>Bank 406<br>AA | GTY Quad 206<br>X1Y6 |
| GTY Quad 105<br>X0Y5<br>CC [L] (RCAL) | PCIE<br>X0Y2 | PCIE<br>X1Y2 | GTY Quad 205<br>X1Y5<br>BD [R] |
| GTY Quad 104<br>X0Y4<br>CB [L] (RCAL) | PCIE<br>X0Y1 | MRMAC<br>X0Y3 | GTY Quad 204<br>X1Y4<br>BC [R] |
| GTY Quad 103<br>X0Y3<br>CA [L] | CPM4 | MRMAC<br>X0Y2 | GTY Quad 203<br>X1Y3<br>BB [R] (RCAL) |
| CPM4 | CPM4 | PCIE<br>X1Y0 | GTY Quad 202<br>X1Y2<br>BA [R] (RCAL) |
| LPDMIO<br>Bank 502 | PMCDIO<br>Bank 503 | MRMAC<br>X0Y1 | GTY Quad 201<br>X1Y1 |
| PMCMIO/PMCDIO<br>Bank 500 | PMCMIO<br>Bank 501 | MRMAC<br>X0Y0 | GTY Quad 200<br>X1Y0 |

| | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | XPIO<br>Bank 700<br>A | XPIO<br>Bank 701<br>B | XPIO<br>Bank 702<br>C | XPIO<br>Bank 703<br>D | XPIO<br>Bank 704 | XPIO<br>Bank 705 | XPIO<br>Bank 706<br>E | XPIO<br>Bank 707<br>F | XPIO<br>Bank 708<br>G | XPIO<br>Bank 709 | XPIO<br>Bank 710 | XPIO<br>Bank 711 |
| DDRMC Only<br>(by nibble): | YYYYYYYYY | YYYYYYYYY | YYYYNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | YYYYYYYYY |

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*Figure 4:* **VC1802 Banks in VSVD1760 Package**

| | | | |
|---|---|---|---|
| GTY Quad 106<br>X0Y6<br>CD [L] | HDIO<br>Bank 306 | HDIO<br>Bank 406 | GTY Quad 206<br>X1Y6 |
| GTY Quad 105<br>X0Y5<br>CC [L] (RCAL) | PCIE<br>X0Y2 | PCIE<br>X1Y2 | GTY Quad 205<br>X1Y5 |
| GTY Quad 104<br>X0Y4<br>CB [L] (RCAL) | PCIE<br>X0Y1 | MRMAC<br>X0Y3 | GTY Quad 204<br>X1Y4<br>BB [R] |
| GTY Quad 103<br>X0Y3<br>CA [L] | CPM4 | MRMAC<br>X0Y2 | GTY Quad 203<br>X1Y3<br>BA [R] (RCAL) |
| CPM4 | CPM4 | PCIE<br>X1Y0 | GTY Quad 202<br>X1Y2 (RCAL) |
| LPDMIO<br>Bank 502 | PMCDIO<br>Bank 503 | MRMAC<br>X0Y1 | GTY Quad 201<br>X1Y1 |
| PMCMIO/PMCDIO<br>Bank 500 | PMCMIO<br>Bank 501 | MRMAC<br>X0Y0 | GTY Quad 200<br>X1Y0 |

| | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | XPIO<br>Bank 700<br>A | XPIO<br>Bank 701<br>B | XPIO<br>Bank 702<br>C | XPIO<br>Bank 703<br>D | XPIO<br>Bank 704<br>E | XPIO<br>Bank 705<br>F | XPIO<br>Bank 706<br>G | XPIO<br>Bank 707<br>H | XPIO<br>Bank 708<br>I | XPIO<br>Bank 709<br>J | XPIO<br>Bank 710<br>K | XPIO<br>Bank 711<br>L |
| DDRMC Only<br>(by nibble): | YYYYYYYYY | YYYYYYYYY | YYYYNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | YYYYYYYYY |

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*Figure 5:* **VC1802 Banks in VSVA2197 Package**

| | | | |
|---|---|---|---|
| GTY Quad 106 X0Y6 CD [L] | HDIO Bank 306 AA | HDIO Bank 406 AB | GTY Quad 206 X1Y6 BG [R] |
| GTY Quad 105 X0Y5 CC [L] (RCAL) | PCIE X0Y2 | PCIE X1Y2 | GTY Quad 205 X1Y5 BF [R] |
| GTY Quad 104 X0Y4 CB [L] (RCAL) | PCIE X0Y1 | MRMAC X0Y3 | GTY Quad 204 X1Y4 BE [R] |
| GTY Quad 103 X0Y3 CA [L] | CPM4 | MRMAC X0Y2 | GTY Quad 203 X1Y3 BD [R] (RCAL) |
| CPM4 | CPM4 | PCIE X1Y0 | GTY Quad 202 X1Y2 BC [R] (RCAL) |
| LPDMIO Bank 502 | PMCDIO Bank 503 | MRMAC X0Y1 | GTY Quad 201 X1Y1 BB [R] |
| PMCMIO/PMCDIO Bank 500 | PMCMIO Bank 501 | MRMAC X0Y0 | GTY Quad 200 X1Y0 BA [R] |

| | XPIO Bank 700 A | XPIO Bank 701 B | XPIO Bank 702 C | XPIO Bank 703 D | XPIO Bank 704 E | XPIO Bank 705 F | XPIO Bank 706 G | XPIO Bank 707 H | XPIO Bank 708 I | XPIO Bank 709 J | XPIO Bank 710 K | XPIO Bank 711 L |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DDRMC Only (by nibble): | YYYYYYYYY | YYYYYYYYY | YYYYNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | YYYYYYYYY |

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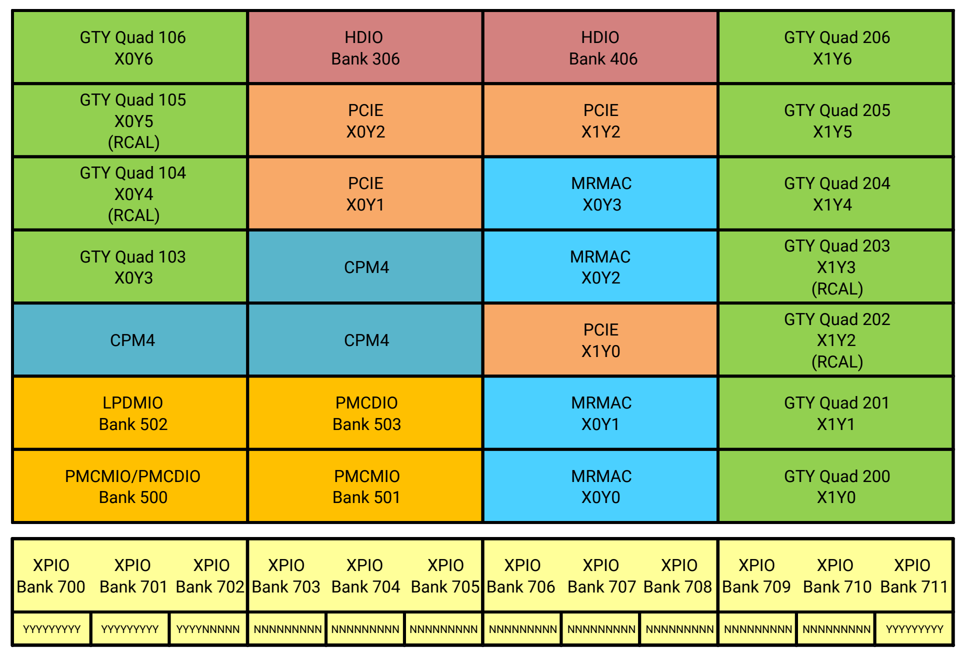
# VC1902 Bank Diagram Overview

*Figure 6:* **VC1902 Banks**



## Bank Diagram by Package for VC1902

*Figure 7:* **VC1902 Banks in VIVA1596 Package**

| | | | |
|---|---|---|---|
| GTY Quad 106<br>X0Y6<br>CD [L] | HDIO<br>Bank 306<br>AB | HDIO<br>Bank 406<br>AA | GTY Quad 206<br>X1Y6 |
| GTY Quad 105<br>X0Y5<br>CC [L] (RCAL) | PCIE<br>X0Y2 | PCIE<br>X1Y2 | GTY Quad 205<br>X1Y5<br>BD [R] |
| GTY Quad 104<br>X0Y4<br>CB [L] (RCAL) | PCIE<br>X0Y1 | MRMAC<br>X0Y3 | GTY Quad 204<br>X1Y4<br>BC [R] |
| GTY Quad 103<br>X0Y3<br>CA [L] | CPM4 | MRMAC<br>X0Y2 | GTY Quad 203<br>X1Y3<br>BB [R] (RCAL) |
| CPM4 | CPM4 | PCIE<br>X1Y0 | GTY Quad 202<br>X1Y2<br>BA [R] (RCAL) |
| LPDMIO<br>Bank 502 | PMCDIO<br>Bank 503 | MRMAC<br>X0Y1 | GTY Quad 201<br>X1Y1 |
| PMCMIO/PMCDIO<br>Bank 500 | PMCMIO<br>Bank 501 | MRMAC<br>X0Y0 | GTY Quad 200<br>X1Y0 |

| | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | XPIO<br>Bank 700<br>A | XPIO<br>Bank 701<br>B | XPIO<br>Bank 702<br>C | XPIO<br>Bank 703<br>D | XPIO<br>Bank 704 | XPIO<br>Bank 705 | XPIO<br>Bank 706<br>E | XPIO<br>Bank 707<br>F | XPIO<br>Bank 708<br>G | XPIO<br>Bank 709 | XPIO<br>Bank 710 | XPIO<br>Bank 711 |
| DDRMC Only (by nibble): | YYYYYYYYY | YYYYYYYYY | YYYYNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | YYYYYYYYY |

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*Figure 8:* **VC1902 Banks in VSVD1760 Package**

| | | | |
|---|---|---|---|
| GTY Quad 106<br>X0Y6<br>CD [L] | HDIO<br>Bank 306 | HDIO<br>Bank 406 | GTY Quad 206<br>X1Y6 |
| GTY Quad 105<br>X0Y5<br>CC [L] (RCAL) | PCIE<br>X0Y2 | PCIE<br>X1Y2 | GTY Quad 205<br>X1Y5 |
| GTY Quad 104<br>X0Y4<br>CB [L] (RCAL) | PCIE<br>X0Y1 | MRMAC<br>X0Y3 | GTY Quad 204<br>X1Y4<br>BB [R] |
| GTY Quad 103<br>X0Y3<br>CA [L] | CPM4 | MRMAC<br>X0Y2 | GTY Quad 203<br>X1Y3<br>BA [R] (RCAL) |
| CPM4 | CPM4 | PCIE<br>X1Y0 | GTY Quad 202<br>X1Y2 (RCAL) |
| LPDMIO<br>Bank 502 | PMCDIO<br>Bank 503 | MRMAC<br>X0Y1 | GTY Quad 201<br>X1Y1 |
| PMCMIO/PMCDIO<br>Bank 500 | PMCMIO<br>Bank 501 | MRMAC<br>X0Y0 | GTY Quad 200<br>X1Y0 |

| | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | XPIO<br>Bank 700<br>A | XPIO<br>Bank 701<br>B | XPIO<br>Bank 702<br>C | XPIO<br>Bank 703<br>D | XPIO<br>Bank 704<br>E | XPIO<br>Bank 705<br>F | XPIO<br>Bank 706<br>G | XPIO<br>Bank 707<br>H | XPIO<br>Bank 708<br>I | XPIO<br>Bank 709<br>J | XPIO<br>Bank 710<br>K | XPIO<br>Bank 711<br>L |
| DDRMC Only (by nibble): | YYYYYYYYY | YYYYYYYYY | YYYYNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | YYYYYYYYY |

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*Figure 9:* **VC1902 Banks in VSVA2197 Package**

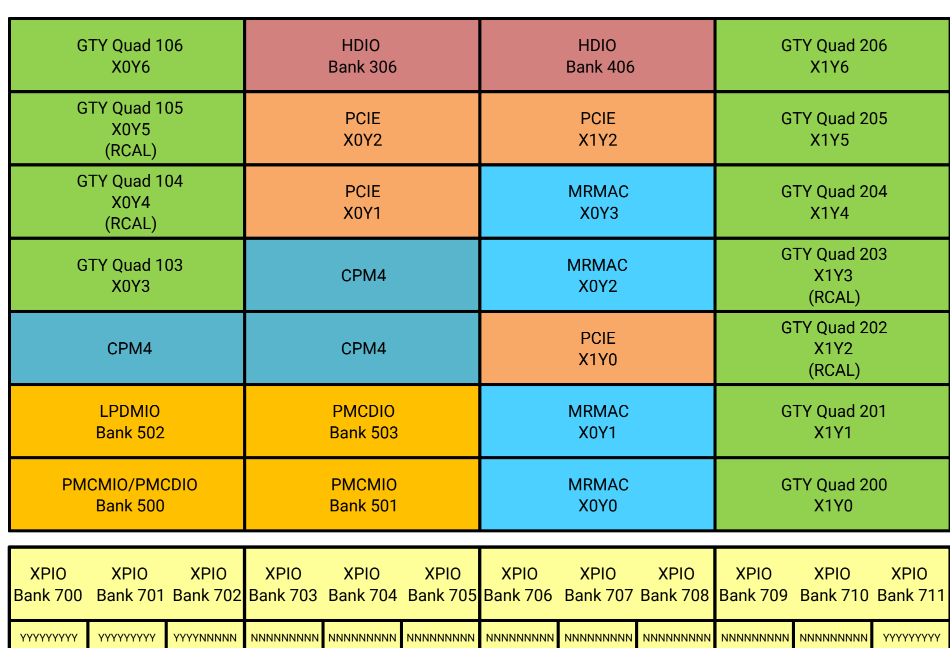
| | | | |
|---|---|---|---|
| GTY Quad 106<br>X0Y6<br>CD [L] | HDIO<br>Bank 306<br>AA | HDIO<br>Bank 406<br>AB | GTY Quad 206<br>X1Y6<br>BG [R] |
| GTY Quad 105<br>X0Y5<br>CC [L] (RCAL) | PCIE<br>X0Y2 | PCIE<br>X1Y2 | GTY Quad 205<br>X1Y5<br>BF [R] |
| GTY Quad 104<br>X0Y4<br>CB [L] (RCAL) | PCIE<br>X0Y1 | MRMAC<br>X0Y3 | GTY Quad 204<br>X1Y4<br>BE [R] |
| GTY Quad 103<br>X0Y3<br>CA [L] | CPM4 | MRMAC<br>X0Y2 | GTY Quad 203<br>X1Y3<br>BD [R] (RCAL) |
| CPM4 | CPM4 | PCIE<br>X1Y0 | GTY Quad 202<br>X1Y2<br>BC [R] (RCAL) |
| LPDMIO<br>Bank 502 | PMCDIO<br>Bank 503 | MRMAC<br>X0Y1 | GTY Quad 201<br>X1Y1<br>BB [R] |
| PMCMIO/PMCDIO<br>Bank 500 | PMCMIO<br>Bank 501 | MRMAC<br>X0Y0 | GTY Quad 200<br>X1Y0<br>BA [R] |

| | XPIO Bank 700 A | XPIO Bank 701 B | XPIO Bank 702 C | XPIO Bank 703 D | XPIO Bank 704 E | XPIO Bank 705 F | XPIO Bank 706 G | XPIO Bank 707 H | XPIO Bank 708 I | XPIO Bank 709 J | XPIO Bank 710 K | XPIO Bank 711 L |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DDRMC Only (by nibble): | YYYYYYYYY | YYYYYYYYY | YYYYNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | YYYYYYYYY |

X24034-052420

# VM1802 Bank Diagram Overview

*Figure 10:* **VM1802 Banks**



## Bank Diagram by Package for VM1802

*Figure 11:* **VM1802 Banks in VFVC1760 Package**

| | | | |
|---|---|---|---|
| GTY Quad 106<br>X0Y6<br>CD [LS] | HDIO<br>Bank 306<br>AE | HDIO<br>Bank 406<br>AF | GTY Quad 206<br>X1Y6<br>BG [RN] |
| GTY Quad 105<br>X0Y5<br>CC [LS] (RCAL) | PCIE<br>X0Y2 | PCIE<br>X1Y2 | GTY Quad 205<br>X1Y5<br>BF [RN] |
| GTY Quad 104<br>X0Y4<br>CB [LS] (RCAL) | PCIE<br>X0Y1 | MRMAC<br>X0Y3 | GTY Quad 204<br>X1Y4<br>BE [RN] |
| GTY Quad 103<br>X0Y3<br>CA [LS] | CPM4 | MRMAC<br>X0Y2 | GTY Quad 203<br>X1Y3<br>BD [RS] (RCAL) |
| CPM4 | CPM4 | PCIE<br>X1Y0 | GTY Quad 202<br>X1Y2<br>BC [RS] (RCAL) |
| LPDMIO<br>Bank 502 | PMCDIO<br>Bank 503 | MRMAC<br>X0Y1 | GTY Quad 201<br>X1Y1<br>BB [RS] |
| PMCMIO/PMCDIO<br>Bank 500 | PMCMIO<br>Bank 501 | MRMAC<br>X0Y0 | GTY Quad 200<br>X1Y0<br>BA [RS] |

| | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | XPIO<br>Bank 700<br>A | XPIO<br>Bank 701<br>B | XPIO<br>Bank 702<br>C | XPIO<br>Bank 703<br>AA | XPIO<br>Bank 704<br>AB | XPIO<br>Bank 705<br>AC | XPIO<br>Bank 706<br>AD | XPIO<br>Bank 707 | XPIO<br>Bank 708 | XPIO<br>Bank 709 | XPIO<br>Bank 710 | XPIO<br>Bank 711 |
| DDRMC Only<br>(by nibble): | YYYYYYYYY | YYYYYYYYY | YYYYNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | YYYYYYYYY |

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*Figure 12:* **VM1802 Banks in VSVD1760 Package**

| | | | |
|---|---|---|---|
| GTY Quad 106<br>X0Y6<br>CD [L] | HDIO<br>Bank 306 | HDIO<br>Bank 406 | GTY Quad 206<br>X1Y6 |
| GTY Quad 105<br>X0Y5<br>CC [L] (RCAL) | PCIE<br>X0Y2 | PCIE<br>X1Y2 | GTY Quad 205<br>X1Y5 |
| GTY Quad 104<br>X0Y4<br>CB [L] (RCAL) | PCIE<br>X0Y1 | MRMAC<br>X0Y3 | GTY Quad 204<br>X1Y4<br>BB [R] |
| GTY Quad 103<br>X0Y3<br>CA [L] | CPM4 | MRMAC<br>X0Y2 | GTY Quad 203<br>X1Y3<br>BA [R] (RCAL) |
| CPM4 | CPM4 | PCIE<br>X1Y0 | GTY Quad 202<br>X1Y2 (RCAL) |
| LPDMIO<br>Bank 502 | PMCDIO<br>Bank 503 | MRMAC<br>X0Y1 | GTY Quad 201<br>X1Y1 |
| PMCMIO/PMCDIO<br>Bank 500 | PMCMIO<br>Bank 501 | MRMAC<br>X0Y0 | GTY Quad 200<br>X1Y0 |

| | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | XPIO<br>Bank 700<br>A | XPIO<br>Bank 701<br>B | XPIO<br>Bank 702<br>C | XPIO<br>Bank 703<br>D | XPIO<br>Bank 704<br>E | XPIO<br>Bank 705<br>F | XPIO<br>Bank 706<br>G | XPIO<br>Bank 707<br>H | XPIO<br>Bank 708<br>I | XPIO<br>Bank 709<br>J | XPIO<br>Bank 710<br>K | XPIO<br>Bank 711<br>L |
| DDRMC Only<br>(by nibble): | YYYYYYYYY | YYYYYYYYY | YYYYNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | YYYYYYYYY |

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*Figure 13:* **VM1802 Banks in VSVA2197 Package**

| | | | |
|---|---|---|---|
| GTY Quad 106<br>X0Y6<br>CD [L] | HDIO<br>Bank 306<br>AA | HDIO<br>Bank 406<br>AB | GTY Quad 206<br>X1Y6<br>BG [R] |
| GTY Quad 105<br>X0Y5<br>CC [L] (RCAL) | PCIE<br>X0Y2 | PCIE<br>X1Y2 | GTY Quad 205<br>X1Y5<br>BF [R] |
| GTY Quad 104<br>X0Y4<br>CB [L] (RCAL) | PCIE<br>X0Y1 | MRMAC<br>X0Y3 | GTY Quad 204<br>X1Y4<br>BE [R] |
| GTY Quad 103<br>X0Y3<br>CA [L] | CPM4 | MRMAC<br>X0Y2 | GTY Quad 203<br>X1Y3<br>BD [R] (RCAL) |
| CPM4 | CPM4 | PCIE<br>X1Y0 | GTY Quad 202<br>X1Y2<br>BC [R] (RCAL) |
| LPDMIO<br>Bank 502 | PMCDIO<br>Bank 503 | MRMAC<br>X0Y1 | GTY Quad 201<br>X1Y1<br>BB [R] |
| PMCMIO/PMCDIO<br>Bank 500 | PMCMIO<br>Bank 501 | MRMAC<br>X0Y0 | GTY Quad 200<br>X1Y0<br>BA [R] |

| | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | XPIO<br>Bank 700<br>A | XPIO<br>Bank 701<br>B | XPIO<br>Bank 702<br>C | XPIO<br>Bank 703<br>D | XPIO<br>Bank 704<br>E | XPIO<br>Bank 705<br>F | XPIO<br>Bank 706<br>G | XPIO<br>Bank 707<br>H | XPIO<br>Bank 708<br>I | XPIO<br>Bank 709<br>J | XPIO<br>Bank 710<br>K | XPIO<br>Bank 711<br>L |
| DDRMC Only (by nibble): | YYYYYYYYY | YYYYYYYYY | YYYYNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | NNNNNNNNN | YYYYYYYYY |

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# Package Files

## About ASCII Package Files

The ASCII package files for each Versal™ ACAP include a comma-separated-values (CSV) version and a text version optimized for a browser or text editor in fixed-width fonts. The information in each of the files includes:

- Header with device/package name (family-device-package), date and time of creation, package specification designator, and revision history
- Seven columns containing data for each pin:
  - Pin—Pin location on the package
  - Pin Name—The name of the assigned pin
  - Bank—Bank number
  - I/O Type—HDIO, XPIO, GTY, GTM, PMCMIO, PMCDIO, or LPDMIO depends on the I/O type. For more information on the I/O type, see *Versal ACAP SelectIO Resources Architecture Manual* (AM010).
  - Super logic region (SLR) number for SSI devices (not applicable for monolithic devices).
  - XPIOPerf—Performance (HIGH, MEDIUM, or LOW) that the LPDDR4 interfaces are specified. See the device data sheet for performance definitions.
  - DDRMC Only—For XPIO pins, YES specifies that the pin is supported for use in DDR applications only and does not include full access to XPIO logic resources. YES_PLUS_GC specifies the pin is supported for use in DDR applications and additionally has full access to clock management resources. NO specifies the pin has full access to XPIO logic resources.
- Total number of pins in the package

**Related Information**

ASCII Pinout Files

# Package Specifications Designations

Package specifications are designated as evaluation only, engineering sample, or production. Each designation is defined as follows.

### Evaluation Only

These package specifications are based on initial device specifications, package routability analysis and mechanical package construction. Package specifications with this designation are not stable and package pinouts are likely to change and these specifications should only be used for initial system level design feasibility.

### Engineering Sample

These package specifications are based on a released package design and validated with ES engineering sample (ES) devices. Package specifications with this designation are considered stable, however some pinout and mechanical specifications might change prior to the production release of the particular device. Package pinouts with this designation are to be used for PCB and Vivado® designs using ES devices.

### Production

These package specifications are released coincident with production release of a particular device. Customers receive formal notification of any subsequent changes.

# ASCII Pinout Files

Links to the ASCII pinout information device/package combinations are listed in the following table.

***Note***: All package files are ASCII files in TXT and CSV file format.

**IMPORTANT!** *IMPORTANT: All packages are available with eutectic BGA balls. To order these packages, the device type starts with an XQ vs. XC or XA, and the Pb-free signifier in the package name is Q.*

*Table 14:* **Package/Device Pinout Files**

| Packages | Footprint Compatible Devices | | | | | Package Status |
|---|---|---|---|---|---|---|
| SFVB625 | VM1102 | | | | | Evaluation Only |
| VBVA1024 | VC1352 | VC1502 | | | | Evaluation Only |
| VFVB1024 | VM1102 | VM1302 | VM1402 | | | Evaluation Only |
| VFVB1369 | VM1302 | VM1402 | VM1502 | | | Evaluation Only |
| VFVF1369 | VM1302 | VM1402 | | | | Evaluation Only |
| VSVE1369 | VC1352 | VC1702 | | | | Evaluation Only |
| VSVG1369 | VC1502 | | | | | Evaluation Only |
| VSVA1596 | VC1502 | VC1702 | | | | Evaluation Only |
| VIVA1596 | VC1802 | VC1902 | | | | Engineering Sample |
| VFVA1760 | VM1302 | VM1402 | VM2602 | | | Evaluation Only |
| VFVC1760 | VM1502 Evaluation Only | VM1802 Engineering Sample | VM2602 Evaluation Only | VM2902 Evaluation Only | | |
| VSVD1760 | VM1802 | VC1802 | VC1902 | | | Engineering Sample |
| VSVA2197 | VM1802 Engineering Sample | VM2502 Evaluation Only | VC1502 Evaluation Only | VC1802 Engineering Sample | VC1902 Engineering Sample | |

**Related Information**

Package Specifications Designations

# Device Diagrams

The diagrams in this chapter show top-view perspective of the package pinout of each Versal™ device/package combination. The following table is a cross reference to the device/package diagrams. The device diagram shows the location of each user I/O, PMCMIO, LPDMIO, PMCDIO, and GTY transceiver and the respective bank or GTY quad, as well as the location of every power pin in the package. See Package Specifications Designations for definitions of Evaluation Only, Engineering Sample, and Production device diagrams.

**IMPORTANT!** *All packages are available with eutectic BGA balls. To order these packages, the device type starts with an XQ vs. XC or XA, and the Pb-free signifier in the package name is Q.*

*Table 15:* **Cross-Reference to Versal Device Diagrams by Package**

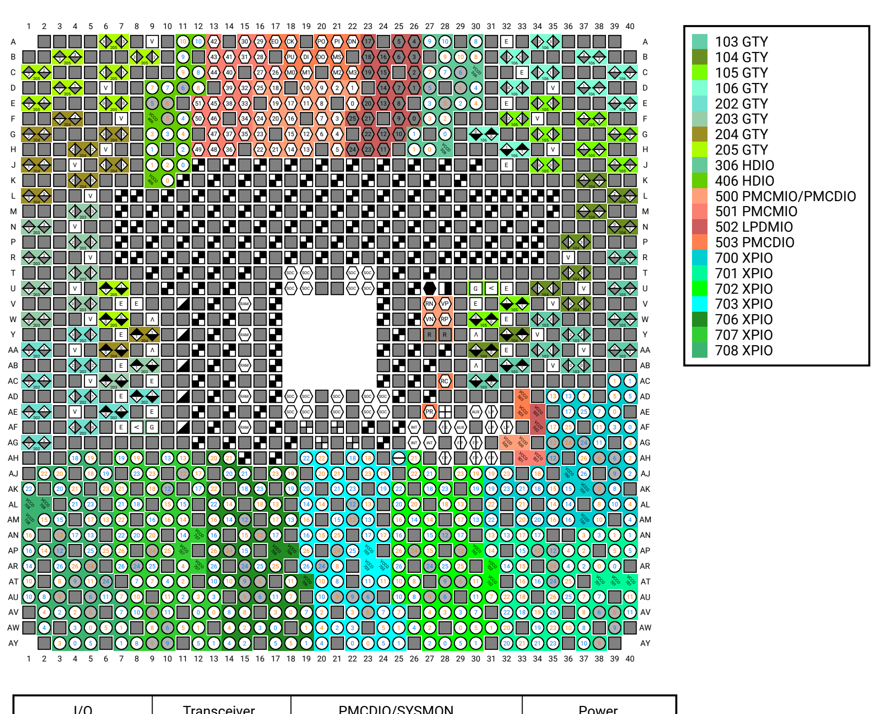
| Package | Footprint Compatible Devices | | | | |
|---|---|---|---|---|---|
| SFVB625 | VM1102<br>Evaluation Only | | | | |
| VBVA1024 | VC1352<br>Evaluation Only | VC1502<br>Evaluation Only | | | |
| VFVB1024 | VM1102<br>Evaluation Only | VM1302<br>Evaluation Only | VM1402<br>Evaluation Only | | |
| VFVF1369 | VM1302<br>Evaluation Only | VM1402<br>Evaluation Only | | | |
| VSVE1369 | VC1352<br>Evaluation Only | VC1702<br>Evaluation Only | | | |
| VSVG1369 | VC1502<br>Evaluation Only | | | | |
| VSVA1596 | VC1502<br>Evaluation Only | VC1702<br>Evaluation Only | | | |
| VIVA1596 | VC1802<br>Engineering Sample | VC1902<br>Engineering Sample | | | |
| VFVA1760 | VM1302<br>Evaluation Only | VM1402<br>Evaluation Only | VM2602<br>Evaluation Only | | |
| VFVC1760 | VM1502<br>Evaluation Only | VM1802<br>Engineering Sample | VM2602<br>Evaluation Only | VM2902<br>Evaluation Only | |
| VSVD1760 | VM1802<br>Engineering Sample | VC1802<br>Engineering Sample | VC1902<br>Engineering Sample | | |

*Table 15:* **Cross-Reference to Versal Device Diagrams by Package** *(cont'd)*

| Package | Footprint Compatible Devices | | | | |
|---|---|---|---|---|---|
| VSVA2197 | VM1802 Engineering Sample | VM2502 Evaluation Only | VC1502 Evaluation Only | VC1802 Engineering Sample | VC1902 Engineering Sample |

# VIVA1596 Package—VC1802

*Figure 14:* **VIVA1596 Package—VC1802 Device Diagram**




| I/O | Transceiver | PMCDIO/SYSMON | Power |
|---|---|---|---|
| IO_L#P<br>IO_L#N<br>IO_L#P_GC<br>IO_L#N_GC<br>IO_VR<br>PMC_MIO<br>LPD_MIO | RXP#<br>RXN#<br>TXP#<br>TXN#<br>REFCLKP#<br>REFCLKN#<br>AVTTRCAL<br>RREF<br>AVCC<br>AVTT<br>AVCCAUX | MODE#<br>ERROR_OUT<br>RTC_PADO<br>RTC_PADI<br>PUDC_B<br>DONE<br>REF_CLK<br>POR_B<br>TCK<br>TDI<br>TDO<br>TMS<br>VREFN<br>VREFP<br>VN<br>VP | VCCINT<br>VCCAUX<br>VCC_IO<br>VCCAUX_PMC<br>VCC_PSFP<br>VCC_PSLP<br>VCC_PMC<br>VCC_SOC<br>VCC_RAM<br>VCC_BATT<br>VCC_FUSE<br>VCCAUX_SMON<br>GND_SMON<br>GND<br>RSVDGND<br>NC |

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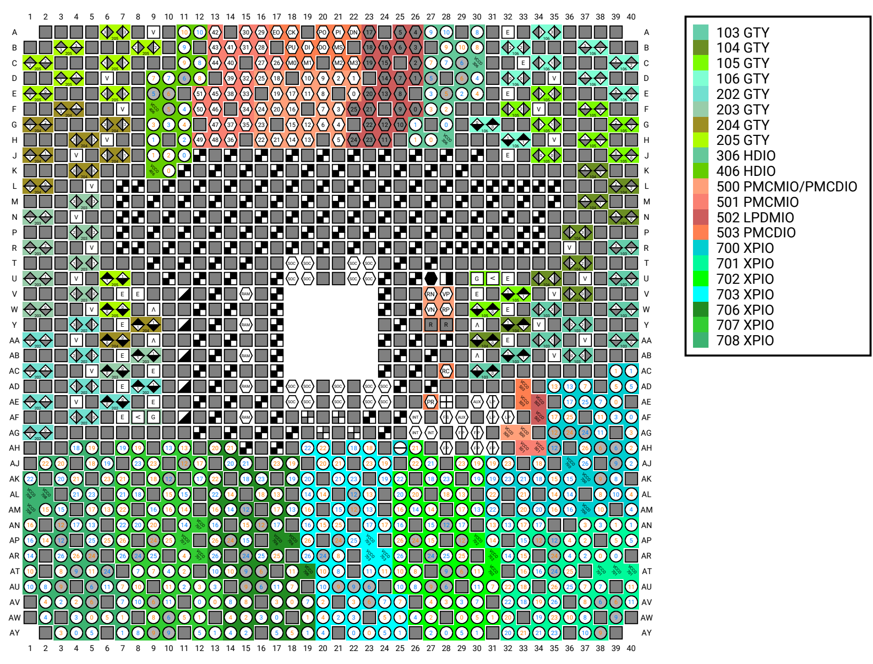
## VIVA1596 Package—VC1902

*Figure 15:* **VIVA1596 Package—VC1902 Device Diagram**




| I/O | Transceiver | PMCDIO/SYSMON | Power |
|---|---|---|---|
| IO_L#P | RXP# | MODE# | VCCINT |
| IO_L#N | RXN# | ERROR_OUT | VCCAUX |
| IO_L#P_GC | TXP# | RTC_PADO | VCC_IO |
| IO_L#N_GC | TXN# | RTC_PADI | VCCAUX_PMC |
| IO_VR | REFCLKP# | PUDC_B | VCC_PSFP |
| PMC_MIO | REFCLKN# | DONE | VCC_PSLP |
| LPD_MIO | AVTTRCAL | REF_CLK | VCC_PMC |
| | RREF | POR_B | VCC_SOC |
| | AVCC | TCK | VCC_RAM |
| | AVTT | TDI | VCC_BATT |
| | AVCCAUX | TDO | VCC_FUSE |
| | | TMS | VCCAUX_SMON |
| | | VREFN | GND_SMON |
| | | VREFP | GND |
| | | VN | RSVDGND |
| | | VP | NC |

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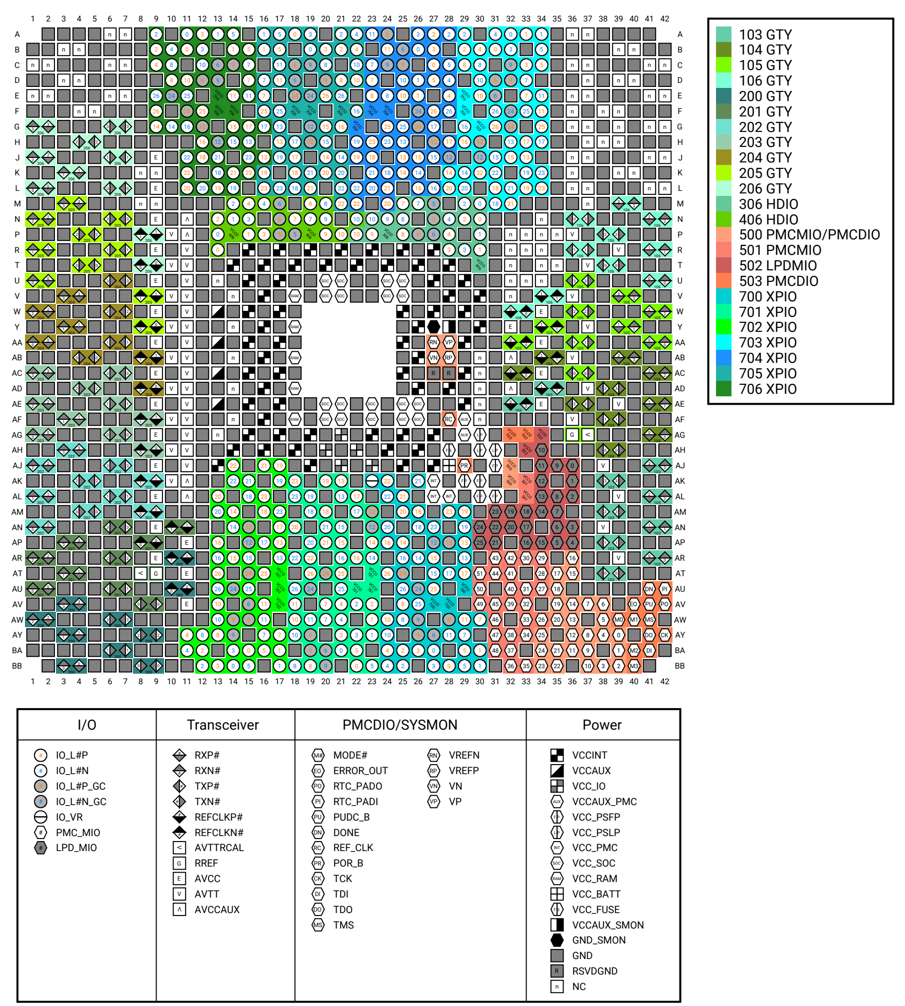
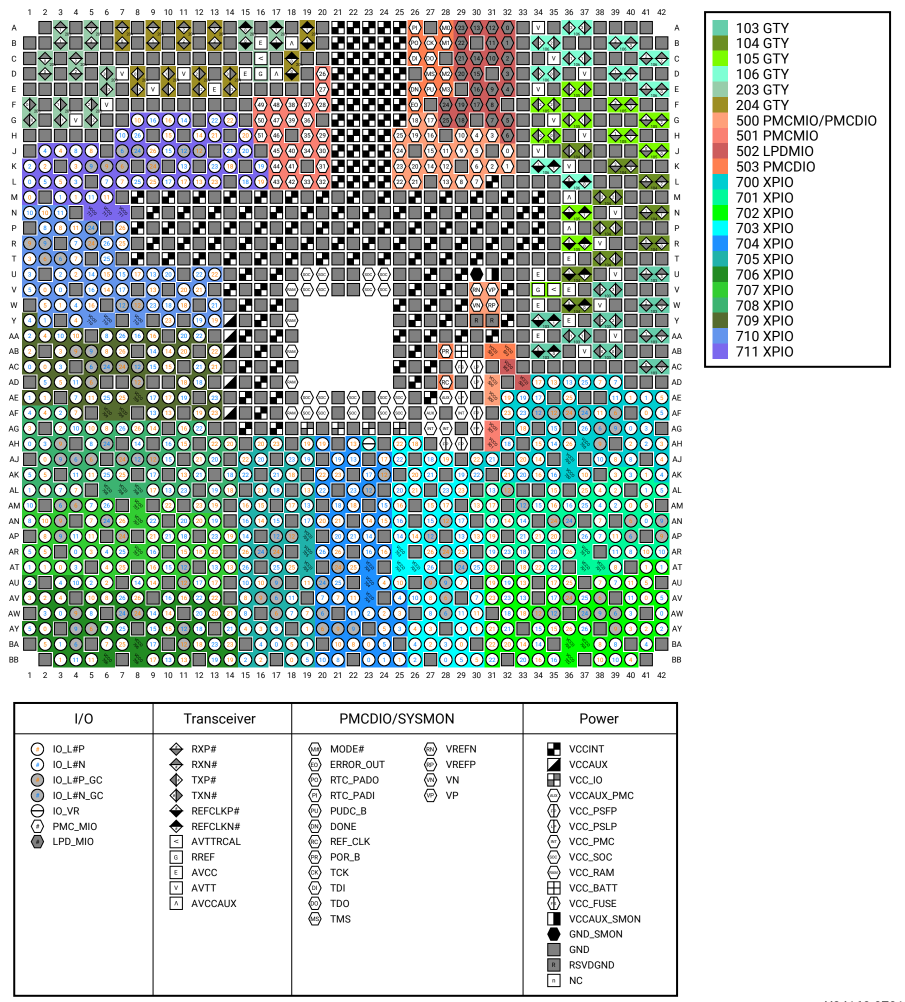
# VFVC1760 Package—VM1802

*Figure 16:* **VFVC1760 Package—VM1802 Device Diagram**



# VSVD1760 Package—VC1802

*Figure 17:* **VSVD1760 Package—VC1802 Device Diagram**

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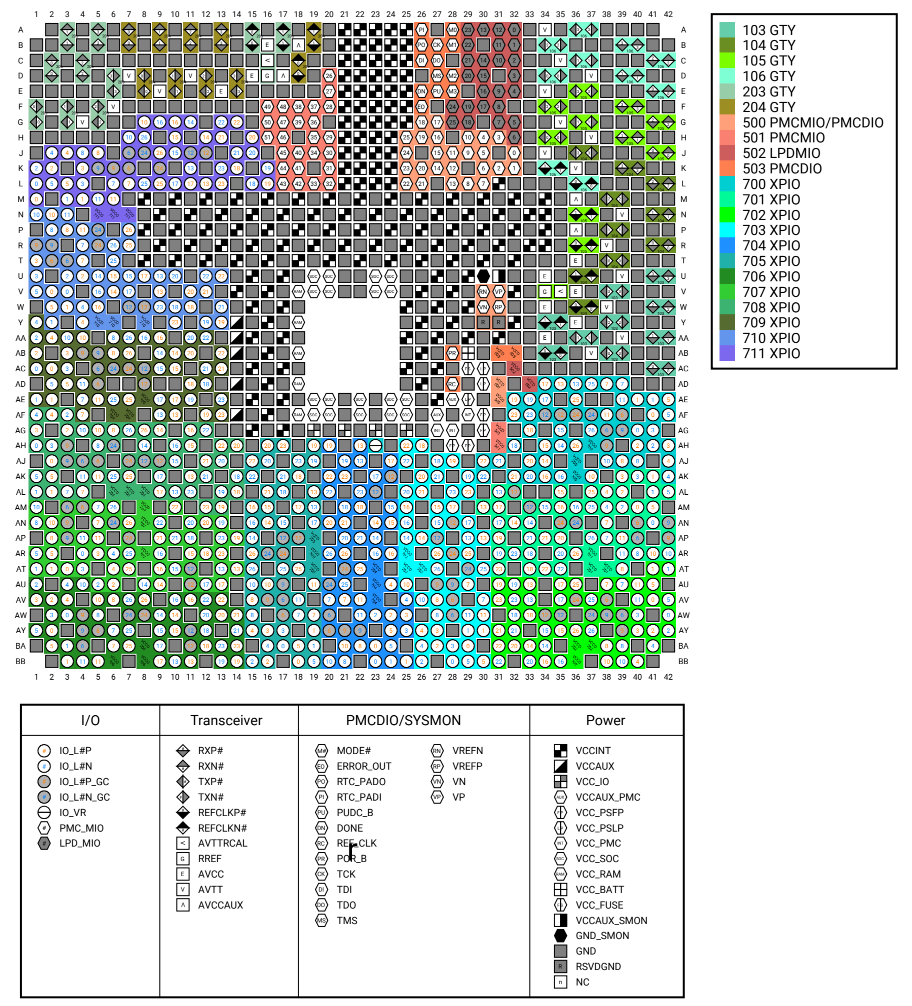
# VSVD1760 Package—VC1902

*Figure 18:* **OLD VSVD1760 Package—VC1902 Device Diagram**



# VSVD1760 Package—VM1802

103 GTY
104 GTY
105 GTY
106 GTY
203 GTY
204 GTY
500 PMCMIO/PMCDIO
501 PMCMIO
502 LPDMIO
503 PMCDIO
700 XPIO
701 XPIO
702 XPIO
703 XPIO
704 XPIO
705 XPIO
706 XPIO
707 XPIO
708 XPIO
709 XPIO
710 XPIO
711 XPIO

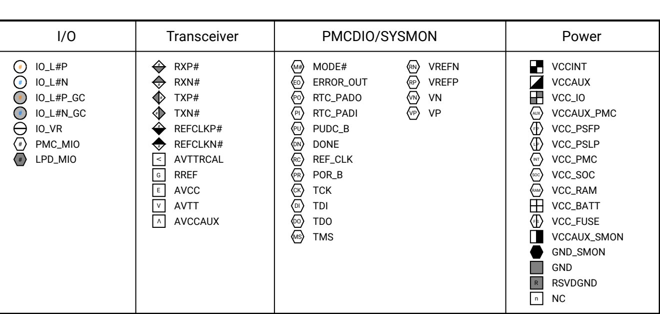



*Figure 19:* **VSVD1760 Package—VM1802 Device Diagram**

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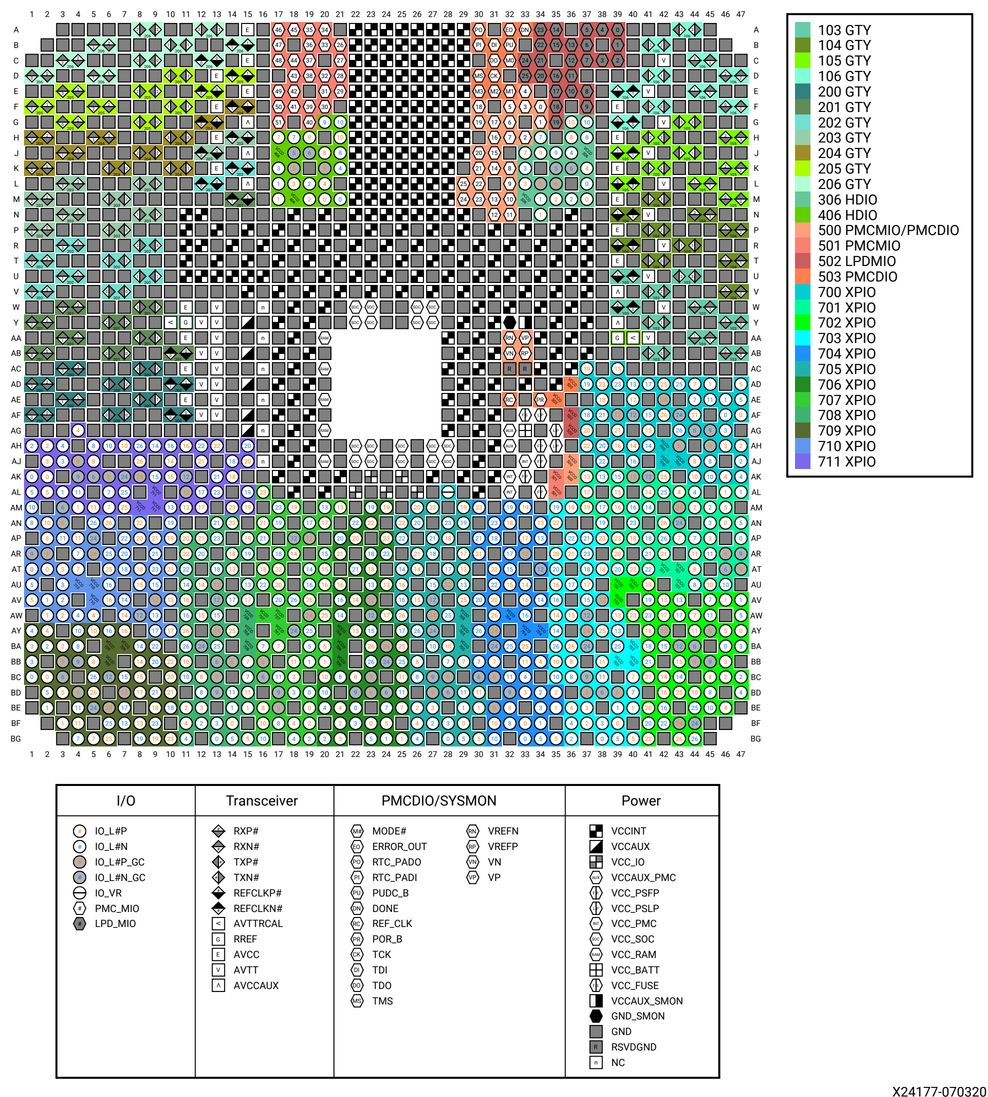
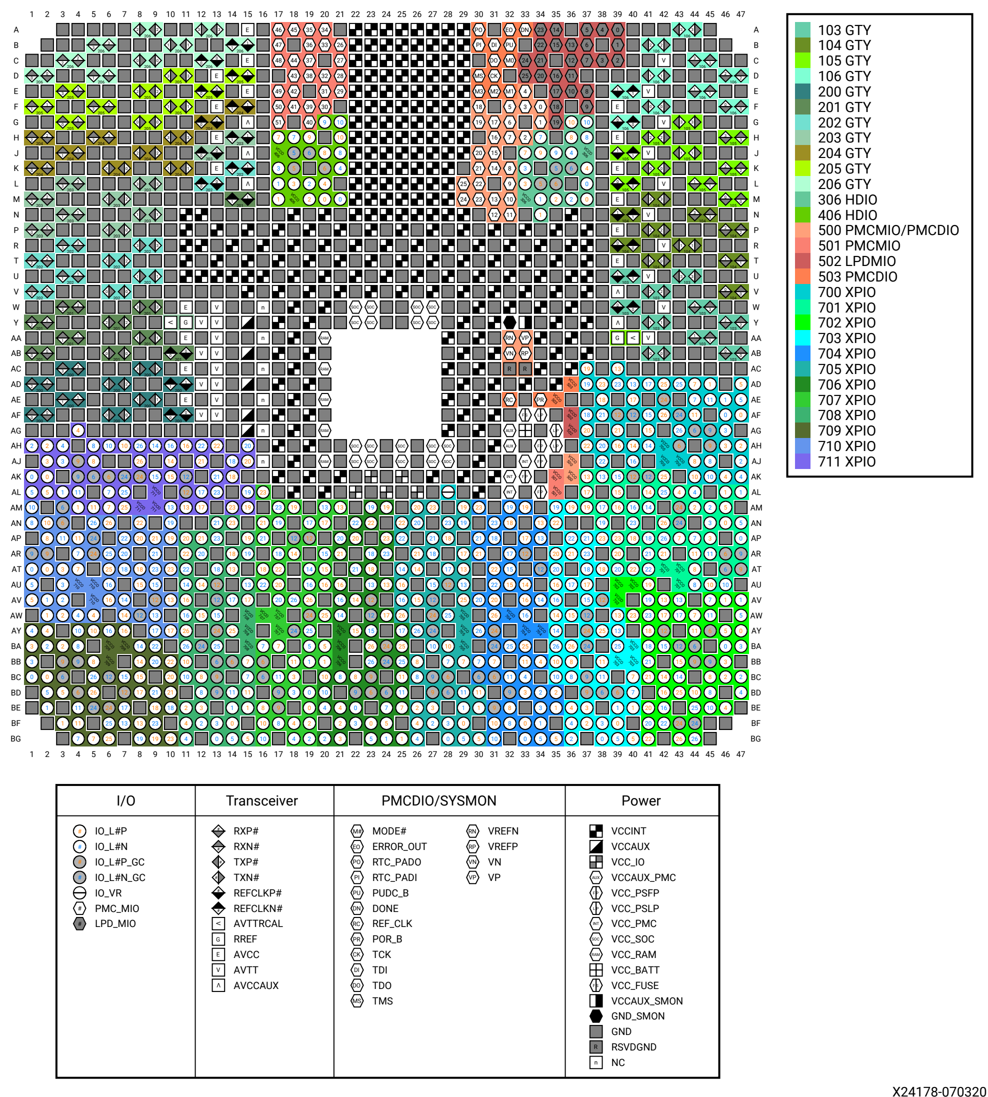
# VSVA2197 Package—VC1802

*Figure 20:* **VSVA2197 Package—VC1902 Device Diagram**



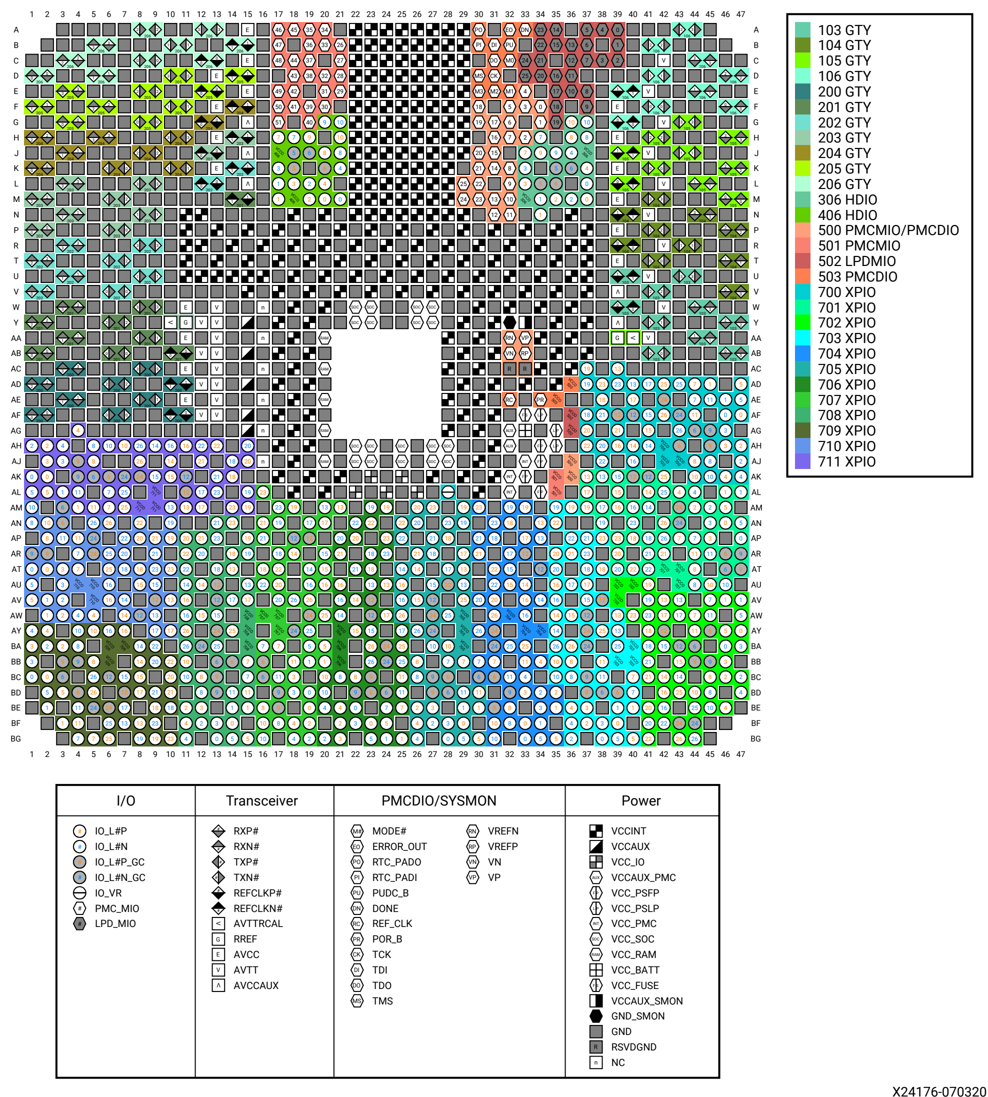
# VSVA2197 Package—VC1902

*Figure 21:* **VSVA2197 Package—VC1902 Device Diagram**



# VSVA2197 Package—VM1802

*Figure 22:* **VSVA2197 Package—VM1802 Device Diagram**



# Mechanical Drawings

This chapter provides mechanical drawings (package specifications) of the Versal™ ACAPs. The following table is a cross-reference to the mechanical drawings by device and package combination. See Package Specifications Designations for definitions of Evaluation Only, Engineering Sample, and Production mechanical drawings.

**IMPORTANT!** *All packages are available with eutectic BGA balls. To order these packages, the device type starts with an XQ vs. XC or XA, and the Pb-free signifier in the package name is Q. For the mechanical drawings, refer to the Pb-free version of these packages.*

See the Table 18: Mechanical Drawing Dimension Definitions table for details on key dimensions/tolerances shown in each mechanical drawing.

*Table 16:* **Cross-Reference to Versal ACAP AI Core Series Mechanical Drawings by Package**

| Package | Devices | | | | |
|---|---|---|---|---|---|
| | VC1352 | VC1502 | VC1702 | VC1802 | VC1902 |
| VBVA1024 | | | | | |
| VSVE1369 | | | | | |
| VSVG1369 | | | | | |
| VSVA1596 | | | | | |
| VIVA1596 | | | | Figure 23<br>Engineering Sample | Figure 23<br>Engineering Sample |
| VSVD1760 | | | | Figure 25<br>Engineering Sample | Figure 25<br>Engineering Sample |
| VSVA2197 | | | | Figure 26<br>Engineering Sample | Figure 26<br>Engineering Sample |

*Table 17:* **Cross-Reference to Versal ACAP Prime Series Mechanical Drawings by Package**

| Package | Devices | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | VM1102 | VM1302 | VM1402 | VM1502 | VM1802 | VM2502 | VM2602 | VM2902 |
| SFVB625 | | | | | | | | |
| VFVB1024 | | | | | | | | |
| VFVB1369 | | | | | | | | |
| VFVF1369 | | | | | | | | |
| VFVA1760 | | | | | | | | |
| VFVC1760 | | | | | Figure 24<br>Engineering Sample | | | |
| VSVD1760 | | | | | Figure 25<br>Engineering Sample | | | |
| VSVA2197 | | | | | Figure 26<br>Engineering Sample | | | |

*Table 18:* **Mechanical Drawing Dimension Definitions**

| Dimension | Definition |
|---|---|
| ⌓ | Bilateral tolerance of package sides with respect to datums A and B |
| ▱ | Flatness tolerance of silicon die or package lid top surface |
| / / | Bilateral tolerance for parallelism of silicon die or package lid top surface with respect to the seating plane datum C |
| A | Thickness of package with respect to the seating plane datum C |
| $A_1$ | Thickness of BGA balls with respect to the seating plane datum C |
| $A_2$ | Thickness of package body, including stiffener ring or lid and excluding BGA balls, with respect to the seating plane datum C |
| $A_3$ | Distance from top of silicon die to top of stiffener ring or lid with respect to the seating plane datum C |
| D/E | Length/width of package with respect to datums A and B |
| $D_1/E_1$ | Length/width of BGA matrix with respect to datums A and B |
| e | BGA ball pitch measured at the center of each ball |
| øb | BGA ball diameter |
| ⌓ aaa | Unidirectional upward tolerance with respect to the seating plane datum C |
| / / bbb | Bilateral tolerance for parallelism of package surface with respect to the seating plane datum C |
| øddd | BGA ball position tolerance of diameter ddd with respect to datums A and B perpendicular to the seating plane datum C in which the center of each ball must lie |
| øeee | BGA ball position tolerance of diameter eee measured with respect to other balls within the BGA matrix in which the center of each ball must lie |
| M | BGA ball matrix size |

# VIVA1596 Package—VC1802 and VC1902

*Figure 23:* **Package Dimensions for VIVA1596 (VC1802 and VC1902)**

| SYMBOL | MILLIMETERS MIN. | NOM. | MAX. | NOTE |
|---|---|---|---|---|
| A | 3.60 | 3.80 | 4.00 | |
| A1 | 0.40 | 0.50 | 0.60 | |
| A2 | 3.10 | 3.30 | 3.50 | |
| A3 | 0.95 | 1.05 | 1.15 | |
| D/E | 40.00 BASIC | | | |
| D1/E1 | 35.88 BASIC | | | |
| e | 0.92 BASIC | | | |
| Øb | 0.50 | 0.64 | 0.70 | |
| aaa | | | 0.20 | |
| bbb | | | 0.35 | |
| ddd | | | 0.25 | |
| eee | | | 0.10 | |
| M | 40 | | | 2 |

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.

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**Related Information**

Mechanical Drawings

# VFVC1760 Package—VM1802

*Figure 24:* **Package Dimensions for VFVC1760 (VM1802)**

BOTTOM VIEW

TOP VIEW

SECTION A–A

VFVA1760 – Sn/Ag/Cu SOLDER BALLS
VFVC1760 – Sn/Ag/Cu SOLDER BALLS

| SYMBOL | MILLIMETERS | | | NOTE |
|---|---|---|---|---|
| | MIN. | NOM. | MAX. | |
| A | 3.49 | 3.69 | 3.89 | |
| $A_1$ | 0.40 | 0.50 | 0.60 | |
| $A_2$ | 2.99 | 3.19 | 3.39 | |
| D/E | 40.00 BASIC | | | |
| $D_1$/$E_1$ | 37.72 BASIC | | | |
| e | 0.92 BASIC | | | |
| Øb | 0.50 | 0.64 | 0.70 | |
| aaa | - | - | 0.20 | |
| bbb | - | - | 0.35 | |
| ddd | - | - | 0.25 | |
| eee | - | - | 0.10 | |
| M | 42 | | | 2 |

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.

X24173-070220

### Related Information

Mechanical Drawings

# VSVD1760 Package—VC1802, VC1902, and VM1802

*Figure 25:* **Package Dimensions for VSVD1760 (VC1802, VC1902, and VM1802)**

BOTTOM VIEW

TOP VIEW

SECTION A–A

VSVD1760 - Sn/Ag/Cu SOLDER BALLS

| SYMBOL | MILLIMETERS MIN. | NOM. | MAX. | NOTE |
|---|---|---|---|---|
| A | 3.60 | 3.80 | 4.00 | |
| $A_1$ | 0.40 | 0.50 | 0.60 | |
| $A_2$ | 3.10 | 3.30 | 3.50 | |
| $A_3$ | 0.95 | 1.05 | 1.15 | |
| D/E | 40.00 BASIC | | | |
| $D_1$/$E_1$ | 37.72 BASIC | | | |
| e | 0.92 BASIC | | | |
| øb | 0.50 | 0.64 | 0.70 | |
| aaa | — | — | 0.20 | |
| bbb | — | — | 0.35 | |
| ddd | — | — | 0.25 | |
| eee | — | — | 0.10 | |
| M | 42 | | | 2 |

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.

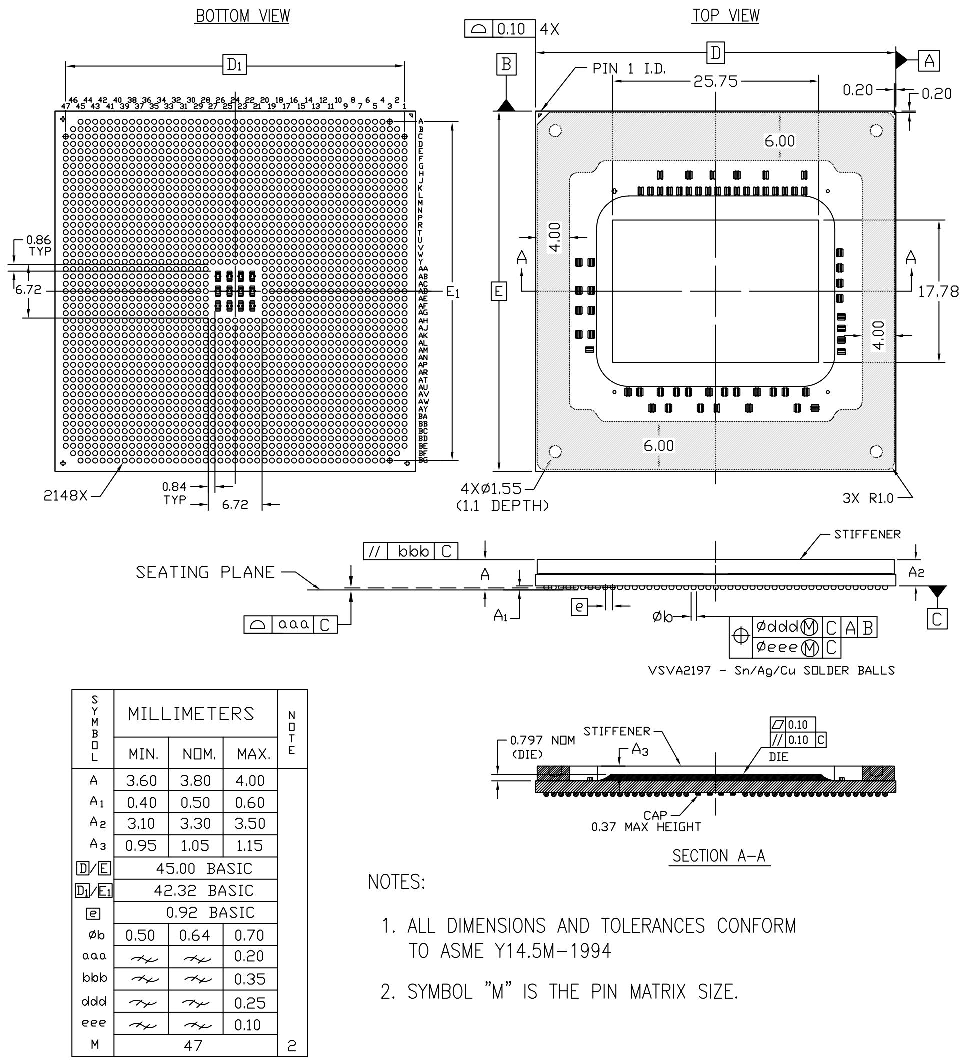
X24171-070120

**Related Information**

Mechanical Drawings

# VSVA2197 Package—VC1802, VC1902, and VM1802

*Figure 26:* **Package Dimensions for VSVA2197 (VC1802, VC1902, and VM1802)**




| SYMBOL | MILLIMETERS MIN. | NOM. | MAX. | NOTE |
|---|---|---|---|---|
| A | 3.60 | 3.80 | 4.00 | |
| $A_1$ | 0.40 | 0.50 | 0.60 | |
| $A_2$ | 3.10 | 3.30 | 3.50 | |
| $A_3$ | 0.95 | 1.05 | 1.15 | |
| D/E | 45.00 BASIC | | | |
| $D_1$/$E_1$ | 42.32 BASIC | | | |
| e | 0.92 BASIC | | | |
| øb | 0.50 | 0.64 | 0.70 | |
| aaa | ~ | ~ | 0.20 | |
| bbb | ~ | ~ | 0.35 | |
| ddd | ~ | ~ | 0.25 | |
| eee | ~ | ~ | 0.10 | |
| M | 47 | | | 2 |

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M−1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.

X24172-070220

### Related Information

Mechanical Drawings

# Package Marking

The package top-markings for the XC and XA Versal™ devices are similar to the examples shown in the following figure.

*Figure 27:* **Versal Devices Package Marking**

Logo
XILINX®
VERSAL™
2D Bar Code
Country Of Origin
X22638-040919

*Table 19:* **Versal Device Marking Definition—Example**

| Item | Definition |
|---|---|
| Xilinx Logo | Xilinx logo, Xilinx name with trademark, and trademark-registered status. |
| Bar Code | A device-specific bar code is marked on each device. |

# Packing and Shipping

Versal™ devices are packed in trays. Trays are used to pack most of Xilinx surface-mount devices because they provide excellent protection from mechanical damage. In addition, they are manufactured using antistatic material to provide limited protection against ESD damage and can withstand a bake temperature of 125°C.

*Table 20:* **Standard Device Counts per Tray and Box**

| Package | Maximum Number of Devices Per Tray | Maximum Number of Units In One Internal Box |
|---|---|---|
| SFVB625 | 60 | 300 |
| VBVA1024 | | |
| VFVB1024 | | |
| VFVB1369 | | |
| VSVE1369 | | |
| VSVA1596 | | |
| VIVA1596 | 12 | 36 |
| VFVA1760 | 12 | 36 |
| VFVC1760 | 12 | 36 |
| VSVD1760 | 12 | 36 |
| VSVA2197 | 12 | 36 |

**IMPORTANT!** *All packages are available with eutectic BGA balls. To order these packages, the device type starts with an XQ vs. XC or XA, and the Pb-free signifier in the package name is Q (for example: VSQD1760).*

# Chapter 8

# Soldering Guidelines

To implement and control the production of surface-mount assemblies, the dynamics of the solder reflow process and how each element of the process is related to the end result must be thoroughly understood.

**RECOMMENDED:** *Xilinx recommends that customers qualify their custom PCB assembly processes using package samples.*

The primary phases of the reflow process are:

- Melting the particles in the solder paste
- Wetting the surfaces to be joined
- Solidifying the solder into a strong metallurgical bond

The peak reflow temperature of a surface-mount component body should not be more than 250°C maximum (260°C for dry rework only) for Pb-free packages and 220°C for eutectic packages, and is package size dependent. For multiple BGAs in a single board and because of surrounding component differences, Xilinx recommends checking all BGA sites for varying temperatures.

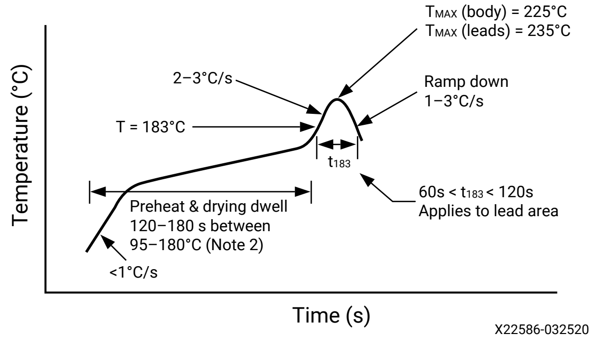
The infrared reflow (IR) process is strongly dependent on equipment and loading. Components might overheat due to lack of thermal constraints. Unbalanced loading can lead to significant temperature variation on the board. These guidelines are intended to assist users in avoiding damage to the components; the actual profile should be determined by those using these guidelines. For complete information on package moisture / reflow classification and package reflow conditions, refer to the Joint IPC/JEDEC Standard J-STD-020C.

**IMPORTANT!** *Following the initial reflow process, devices should not be reworked more than once. Any additional rework beyond that is likely to cause irreparable damage to the device.*

# Sn/Pb Reflow Soldering

The following figure shows typical conditions for solder reflow processing of Sn/Pb soldering using IR/convection. Both IR and convection furnaces are used for BGA assembly. The moisture sensitivity of surface-mount components must be verified prior to surface-mount flow.

*Figure 28:* **Typical Conditions for IR Reflow Soldering of Sn/Pb Solder**




Notes in figure:

1. Maximum temperature range = 225°C (body). Minimum temperature range before 205°C (leads/balls).
2. Preheat dwell 95–180°C for 120–180 seconds.
3. IR reflow must be performed on dry packages.

# Pb-Free Reflow Soldering

Xilinx uses SnAgCu solder balls for commercial-grade (XC) and automotive-grade (XA) BGA packages. In addition, suitable material are qualified for the higher reflow temperatures (250°C maximum, 260°C for dry rework only) required by Pb-free soldering processes.

Xilinx does not support soldering SnAgCu BGA packages with SnPb solder paste using a Sn/Pb soldering process. Traditional Sn/Pb soldering processes have a peak reflow temperature of 220°C. At this temperature range, the SnAgCu BGA solder balls do not properly melt and wet to the soldering surfaces. As a result, reliability and assembly yields can be compromised.

The optimal profile must take into account the solder paste/flux used, the size of the board, the density of the components on the board, and the mix between large components and smaller, lighter components. Profiles should be established for all new board designs using thermocouples at multiple locations on the component. In addition, if there is a mixture of devices on the board, then the profile should be checked at various locations on the board. Ensure that the minimum reflow temperature is reached to reflow the larger components and at the same time, the temperature does not exceed the threshold temperature that might damage the smaller, heat sensitive components.

The following tables and figure provide guidelines for profiling Pb-free solder reflow. In general, a gradual, linear ramp into a spike has been shown by various sources to be the optimal reflow profile for Pb-free solders. This profile has been shown to yield better wetting and less thermal shock than conventional ramp-soak-spike profile for the Sn/Pb system. SnAgCu alloy reaches full liquidus temperature at 235°C. When profiling, identify the possible locations of the coldest solder joints and ensure that those solder joints reach a minimum peak temperature of 235°C for at least 10 seconds. Reflowing at high peak temperatures of 260°C and above can damage the heat sensitive components and cause the board to warp. Users should reference the latest IPC/JEDEC J-STD-020 standard for the allowable peak temperature on the component body. The allowable peak temperature on the component body is dependent on the size of the component. The table lists the peak package reflow body temperature information. In any case, use a reflow profile with the lowest peak temperature possible.

*Table 21:* **Pb-Free Reflow Soldering Guidelines for Package Sizes Up to 45 mm x 45 mm**

| Profile Feature | Convection, IR/Convection |
|---|---|
| Preheat ramp-up rate 30°–150°C | 2°C/s maximum<br>1°C/s maximum for lidless packages with stiffener ring |
| Preheat temperature soak time 150°–200°C | 60–120 seconds |
| Temperature maintained above 217°C | 60–150 seconds (60–90 seconds typical) |
| Time within 5°C of actual peak temperature | 30 seconds maximum |
| Peak temperature (lead/ball) | 230°C–245°C typical (depends on solder paste, board size, component mixture) |
| Maximum peak temperature (body) | 240°C–250°C, package body size dependent (see the specific Versal ACAP Data Sheet). |
| Ramp-down rate | 2°C/s maximum |
| Time 25°C to peak temperature | 3.5 minutes minimum, 5.0 minutes typical, 8 minutes maximum |

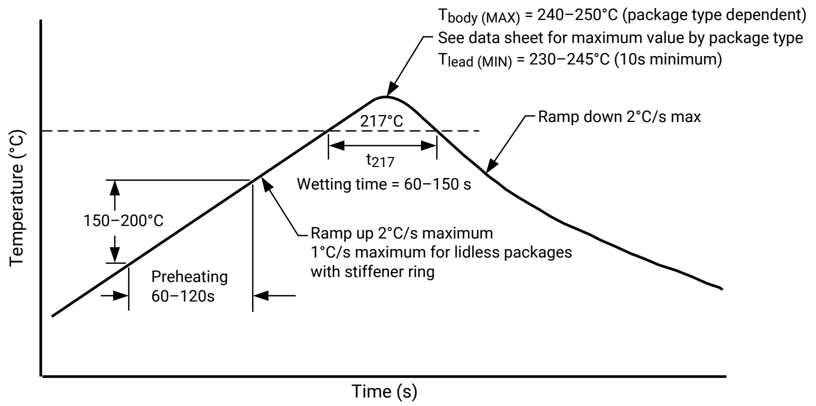
*Table 22:* **Pb-Free Reflow Soldering Guidelines for Package Sizes Greater than 45 mm x 45 mm and Up to 55 mm x 55 mm**

| Profile Feature | Convection, IR/Convection |
|---|---|
| Preheat ramp-up rate 30°–150°C | 0.5°C/s–1.5°C/s |
| Preheat temperature soak time 150°–190°C | 65–70 seconds |
| Temperature maintained above 217°C | 50–60 seconds |
| Maximum peak temperature (body) | 234°C–238°C, package body size dependent (see the specific Versal ACAP Data Sheet). |
| Ramp-down rate 240°–125°C | 1°C/s–2°C/s |

*Table 23:* **Pb-Free Reflow Soldering Guidelines for Package Sizes Greater than 55 mm x 55 mm**

| Profile Feature | Convection, IR/Convection |
|---|---|
| Preheat ramp-up rate 30°–150°C | 0.5°C/s–1.5°C/s |
| Preheat temperature soak time 150°–190°C | 76–81 seconds |
| Temperature maintained above 217°C | 77–93 seconds |
| Maximum peak temperature (body) | 231°C–240°C, package body size dependent (see the specific Versal ACAP Data Sheet). |
| Ramp-down rate 240°–185°C | 0.7°C/s–0.8°C/s |
| Ramp-down rate 185°–125°C | 1.6°C/s–1.75°C/s |

*Figure 29:* **Typical Conditions for Pb-Free Reflow Soldering**




# Peak Package Reflow Temperatures

*Table 24:* **Peak Package Reflow Body Temperature (Based on J-STD-020 Standard)**

| Package | Product Category | Peak Package Reflow Body Temperature[1] | JEDEC Moisture Sensitivity Level (MSL) |
|---|---|---|---|
| SFVB625 | All | Mass reflow: 250°C<br>Dry rework: 260°C | 4 |
| VBVA1024 | All | Mass reflow: 240°C<br>Dry rework: 260°C | 4 |
| VFVB1024 | | | |
| VFVB1369 | | | |
| VSVE1369 | | | |
| VSVA1596 | | | |
| VIVA1596 | | | |
| VFVA1760 | | | |
| VFVC1760 | | | |
| VSVD1760 | | | |
| VSVA2197 | | | |
| VSVA2785 | | | |

**Notes:**

1. See the specific Versal ACAP Data Sheet for the most up-to-date specifications.
2. For devices with the Pb-free signifier in the package name (labeled as Q vs. V) use the temperatures and MSL listed for the XQ product category.

For sophisticated boards with a substantial mix of large and small components, it is critical to minimize the ΔT across the board (<10°C) to minimize board warpage and thus, attain higher assembly yields. Minimizing the ΔT is accomplished by using a slower rate in the warm-up and preheating stages.

It is also important to minimize the temperature gradient on the component, between top surface and bottom side, especially during the cooling down phase. The key is to optimize cooling while maintaining a minimal temperature differential between the top surface of the package and the solder joint area. The temperature differential between the top surface of the component and the solder balls should be maintained at less than 7°C during the critical region of the cooling phase of the reflow process. This critical region is in the part of the cooling phase where the balls are not completely solidified to the board yet, usually between the 200°C–217°C range. To efficiently cool the parts, divide the cooling section into multiple zones, with each zone operating at different temperatures.

The optimal profile must take into account the solder paste/flux used, the size of the board, the density of the components on the board, and the mix between large components and smaller, lighter components. Profiles should be established for all new board designs using thermocouples at multiple locations on the component. In addition, if there is a mixture of devices on the board, then the profile should be checked at various locations on the board, as shown in the following thermocouple pictures. Ensure that the minimum reflow temperature is reached to reflow the larger components and at the same time, the temperature does not exceed the threshold temperature that might damage the smaller, heat sensitive components.

*Figure 30:* **Thermocouple Top**

**TOP Profile,**
**TC 1 : U17 Edge 1**
**TC 2 : U17 Edge 2**
**TC 3 : U17 Edge 3**
**TC 4 : U17 Edge 4**
**TC 5 : U17 Middle 1**
**TC 6 : U17 Middle 2**
**TC 7 : U17 Body**
**TC 8 : Q25**
**TC 9 : U25**

*Figure 31:* **Thermocouple Bottom**

## Post Reflow/Cleaning/Washing

Many PCB assembly subcontractors use a no-clean process in which no post-assembly washing is required. Although a no-clean process is recommended, if cleaning is required, Xilinx recommends a water-soluble paste and a washer using a deionized-water. Baking after the water wash is recommended to prevent fluid accumulation. Cleaning solutions or solvents are not recommended because some solutions contain chemicals that can compromise the lid adhesive, thermal compound, or components inside the package.

## Conformal Coating

Xilinx does not have information regarding the reliability of flip-chip BGA packages on a board after exposure to any specific conformal coating process. Therefore, any process using conformal coating should be qualified for the specific use case to cover the materials and process steps.

Ruggedized XQ packages are designed to support conformal coating, with vented lids that ensure proper cleaning can occur after the etching process and prior to conformal coating.

**RECOMMENDED:** *When a conformal coating is required, Parylene-based material should be used to avoid potential risk of weakening the lid adhesive used in Xilinx packages.*

# Strain Gauge Measurement

Strain gauge measurements are recommended to be done at each process step that has the potential to cause excessive board flexing leading to solder joint cracking. Assembly processes where strain gauge measurements are recommended include:

- PCB router (during PCB loading/unloading into fixture and during the routing process)
- PTH solder assembly during top-catch loading/unloading
- Press fit assembly during press base and tooling loading/unloading and during machine pressing process
- DIMM memory (during PCB loading/unloading and during insertion/removal of DIMM)
- Heat-sink assembly process (during PCB loading/unloading and during entire screw assembly process)
- X-ray fixture (during PCBA loading/unloading)

Strain gauge measurements should be in the range of ±500 µstrain. Dye and pry analysis is required to confirm if the measured strain causes solder joint cracking. It is recommended to conduct dye and pry analysis for any strain reading greater than 500 µstrain. To reduce the affects of strain on a device, edge bonding can be used and is recommended for larger packages. See Chapter 10: Edge Bonding Guidelines for implementation details.

# Solder Paste

Solder paste consists of solder alloy and a flux system. A typical solder paste composition by volume is split between about 50% alloy and 50% flux. The metal load mass (solder alloy powder) is around 90%, with the remaining 10% mass a flux system. The primary purpose of the flux system is to remove the contaminants from the solder joints during the soldering process. The capability of removing contaminants is determined by the activation level of the type of solder paste. The preferred solder paste metal alloy has a lead-free composition (SnAgCu where Ag is 3–4% and Cu is 0.5–1%). A no-clean solder paste is preferred to eliminate any risk of improper cleaning that could leave active residue beneath the device and other BTC components. The paste must be suitable for printing the solder stencil aperture dimensions. Type 4 paste is recommended for better paste release performance. When using a solder paste, you must adhere to the handling recommendations of the paste manufacturer.

# Component Placement

**IMPORTANT!** *The following component placement guidelines apply to all package types included in this guide (lidded, lidless, bare-die, etc.).*

Xilinx device packages must be placed accurately according to their geometry outline. Positioning packages manually via hand mounting is not recommended. Typical component placement accuracies of ±50 µm can be achieved using standard pick and place equipment with vision system. The PCB and components are optically checked and measured by the pick and place vision system. The pick and place machine detects the fiducial on the PCB immediately prior to the placement of the Versal device. Recognition of the packages is performed by the vision system, to ensure correct centering of the Versal device placement on the PCB pad array. BGA packages with solder balls can self-align during the reflow process because of the solder high surface tension that enables the pulling and centering of the device, and where a slight offset of the placement is still allowed. For guidance, the maximum tolerable offset of device placement is around 30% of the pad diameter on the PCB for typical non-solder mask defined pads. This means that the misalignment of solder ball device packages to the PCB pad must be better than 150 µm to assure a robust mounting process. Generally, this is achievable using a wide range of modern pick and placement systems. The following setup conditions are important for the pick and placement systems:

- The pick and place nozzle type should be selected based on the dimensions of the Versal device. The nozzle needs to firmly hold the device package during the pick and place stage. The appropriate nozzle type for the device package can be chosen from the manual provided by the pick and place equipment manufacturer.
- The ball recognition capabilities of the placement system should be used and package outline centering should be avoided. This eliminates the solder ball to package edge tolerances of the package. Refer to the specific package outline drawing for details.
- To ensure the proper identification of the device package during vision recognition, prior to its placement, a suitable lighting system and the correct choice of the features of the measuring method are essential. The most suitable settings can be chosen from the manual provided by the pick and place equipment manufacturer.
- To avoid solder bridging or solder smear, ensure the proper placement force of the device package during placement on the PCB. Excessive placement force can lead to excess solder paste and cause solder bridging. However, a slight placement force can lead to insufficient solder paste contact between the device package solder balls and the solder paste, causing solder defects including open solder joints, badly centered packages, or even head-in-pillow (HIP) defects.

# Component Pick-up Tool Consideration

For pick and place machines to place lidless and bare-die flip-chip BGAs onto PCBs, Xilinx recommends using soft tips or suction cups for the nozzles. This prevents chipping, scratching, or even cracking of the bare die.

*Figure 32:* **Recommended Method For Using Pick-up Tools**

*Chapter 9*

# Recommended PCB Design Rules for BGA

Xilinx provides the diameter of a land pad on the package side. This information is required prior to the start of the board layout so the board pads can be designed to match the component-side land geometry. The typical values of these land pads are shown in the following figure and summarized in the table. For Xilinx BGA packages, non-solder mask defined (NSMD) pads on the board are suggested to allow a clearance between the land metal (diameter L) and the solder mask opening (diameter M) as shown in the following figure.

*Figure 33:* **Suggested Board Layout of Soldered Pads for BGA Packages**

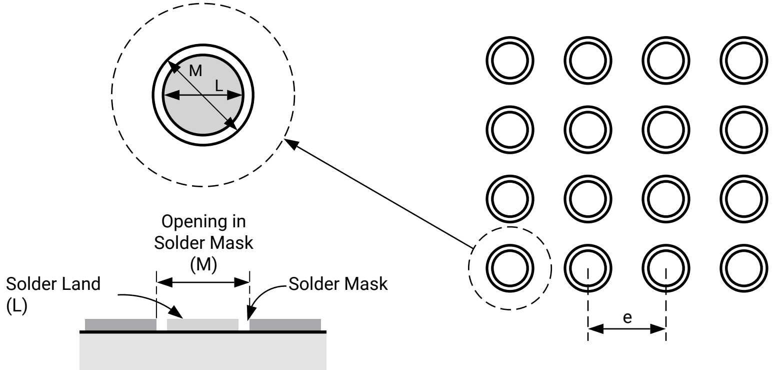



*Table 25:* **BGA Package Design Rules**

| Flip-Chip BGA Packages | 1.0 mm Pitch | 0.92 mm Pitch | 0.80 mm Pitch |
|---|---|---|---|
| **Design Rule** | **BGA packages, non-solder mask defined dimensions in mm (mils)** | | |
| Package land pad opening (SMD) | 0.53 mm (20.9 mils) | 0.53 mm (20.9 mils) | 0.40 mm (15.7 mils) |
| Maximum PCB solder land (L) diameter | 0.53 mm (20.9 mils) | 0.51 mm (20.0 mils) | 0.40 mm (15.7 mils) |
| Opening in PCB solder mask (M) diameter | 0.63 mm (24.8 mils) | 0.61 mm (24.0 mils) | 0.50 mm (19.7 mils) |
| Solder ball land pitch (e) | 1.00 mm (39.4 mils) | 0.92 mm (36.2 mils) | 0.80 mm (31.5 mils) |

An example of an NSMD PCB pad solder joint is shown in the following figure. The space between the NSMD pad and the solder mask, as well as the actual signal trace widths, depend on the capability of the PCB vendor. The cost of the PCB is higher when the line width and spaces are smaller.

> **RECOMMENDED:** *Xilinx recommends not mixing PCB pad isolated via-in-pad plated over (VIPPO) and non-VIPPO design styles because they can cause hot-tear defects that are related to localized Z-direction thermal expansion coefficient mismatch between VIPPO and non-VIPPO vias. A VIPPO via expands less than a non-VIPPO via.*

> **RECOMMENDED:** *Xilinx recommends not mixing PCB pad of solder mask defined (SMD) and non-solder mask defined (NSMD) design styles, because this can cause solder bridging defects. For violation, customers need to work with their CM to optimize the stencil design and assembly process.*

> **RECOMMENDED:** *For packages with names beginning with V or L (e.g., VSVA2197 and LSVA3112), the region underneath the land-side capacitors (LSCs) should be covered by solder mask. If traces are routed on the PCB top layer within the LSC region, clearance space between the PCB traces/solder mask and the capacitors must be ensured. Typically, there is 0.13 mm of clearance between the seating plane (PCB) and the surface of the capacitors. Refer to* Chapter 5: Mechanical Drawings *for LSC locations and relevant dimensions for each package.*

*Figure 34:* **Example of an NSMD PCB Pad Solder Joint**



# Stencil

Solder paste is applied to PCB metal pads by screen printing. The volume of the printed solder paste is determined by the stencil aperture and the stencil thickness. In most cases, the thickness of a stencil must be matched to the needs of all components on the PCB. Stencil apertures should be a circular shape. To ensure a uniform and high-solder paste transfer to the PCB, laser-cut stencil, made from mostly stainless steel, is typically used. Nickel Blank stencils, referring to stencils where the entire foil is laser-cut from a sheet of pure nickel material, can also be used. However, high-quality nano-coated stencils (laser cut from stainless steel) can perform as well as or better than Nickel Blanks.

### Uniform Stencil Aperture Design

- For packages with 0.92 mm ball pitch, a uniform stencil aperture opening of 19.7 mils to 20.0 mils round is recommended, matching the PCB pad size.
- For packages less than 55 mm x 55 mm with 1 mm ball pitch, a uniform stencil aperture opening of 19.7 mils to 20.0 mils round is also recommended.

### Bull's Eye Stencil Recommendation

Another option is to use a *Bull's Eye* stencil aperture, where the board land-pad diameter increases from the center of the device outward, matching the variable aperture diameter of the stencil, at a rate that depends on the warpage as a function of thermal expansion and mechanical attachment. This can vary depending on the PCB. The bull's eye offers a capture margin, because with an increased opening size with respect to the outer BGA balls, more solder paste is printed. A recommended stencil design for the bull's eye design is shown in the following figure. Similar stencil designs are recommended for packages 55 mm x 55 mm and larger with 1 mm ball pitch. The final stencil design should be based on an evaluation of the board design. Designers should work with their CM to optimize the stencil design and assembly process.

**RECOMMENDED:** *Xilinx recommends using a 5 mil thick stencil.*

**RECOMMENDED:** *Xilinx recommends using a uniform stencil aperture opening of 19.7 mils to 20 mils round, matching the PCB pad size for packages with 0.92 mm ball pitch.*

**RECOMMENDED:** *Xilinx recommends using a uniform stencil aperture opening of 19.7 mils to 20 mils round, matching the PCB pad size for packages less than 55 mm x 55 mm with 1.0 mm ball pitch.*

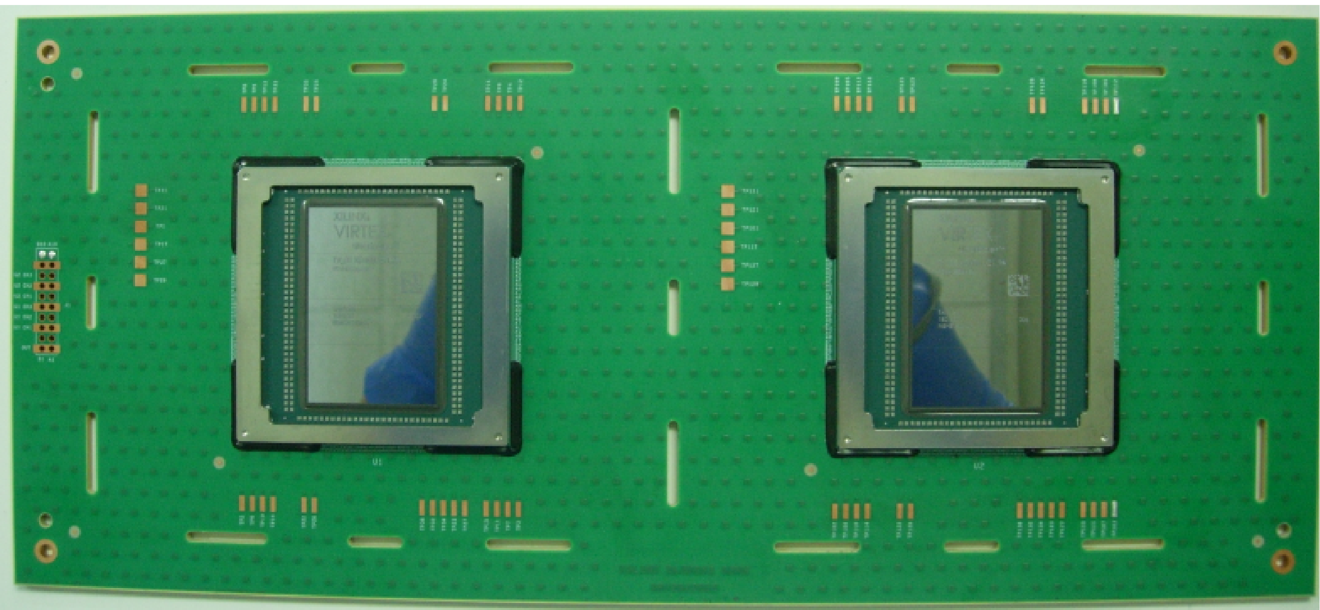
**RECOMMENDED:** *Xilinx recommends using a non-uniform (bull's eye) stencil aperture opening for packages 55 mm x 55 mm and larger with 1.0 mm ball pitch.*

*Figure 35:* **Bull's Eye Stencil Aperture**

# Edge Bonding Guidelines

The edge bonding technique uses high-adhesion adhesives dispensed along the periphery of a component, as shown in the following figure. Xilinx recommends edge bonding larger packages (55 mm x 55 mm or larger) for increased mechanical reliability.

*Figure 36:* **Edge Bonded BGA Packages**



## Edge Bonding Implementation

Edge bonding is the dispensing of an epoxy material around the periphery of the package after board mount. Xilinx requires the use of the Zymet UA-2605-B edge-bonding material. Edge bonding is not intended to under fill the package or contact the solder balls. This technique allows for component rework and improves the robustness of the mounted component by controlling the expansion and warpage of the board during normal operating conditions To place the adhesive while using an in-line soldering robot, Xilinx recommends the parameters shown in the following table.

*Table 26:* **Process Parameters for Edge Bonding**

| Process Parameter | Range Specification |
|---|---|
| Needle size | Range: 25 - 18 gauge<br>Recommended: 18 gauge |
| Needle height | Range: Above the device edge midpoint, or 0 to 1.5 mm below the top surface of the device<br>Recommended: 1.0 mm below the top surface of the device |
| Needle edge spacing | Range: Half to three quarters of needle outer diameter (D)<br>Recommended: Half of needle diameter (D/2), approximately 1.0 mm |
| Dispense needle speed | Range: 0.1 to 200 mm/second<br>Recommended: 9 mm/second |
| Value pressure | Range: 20 to 60 psi<br>Recommended: 1.2 kgf/$cm^2$ @17 psi |

The adhesive is dispensed along the perimeter of the assembled component at a width of 3 mm and a height of 50% to 90% the substrate height, leaving a small section at the center of each edge unbonded, as illustrated in the following figure. This is to ensure that there is an outlet for any expansion of the air during processing. Xilinx recommends centering the opening on each side with a width of 25–30% the length of the package substrate. The exact locations and size of the openings can be varied depending on the design and rework.

*Figure 37:* **Edge Bonding Adhesive Placement Parameters**

**RECOMMENDED:** *Curing conditions are 155°C for 10 minutes.*

## Component Clearance Surrounding Edge Bond

An adjacent component clearance surrounding the Xilinx device is necessary to have the 30° to 45° angle required for the edge bond dispenser to dispense the edge bond adhesive material. The surrounding component height and distance from the device is validated based on each unique product design layout.

# Edge Bond Removal

Edge bond material can be removed by heating to 170–180°C, and scraping using a stiff probe made of stable organic material such as a non-resinous wood or Teflon. Use a hot air blower on the edge bond area and slowly remove the edge bond adhesive from side to side. Do not use force to remove the edge bond adhesive. Excess adhesive on the PCB can be removed using a chisel-tip soldering iron, with sufficient precautions to limit damage to the PCB surface.

Xilinx has successfully evaluated the application processes used by Flex and Celestica and recommends these contract manufacturers for edge bond assembly of Xilinx packages.

- https://flex.com/
- https://www.celestica.com/

Chapter 11

# Thermal Specifications

Versal™ ACAPs are offered exclusively in thermally efficient flip-chip BGA packages. These flip-chip packages range in pin-count from the smaller 21 × 21 mm SFVB625 to the 52.5 × 52.5 mm VSVA2197. This suite of packages is used to address the various power requirements of the Versal ACAPs. Versal devices are implemented in the 7 nm process technology. Unlike features in an ASIC, the combination of Versal ACAP features used in a user application is not known to the component supplier. Therefore, it remains a challenge for Xilinx to predict the power requirements of a given Versal device when it leaves the factory. Accurate estimates are obtained when the board design takes shape. For this purpose, Xilinx offers and supports a suite of integrated device power analysis tools to help users quickly and accurately estimate their design power requirements. Versal ACAPs are supported similarly to previous products. The uncertainty of design power requirements makes it difficult to apply canned thermal solutions to fit all users. Therefore, Xilinx devices do not come with preset thermal solutions. The operating conditions of your design dictate the appropriate solution.

## Support for Thermal Models

Xilinx offers and supports a suite of integrated device power analysis tools to help you quickly and accurately estimate your design power requirements.

The variability of design power requirements makes it difficult to apply pre-determined thermal solutions to fit all designs. The estimated power of the device using XPE, coupled with the your operating conditions and system constraints, dictate the appropriate solution. You must establish a thermal margin to account for the impact of the following (but not limited to) variations.

- Impact of the thermal sensor accuracy
- Impact of the power variation from one package to another package
- Impact of the manufacturing variation between fans
- Impact of the manufacturing variation between heat-sink fins
- Impact of the package manufacturing variation between heat-sink flatness
- Impact of the manufacturing variation of heat sink TIM contact/thickness

For example, when targeting maximum junction temperature (100°C) minus 8°C you must account for any additional system/environmental errors.

The detailed thermal model is a direct representation of the specified FCBGA package. The model provides geometric details describing the package, specifically in regards to the lid, TIM, die, underfill, substrate, and solder balls or leads. Each specific component in the detailed model has material properties associated. When using this detailed model, several key facts must be considered:

- Two variations of the detailed thermal model are provided: Full detailed thermal model and simplified thermal model.
- The full detailed thermal model provides all the intricate geometries representing the physical package and can be used for mechanical evaluation of the device. However, it should not be used to perform thermal simulations because the detailed geometries create a large meshing size and high-computation time with little to no increase in overall accuracy.
- The simplified detailed model removes certain geometries including substrate trace layers and stiffener ring that do not have a material impact on thermal simulation accuracy and significantly increase computational time. This simplified model provides a much smaller meshing size and less computation time for simulation with less than a 5% difference in simulation accuracy from the full detailed model.
- The correct package top surface contact must be used when modeling the TIM on top of the detailed model because the top surface contact might not be the actual full package size.
- The junction temperature monitor point is at the die center by default. Junction temperature monitor points need to be positioned or added to the location of interest for your design.
- The uniform power defined in the die for the models provided is default power and does not apply to any specific cases. Power setting input is required.

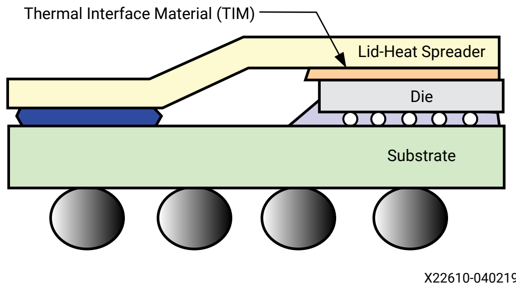
# Thermal Management Strategy

Xilinx relies on a multi-pronged approach to consuming less power and dissipating heat for systems using devices.

## Flip-Chip Packages

Versal™ devices are offered in flip-chip BGA packages, which present a low thermal path. Packages primarily consist of lidless with stiffener ring variations, with the exception of the bare-die packages and lidded packages incorporating a heat spreader with an additional thermal interface material (TIM), as shown in the following figure.

*Figure 38:* **Heat Spreader with Thermal Interface Material**




Materials with high thermal conductivity and consistent process are expected to be used to deliver low thermal resistance to a heat sink, and are included in lidded packages with a heat spreader. An effort to ensure optimized package electrical return paths produces the added benefit of enhanced power and ground plane arrangement in the packages. A boost in copper density on the planes improves the overall thermal conductivity through the laminate. In addition, the extra dense and distributed via fields in the package increase the vertical thermal conductivity.

# System Level Heat Sink Solutions

To complete a comprehensive thermal management strategy, an overall thermal budget that includes custom or OEM heat sink solutions depends on the physical and mechanical constraints of the system. A heat-sink solution, managed by the system-level designer, should be tailored to the design and specific system constraints. This includes understanding the inherent device capabilities for delivering heat to the surface.

By considering the system's physical, mechanical, and environmental constraints, the overall thermal budget is maintained and does not exceed the device's maximum operating temperature. The heat sink is an integral part of the thermal management solution to maintain a safe operating temperature. As a result, the system-level designer must be aware of the following:

- For lidless packages, the nominal stiffener height can be different from the height of the die. Therefore, the heat sink must have an island to contact the die.
- Especially for lidless packages, Run thermal simulations of the system in worst-case environmental conditions using detailed thermal models, which accurately represent the device thermal performance under all boundary conditions.
- Consider the mechanical specifications of the package as well as the selection of the thermal interface between the die and the thermal management solution to ensure the lowest thermal contact resistance.
- The total thermal contact of the thermal interface material is determined based on parameters from the data sheet supplied by the thermal interface manufacturer.
- See the applied pressure recommendation section. Lower pressure runs the risk of poor thermal contact and higher pressure runs the risk of damaging the device; therefore, strict control of pressure is required. The use of a smart-torque tool is suggested when applying a heat sink to control the rate of short-term transient pressure as the thermal interface material (TIM) relaxes. Specifications from the TIM supplier should be taken into consideration.
- Consider all uncertainties in thermal modeling, including manufacturing variations from the thermal solutions (for example, fan airflow tolerance, heat pipe or vapor chamber performance tolerance, variation of the attachment of fins to heat sink base, and surface flatness).

# Thermal Interface Material

When installing heat sinks for Versal devices, a suitable thermal interface material (TIM) must be used. This thermal material significantly aids the transfer of heat from the component to the heat sink.

For lidless and bare-die flip-chip BGAs, the surface of the silicon contacts the heat sink. For lidded flip-chip BGAs, the lid contacts the heat sink. The surface size of the lidless or bare-die flip-chip BGA and lidded flip-chip BGAs are different. Xilinx recommends a different type of thermal material for long-term use with each type of flip-chip BGAs package.

Thermal interface material is needed because even the largest heat sink and fan cannot effectively cool an Versal device unless there is good physical contact between the base of the heat sink and the top of the Versal device. The surfaces of both the heat sink and the Versal device silicon are not absolutely smooth. This surface roughness is observed when examined at a microscopic level. Because surface roughness reduces the effective contact area, attaching a heat sink without a thermal interface material is not sufficient due to inadequate surface contact.

A thermal interface material such as phase-change material, thermal grease, or thermal pads fills these gaps and allows effective transference of heat between the Versal device die and the heat sink.

The selection of the thermal interface material (TIM) between the package and the thermal management solution is critical to ensure the lowest thermal contact resistance. Therefore, the following parameters must be considered.

1. The flatness of the lid and the flatness of the contact surface of the thermal solution.
2. The applied pressure of the thermal solution on the package, which must be within the allowable maximum pressure that can be applied on the package. The use of a smart-torque tool is suggested when applying a thermal solution to control the rate of short-term transient pressure as the TIM material relaxes. Specifications from the TIM supplier should be taken into consideration.
3. The total thermal contact of the thermal interface material. This value is determined based on the parameters in step 1 and step 2, which are published in the data sheet of the TIM supplier.

## Types of TIM

There are many type of TIM available for sale. The most commonly used thermal interface materials are listed.

- Thermal grease
- Thermal pads
- Phase change material
- Thermal paste
- Thermal adhesives
- Thermal tape

## Guidelines for Thermal Interface Materials

Five factors affect the choice, use, and performance of the thermal interface material (TIM) used between the device and the heat sink. Each factor is discussed in this section.

- Thermal conductivity of the material
- Electrical conductivity of the material
- Spreading characteristics of the material
- Long-term stability and reliability of the material
- Ease of application
- Applied pressure from heat sink to the package through the TIM

### Thermal Conductivity of the Material

Thermal conductivity is the quantified ability of any material to transfer heat. The thermal conductivity of the interface material has a significant impact on its thermal performance. The higher the thermal conductivity, the more efficient the material is at transferring heat. Materials that have a lower thermal conductivity are less efficient at transferring heat, causing a higher temperature differential to exist across the interface. To overcome this less efficient heat transfer, a better cooling solution (typically, a more costly solution) must be used to achieve the desired heat dissipation.

### Electrical Conductivity of the Material

Some metal-based TIM compounds are electrically conductive. Ceramic-based compounds are typically not electrically conductive. Manufacturers produce metal-based compounds with low-electrical conductivity, but some of these materials are not completely electrically inert. Metal-based thermal compounds are not hazardous to the Versal ACAP die itself, but other elements on the Versal device or motherboard can be at risk if they become contaminated by the compound. For this reason, Xilinx does not recommend the use of electrically conductive thermal interface material.

### Spreading Characteristics of the Material

The spreading characteristics of the thermal interface material determines its ability, under the pressure of the mounted heat sink, to spread and fill in or eliminate the air gaps between the Versal device and the heat sink. Because air is a very poor thermal conductor, the more completely the interface material fills the gaps, the greater the heat transference.

### Long-Term Stability and Reliability of the Material

The long-term stability and reliability of the thermal interface material is described as the ability to provide a sufficient thermal conductance even after an extended time or extensive. Low-quality compounds can harden or leak out over time (the pump-out effect), leading to overheating or premature failure of the Versal device. High-quality compounds provide a stable and reliable thermal interface material throughout the lifetime of the device. Thermal greases with higher viscosity are typically more resistant to pump out effects on bare-die devices.

### Ease of Application

A spreadable thermal grease requires the surface mount supplier to carefully use the appropriate amount of material. Too much or too little material can cause problems. The thermal pad is a fixed size and is therefore easier to apply in a consistent manner.

### Applied Pressure from Heat Sink to the Package via Thermal Interface Materials

Measure applied pressure using a calibrated pressure sensor on multiple locations between the device and the heat sink assembly as shown in the following figure.

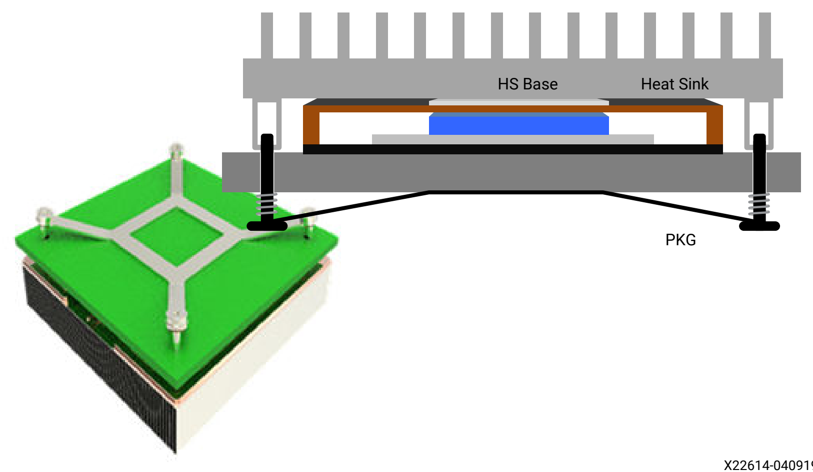
*Figure 39:* **Pressure Sensor**

**RECOMMENDED:** *Xilinx recommends that the applied pressure on the package be in the range of 20 to 50 PSI for optimum performance of the TIM between the package and the heat sink. Thermocouples should not be present between the package and the heat sink, as their presence will degrade the thermal contact and result in incorrect thermal measurements. The best practice is to select the appropriate pressure (in the 20 to 50 PSI range) for the optimum thermal contact performance between the package and the thermal system solution, and the mechanical integrity of the package (with the thermal solution to pass all mechanical stress and vibration qualification tests). The use of a smart-torque tool is suggested when applying a heat sink to control the rate of short-term transient pressure as the TIM material relaxes. Specifications from the TIM supplier should be taken into consideration.*

**TIP:** *These recommendations and specifications are the same for both lidded and lidless devices.*

**RECOMMENDED:** *Xilinx recommends using dynamic mounting around the four corners of the device package. On the PCB, use a bracket clip as part of the heat sink attachment to provide mechanical package support. See the following figure.*

*Figure 40:* **Dynamic Mounting and Bracket Clips on Heat Sink Attachment**




# Heat Sink Removal

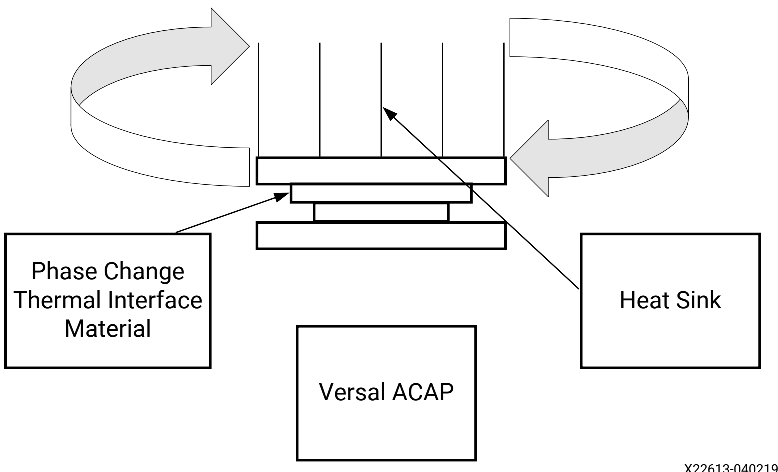
When removing or reworking heat sinks, the phase-change material residue must be removed from the surface of the die. Laird Technologies, Inc. provides the following guidance for complete removal of the phase-change material from the component.

### Instructions for Removal of Phase-change Material

1. Separate the Components

At room temperature, if possible, use a back and forth twisting motion to break the bond between the phase-change thermal interface material and mated components (i.e., heat sink and Versal device). See the following figure.

*Figure 41:* **Breaking the Bond between Thermal Interface Material and Mated Components**




For smaller components (typically 15 mm x 15 mm or less), the bond usually breaks free easily at room temperature. For larger components, in situations where minimal movement is available, or if using fragile components, heat the component (preferred) or heat sink to about 40°C–60°C before removal.

The guideline is 40°C–60°C, however, you might find that for your application, heating to 35°C is adequate. You might prefer to heat to 70°C which makes the phase-change thermal interface material very soft and the components can be easily separated.

2. Scrape Away Thick Residue

   For a faster clean-up once components are separated, scrape away any large residual material amounts with a plastic spatula or a wooden tongue depressor. A clean dry rag can be used to wipe away excess material.

3. Clean Remaining Residue with Solvent

   Using a clean cloth/wipe, wet it with your choice of solvent (see the following list) and wipe away any remaining residue.

   - Toluene (easiest)
   - Acetone (very good)
   - Isoparaffinic hydrocarbon: Isopar, Soltrol (trade names) (very good)
   - Isopropyl alcohol (OK)

4. Working with Laird Material

Safe handling, disposal, and first-aid measures for working with phase-change material are included in the Laird Technologies material safety data sheet (MSDS). Read the MSDS before using or handling. See the Laird Technologies, Inc. website.

# Measurement Debug

When performing in-system thermal testing, to ensure accurate data and not incur damage to the device, do not place a thermocouple in between the device and the heat sink. On the extreme side, it might cause additional mechanical and/or thermal stress to the device, leading to damage. Even if damage does not occur, it often leads to a thicker and or uneven thermal interface material thickness, leading to a thermal performance difference from a system without a thermocouple. To obtain the device temperature, use the System Monitor as a non-invasive means to get accurate device measurements while debugging the system.

Chapter 13

# Heat Sink Guidelines for Bare-die VB Packages

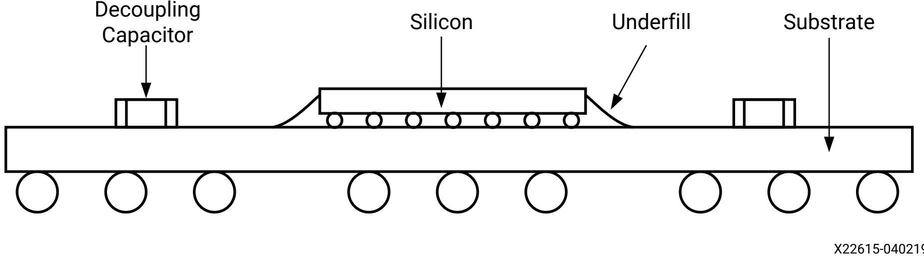
## Heat Sink Attachments

Heat sinks can be attached to the package in multiple ways. For heat to dissipate effectively, the advantages and disadvantages of each heat sink attachment method must be considered. Factors influencing the selection of the heat sink attachment method include the package type, contact area of the heat source, and the heat sink type.

### Silicon and Decoupling Capacitors Height Consideration

When designing heat sink attachments for bare-die flip-chip BGA packages, the height of the die above the substrate and also the height of decoupling capacitors must be considered (see the following figure). This is to prevent electrical shorting between the heat sink (metal) and the decoupling capacitors.

*Figure 42:* **Cross Section of Bare-die Flip-chip BGA**



# Types of Heat Sink Attachments

There are six main methods for heat sink attachment. The following table lists their advantages and disadvantages.

- Thermal tape
- Thermally conductive adhesive or glue
- Wire form Z-clips
- Plastic clip-ons
- Threaded stand-offs (PEMs) and compression springs
- Push-pins and compression springs

*Table 27:* **Heat Sink Attachment Methods**

| Attachment Method | Advantages | Disadvantages |
|---|---|---|
| Thermal tape | • Generally it is easy to attach and is inexpensive<br>• Lowest cost approach for aluminum heat sink attachment<br>• No additional space required on the PCB | • The surfaces of the heat sink and the chip must be very clean to allow the tape to bond correctly<br>• Because of the small contact area, the tape might not provide sufficient bond strength<br>• Tape is a moderate to low thermal conductor that could affect the thermal performance |
| Thermally conductive adhesive or glue | • Outstanding mechanical adhesion<br>• Somewhat inexpensive, costs a little more than tape<br>• No additional space required on the PCB | • Adhesive application process is challenging and it is difficult to control the amount of adhesive to use.<br>• Difficult to rework<br>• Because of the small contact area, the adhesive might not provide sufficient bond strength |
| Wire form Z-clips | • It provides a strong and secure mechanical attachment. In environments that require shock and vibration testing, this type of strong mechanical attachment is necessary.<br>• Easy to apply and remove. Does not cause the semiconductors to be destroyed (epoxy and occasionally tape can destroy the device).<br>• It applies a preload onto the thermal interface material (TIM). Preloads actually improve thermal performance. | • Requires additional space on the PCB for anchor locations |
| Plastic clip-ons | • Suitable for designs where space on the PCB is limited<br>• Easy to rework by allowing heat sinks to be easily removed and reapplied without damaging the PCB board<br>• Can provide a strong enough mechanical attachment to pass shock and vibration test | • Needs a keep out area around the silicon devices to use the clip<br>• Caution is required when installing or removing clip-ons because localized stress can damage the solder balls or chip substrate |

*Table 27:* **Heat Sink Attachment Methods** *(cont'd)*

| Attachment Method | Advantages | Disadvantages |
|---|---|---|
| Threaded stand-offs (PEMs) and compression springs | • Provides stable attachments to heat source and transfers load to the PCB, backing plate, or chassis<br>• Suitable for high mass heat sinks<br>• Allows for tight control over mounting force and load placed on chip and solder balls | • Holes are required in the PCB taking valuable space that can be used for trace lines<br>• Tends to be expensive, especially because holes need to be drilled or predrilled onto the PCB board to use stand-offs |
| Push-pins and compression springs | • Provides a stable attachment to a heat source and transfers load to the PCB<br>• Allows for tight control over mounting force and load placed on chip and solder balls | • Requires additional space on the PCB for push-pin locations |

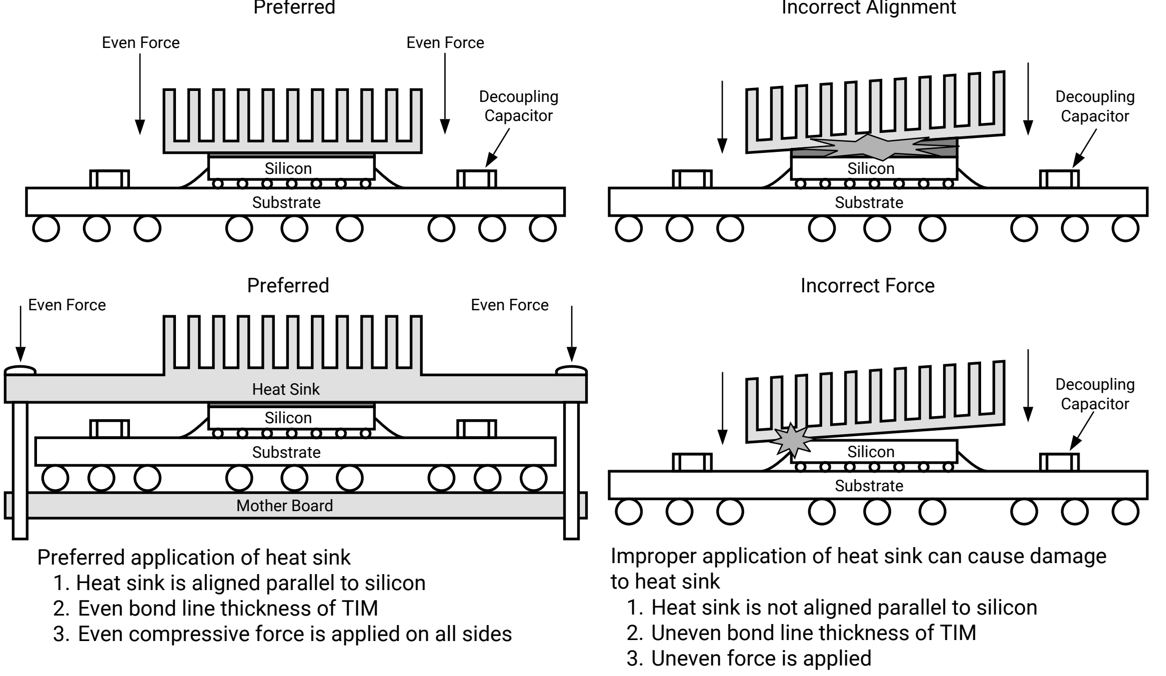
# Heat Sink Attachment Process Considerations

After the component is placed onto the PCBs, when attaching a heat sink to the bare-die package, the factors in the following table must be carefully considered (as shown in the following figure).

*Table 28:* **Heat Sink Attachment Considerations**

| Consideration(s) | Effect(s) | Recommendation(s) |
|---|---|---|
| In a heat sink attach process, what factors can cause damage to the exposed die and passive capacitors? | • Uneven heat sink placement<br>• Uneven TIM thickness<br>• Uneven force applied when placing heat sink placement | • Even heat sink placement<br>• Even TIM thickness<br>• Even force applied when placing heat sink placement |
| Does the heat sink tilt or tip the post attachment? | • Uneven heat sink placement will damage the silicon and can cause field failures | • Careful handling not to contact the heat sink with the post attachment<br>• Use a fixture to hold the heat sink in place with post attachment until it is glued to the silicon |

*Figure 43:* **Recommended Application of Heat Sink**




# Standard Heat Sink Attach Process with Thermal Conductive Adhesive

Prior to attaching the heat sink, theVersal device needs be surface mounted on the motherboard.

1. Place the motherboard into a jig or a fixture to hold the motherboard steady to prevent any movement during the heat sink attachment process.
2. Thermoset material (electrically non-conductive) is applied over the backside surface of silicon in a pattern using automated dispensing equipment. Automated dispensers are often used to provide a stable process speed at a relatively low cost. The optimum dispensing pattern needs to be determined by the SMT supplier.

   ***Note*:** Minimal volume coverage of the backside of the silicon can result in non-optimum heat transfer
3. The heat sink is placed on the backside of the silicon with a pick and place machine. A uniform pressure is applied over the heat sink to the backside of the silicon. As the heat sink is placed, the adhesive spreads to cover the backside silicon. A force transducer is normally used to measure and limit the placement force.
4. The epoxy is cured with heat at a defined time.

   ***Note*:** The epoxy curing temperature and time is based on manufacturer's specifications.

## Standard Heat Sink Attach Process with Thermal Adhesive Tape

Prior to attaching the heat sink, the Versal device needs be surface mounted on the motherboard.

1. Place the motherboard into a jig or a fixture to hold the motherboard steady to prevent any movement during the heat sink attachment process.
2. Thermal adhesive tape cut to the size of the heat sink is applied on the underside of the heat sink at a modest angle with the use of a squeegee rubber roller. Apply pressure to help reduce the possibility of air entrapment under the tape during application.
3. The heat sink is placed on the backside of the silicon with a pick and place machine. A uniform pressure is applied over the heat sink to the backside of the silicon. As the heat sink is placed, the thermal adhesive tape is glued to the backside of the silicon. A force transducer is normally used to measure and limit the placement force.
4. A uniform and constant pressure is applied uniformly over the heat sink and held for a defined time.

   ***Note***: The thermal adhesive tape hold time is based on manufacturer's specifications.

## Push-Pin and Shoulder Screw Heat Sink Attachment Process with Phase Change Material (PCM) Application

Prior to attaching the heat sink, the Versal device needs be surface mounted on the motherboard.

1. Place the motherboard into a jig or a fixture to hold the motherboard steady to prevent any movement during the heat sink attachment process.

   ***Note***: The jig or fixture needs to account for the push pin depth of the heat sink.

2. PCM tape, cut to the size of the heat sink, is applied on the underside of the heat sink at a modest angle with the use of a squeegee rubber roller. Apply pressure to help reduce the possibility of air entrapment under the tape during application.
3. Using the push-pin tool, heat sinks are applied over the packages ensuring a pin locking action with the PCB holes. The compression load from springs applies the appropriate mounting pressure required for proper thermal interface material performance.

   ***Note***: Heat sinks must not tilt during installation. This process cannot be automated due to the mechanical locking action which requires manual handling. The PCB drill hole tolerances need to be close enough to eliminate any issues concerning the heat sink attachment.

Chapter 14

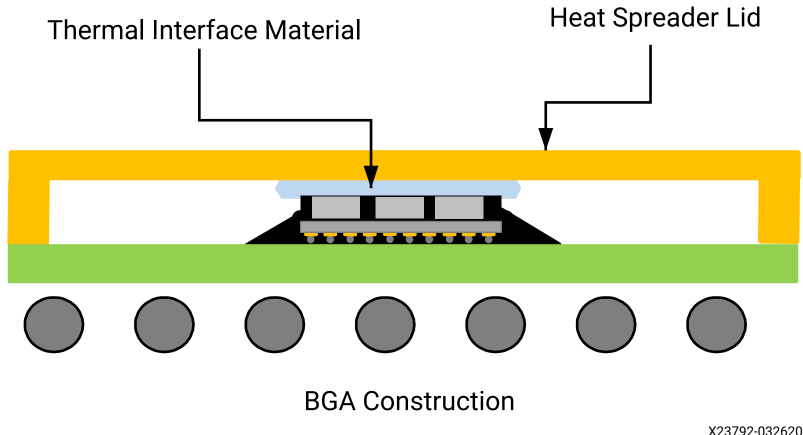
# Mechanical and Thermal Design Guidelines for Lidless Flip-chip Packages

This section discusses the challenges of thermal management including reducing device thermal resistance and optimal power dissipation without an increase in junction temperature. The lidless Versal ACAP packages target the largest devices while allowing for cooler operation temperatures (up to 10°C) with the same power dissipation. Precise mechanical design and component thermal management is vital for device and system performance. This document presents the unique thermal and mechanical design requirements for lidless devices.

## Lidless Flip-Chip Packages

The Xilinx flip-chip BGA packages exhibit a low-resistance thermal path that adequately cools devices. These packages incorporate a heat spreader lid with additional thermal interface material as shown in the following figure.

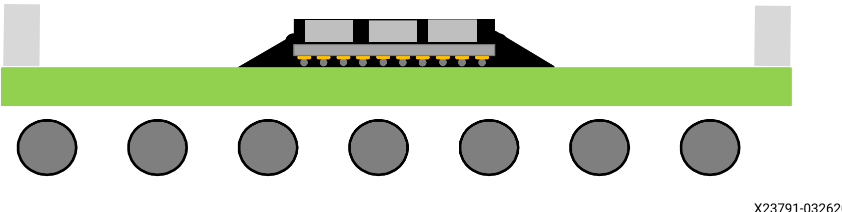
*Figure 44:* **Flip-Chip BGA Construction with Heat Spreader and Thermal Interface Material**



Materials with high thermal conductivity and consistent process applications deliver low thermal resistance up to the heat spreader. A parallel effort to ensure optimized package electrical return paths produces an enhanced power and ground plane arrangement in the package. A boost in copper density on the planes improves the overall thermal conductivity through the laminate. The extra density and distribution via fields in the package also increases the vertical thermal conductivity.

The lidless packages (see the following figure) offer the same package substrate design with electrical and board thermal conductivity similar to the flip-chip BGA packages. However, removing the lid (heat spreader) and the thermal interface material allows for direct contact between the external heat sink and the die. This further reduces the thermal resistance and exhibits improved thermal behaviors. The use of custom passive or active heat-sink designs is facilitated by incorporating two-phase (heat pipe, vapor chamber, or even liquid) cooling methods directly adjacent to the source of the dissipated heat on the die, which allows for a more efficient means of removing the heat from the device. Consequently, the device can operate at higher ambient temperatures while in area-constrained surroundings resulting in operational power advantages.

*Figure 45:* **Lidless Flip-Chip BGA Construction**




A unique feature of lidless packages is the addition of a stiffener ring around the periphery of the package substrate, providing additional package rigidity and helping to improve the overall package coplanarity (flatness). It also serves as a guide for the heat sink solution applied to the device. For examples, see the VSVD1760 Package—VC1802, VC1902, and VM1802 or VSVA2197 Package—VC1802, VC1902, and VM1802. In the lidless packages, capacitors can be placed in the area surrounding the die. Contact with electrically conductive materials must be avoided because the die-side capacitors, which are only slightly shorter than the die height, could be electrically conductive. Any thermal and mechanical solution higher than the die must not interfere with the package stiffener. Therefore, the thermal solution must have an island, see System Level Heat Sink Solutions. For further guidelines on mechanical and thermal designs of lidless packages, refer to *Mechanical and Thermal Design Guidelines for Lidless Flip-Chip Packages* (XAPP1301).

# Additional Resources and Legal Notices

## Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

## Documentation Navigator and Design Hubs

Xilinx® Documentation Navigator (DocNav) provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open DocNav:

- From the Vivado® IDE, select **Help → Documentation and Tutorials**.
- On Windows, select **Start → All Programs → Xilinx Design Tools → DocNav**.
- At the Linux command prompt, enter `docnav`.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In DocNav, click the **Design Hubs View** tab.
- On the Xilinx website, see the Design Hubs page.

***Note*:** For more information on DocNav, see the Documentation Navigator page on the Xilinx website.

# References

These documents provide supplemental material useful with this guide:

1. Versal ACAP data sheets:
   - *Versal Architecture and Product Data Sheet: Overview* (DS950)
   - *Versal Prime Series Data Sheet: DC and AC Switching Characteristics* (DS956)
   - *Versal AI Core Series Data Sheet: DC and AC Switching Characteristics* (DS957)
2. *Versal ACAP SelectIO Resources Architecture Manual* (AM010)

### Heat Management and Contact Information

The following websites contain additional information on heat management and contact information.

- Wakefield
- Boyd/Aavid
- Advanced Thermal Solutions
- Radian Thermal Products
- Thermo Cool
- CTS

### Interface Material Sources

- Henkel
- AOS Thermal Compound
- Parker Chomerics
- Kester

### CDF Tools

Refer to the following websites for CFD tools Xilinx supports with thermal models.

- Mentor Flotherm
- ANSYS Icepak

### Thermal Modeling References

The following papers are referenced for more information on thermal modeling.

- Lemczyk, T.F., Mack, B., Culham, J.R. and Yovanovich, M.M., 1992, "Printed Circuit Board Trace Thermal Analysis and Effective Conductivity", ASME J. Electronic Packaging, Vol. 114, pp. 413 - 419.50.
- Refai-Ahmed, G. and Karimanal, K., 2003, "Validation of Compact Conduction Models of BGA Under Realistic Boundary," J. of Components and Packaging Technology, Vol. 26, No. 3, pp. 610-615.
- Sansoucy, E, Refai-Ahmed, G., and Karimanal, K., 2002, "Thermal Characterization of TBGA Package for an integration in Board Level Analysis," Eighth Intersociety on Thermal Conference Phenomena in Electronic Systems, San Diego., USA.
- Karimanal, K. and Refai-Ahmed, G., 2002, "Validation of Compact Conduction Models of BGA Under Realistic Boundary Conditions," Eighth Intersociety on Thermal Conference Phenomena in Electronic Systems, San Diego, USA.
- Karminal, K. and Refai-Ahmed, G., 2001, "Compact conduction Model (CCM) of Microelectronic Packages- A BGA Validation Study," APACK Conference on Advances in Packaging, Singapore.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