Versal Prime Series Data Sheet: DC and AC Switching Characteristics

DS956 (v1.2) July 1, 2021 **Product Specification**

Summary

The Xilinx® Versal™ Prime series devices are available in -3 (highest performance), -2, -1 speed grades. The -3 devices can operate at a V_{CCINT} voltage of 0.88V (H), the -2 devices can operate at a V_{CCINT} voltage of 0.88V (H), 0.80V (M), or 0.70V (L), and the -1 devices can operate at a V_{CCINT} voltage of 0.80V (M) or 0.70V (L). Primary supply operating voltages typically scale with V_{CCINT}, except for supported overdrive of the V_{CC_PMC}, V_{CC_PSFP}, and V_{CC_PSLP} at 0.88V (H) when V_{CCINT} and other primary supplies operate at 0.70V (L). Similar to speed grades, a higher operating voltage typically has higher performance specifications. All devices are screened for standard (S) or low (L) maximum static power. See *Versal Architecture and Product Data Sheet: Overview* (DS950) for available device ordering options.

DC and AC characteristics are specified in extended (E) and industrial (I) temperature ranges. Except the operating temperature range or unless otherwise noted, all the DC and AC electrical parameters are the same for a particular speed grade and operating voltage (that is, the timing characteristics of a -1 speed grade extended (E) temperature range device operating at a V_{CCINT} voltage of 0.80V (M) are the same as for a -1 speed grade industrial (I) temperature range device operating at a V_{CCINT} voltage of 0.80V (M)). However, only selected speed grades, operating voltages, maximum static power screens, and/or devices are available in each temperature range.

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications.

This data sheet, part of an overall set of documentation on the Versal ACAPs, is available on the Xilinx website at https://www.xilinx.com/versal.

DC Characteristics

Absolute Maximum Ratings

Table 1: **Absolute Maximum Ratings—Power, Voltages, and Current**

Symbol	Description[1]	Min	Max	Units
V_{CCAUX}	Programmable logic auxiliary power supply	–0.500	1.650	V
V_{CCAUX_PMC}	Platform management controller (PMC) auxiliary power supply voltage	–0.500	1.650	V
V_{CCAUX_SMON}[2]	PMC system monitor power supply relative to GND_SMON	–0.500	1.650	V

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Table 1: **Absolute Maximum Ratings—Power, Voltages, and Current** *(cont'd)*

Symbol	Description[1]	Min	Max	Units
V_{CC_BATT}	Battery power supply	–0.500	1.650	V
V_{CC_FUSE}	eFUSE programming power supply	–0.500	2.000	V
V_{CCINT}	Programmable logic primary power supply	–0.500	0.970	V
V_{CC_IO}[3]	XPIO power supply	–0.500	0.970	V
V_{CCO}[4]	XPIO bank 7## output driver power supply Where the bank number is the three-digit bank number beginning with 7	–0.500	1.650	V
	HDIO bank 3## and bank 4## output driver power supply Where the bank number is the three-digit bank number beginning with 3 or 4	–0.500	3.465	V
	PSIO bank 5## power supplies Where the bank number is the three-digit bank number beginning with 5	–0.500	3.465	V
V_{CC_PMC}	PMC primary power supply	–0.500	0.970	V
V_{CC_PSFP}	PS full-power domain power supply	–0.500	0.970	V
V_{CC_PSLP}	PS low-power domain power supply	–0.500	0.970	V
V_{CC_RAM}	PL RAM and clocking network power supply	–0.500	0.970	V
V_{CC_SOC}[3]	Network on Chip (NoC) and DDR memory controller power supply	–0.500	0.970	V
V_{IN}[4, 5]	I/O input voltage for PSIO, HDIO, and XPIO banks	–0.550	V_{CCO} + 0.550	V
GTY/GTYP Transceivers				
V_{GTY_AVCC}	GTY/GTYP transceiver primary analog power supply[6]	–0.500	0.970	V
$V_{GTY\_AVCCAUX}$	GTY/GTYP transceiver auxiliary analog (PLL) power supply[6]	–0.500	1.650	V
V_{GTY_AVTT}	GTY/GTYP transceiver termination power supply[6]	–0.500	1.320	V
$V_{GTY\_AVTTRCAL}$	GTY/GTYP transceiver analog resistor calibration power supply[6]	–0.500	1.320	V
$V_{GTY\_REFCLK\_DC}$	Transceiver reference clock absolute input DC voltage	–0.500	1.300	V
$V_{GTY\_REFCLK\_AC}$	Transceiver reference clock absolute input AC voltage[7]	–1.000	1.500	V
V_{IN}	Receiver (RXP/RXN) and transmitter (TXP/TXN) absolute input voltage	–0.500	1.200	V
I_{DCIN_FLOAT}	DC input current for receiver input pins DC coupled RX termination = floating[8]	–	10	mA
$I_{DCIN\_GTY\_AVTT}$	DC input current for receiver input pins DC coupled RX termination = V_{GTY_AVTT}	–	10	mA
I_{DCIN_GND}	DC input current for receiver input pins DC coupled RX termination = GND[9]	–	0	mA
I_{DCIN_PROG}	DC input current for receiver input pins DC coupled RX termination = programmable[10]	–	0	mA
I_{DCOUT_FLOAT}	DC output current for transmitter pins DC coupled RX termination = floating	–	6	mA
$I_{DCOUT\_GTY\_AVTT}$	DC output current for transmitter pins DC coupled RX termination = V_{GTY_AVTT}	–	6	mA
Other Ratings				
I_{DC}	Available output current at the pad	–20	20	mA
I_{RMS}	Available RMS output current at the pad	–20	20	mA

Table 1: **Absolute Maximum Ratings—Power, Voltages, and Current** *(cont'd)*

Symbol	Description[1]	Min	Max	Units
$I_{DCIN-FLOAT}$	DC input current for receiver input pins DC coupled RX termination = floating[11]	–	10	mA

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. V_{CCAUX_SMON} must be connected to V_{CCAUX_PMC}. See *Versal ACAP System Monitor Architecture Manual* (AM006) for V_{CCAUX_SMON} information and filter considerations.
3. V_{CC_IO} must be connected to V_{CC_SOC}.
4. When operating outside of the recommended operating conditions, refer to Table 6 and Table 7 for maximum overshoot and undershoot specifications.
5. The lower absolute voltage specification always applies.
6. For more information on supported GTY/GTYP transceiver terminations see the *Versal ACAP GTY and GTYP Transceivers Architecture Manual* (AM002).
7. GTY_REFCLK AC signal operates in the reference clock frequency range. See GTY and GTYP Transceiver Reference Clock Switching Characteristics.
8. AC coupled operation is not supported for RX termination = floating.
9. For GTY/GTYP transceivers, DC coupled operation is not supported for RX termination = GND.
10. DC coupled operation is not supported for RX termination = programmable.
11. AC coupled operation is not supported for RX termination = floating.

Table 2: **Absolute Maximum Ratings—Temperature**

Symbol	Description[1]	Min	Max	Units
T_{STG}	Storage temperature (ambient, unpowered)	–55	125	°C
T_{SOL}[2]	Maximum dry rework soldering temperature	–	260	°C
	Maximum reflow soldering temperature for packages with fewer than 900 balls	–	250	°C
	Maximum reflow soldering temperature for packages with 900, or more, balls	–	245	°C
	Maximum reflow soldering temperature for lidless packages with stiffener ring	–	245	°C
	Maximum reflow soldering temperature for packages with leaded balls	–	235	°C
T_j	Maximum junction temperature	–	125	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. For soldering guidelines and thermal considerations, see the *Versal ACAP Packaging and Pinouts Architecture Manual* (AM013).

Recommended Operating Conditions

Table 3: **Recommended Operating Conditions**

Symbol	Description[1, 2, 3]	Min	Typ	Max	Units
V_{CCAUX}	Auxiliary power supply	1.455	1.500	1.545	V
V_{CCAUX_PMC}	PMC auxiliary power supply voltage	1.455	1.500	1.545	V
V_{CCAUX_SMON}[4]	PMC system monitor power supply relative to GND_SMON	1.455	1.500	1.545	V
V_{CC_BATT}[5]	Battery power supply to the battery-backed RAM and battery-backed real-time clock (RTC)	1.200	–	1.500	V
V_{CC_FUSE}[6]	eFUSE programming power supply	1.745	1.800	1.854	V

Table 3: **Recommended Operating Conditions** *(cont'd)*

Symbol	Description[1, 2, 3]	Min	Typ	Max	Units
V_{CCINT}	PL primary power supply, low (L) voltage	0.676	0.700	0.724	V
	PL primary power supply, mid (M) voltage	0.775	0.800	0.825	V
	PL primary power supply, high (H) voltage	0.854	0.880	0.906	V
V_{CC_IO}[7]	XPIO power supply, low (L) and mid (M) voltage	0.775	0.800	0.825	V
	XPIO power supply, high (H) voltage	0.854	0.880	0.906	V
V_{CCO}[8]	XPIO bank 7## output driver power supply Includes V_{CCO} of 1.0V, 1.1V, 1.2V, 1.35V, 1.5V at ±5%	0.950	–	1.575	V
	HDIO bank 3## and bank 4## output driver power supply Includes V_{CCO} of 1.8V, 2.5V at ±5%, and 3.3V at +3/–5%	1.710	–	3.400	V
	PSIO bank 5## power supplies Includes V_{CCO} of 1.8V, 2.5V at ±5%, and 3.3V at +3/–5%	1.710	–	3.400	V
V_{CC_PMC}[9]	PMC primary power supply, low (L) voltage	0.676	0.700	0.724	V
	PMC primary power supply, mid (M) voltage	0.775	0.800	0.825	V
	PMC primary power supply, high (H) voltage	0.854	0.880	0.906	V
	PMC primary power supply, overdrive voltage for higher PMC performance in -1LSI and -1LLI devices	0.854	0.880	0.906	V
V_{CC_PSFP}	PS full-power domain power supply, low (L) voltage	0.676	0.700	0.724	V
	PS full-power domain power supply, mid (M) voltage	0.775	0.800	0.825	V
	PS full-power domain power supply, high (H) voltage	0.854	0.880	0.906	V
	PS full-power domain power supply, overdrive voltage for higher PS performance in -1LSI and -1LLI devices	0.854	0.880	0.906	V
V_{CC_PSLP}	PS low-power domain power supply, low (L) voltage	0.676	0.700	0.724	V
	PS low-power domain power supply, mid (M) voltage	0.775	0.800	0.825	V
	PS low-power domain power supply, high (H) voltage	0.854	0.880	0.906	V
	PS low-power domain power supply, overdrive voltage for higher PS performance in -1LSI and -1LLI devices	0.854	0.880	0.906	V
V_{CC_RAM}	PL RAM and clocking network power supply, low (L) and mid (M) voltage	0.775	0.800	0.825	V
	PL RAM and clocking network power supply, high (H) voltage	0.854	0.880	0.906	V
V_{CC_SOC}[7]	Network on Chip (NoC) and DDR memory controller power supply, low (L) and mid (M) voltage	0.775	0.800	0.825	V
	NoC and DDR memory controller power supply, high (H) voltage	0.854	0.880	0.906	V
V_{GTY_AVCC}[10]	GTY/GTYP transceiver primary analog power supply	0.854	0.880	0.906	V
$V_{GTY\_AVCCAUX}$[10]	GTY/GTYP transceiver auxiliary analog (PLL) power supply	1.455	1.500	1.545	V
V_{GTY_AVTT}[10]	GTY/GTYP transceiver termination power supply	1.164	1.200	1.236	V
$V_{GTY\_AVTTRCAL}$[10]	GTY/GTYP transceiver analog resistor calibration power supply	1.164	1.200	1.236	V
V_{IN}[11,12]	I/O input voltage for PSIO, HDIO, and XPIO banks	–0.200	–	V_{CCO} + 0.200	V
I_{IN}[13]	Maximum current through any PL, PMC, or PS pin in a powered or unpowered bank when forward biasing the clamp diode	–	–	10	mA

Table 3: **Recommended Operating Conditions** *(cont'd)*

Symbol	Description[1, 2, 3]	Min	Typ	Max	Units
T_j[14]	Junction temperature operating range for extended (E) temperature devices[15]	0	–	100	°C
	Junction temperature operating range for industrial (I) temperature devices[15]	–40	–	100	°C
	Junction temperature operating range for eFUSE programming	–40	–	125	°C

Notes:

1. All voltages are relative to GND and in relation to the BGA package ball.
2. For the design of the power distribution system consult the *Versal ACAP PCB Design User Guide* (UG863) and Xilinx Power Estimator (XPE) spreadsheet tool (download at www.xilinx.com/power).
3. Each voltage listed requires decoupling as described in the *Versal ACAP PCB Design User Guide* (UG863). Refer to the Xilinx Power Estimator (XPE) spreadsheet tool (download at www.xilinx.com/power) for design specific decoupling recommendations.
4. V_{CCAUX_SMON} must be connected to V_{CCAUX_PMC}. See *Versal ACAP System Monitor Architecture Manual* (AM006) for V_{CCAUX_SMON} information and filter considerations.
5. When the battery-backed RAM and the real-time clock are not used, connect to GND.
6. V_{CC_FUSE} must be within the recommended operating conditions during eFUSE programming. When V_{CC_FUSE} is not used, connect to GND.
7. V_{CC_IO} must be connected to V_{CC_SOC}.
8. For XPIO and HDIO operation, see the *Versal ACAP SelectIO Resources Architecture Manual* (AM010). For PSIO operation, see the *Versal ACAP Technical Reference Manual* (AM011)
9. The physical unclonable function (PUF) is only supported when using a nominal V_{CC_PMC} of 0.70V. Refer to the *Versal ACAP Security Manual* (UG1508) in the Design Security Lounge for detailed information on PUF usage.
10. Each voltage listed requires filtering as described in the *Versal ACAP GTY and GTYP Transceivers Architecture Manual* (AM002). The noise beyond the recommended operating conditions at the power pins must not exceed 10 mVpp over the band from 10 kHz to 80 MHz.
11. The lower absolute voltage specification always applies.
12. In XPIO banks, V_{IN} overshoot above V_{CCO} and undershoot below GND can reduce the performance of V_{REF}-based receivers within the same nibble.
13. A total of 200 mA per bank should not be exceeded.
14. Junction temperature specification is in relation to the absolute value reported by SYSMON.
15. Devices labeled with the -2E speed/temperature grade and all industrial (I) temperature grade devices can operate for a limited time at a junction temperature between 100°C and 110°C based on the temperature read from the SYSMON. Timing parameters adhere to the same speed file at up to 110°C as they do at up to 100°C. Operation up to T_j = 110°C is limited to 3% of the device lifetime and can occur sequentially or at regular intervals as long as the total time does not exceed 3% of the device lifetime. For more information on excursion temperature see *Extending the Thermal Solution by Utilizing Excursion Temperatures* (WP517).

Available Speed Grades and Operating Voltages

The following table describes the speed grades per device and operating supply voltages for the PMC, PS low power, PS full power, and PL domains. For more information on selecting devices and speed grades, see the *Versal Architecture and Product Data Sheet: Overview* (DS950).

Table 4: **Available Speed Grades and Operating Voltages**

Speed Grade	Mode[1]	V_{CCINT}	V_{CC_PSLP}	V_{CC_PSFP}	V_{CC_PMC}[2]	V_{CC_SOC} and V_{CC_IO}	V_{CC_RAM}	Units
-3HSE	Standard	0.88	0.88	0.88	0.88	0.88	0.88	V
-2HSI	Standard	0.88	0.88	0.88	0.88	0.88	0.88	V
-2MSE	Standard	0.80	0.80	0.80	0.80	0.80	0.80	V
-2MSI	Standard	0.80	0.80	0.80	0.80	0.80	0.80	V
-2MLE	Standard	0.80	0.80	0.80	0.80	0.80	0.80	V
-2MLI	Standard	0.80	0.80	0.80	0.80	0.80	0.80	V
-2LSE	Standard	0.70	0.70	0.70	0.70	0.80	0.80	V
-2LLE	Standard	0.70	0.70	0.70	0.70	0.80	0.80	V
-1MSI	Standard	0.80	0.80	0.80	0.80	0.80	0.80	V
-1MLI	Standard	0.80	0.80	0.80	0.80	0.80	0.80	V
-1MSE	Standard	0.80	0.80	0.80	0.80	0.80	0.80	V
-1LSI	Standard	0.70	0.70	0.70	0.70	0.80	0.80	V
	Overdrive	0.70	0.88	0.88	0.88	0.80	0.80	V
-1LLI	Standard	0.70	0.70	0.70	0.70	0.80	0.80	V
	Overdrive	0.70	0.88	0.88	0.88	0.80	0.80	V
-1LSE	Standard	0.70	0.70	0.70	0.70	0.80	0.80	V

Notes:

1. -1LSI and -1LLI devices allow dual-voltage operation of the PMC and PS supplies in overdrive mode (0.88V) or standard drive mode (0.70V).
2. The physical unclonable function (PUF) is only supported when using a nominal V_{CC_PMC} of 0.70V. Refer to the *Versal ACAP Security Manual* (UG1508) in the Design Security Lounge for detailed information on PUF usage.

DC Characteristics Over Recommended Operating Conditions

Table 5: **DC Characteristics Over Recommended Operating Conditions**

Symbol	Description	Min	Typ[1]	Max	Units
I_{RPU}	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO} = 3.3V	60	–	200	µA
	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO} = 2.5V	50	–	169	µA
	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO} = 1.8V	29	–	120	µA
	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO} = 1.5V	30	–	120	µA
	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO} = 1.2V	10	–	100	µA
I_{RPD}	Pad pull-down (when selected) at V_{IN} = 3.3V	60	–	200	µA
	Pad pull-down (when selected) at V_{IN} = 1.8V	29	–	120	µA
I_{CC_BATT}[2, 3]	Battery supply current at V_{CC_BATT} = 1.50V, RTC enabled	–	–	3500	nA
	Battery supply current at V_{CC_BATT} = 1.50V, RTC disabled	–	–	300	nA
	Battery supply current at V_{CC_BATT} = 1.20V, RTC disabled	–	–	150	nA

Table 5: **DC Characteristics Over Recommended Operating Conditions** *(cont'd)*

Symbol	Description	Min	Typ[1]	Max	Units
I_{CC_FUSE}	V_{CC_FUSE} supply current during eFUSE programming	–	–	165	mA
Calibrated programmable on-die termination (DCI) in XPIO banks[4] (measured per JEDEC specification)					
R[6]	Thevenin equivalent resistance of programmable input termination where x = target impedance of 48, 60, 120, or 240	–20%[5]	ODT = RTT_x	+20%[5]	Ω
Uncalibrated programmable on-die termination in HDIO banks (measured per JEDEC specification)					
R[6]	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where ODT = RTT_48	–50%	48	+50%	Ω
Differential termination	Programmable differential termination (TERM_100) for XPIO banks	–35%	100	+35%	Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. Maximum value specified for worst case process at 25°C.
3. Battery-backed RAM (BBRAM) is always enabled and included in I_{CC_BATT}.
4. VR resistor tolerance is (240Ω ±1%)
5. The tolerance limits are specified after calibration with stable voltage and temperature.
6. On-die input termination resistance, for more information see the *Versal ACAP SelectIO Resources Architecture Manual* (AM010).

V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot

Table 6: **V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for HDIO and PSIO Banks**

AC Voltage Overshoot[1]	% of UI[2] at –40°C to 100°C	AC Voltage Undershoot[1]	% of UI[2] at –40°C to 100°C
V_{CCO} + 0.20	100%	–0.20	100%
V_{CCO} + 0.25	100%	–0.25	75%
V_{CCO} + 0.30	75%	–0.30	75%
V_{CCO} + 0.35	75%	–0.35	75%
V_{CCO} + 0.40	75%	–0.40	60%
V_{CCO} + 0.45	50%	–0.45	30%
V_{CCO} + 0.50	30%	–0.50	0%
V_{CCO} + 0.55	20%	–0.55	0%
V_{CCO} + 0.60	20%	–0.60	0%
V_{CCO} + 0.65	10%	–0.65	0%
V_{CCO} + 0.70	10%	–0.70	0%
V_{CCO} + 0.75	10%	–0.75	0%
V_{CCO} + 0.80	10%	–0.80	0%
V_{CCO} + 0.85	8%	–0.85	0%
V_{CCO} + 0.90	6%	–0.90	0%
V_{CCO} + 0.95	2%	–0.95	0%

Notes:

1. A total of 200 mA per bank should not be exceeded.
2. For UI smaller than 20 µs.

Table 7: **V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for XPIO Banks**

AC Voltage Overshoot[1]	% of UI[2] at –40°C to 100°C	AC Voltage Undershoot[1]	% of UI[2] at –40°C to 100°C
V_{CCO} + 0.20	100%	–0.20	100%
V_{CCO} + 0.25	100%	–0.25	100%
V_{CCO} + 0.30	100%	–0.30	10%
V_{CCO} + 0.35	100%	–0.35	0%
V_{CCO} + 0.40	96%	–0.40	0%
V_{CCO} + 0.45	2%	–0.45	0%

Notes:

1. A total of 200 mA per bank should not be exceeded.
2. For UI smaller than 20 µs.
3. In XPIO banks, V_{IN} overshoot above V_{CCO} and undershoot below GND can reduce the performance of V_{REF}-based receivers within the same nibble.

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

PSIO Levels

Table 8: **PSIO DC Input and Output Levels**

I/O Standard[1]	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVCMOS18	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	Note 3	Note 3
LVCMOS25	–0.300	0.700	1.700	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	Note 3	Note 3
LVCMOS33	–0.300	0.800	2.000	3.400	0.400	V_{CCO} – 0.400	Note 3	Note 3

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *Versal ACAP Technical Reference Manual* (AM011).
3. Supported drive strengths of 4, 8, or 12 mA.

SelectIO Levels

Table 9: **SelectIO DC Input and Output Levels For HDIO Banks**

I/O Standard[1, 2]	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
HSTL_I_18	–0.300	50% V_{CCO} – 0.100	50% V_{CCO} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	8.0	–8.0
LVCMOS18	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	Note 3	Note 3
LVCMOS25	–0.300	0.700	1.700	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	Note 3	Note 3
LVCMOS33	–0.300	0.800	2.000	3.400	0.400	V_{CCO} – 0.400	Note 3	Note 3
LVTTL	–0.300	0.800	2.000	3.400	0.400	2.400	Note 3	Note 3
SSTL18_I	–0.300	50% V_{CCO} – 0.125	50% V_{CCO} + 0.125	V_{CCO} + 0.300	$V_{CCO}/2$ – 0.470	$V_{CCO}/2$ + 0.470	8.0	–8.0

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *Versal ACAP SelectIO Resources Architecture Manual* (AM010).
3. Supported drive strengths of 4, 8, or 12 mA in HDIO banks.

Table 10: **SelectIO DC Input and Output Levels for XPIO Banks**

I/O Standard[1, 2, 3]	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
HSTL_I	–0.300	50% V_{CCO} – 0.100	50% V_{CCO} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	5.8	–5.8
HSTL_I_12	–0.300	50% V_{CCO} – 0.080	50% V_{CCO} + 0.080	V_{CCO} + 0.300	25% V_{CCO}	75% V_{CCO}	4.1	–4.1
HSUL_12	–0.300	50% V_{CCO} – 0.130	50% V_{CCO} + 0.130	V_{CCO} + 0.300	20% V_{CCO}	80% V_{CCO}	0.1	–0.1
LVCMOS12	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	Note 4	Note 4
LVCMOS15	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	Note 5	Note 5
LVDCI_15	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	7.0	–7.0
SSTL12	–0.300	50% V_{CCO} – 0.100	50% V_{CCO} + 0.100	V_{CCO} + 0.300	$V_{CCO}/2$ – 0.150	$V_{CCO}/2$ + 0.150	8.0	–8.0
SSTL135	–0.300	50% V_{CCO} – 0.090	50% V_{CCO} + 0.090	V_{CCO} + 0.300	$V_{CCO}/2$ – 0.150	$V_{CCO}/2$ + 0.150	9.0	–9.0
SSTL15	–0.300	50% V_{CCO} – 0.100	50% V_{CCO} + 0.100	V_{CCO} + 0.300	$V_{CCO}/2$ – 0.175	$V_{CCO}/2$ + 0.175	10.0	–10.0

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *Versal ACAP SelectIO Resources Architecture Manual* (AM010).
3. POD10 and POD12 DC input and output levels are shown in Table 11, Table 16, and Table 17.
4. Supported drive strengths of 2, 4, 6, or 8 mA in XPIO banks.
5. Supported drive strengths of 2, 4, 6, 8, or 12 mA in XPIO banks.

Table 11: **DC Input Levels for Single-ended POD10, POD12, LVSTL06_12, and LVSTL_11 I/O Standards**

I/O Standard[1, 3]	V_{IL}		V_{IH}	
	V, Min	V, Max	V, Min	V, Max
POD10	–0.300	70% V_{CCO} – 0.068	70% V_{CCO} + 0.068	V_{CCO} + 0.300
POD12	–0.300	70% V_{CCO} – 0.068	70% V_{CCO} + 0.068	V_{CCO} + 0.300
LVSTL06_12	–0.300	$V_{CCO}/8$ – 0.100	$V_{CCO}/8$ + 0.100	V_{CCO} + 0.300
LVSTL_11	–0.300	$V_{CCO}/6$ – 0.100	$V_{CCO}/6$ + 0.100	V_{CCO} + 0.300

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *Versal ACAP SelectIO Resources Architecture Manual* (AM010).

Table 12: **Differential SelectIO DC Input and Output Levels for MIPI_DPHY**

I/O Standard	V_{ICM} (V)[1]			V_{ID} (V)[2]			V_{ILHS}[3]	V_{IHHS}[3]	V_{OCM} (V)[4]			V_{OD} (V)[5]		
	Min	Typ	Max	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max
MIPI_DPHY for operation <1.5 GB/s[7]	0.070	–	0.330	0.070	–	–	–0.040	0.460	0.150	0.200	0.250	0.140	0.200	0.270
MIPI_DPHY for operation at >1.5G GB/s[7]	0.070	–	0.330	0.040	–	–	–0.040	0.460	0.150	0.200	0.250	0.140	0.200	0.270

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage (Q – $\overline{Q}$).
3. V_{IHHS} and V_{ILHS} are the single-ended input high and low voltages, respectively.
4. V_{OCM} is the output common mode voltage.
5. V_{OD} is the output differential voltage (Q – $\overline{Q}$).
6. LVDS15 is specified in Table 18.
7. High-speed option for MIPI_DPHY. The V_{ID} maximum is aligned with the standard's specification. A higher V_{ID} is acceptable as long as the V_{IN} specification is also met.

Table 13: **Complementary Differential SelectIO DC Input and Output Levels for HDIO Banks**

I/O Standard	V_{ICM} (V)[1]			V_{ID} (V)[2]		V_{OL} (V)[3]	V_{OH} (V)[4]	I_{OL}	I_{OH}
	Min	Typ	Max	Min	Max	Max	Min	mA	mA
DIFF_HSTL_I_18	0.300	0.900	1.425	0.100	–	0.400	V_{CCO} – 0.400	8.0	–8.0
DIFF_SSTL18_I	0.300	0.900	1.425	0.100	–	(V_{CCO}/2) – 0.47	(V_{CCO}/2) + 0.47	8.0	–8.0
LVDS_25	0.300	1.200	1.425	0.100	0.600	–	–	–	–
SUB_LVDS	0.500	0.900	1.300	0.070	–	–	–	–	–
LVPECL	0.300	1.200	1.425	0.100	0.600	–	–	–	–
SLVS_400_25	0.070	0.200	0.330	0.140	0.450	–	–	–	–

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage (Q – $\overline{Q}$).
3. V_{OL} is the single-ended low-output voltage.
4. V_{OH} is the single-ended high-output voltage.

Table 14: **Complementary Differential SelectIO DC Input and Output Levels for XPIO Banks**

I/O Standard[1]	V_{ICM} (V)[2]			V_{ID} (V)[3]		V_{OL} (V)[4]	V_{OH} (V)[5]	I_{OL}	I_{OH}
	Min	Typ	Max	Min	Max	Max	Min	mA	mA
DIFF_HSTL_I	0.680	$V_{CCO}/2$	$(V_{CCO}/2) + 0.150$	0.100	–	0.400	$V_{CCO} - 0.400$	5.8	–5.8
DIFF_HSTL_I_12	0.400 x V_{CCO}	$V_{CCO}/2$	0.600 x V_{CCO}	0.100	–	0.250 x V_{CCO}	0.750 x V_{CCO}	4.1	–4.1
DIFF_HSUL_12	$(V_{CCO}/2) - 0.120$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.120$	0.100	–	20% V_{CCO}	80% V_{CCO}	0.1	–0.1
DIFF_SSTL12	$(V_{CCO}/2) - 0.150$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.150$	0.100	–	$(V_{CCO}/2) - 0.150$	$(V_{CCO}/2) + 0.150$	8.0	–8.0
DIFF_SSTL135	$(V_{CCO}/2) - 0.150$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.150$	0.100	–	$(V_{CCO}/2) - 0.150$	$(V_{CCO}/2) + 0.150$	9.0	–9.0
DIFF_SSTL15	$(V_{CCO}/2) - 0.175$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.175$	0.100	–	$(V_{CCO}/2) - 0.175$	$(V_{CCO}/2) + 0.175$	10.0	–10.0

Notes:

1. DIFF_POD10 and DIFF_POD12 XPIO bank specifications are shown in Table 15, Table 16, and Table 17.
2. V_{ICM} is the input common mode voltage.
3. V_{ID} is the input differential voltage.
4. V_{OL} is the single-ended low-output voltage.
5. V_{OH} is the single-ended high-output voltage.

Table 15: **DC Input Levels for Differential POD10, POD12, LVSTL06_12, and LVSTL_11 I/O Standards**

I/O Standard[1, 2]	V_{ICM} (V)			V_{ID} (V)	
	Min	Typ	Max	Min	Max
DIFF_POD10	0.630	0.700	0.770	0.140	–
DIFF_POD12	0.756	0.840	0.924	0.160	–
DIFF_LVSTL06_12	0.143	0.150	0.157	0.140	–
DIFF_LVSTL_11	0.174	0.183	0.193	0.140	–

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *Versal ACAP SelectIO Resources Architecture Manual* (AM010).

Table 16: **DC Output Levels for Single-ended and Differential POD10, POD12, LVSTL06_12, and LVSTL_11 I/O Standards**

I/O Standard	Symbol	Description[1, 2, 3]	V_{OUT}	Min	Typ	Max	Units
POD10 and POD12	R_{OL}	Pull-down resistance	V_{OM_DC} (as described in Table 17)	32	40	48	Ω
	R_{OH}	Pull-up resistance	V_{OM_DC} (as described in Table 17)	32	40	48	Ω
LVSTL06_12	R_{OL}	Pull-down resistance	$V_{OCM\_DC\_LOW}$	32	40	48	Ω
	R_{OH}	Pull-up resistance	$V_{OCM\_DC\_HIGH}$	32	40	48	Ω
LVSTL_11 (V_{OH} = 50)	R_{OL}	Pull-down resistance	V_{OM_DC} (as described in Table 17)	32	40	48	Ω
	R_{OH}	Pull-up resistance	V_{OM_DC} (as described in Table 17)	32	40	48	Ω

Notes:

1. Tested according to relevant specifications.
2. The tolerance limits are specified after calibration with stable voltage and temperature.
3. Standards specified using the default I/O standard configuration. For details, see the *Versal ACAP SelectIO Resources Architecture Manual* (AM010).

Table 17: **Definitions for DC Output Levels for Single-ended and Differential POD10, POD12, LVSTL06_12, and LVSTL_11 I/O Standards**

I/O Standard	Symbol	Description	All Speed Grades	Units
POD10 and POD12	V_{OM_DC}	DC output mid measurement level (for IV curve linearity)	0.8 x V_{CCO}	V
LVSTL_11 (V_{OH} = 50)	V_{OM_DC}	DC output mid measurement level (for IV curve linearity)	V_{CCO}/2	V
LVSTL06_12	$V_{OCM\_DC\_LOW}$	DC output mid measurement level (for IV curve linearity), drive logic Low	V_{CCO}/2	V
	$V_{OCM\_DC\_HIGH}$	DC output measurement level (for IV curve linearity), drive logic High	V_{CCO}/2 to V_{CCO}/4	V

LVDS DC Specifications (LVDS15)

The LVDS15 standard is available in the XPIO banks. See the *Versal ACAP SelectIO Resources Architecture Manual* (AM010) for more information.

Table 18: **LVDS15 DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}[1]	Supply voltage		1.425	1.500	1.575	V
V_{ODIFF}[2]	Differential output voltage: (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	R_T = 100Ω across Q and $\overline{Q}$ signals	247	350	454	mV
V_{OCM}[2]	Output common-mode voltage	R_T = 100Ω across Q and $\overline{Q}$ signals	1.000	1.20	1.320	V
V_{IDIFF}[3]	Differential input voltage: (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High		100	350	600[3]	mV
V_{ICM_DC}[4]	Input common-mode voltage (DC coupling)		0.300	1.200	1.320	V
V_{ICM_AC}[5]	Input common-mode voltage (AC coupling)		200	–	330	mV

Notes:

1. In XPIO banks, when LVDS15 is used with input-only functionality, it can be placed in a bank where the V_{CCO} levels are different from the specified level only if internal differential termination is not used. In this scenario, V_{CCO} must be chosen to ensure the input pin voltage levels do not violate the Recommended Operating Condition (Table 3) specification for the V_{IN} I/O pin voltage.
2. V_{OCM} and V_{ODIFF} values are for LVDS_PRE_EMPHASIS = FALSE.
3. Maximum V_{IDIFF} value is specified for the maximum V_{ICM} specification. With a lower V_{ICM}, a higher V_{DIFF} is tolerated only when the recommended operating conditions and overshoot/undershoot V_{IN} specifications are maintained.
4. Input common mode voltage for DC coupled configurations. EQUALIZATION = EQ_NONE (Default).
5. AC coupling with external bias and external differential termination with EQUALIZATION settings enabled. EQUALIZATION = EQ_LEVEL0, EQ_LEVEL1, EQ_LEVEL2, EQ_LEVEL3, or EQ_LEVEL4, any setting except EQ_NONE.

Power Supply Requirements

Versal Prime devices have multiple power domains. Certain power domains can be powered down to save power. The required sequences are defined for minimum power-on current and to minimize I/O transients during the power sequences. Only the required sequences are characterized, documented, and supported. When the Recommended Operating Conditions are the same, supplies with the same voltage can be combined or ramped together. The required sequencing and power delivery options are shown in the power design tab in the Xilinx® Power Estimator (XPE). For more information, see https://www.xilinx.com/power.

Table 19: **Power Supply Ramp Time**

Symbol	Description	Min	Max	Units
T_{VCCAUX}	Ramp time from GND to 95% of V_{CCAUX}	0.2	40	ms
T_{VCCAUX_PMC}	Ramp time from GND to 95% of V_{CCAUX_PMC}	0.2	40	ms
T_{VCCAUX_SMON}	Ramp time from GND to 95% of V_{CCAUX_SMON}	0.2	40	ms
T_{VCC_FUSE}	Ramp time from GND to 95% of V_{CC_FUSE}	0.2	40	ms
T_{VCCINT}	Ramp time from GND to 95% of V_{CCINT}	0.2	40	ms
$T_{VCC\_IO\_VCC\_SOC}$	Ramp time from GND to 95% of V_{CC_IO} and V_{CC_SOC}	0.2	40	ms
T_{VCCO}	Ramp time from GND to 95% of V_{CCO}	0.2	40	ms
T_{VCC_PMC}	Ramp time from GND to 95% of V_{CC_PMC}	0.2	40	ms
T_{VCC_PSFP}	Ramp time from GND to 95% of V_{CC_PSFP}	0.2	40	ms
T_{VCC_PSLP}	Ramp time from GND to 95% of V_{CC_PSLP}	0.2	40	ms
T_{VCC_RAM}	Ramp time from GND to 95% of V_{CC_RAM}	0.2	40	ms
T_{GTY_AVCC}	Ramp time from GND to 95% of V_{GTY_AVCC}	0.2	40	ms
$T_{GTY\_AVCCAUX}$	Ramp time from GND to 95% of $V_{GTY\_AVCCAUX}$	0.2	40	ms
T_{GTY_AVTT}	Ramp time from GND to 95% of V_{GTY_AVTT}	0.2	40	ms

AC Switching Characteristics

All values represented in this data sheet are based on the speed specifications in the Vivado® Design Suite as outlined in the following table.

Table 20: **Speed Specification Version By Device**

2021.1	Device
2.01	XCVM1802

Switching characteristics are specified on a per-speed-grade basis and can be designated as engineering sample, pre-production, or production. Each designation is defined as follows:

- **Engineering Sample Product Specification:** These specifications are based on simulations only and are typically available soon after dice design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.
- **Pre-production Product Specification:** These specifications are based on almost complete silicon characterization. Dices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to engineering sample (ES) data.
- **Production Product Specification:** These specifications are released once enough production silicon of a particular dice family member has been characterized to provide full correlation between specifications and dices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to production before faster speed grades.

Testing of AC Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. All AC switching characteristics are representative of worst-case supply voltage and junction temperature conditions.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Versal Prime devices.

Speed Grade Designations

Because individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. Table 21 correlates the current status of the Versal Prime device on a per speed grade basis. See Table 4 for operating voltages listed by speed grade.

Table 21: **Speed Grade Designations by Device**

Device	Speed Grade, Temperature Ranges, Static Screen, and V_{CCINT} Operating Voltages		
	Engineering Sample	Pre-production	Production
XCVM1102	-3HSE, -3HLE, -2HSE, and -2HLE (V_{CCINT} = 0.88V) -2MSE, -2MLE, -2MSI, -2MLI (V_{CCINT} = 0.80V) -2LSE, -2LLE (V_{CCINT} = 0.70V) -1MSE, -1MLE, -1MSI, -1MLI (V_{CCINT} = 0.80V) -1LSE, -1LLE, -1LSI, -1LLI (V_{CCINT} = 0.70V)		
XCVM1302	-3HSE, -3HLE, -2HSE, and -2HLE (V_{CCINT} = 0.88V) -2MSE, -2MLE, -2MSI, -2MLI (V_{CCINT} = 0.80V) -2LSE, -2LLE (V_{CCINT} = 0.70V) -1MSE, -1MLE, -1MSI, -1MLI (V_{CCINT} = 0.80V) -1LSE, -1LLE, -1LSI, -1LLI (V_{CCINT} = 0.70V)		
XCVM1402	-3HSE, -3HLE, -2HSE, and -2HLE (V_{CCINT} = 0.88V) -2MSE, -2MLE, -2MSI, -2MLI (V_{CCINT} = 0.80V) -2LSE, -2LLE (V_{CCINT} = 0.70V) -1MSE, -1MLE, -1MSI, -1MLI (V_{CCINT} = 0.80V) -1LSE, -1LLE, -1LSI, -1LLI (V_{CCINT} = 0.70V)		
XCVM1502	-3HSE, -3HLE, -2HSE, and -2HLE (V_{CCINT} = 0.88V) -2MSE, -2MLE, -2MSI, -2MLI (V_{CCINT} = 0.80V) -2LSE, -2LLE (V_{CCINT} = 0.70V) -1MSE, -1MLE, -1MSI, -1MLI (V_{CCINT} = 0.80V) -1LSE, -1LLE, -1LSI, -1LLI (V_{CCINT} = 0.70V)		
XCVM1802	-3HSE, -3HLE, -2HSE, and -2HLE (V_{CCINT} = 0.88V)		-2MSE, -2MLE, -2MSI, -2MLI (V_{CCINT} = 0.80V) -2LSE, -2LLE (V_{CCINT} = 0.70V) -1MSE, -1MLE, -1MSI, -1MLI (V_{CCINT} = 0.80V) -1LSE, -1LLE, -1LSI, -1LLI (V_{CCINT} = 0.70V)
XCVM2502	-3HSE, -3HLE, -2HSE, and -2HLE (V_{CCINT} = 0.88V) -2MSE, -2MLE, -2MSI, -2MLI (V_{CCINT} = 0.80V) -2LSE, -2LLE (V_{CCINT} = 0.70V) -1MSE, -1MLE, -1MSI, -1MLI (V_{CCINT} = 0.80V) -1LSE, -1LLE, -1LSI, -1LLI (V_{CCINT} = 0.70V)		
XCVM2602	-3HSE, -3HLE, -2HSE, and -2HLE (V_{CCINT} = 0.88V) -2MSE, -2MLE, -2MSI, -2MLI (V_{CCINT} = 0.80V) -2LSE, -2LLE (V_{CCINT} = 0.70V) -1MSE, -1MLE, -1MSI, -1MLI (V_{CCINT} = 0.80V) -1LSE, -1LLE, -1LSI, -1LLI (V_{CCINT} = 0.70V)		
XCVM2902	-3HSE, -3HLE, -2HSE, and -2HLE (V_{CCINT} = 0.88V) -2MSE, -2MLE, -2MSI, -2MLI (V_{CCINT} = 0.80V) -2LSE, -2LLE (V_{CCINT} = 0.70V) -1MSE, -1MLE, -1MSI, -1MLI (V_{CCINT} = 0.80V) -1LSE, -1LLE, -1LSI, -1LLI (V_{CCINT} = 0.70V)		

Production Silicon and Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (engineering sample, pre-production, production). Any labeling discrepancies are corrected in subsequent speed specification releases.

The following table lists the production released Versal Prime device, speed grade, and the minimum corresponding supported speed specification version and Vivado® software versions. The Vivado software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 22: **Production Software and Speed Specification Release**

Device	Performance as a Function of Speed Grade and Operating Voltage (V_{CCINT})[1, 2]					
	0.88V (H)		0.80V (M)		0.70V (L)	
	-3	-2	-2	-1	-2	-1
XCVM1102						
XCVM1302						
XCVM1402						
XCVM1502						
XCVM1802			Vivado tools 2021.1 v2.01		Vivado tools 2020.3 v2.00	
XCVM2502						
XCVM2602						
XCVM2902						

Notes:

1. See Table 4 for the complete list of operating voltages by speed grade.
2. Blank entries indicate a device and/or speed grade in engineering sample or pre-production status.

Device Identification

The combined IDCODE and EXTENDED_IDCODE value provide the Xilinx device type identification as listed in the following table. For more information on the IDCODE and EXTENDED_IDCODE, see the *Versal ACAP Technical Reference Manual* (AM011).

Table 23: **Device Identification**

Device	IDCODE[31:0] (Hex)[1]	EXTENDED_IDCODE[31:0] (Binary)[2]
XCVM1102	X4C00093	XXXX 0000 0000 0000 01XX XXXX XXXX XXXX
XCVM1302	X4C09093	XXXX 0000 0000 0000 01XX XXXX XXXX XXXX
XCVM1402	X4C08093	XXXX 0000 0000 0000 01XX XXXX XXXX XXXX
XCVM1502	X4C99093	XXXX 0000 0000 0000 01XX XXXX XXXX XXXX
XCVM1802	14CAA093	XXXX 0000 0000 0000 01XX XXXX XXXX XXXX
XCVM2502	X4D01093	XXXX 0000 0000 0000 01XX XXXX XXXX XXXX
XCVM2602	X4C19093	XXXX 0000 0000 0000 01XX XXXX XXXX XXXX
XCVM2902	X4C23093	XXXX 0000 0000 0000 01XX XXXX XXXX XXXX

Notes:

1. An X at the location of the IDCODE[31:28] revision field is a placeholder until the production revision is defined.
2. Only the EXTENDED_IDCODE[27:14] bit values are relevant to device identification. The X in other bit positions indicate that they can be any value and must be ignored during device identification.

Processing System Performance Characteristics

Table 24: **Processor Performance**

Symbol	Description	Performance as a Function of Speed Grade and Operating Voltage						Units
		0.88V (H)		0.80V (M)		0.70V (L)		
		-3	-2	-2	-1	-2	-1	
F_{APUMAX}	Maximum APU clock frequency where the operating voltage = V_{CC_PSFP}	1700	1650	1400	1300	1080	1000[1]	MHz
F_{RPUMAX}	Maximum RPU clock frequency where the operating voltage = V_{CC_PSLP}	800	800	600	600	450	400[2]	MHz

Notes:

1. The -1LLI and -1LSI low-power devices support an overdrive voltage where the maximum APU reference clock frequency is 1600 MHz when V_{CC_PSFP} = 0.88V.
2. The -1LLI and -1LSI low-power devices support an overdrive voltage where the maximum RPU reference clock frequency is 800 MHz V_{CC_PSLP} = 0.88V.

Table 25: **PS-PL Interface Performance**

Symbol	Description	Performance as a Function of Speed Grade and Operating Voltage						Units
		0.88V (H)		0.80V (M)		0.70V (L)		
		-3	-2	-2	-1	-2	-1	
F_{AXI_CLK}	Maximum AXI4 and ACE-LITE interface frequency	400	400	350	350	300	250[1]	MHz
F_{PLAT_CLK}	Maximum PL address translation (AT) interface frequency	400	400	350	350	300	250[2]	MHz
F_{PLATB_CLK}	Maximum PL-PS advanced trace bus (ATB) interface frequency	400	400	350	350	300	250[2]	MHz
F_{PSACE_CLK}	Maximum AXI4 coherency extensions (ACE) interface frequency	400	400	350	350	300	250[2]	MHz
F_{PSACP_CLK}	Maximum accelerator coherency port (ACP) interface frequency	400	400	350	350	300	250[2]	MHz
$F_{PSFCIDMA\_CLK}$	Maximum DMA flow-control interface (FCI) frequency	400	400	350	350	300	250[3]	MHz

Notes:

1. The -1LLI and -1LSI low-power devices support an overdrive voltage where the maximum clock frequency is 280 MHz for AXI4 (when V_{CC_PSFP} = 0.88V or V_{CC_PSLP} = 0.88V) and ACE-LITE (when V_{CC_PSFP} = 0.88V).
2. The -1LLI and -1LSI low-power devices support an overdrive voltage where the maximum clock frequency is 280 MHz when V_{CC_PSFP} = 0.88V.
3. The -1LLI and -1LSI low-power devices support an overdrive voltage where the maximum clock frequency is 280 MHz when V_{CC_PSLP} = 0.88V.

PS and PMC Switching Characteristics

Clocks and Reset

Table 26: Reference Clock Requirements

Symbol	Description	Min	Max	Units
F_{REFCLK}	Reference clock (REF_CLK) frequency	27	60	MHz
T_{RMSJ_REFCLK}	REF_CLK input RMS clock jitter	–	3	ps
T_{INPJ_REFCLK}	REF_CLK input period jitter (peak-to-peak) Number of clock cycles = 10,000	–	50	ps
T_{DC_REFCLK}	REF_CLK duty cycle	45	55	%
T_{REFCLK}	REF_CLK rise time (20%–80%) and fall time (80%–20%) at 3.3V	–	3	ns
	REF_CLK rise time (20%–80%) and fall time (80%–20%) at 1.8V or 2.5V	–	3.5	ns
	REF_CLK rise time (10%–90%) and fall time (90%–10%) at 3.3V	–	4	ns
	REF_CLK rise time (10%–90%) and fall time (90%–10%) at 1.8V or 2.5V	–	4.66	ns

Notes:

1. The F_{REFCLK} clock frequency range and T_{DC_REFCLK} duty cycle specifications also apply to the PL alternative reference clock inputs (PL_PMC_ALT_REF_CLK, PL_LPD_ALT_REF_CLK, and PL_FPD_ALT_REF_CLK).

Table 27: RTC Crystal Requirements

Symbol	Description	Min	Typ	Max	Units
F_{XTAL}	Parallel resonance crystal frequency	–	32.768	–	kHz
T_{FTXTAL}	Frequency tolerance	–20	–	20	ppm
C_{XTAL}	Load capacitance for crystal parallel resonance	–	12.5	–	pF
R_{ESR}	Crystal ESR (16.8 and 19.2 MHz)	–	70	–	kΩ
C_{SHUNT}	Crystal shunt capacitance	–	1.4	–	pF

Table 28: Power-on Reset Assertion Timing Requirements

Symbol	Description	Min	Typ	Max	Units
T_{POR_B}	Required POR_B assertion time[1, 2]	10	–	–	µs
$T_{MODEPOR}$	MODE[3:0] setup time to POR_B rising edge	74	–	–	ns
$T_{PORMODE}$	POR_B rising edge to MODE[3:0] hold time	74	–	–	ns

Notes:

1. The POR_B input must be asserted Low during the power-on sequence and continue to be asserted for a duration T_{POR_B} after all the required supplies of the PMC have reached minimum voltage levels. The PS, system, and PL domains can be independently powered on or off with additional power management. If the PS, system, and/or PL domains are expected to be functional at initial power-on without additional power management, then the POR_B input must be held Low until all required domain power supplies have also reached minimum voltage levels. For additional power-on sequence information, refer to the Xilinx Power Estimator (XPE). For additional power management information, see the *Versal ACAP Technical Reference Manual* (AM011) or the *Versal ACAP System Software Developers Guide* (UG1304).
2. Before the de-assertion of POR_B, the REF_CLK must be operating within specification.

Table 29: **PS FPD Clocks Switching Characteristics**

Symbol	Description	Performance as a Function of Speed Grade and Operating Voltage (V_{CC_PSFP})						Units
		0.88V (H)		0.80V (M)		0.70V (L)		
		-3	-2	-2	-1	-2	-1	
$F_{FPD\_LSBUS\_CLK}$	Maximum FPD LSBUS clock frequency	150	150	150	150	100	100[1]	MHz
$F_{FPD\_TOPSW\_CLK}$	Maximum FPD top-switch clock frequency	1000	950	825	800	600	550[2]	MHz
$F_{DBG\_FPD\_CLK}$	Maximum debug FPD clock frequency	400	400	400	400	400	333[3]	MHz

Notes:

1. The -1LLI and -1LSI low-power devices support an overdrive voltage where the maximum FPD LSBUS clock frequency is 150 MHz when V_{CC_PSFP} = 0.88V.
2. The -1LLI and -1LSI low-power devices support an overdrive voltage where the maximum FPD top-switch clock frequency is 800 MHz when V_{CC_PSFP} = 0.88V.
3. The -1LLI and -1LSI low-power devices support an overdrive voltage where the maximum debug FPD clock frequency is 400 MHz when V_{CC_PSFP} = 0.88V.

Table 30: **PS LPD Clocks Switching Characteristics**

Symbol	Description	Performance as a Function of Speed Grade and Operating Voltage (V_{CC_PSLP})						Units
		0.88V (H)		0.80V (M)		0.70V (L)		
		-3	-2	-2	-1	-2	-1	
$F_{RPLL\_TO\_XPD\_CLK}$	Maximum RPU PLL to XPD clock frequency	1200	1200	1200	1200	1000	1000	MHz
$F_{LPD\_TOPSW\_CLK}$	Maximum LPD top-switch clock frequency[1]	750	700	600	600	450	400[2]	MHz
$F_{LPD\_LSBUS\_CLK}$	Maximum LPD LSBUS clock frequency[1]	150	150	150	150	100	100[3]	MHz
$F_{IOP\_SW\_CLK}$	Maximum I/O peripherals (IOP) switch clock frequency	250	250	250	250	250	250	MHz
F_{TS_REFCLK}	Maximum time-stamp reference clock frequency	100	100	100	100	100	100	MHz
F_{PSM_REFCLK}	Maximum PS manager (PSM) reference clock frequency	460	460	460	460	368	368[4]	MHz
$F_{DBG\_LPD\_CLK}$	Maximum debug LPD clock frequency	400	400	400	400	400	333[5]	MHz
$F_{DBG\_TS\_CLK}$	Maximum debug time-stamp clock frequency	400	400	400	400	400	333[6]	MHz
F_{USB_REFCLK}	Maximum USB reference clock frequency	60	60	60	60	60	60	MHz
$F_{CPM4\_TOPSW\_CLK}$	Maximum CPM4 top-switch clock frequency	1000	950	825	800	600	550	MHz

Notes:

1. The LPD_TOPSW_CLK operating frequency must be greater than the LPD_LSBUS_CLK operating frequency.
2. The -1LLI and -1LSI low-power devices support an overdrive voltage where the maximum LPD top-switch clock frequency is 600 MHz when V_{CC_PSLP} = 0.88V.
3. The -1LLI and -1LSI low-power devices support an overdrive voltage where the maximum LPD LSBUS clock frequency is 150 MHz when V_{CC_PSLP} = 0.88V.
4. The -1LLI and -1LSI low-power devices support an overdrive voltage where the maximum PSM reference clock frequency is 400 MHz when V_{CC_PSLP} = 0.88V.
5. The -1LLI and -1LSI low-power devices support an overdrive voltage where the maximum debug LPD clock frequency is 400 MHz when V_{CC_PSLP} = 0.88V.
6. The -1LLI and -1LSI low-power devices support an overdrive voltage where the maximum debug time-stamp clock frequency is 400 MHz when V_{CC_PSLP} = 0.88V.

Table 31: **PMC IRO Clock Switching Characteristics**

Symbol	Description	Performance as a Function of Speed Grade and Operating Voltage (V_{CC_PMC})						Units
		0.88V (H)		0.80V (M)		0.70V (L)		
		-3	-2	-2	-1	-2	-1	
$F_{PMC\_IRO\_CLK}$	PMC internal clock source typical frequency	400	400	400	400	320	320	MHz
	PMC internal clock source tolerance	+10/–17	+10/–17	+10/–17	+10/–17	+10/–17	+10/–17	%

Table 32: **PMC Clocks Switching Characteristics**

Symbol	Description	Performance as a Function of Speed Grade and Operating Voltage (V_{CC_PMC})						Units
		0.88V (H)		0.80V (M)		0.70V (L)		
		-3	-2	-2	-1	-2	-1	
F_{EFUSE_REFCLK}	Maximum eFUSE reference clock frequency for reading	115	115	115	115	92	92	MHz
	Maximum eFUSE reference clock frequency for programming	60	60	60	60	60	60	MHz
F_{SMON_REFCLK}	Maximum system monitor reference clock frequency	300	300	300	300	300	300	MHz
$F_{USB\_SREFCLK}$	Maximum USB suspend reference clock frequency	115	115	115	115	92	92	MHz
$F_{AXI\_TO\_REFCLK}$	Maximum AXI4 timeout reference clock frequency	115	115	115	115	92	92	MHz
F_{CFU_REFCLK}	Maximum configuration frame unit (CFU) reference clock frequency[1]	400	400	400	400	320	320	MHz
	Minimum CFU reference clock frequency	20	20	20	20	20	20	MHz
F_{LSBUS_REFCLK}	Maximum PMC LSBUS reference clock frequency	150	150	150	150	100	100	MHz
F_{NPI_REFCLK}	Maximum NoC programming interface (NPI) reference clock frequency	300	300	300	300	300	300	MHz
F_{HSM1_REFCLK}	Maximum horizontal super module (HSM1) reference clock frequency used with XPIO[2]	200	200	200	200	200	200	MHz
F_{PL0_REFCLK}	Maximum PL0 reference clock frequency	400	400	350	350	300	250[3]	MHz
F_{PL1_REFCLK}	Maximum PL1 reference clock frequency	400	400	350	350	300	250[3]	MHz
F_{PL2_REFCLK}	Maximum PL2 reference clock frequency	400	400	350	350	300	250[3]	MHz
F_{PL3_REFCLK}	Maximum PL3 reference clock frequency	400	400	350	350	300	250[3]	MHz
$F_{PPLL\_TO\_XPD\_CLK}$	Maximum PMC PLL to XPD clock frequency	1200	1200	1200	1200	1000	1000	MHz
$F_{NPLL\_TO\_XPD\_CLK}$	Maximum NoC PLL to XPD clock frequency	1200	1200	1200	1200	1000	1000	MHz

Notes:

1. The maximum configuration frame interface (CFI) clock frequency is the same as the CFU reference clock. When the programmable device image (PDI) is compressed, the compressed data rate through the CFU decompressor is limited to half of the CFI data rate.
2. When the HSM1 reference clock is used as the source clock to the XPLL, the frequency range is limited from 100 MHz to 200 MHz.
3. The -1LLI and -1LSI low-power devices support an overdrive voltage where the maximum PL0, PL1, PL2, and PL3 reference clock frequency is 280 MHz when V_{CC_PMC} = 0.88V

Table 33: **PMC PLL Switching Characteristics**

Symbol	Description	Performance as a Function of Speed Grade and Operating Voltage (V_{CC_PMC})						Units
		0.88V (H)		0.80V (M)		0.70V (L)		
		-3	-2	-2	-1	-2	-1	
F_{PMCPLL}	PMC PLL output frequency	2000	2000	1800	1600	1300	1300	MHz, Max
		270	270	270	270	270	270	MHz, Min
$F_{PMCPLLVCO}$	PMC PLL VCO frequency	4320	4320	4320	4320	4320	4320	MHz, Max
		2160	2160	2160	2160	2160	2160	MHz, Min
$T_{PMCPLLLOCK}$	PMC PLL lock time	100	100	100	100	100	100	µs, Max

Notes:

1. The -1LLI and -1LSI low-power devices support an overdrive voltage where the maximum reference clock frequency is 1600 MHz when V_{CC_PMC} = 0.88V.

Table 34: **NoC PLL Switching Characteristics**

Symbol	Description	Performance as a Function of Speed Grade and Operating Voltage (V_{CC_PMC})						Units
		0.88V (H)		0.80V (M)		0.70V (L)		
		-3	-2	-2	-1	-2	-1	
F_{NOCPLL}	NoC PLL output frequency	2000	2000	1800	1600	1300	1300	MHz, Max
		270	270	270	270	270	270	MHz, Min
$F_{NOCPLLVCO}$	NoC PLL VCO frequency	4320	4320	4320	4320	4320	4320	MHz, Max
		2160	2160	2160	2160	2160	2160	MHz, Min
$T_{NOCPLLLOCK}$	NoC PLL lock time	100	100	100	100	100	100	µs, Max

Table 35: **PS APU PLL Switching Characteristics**

Symbol	Description	Performance as a Function of Speed Grade and Operating Voltage (V_{CC_PSFP})						Units
		0.88V (H)		0.80V (M)		0.70V (L)		
		-3	-2	-2	-1	-2	-1	
F_{PSAPLL}	APU PLL output frequency	2000	2000	1800	1600	1300	1300[1]	MHz, Max
		270	270	270	270	270	270	MHz, Min
$F_{PSAPLLVCO}$	APU PLL VCO frequency	4320	4320	4320	4320	4320	4320	MHz, Max
		2160	2160	2160	2160	2160	2160	MHz, Min
$T_{PSAPLLLOCK}$	APU PLL lock time	100	100	100	100	100	100	µs, Max

Notes:

1. The -1LLI and -1LSI low-power devices support an overdrive voltage where the maximum reference clock frequency is 1600 MHz when V_{CC_PSFP} = 0.88V.

Table 36: **PS RPU PLL Switching Characteristics**

Symbol	Description	Performance as a Function of Speed Grade and Operating Voltage (V_{CC_PSLP})						Units
		0.88V (H)		0.80V (M)		0.70V (L)		
		-3	-2	-2	-1	-2	-1	
F_{PSRPLL}	RPU PLL output frequency	2000	2000	1800	1600	1300	1300[1]	MHz, Max
		270	270	270	270	270	270	MHz, Min
$F_{PSRPLLVCO}$	RPU PLL VCO frequency	4320	4320	4320	4320	4320	4320	MHz, Max
		2160	2160	2160	2160	2160	2160	MHz, Min
$T_{PSRPLLLOCK}$	RPU PLL lock time	100	100	100	100	100	100	µs, Max

Notes:

1. The -1LLI and -1LSI low-power devices support an overdrive voltage where the maximum reference clock frequency is 1600 MHz when V_{CC_PSLP} = 0.88V.

Table 37: **CPM4 PLL Switching Characteristics**

Symbol	Description	Performance as a Function of Speed Grade and Operating Voltage (V_{CCINT})						Units
		0.88V (H)		0.80V (M)		0.70V (L)		
		-3	-2	-2	-1	-2	-1	
$F_{CPM4PLL}$	CPM4 PLL output frequency	1200	1080	900	900	810	720	MHz, Max
		270	270	270	270	270	270	MHz, Min
$F_{CPM4PLLVCO}$	CPM4 PLL VCO frequency	4320	4320	4320	4320	4320	4320	MHz, Max
		2160	2160	2160	2160	2160	2160	MHz, Min
$T_{CPM4PLLLOCK}$	CPM4 PLL lock time	100	100	100	100	100	100	µs, Max

PMC JTAG and SelectMAP

Table 38: **JTAG/Boundary-Scan Port Switching Characteristics**

Symbol	Description	Performance as a Function of Speed Grade and Operating Voltage (V_{CCINT})						Units
		0.88V		0.80V		0.70V		
		-3	-2	-2	-1	-2	-1	
F_{TCK}	JTAG clock frequency	70	70	70	70	60	60	MHz, Max
T_{TCKL}	TCK Low pulse time	5.5	5.5	5.5	5.5	6.0	6.0	ns, Min
T_{TCKH}	TCK High pulse time	2.0	2.0	2.0	2.0	2.0	2.0	ns, Min
T_{TAPTCK}/T_{TCKTAP}	TMS and TDI setup and hold	3.0/2.0	3.0/2.0	3.0/2.0	3.0/2.0	3.0/2.0	3.0/2.0	ns, Min
T_{TCKTDO}	TCK falling edge to TDO output	5.5	5.5	5.5	5.5	6.0	6.0	ns, Max

Table 39: **SelectMap Interface Switching Characteristics**

Symbol	Description	Performance as a Function of Speed Grade and Operating Voltage (V_{CCINT})						Units
		0.88V		0.80V		0.70V		
		-3	-2	-2	-1	-2	-1	
$F_{SMAPCLK}$	SelectMap clock frequency, write	200	200	200	200	200	200	MHz, Max
	SelectMap clock frequency, read	120	120	120	120	120	120	MHz, Max
$T_{SMAPCLKL}$	SelectMAP clock Low time	2.5	2.5	2.5	2.5	2.5	2.5	ns, Min
$T_{SMAPCLKH}$	SelectMAP clock High time	2.5	2.5	2.5	2.5	2.5	2.5	ns, Min
$T_{SMAPDCLK/SMAPCLKD}$	SelectMAP data (SMAP_IO[31:0]) setup and hold	3.0/0.0	3.0/0.0	3.0/0.0	3.0/0.0	4.5/0.0	4.5/0.0	ns, Min
$T_{SMAPCSCLK/SMAPCLKCS}$	SelectMAP chip select (SMAP_CS_b) setup and hold	3.0/0.0	3.0/0.0	3.0/0.0	3.0/0.0	4.0/0.0	4.0/0.0	ns, Min
$T_{SMAPRWCLK/SMAPCLKRW}$	SelectMAP read write (SMAP_RDWR_b) setup and hold	3.0/0.0	3.0/0.0	3.0/0.0	3.0/0.0	4.0/0.0	4.0/0.0	ns, Min
$T_{SMAPCLKO}$	SelectMAP clock to data output	13.0	13.0	13.0	13.0	13.0	13.0	ns, Max
$C_{SMAPBUSYCS}$	SelectMAP busy assertion to chip select de-assertion	24	24	24	24	24	24	clock cycles, Max

PS and PMC Interface Specifications

PMC Quad-SPI Controller Interface

Table 40: **Quad-SPI Interface**

Symbol	Description[1, 2]	Min	Max	Units
Quad-SPI device clock frequency operating at >100 MHz up to 150 MHz. Loopback enabled.[3]				
F_{QSPI_CLK}	Quad-SPI device clock frequency	100	150	MHz
F_{QSPI_REFCLK}[4]	Quad-SPI reference clock frequency	2 × F_{QSPI_CLK}		MHz
$T_{QSPIDCK}$	Setup time, all inputs	0.77	–	ns
$T_{QSPICKD}$	Hold time, all inputs	1.0	–	ns
$T_{QSPICKO}$	Clock to output delay, all outputs	2.9	4.5	ns
$T_{QSPICSCLK}$[5]	Chip select asserted to next clock edge	5.0	–	ns
$T_{QSPICLKCS}$	Clock edge to chip select deasserted	5.0	–	ns
$T_{DCQSPICLK}$	Quad-SPI clock duty cycle	45	55	%
Quad-SPI device clock frequency operating at >37.5 MHz up to 100 MHz. Loopback enabled.[3]				
F_{QSPI_CLK}	Quad-SPI device clock frequency	37.5	100	MHz
F_{QSPI_REFCLK}[4]	Quad-SPI reference clock frequency	2 × F_{QSPI_CLK}		MHz
$T_{QSPIDCK}$	Setup time, all inputs	2.0	–	ns
$T_{QSPICKD}$	Hold time, all inputs	0.0	–	ns
$T_{QSPICKO}$	Clock to output delay, all outputs	3.2	7.8	ns
$T_{QSPICSCLK}$[5]	Chip select asserted to next clock edge	5.0	–	ns
$T_{QSPICLKCS}$	Clock edge to chip select deasserted	5.0	–	ns
$T_{DCQSPICLK}$	Quad-SPI clock duty cycle	45	55	%
Quad-SPI device clock frequency operating at ≤37.5 MHz. Loopback disabled.				
F_{QSPI_CLK}	Quad-SPI device clock frequency		37.5	MHz
F_{QSPI_REFCLK}[4]	Quad-SPI reference clock frequency		150	MHz
$T_{QSPIDCK}$	Setup time, all inputs	19.1	–	ns
$T_{QSPICKD}$	Hold time, all inputs	0.0	–	ns
$T_{QSPICKO}$	Clock to output delay, all outputs	5.2	21.5	ns
$T_{QSPICSCLK}$	Chip select asserted to next clock edge	9.0	–	ns
$T_{QSPICLKCS}$[5]	Clock edge to chip select deasserted	9.0	–	ns
$T_{DCQSPICLK}$	Quad-SPI clock duty cycle	45	55	%

Notes:

1. The test conditions are configured for the generic Quad-SPI interface with a 12 mA drive strength, fast slew rate, and load conditions (15 pF/30 pF for a Quad-SPI device clock frequency up to 100 MHz and 15 pF for a Quad-SPI device clock frequency > 100 MHz), tested at 3.3V and 1.8V.
2. 30 pF loads are for QSPI dual-stacked or QSPI dual-parallel modes.
3. When the Quad-SPI device clock frequency is >37.5 MHz, the Quad-SPI loopback clock output (QSPI_LPBK_CLK) must be enabled in the control, interface, and processing system (CIPS), and the associated MIO[6] pin must be left unconnected on the board.
4. The Quad-SPI reference clock frequency must be 2x the Quad-SPI device clock frequency when it is >37.5 MHz.
5. $T_{QSPICSCLK}$ is only valid when two reference clock cycles are programmed between the chip select and clock.

PMC Octal-SPI Controller Interface

Table 41: **Octal-SPI Interface**

Symbol	Description[1]	Min	Max	Units
Octal-SPI device clock frequency operating at DDR 50 MHz up to 200 MHz.				
F_{OSPI_CLK}	Octal-SPI device clock frequency	50	200	MHz
F_{OSPI_REFCLK}	Octal-SPI reference clock frequency	= F_{OSPI_CLK}[2]		MHz
$T_{OSPIDCCLK}$	Octal-SPI clock duty cycle	45	55	%
Octal-SPI device clock frequency operating at SDR 50 MHz to 166 MHz.				
F_{OSPI_CLK}	Octal-SPI device clock frequency	50	166	MHz
F_{OSPI_REFCLK}	Octal-SPI reference clock frequency	= F_{OSPI_CLK}[2]		MHz
$T_{OSPIDCCLK}$	Octal-SPI clock duty cycle	45	55	%
Octal-SPI device clock frequency operating at SDR <50 MHz.				
F_{OSPI_CLK}	Octal-SPI device clock frequency	–	50	MHz
F_{OSPI_REFCLK}	Octal-SPI reference clock frequency	4 × F_{OSPI_CLK}	200	MHz
$T_{OSPIDCCLK}$	Octal-SPI clock duty cycle	45	55	%

Notes:

1. The test conditions are configured for the Octal-SPI interface with a 12 mA drive strength, fast slew rate, and 20pF load.
2. The Octal-SPI reference clock frequency must be equal to F_{OSPI_CLK} when the Octal-SPI device clock frequency is ≥50 MHz.

PS SPI Controller Interface

Table 42: **SPI Controller Interface**

Symbol	Description[1]	Min	Max	Units
SPI Master Interface				
F_{MSPI_CLK}	SPI master device clock frequency (MIO)	–	50	MHz
	SPI master device clock frequency (EMIO)	–	25	MHz
F_{SPI_REFCLK}	SPI reference clock frequency	–	200	MHz
$T_{DCMSPICLK}$	SPI master mode clock duty cycle	45	55	%
$T_{MSPISSSCLK}$	Master select asserted to first active clock edge[2]	1	–	SPI_REFCLK cycles
$T_{MSPISCLKSS}$	Last active clock edge to slave select deasserted[2]	1	–	SPI_REFCLK cycles
$T_{MSPIDCK}$	Input setup time for master in/slave out (MISO)	9.9	–	ns
$T_{MSPICKD}$	Input hold time for MISO	0.0	–	ns
$T_{MSPICKO}$	Master out/slave in (MOSI) and slave select clock-to-out delay	–3.7	5.0	ns
SPI Slave Interface				
F_{SSPI_CLK}	SPI slave device clock frequency	–	25	MHz
F_{SPI_REFCLK}	SPI reference clock frequency	–	200	MHz
$T_{SSPISSSCLK}$	Slave select asserted to first active clock edge	1	–	SPI_REFCLK cycles
$T_{SSPISCLKSS}$	Last active clock edge to slave select deasserted	1	–	SPI_REFCLK cycles
$T_{SSPIDCK}$	Input setup time for MISO	5.0	–	ns
$T_{SSPICKD}$	Input hold time for MISO	5.0	–	ns

Table 42: **SPI Controller Interface** *(cont'd)*

Symbol	Description[1]	Min	Max	Units
$T_{SSPICKO}$	MOSI clock-to-out delay	0.0	13	ns

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and 15 pF load.
2. The test conditions use the SPI delay register where XSPIPS_DR_OFFSET[xspips_dr_init_mask] = 2 and XSPIPS_DR_OFFSET[xspips_dr_after_mask] = 2.

PS USB Controller Interface

Table 43: **ULPI Interface**

Symbol	Description[1]	Min	Max	Units
$T_{ULPIDCK}$	Input setup to ULPI clock, all inputs	4.5	–	ns
$T_{ULPICKD}$	Input hold to ULPI clock, all inputs	0	–	ns
$T_{ULPICKO}$	ULPI clock to output valid, all outputs	2.0	8.9	ns
$F_{ULPICLK}$	ULPI clock frequency	–	60	MHz

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.

PS Gigabit Ethernet MAC Controller Interface

Table 44: **RGMII Interface**

Symbol	Description[1]	Min	Max	Units
$F_{GEMTXCLK}$	RGMII_TX_CLK transmit clock frequency	–	125	MHz
$F_{GEMRXCLK}$	RGMII_RX_CLK receive clock frequency	–	125	MHz
$F_{GEMREFCLK}$	Gigabit Ethernet MAC (GEM) reference clock frequency	–	125	MHz
$F_{GEMTSUREFCLK}$	Gigabit Ethernet MAC time-stamp unit reference clock frequency	–	250	MHz
$T_{DCGEMTXCLK}$	Transmit clock duty cycle	45	55	%
$T_{GEMTXCKO}$	TXD output clock to out time	–0.5	0.5	ns
$T_{GEMRXDCK}$	RXD input setup time	0.8	–	ns
$T_{GEMRXCKD}$	RXD input hold time	0.8	–	ns
$T_{MDIOCLK}$	MDC output clock period	400	–	ns
$T_{MDIOCKL}$	MDC Low time	160	–	ns
$T_{MDIOCKH}$	MDC High time	160	–	ns
$T_{MDIODCK}$	MDIO input data setup time	80	–	ns
$T_{MDIOCKD}$	MDIO input data hold time	0.0	–	ns
$T_{MDIOCKO}$	MDIO output data delay time	–3.0	15.0	ns

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.

PMC SD/SDIO Controller Interface

Table 45: **SD/SDIO Interface**

Symbol	Description[1]	Min	Max	Units
F_{SD_REFCLK}	SD reference clock frequency	–	200	MHz
F_{SDDLL_REFCLK}	SD DLL reference clock frequency	–	1200	MHz
SD/SDIO Interface Default Speed Mode				
F_{SDS_CLK}[2]	SD standard device clock frequency	–	20	MHz
F_{SDID_CLK}	Clock frequency in identification mode	–	400	kHz
T_{SDDC_CLK}	SD standard device clock duty cycle	45	55	%
SD/SDIO Interface High-speed Mode				
F_{SDHS_CLK}	SD high-speed device clock frequency	25	50	MHz
T_{SDHSDC_CLK}	SD high-speed device clock duty cycle	45	55	%
SD/SDIO Interface SDR12 Mode				
$F_{SDSDR12\_CLK}$[2]	SD SDR12 device clock frequency	–	25	MHz
$T_{DCSDSDR12\_CLK}$	SD SDR12 device clock duty cycle	30	70	%
SD/SDIO Interface SDR25/SDR50 Mode				
F_{SDSDR_CLK}	SDR25 device clock frequency	25	50	MHz
	SDR50 device clock frequency	25	100	MHz
$T_{SDSDRDC\_CLK}$	SD SDR50/SDR25 device clock duty cycle	30	70	%
SD/SDIO Interface SDR104 Mode				
$F_{SDSDR104\_CLK}$	SDR104 device clock frequency	25	200	MHz
$T_{DCSDSDR104\_CLK}$	SD SDR104 device clock duty cycle	30	70	%
SD/SDIO Interface DDR50 Mode				
F_{SDDDR_CLK}	SD DDR50 device clock frequency	25	50	MHz
$T_{DCSDDDR\_CLK}$	SD DDR50 device clock duty cycle	45	55	%

Notes:

1. The test conditions for SD/SDIO modes use a 12 mA drive strength, fast slew rate, and a 15 pF load.
2. EMIO is supported in SD default speed mode and SDR12 mode.

PMC eMMC Controller Interface

Table 46: **eMMC Controller Interface**

Symbol	Description[1]	Min	Max	Units
eMMC Interface Standard Mode				
$F_{EMMCSCLK}$	eMMC standard device clock frequency[2]	–	25	MHz
$T_{DCEMMCCLK}$	eMMC clock duty cycle	45	55	%
eMMC Interface High-speed SDR Mode				
$F_{EMMCSDRCLK}$	eMMC high-speed SDR device clock frequency	25	50	MHz
$T_{DCEMMCSDRCLK}$	eMMC high-speed SDR clock duty cycle	45	55	%
eMMC Interface High-speed DDR Mode				
$F_{EMMCDDRCLK}$	eMMC high-speed DDR device clock frequency	25	50	MHz
$T_{DCEMMCDDRCLK}$	eMMC high-speed DDR clock duty cycle	45	55	%

Table 46: **eMMC Controller Interface** *(cont'd)*

Symbol	Description[1]	Min	Max	Units
eMMC Interface HS200 Mode				
$F_{EMMCHS200CLK}$	eMMC HS200 device clock frequency	25	200	MHz
$T_{DCEMMCHS200CLK}$	eMMC HS200 clock duty cycle	30	70	%

Notes:

1. The test conditions for the eMMC modes use a 12 mA drive strength, fast slew rate, and a 15 pF load.
2. EMIO is supported in the eMMC standard mode.

PS and PMC I2C Controller Interface

Table 47: **I2C Controller Interface**

Symbol	Description[1]	Min	Max	Units
I2C Fast-mode Interface				
F_{I2CF_CLK}	Serial clock line (SCL) clock frequency	–	400	kHz
F_{I2C_REFCLK}[2]	I2C reference clock frequency	–	100	MHz
$T_{I2CFCKL}$	SCL Low time	1.3	–	µs
$T_{I2CFCKH}$	SCL High time	0.6	–	µs
$T_{I2CFCKO}$	Serial data line (SDA) clock-to-out delay	–	900	ns
$T_{I2CFDCK}$	SDA input setup time	100	–	ns
$T_{I2CFCKD}$	SDA input data hold time	0	–	ns
I2C Standard-mode Interface				
F_{I2CS_CLK}	SCL clock frequency	–	100	kHz
F_{I2C_REFCLK}[2]	I2C reference clock frequency	–	100	MHz
$T_{I2CSCKL}$	SCL Low time	4.7	–	µs
$T_{I2CSCKH}$	SCL High time	4.0	–	µs
$T_{I2CSCKO}$	SDA clock-to-out delay	–	3450	ns
$T_{I2CSDCK}$	SDA input setup time	250	–	ns
$T_{I2CSCKD}$	SDA input data hold time	0	–	ns

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.
2. F_{I2C_REFCLK} specification applies to PMC_I2C_REFCLK, LPD_I2C0_REFCLK, LPD_I2C1_REFCLK, and SYSMON_I2C_REFCLK.

PS CAN FD Controller Interface

Table 48: **CAN FD Controller Interface**

Symbol	Description[1]	Min	Max	Units
$F_{CAN\_FD\_REFCLK}$[2]	CAN FD reference clock frequency 1x	–	80	MHz
	CAN FD reference clock frequency 2x	–	160	MHz
$T_{CAN\_FD\_PWRX}$	Receive pulse width	125	–	ns
$T_{CAN\_FD\_PWTX}$	Transmit pulse width	125	–	ns

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.
2. The APB interface (LPD_LSBUS_CLK) operating frequency must be greater than or equal to the CAN FD operating frequency (which is the CAN_FD_REFCLK frequency divided by the CAN[0|1]_REF_CTRL[DIVISOR]).

PS UART Controller Interface

Table 49: **UART Controller Interface**

Symbol	Description[1]	Min	Max	Units
$F_{UART\_REF\_CLK}$	UART reference clock frequency	–	100	MHz
$BAUD_{TXMAX}$	Transmit baud rate	–	6.25	Mb/s
$BAUD_{RXMAX}$	Receive baud rate	–	6.25	Mb/s

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.

PS General Purpose I/O Interface

Table 50: **General Purpose I/O (GPIO) Interface**

Symbol	Description[1]	Min	Max	Units
T_{GPIOH}	LPD GPIO input High pulse width	10 x $1/F_{LPD\_LSBUS\_CLK}$	–	µs
	PMC GPIO input High pulse width	10 x $1/F_{PMC\_LSBUS\_CLK}$	–	µs
T_{GPIOH}	LPD GPIO input Low pulse width	10 x $1/F_{LPD\_LSBUS\_CLK}$	–	µs
	PMC GPIO input Low pulse width	10 x $1/F_{PMC\_LSBUS\_CLK}$	–	µs

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and 15 pF load.

PS Trace Interface

Table 51: **Trace Interface**

Symbol	Description[1]	Performance as a Function of Speed Grade and Operating Voltage (V_{CC_PSFP})												Units
		0.88V (H)				0.80V (M)				0.70V (L)				
		-3		-2		-2		-1		-2		-1		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
F_{TCECLK}	Trace clock frequency (MIO)	–	200	–	200	–	200	–	200	–	200	–	167[2]	MHz
	Trace clock frequency (EMIO)	–	400	–	400	–	350	–	350	–	300	–	250[3]	MHz
$F_{DBGTCECLK}$	Trace debug (DBG_TRACE) clock frequency	–	400	–	400	–	400	–	400	–	400	–	333[4]	MHz
T_{TCECKO}	Trace clock to output delay, all outputs	–0.5	0.5	–0.5	0.5	–0.5	0.5	–0.5	0.5	–0.5	0.5	–0.5	0.5	ns
T_{TCECKO}	Trace clock duty cycle	45	55	45	55	45	55	45	55	45	55	45	55	%

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.
2. The -1LLI and -1LSI low-power devices support an overdrive voltage where the maximum trace clock frequency (MIO) is 200 MHz when V_{CC_PSLP} = 0.88V or V_{CC_PMC} = 0.88V.
3. The -1LLI and -1LSI low-power devices support an overdrive voltage where the maximum trace clock frequency (EMIO) is 280 MHz when V_{CC_PSFP} = 0.88V.
4. The -1LLI and -1LSI low-power devices support an overdrive voltage where the maximum trace debug clock frequency is 400 MHz when V_{CC_PSFP} = 0.88V.

PS Triple-timer Counter Interface

Table 52: **Triple-timer Counter Interface**

Symbol	Description	Min	Max	Units
$F_{TTCX\_REF\_CLK}$	Triple-timer counter input clock frequency (TTCx_REF_CLK)[1]	–	See Note 1	MHz
$F_{TTCX\_IO\_REF\_CLKX}$	Triple-timer counter MIO-EMIO input clock frequency (TTCx_IO_REF_CLKx)[2]	–	50[3]	MHz
$T_{TTCICLK}$	Triple-timer counter MIO-EMIO input clock High pulse width	$2/F_{TTCX\_IO\_REF\_CLKX}$[2]	–	µs
	Triple-timer counter MIO-EMIO input clock Low pulse width	$2/F_{TTCX\_IO\_REF\_CLKX}$[2]	–	µs
$F_{TTCICLK}$	Triple-timer counter output clock frequency	–	$F_{TTCX\_REF\_CLK}/2$[1]	MHz
			$F_{TTCX\_IO\_REF\_CLKX}/2$[2]	MHz
$T_{TTCOCLK}$	Triple-timer counter output clock period	$2/F_{TTCX\_REF\_CLK}$[1]	–	µs
		$2/F_{TTCX\_IO\_REF\_CLKX}$[2]	–	µs

Notes:

1. TTCx_REF_CLK source is used. TTCx_REF_CLK source can be the REF_CLK (F_{REFCLK}), LPD_LSBUS_CLK ($F_{LPD\_LSBUS\_CLK}$), or the RPU_REF_CLK (F_{RPUMAX}).
2. TTCx_IO_REF_CLKx source is used. TTCx_IO_REF_CLKx source can be MIO or EMIO.
3. The maximum $F_{TTCx\_IO\_REF\_CLKx}$ is the lesser of the specified maximum $F_{TTCX\_IO\_REF\_CLKX}$ or $F_{TTCX\_REF\_CLK}/2$.

PS System Watchdog Timer Interface

Table 53: **System Watchdog Timer Interface**

Symbol	Description	Min	Max	Units
$F_{SWDTCLK}$	System watchdog timer input clock frequency	–	100	MHz

PMC System Monitor Specifications

Table 54: **PMC System Monitor Specifications**

Parameter[1]	Symbol	Conditions[2]	Min	Typ	Max	Units
V_{CCAUX_SMON} = 1.5V ±3%, V_{REFP} = 1.024V[3], V_{REFN} = 0V, T_j = –40°C to 100°C, typical values at T_j = 40°C						
ADC Accuracy[4]						
Resolution			10	–	–	Bits
Integral nonlinearity	INL		–1	–	1	LSBs
Differential nonlinearity	DNL	No missing codes, guaranteed monotonic	–1	–	1	LSBs
Offset error		Calibrated	–2	–	2	LSBs
Gain error		Calibrated	–0.4	–	0.4	%
Sample rate				0.25		MS/s
RMS code noise		External 1.024V reference	–	–	1	LSBs
		On-chip reference	–	–	1	LSBs
Analog Inputs						
ADC input ranges (V_P–V_N)		Unipolar operation	0		1	V
		Bipolar operation	–0.5	–	0.5	V
ADC input common mode ranges		Unipolar common mode range (FS input)	0	–	0.25	V
		Bipolar common mode range (FS input)	0.5	–	0.6	V
Maximum external channel input ranges		Adjacent channels set within these ranges should not corrupt measurements on adjacent channels	–0.1	–	V_{CCAUX_SMON}	V
On-Chip Sensors						
Supply sensor error		Measurement range up to V_{CCAUX_SMON} ±3% T_j = –55°C to 125°C, internal or external reference	–1	–	1	%
System Monitor Reference[5]						
External reference	V_{REFP}	Externally supplied reference voltage	0.973	1.024	1.075	V
On-chip reference		Tie V_{REFP} to AGND, T_j = –40°C to 125°C	1.019	1.024	1.029	V

Notes:

1. For more information, see the *Versal ACAP System Monitor Architecture Manual* (AM006).
2. All the reference voltages required by the ACAP cannot sleep.
3. All the accuracy specs are at V_{REFP} = 1.024V (precisely). Variation in V_{REFP} will cause a proportional gain error which should be added to see the true accuracy. The temperature range is in Kelvin so the gain error is proportional.
4. Gross offset and gain errors are removed by automatic calibration. The specification quotes the net error.
5. Any variation in the reference voltage from the nominal V_{REFP} = 1.024V and V_{REFN} = 0V will result in a deviation from the ideal transfer function. This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric-type applications allowing the reference to vary by ±5% is permitted. On-chip reference variation is ±0.5%.

Network on Chip Switching Characteristics

Table 55: **Network on Chip Switching Characteristics**

Symbol	Description	Performance as a Function of Speed Grade and Operating Voltage (V_{CC_SOC})						Units
		0.88V (H)		0.80V (M)		0.80V (L)[1]		
		-3	-2	-2	-1	-2	-1	
F_{MAX}	Network on Chip (NoC) clock maximum frequency	1080	1080	1000	960	1000	960	MHz
F_{MAX_NMU}	NoC master unit clock maximum frequency	540	540	500	480	500	480	MHz

Notes:

1. The NoC is powered by the V_{CC_SOC} supply that operates at 0.80V in low (L) voltage operation, see Table 4.

Programmable Logic Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in the Versal Prime devices. These values are subject to the same guidelines as the AC Switching Characteristics section.

In each of the following performance tables, the I/O bank type is either XPIO or HDIO.

Table 56: **I/O Logic Performance**

Description	Performance as a Function of Speed Grade and Operating Voltage (V_{CCINT})												Units
	0.88V (H)				0.80V (M)				0.70V (L)				
	-3		-2		-2		-1		-2		-1		
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
TX DDR	0	250	0	250	0	250	0	250	0	200	0	200	Mb/s
TX SDR	0	125	0	125	0	125	0	125	0	100	0	100	Mb/s
RX DDR	0	250	0	250	0	250	0	250	0	200	0	200	Mb/s
RX SDR	0	125	0	125	0	125	0	125	0	100	0	100	Mb/s

Table 57: **XPHY I/O Performance**

Description[1, 2]	Data Width	Performance as a Function of Speed Grade and Operating Voltage (V_{CCINT})												Units
		0.88V (H)				0.80V (M)				0.70V (L)				
		-3		-2		-2		-1		-2		-1		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
TX DDR	8	200	1800	200	1800	200	1800	200	1800	200	1800	200	1800	Mb/s
	4	200	1600	200	1600	200	1468	200	1468	200	1332[3]	200	1332[3]	Mb/s
	2	200	800	200	800	200	734	200	734	200	666[4]	200	666[4]	Mb/s
RX DDR[5]	8	200	1800	200	1800	200	1800	200	1800	200	1800	200	1800	Mb/s
	4	200	1600	200	1600	200	1468	200	1468	200	1332[3]	200	1332[3]	Mb/s
	2	200	800	200	800	200	734	200	734	200	666[4]	200	666[4]	Mb/s

Notes:

1. XPHY I/O is supported through the Advanced I/O Wizard available with the Vivado Design Suite. The performance values assume a source-synchronous interface.
2. Package skews are not included and should be removed through PCB routing.
3. For multi-bank interfaces, the performance is specified at 1066.5 Mb/s.
4. For multi-bank interfaces, the performance is specified at 533.25 Mb/s.
5. SDR specifications are a subset of the DDR specifications.

Table 58: **MIPI D-PHY Performance**

Description	I/O Bank Type	Performance as a Function of Speed Grade and Operating Voltage (V_{CCINT})						Units
		0.88V (H)		0.80V (M)		0.70V (L)		
		-3	-2	-2	-1	-2	-1	
MIPI D-PHY transmitter or receiver	XP	3200	3200	3200	3200	3200	3200	Mb/s

Table 59: **Maximum Physical Interface (PHY) Rate for Soft Memory Interface Controller**

Memory Standard	DRAM Type	DIMM Slots	XPIO Bank Performance [1]	Performance as a Function of Speed Grade and Operating Voltage (V_{CCINT})						Units
				0.88V (H)		0.80V (M)		0.70V (L)		
				-3	-2	-2	-1	-2	-1	
DDR4	Single rank component		All	3200	3200	2933	2667	2667	2133	Mb/s
	1 rank RDIMM, DIMM[2]	1	All	3200	3200	2933	2667	2133	2133	Mb/s
	2 rank RDIMM, LRDIMM, DIMM[2]	1	All	2933	2933	2667	2667	2133	2133	Mb/s
	4 rank LRDIMM	1	All	2667	2667	2400	2400	2133	2133	Mb/s
	1 rank RDIMM	2	All	2667	2667	2400	2400	2133	2133	Mb/s
	1 rank DIMM[2]	2	All	2400	2400	2133	2133	1867	1867	Mb/s
	2 rank LRDIMM	2	All	2667	2667	2400	2400	2133	2133	Mb/s
	2 rank RDIMM	2	All	2133	2133	2133	2133	2133	2133	Mb/s
	2 rank DIMM[2]	2	All	1866	1866	1866	1866	1866	1866	Mb/s
RLDRAM3			All	1066	1066	1066	1066	1066	1066	MHz
QDRIV	HP		All	933	933	933	933	933	933	MHz
	XP[3]		All	1066	1066	1066	1066	1066	1066	MHz

Notes:

1. The Versal device package pinout files specify XPIO bank performance (XPIOperf). See ASCII package files information in the *Versal ACAP Packaging and Pinouts Architecture Manual* (AM013).
2. Dual in-line memory module (DIMM) includes SODIMM and UDIMM
3. The QDRIV XP performance values are for 18-bit interfaces, for 36-bit interfaces the maximum performance is 933 MHz.

Programmable Logic Switching Characteristics

Block RAM Switching Characteristics

Table 60: **Block RAM Switching Characteristics**

Symbol	Description	Performance as a Function of Speed Grade and Operating Voltage (V_{CC_RAM})						Units
		0.88V (H)		0.80V (M)		0.80V (L)[1]		
		-3	-2	-2	-1	-2	-1	
Maximum Frequency								
$F_{MAX\_WF\_NC}$	Block RAM (WRITE_FIRST and NO_CHANGE modes)	1000	1000	850	800	650	615	MHz
F_{MAX_RF}	Block RAM (READ_FIRST mode)	850	850	725	675	550	510	MHz
Block RAM Clock-to-Out Delays								
T_{RCKO_DO}	Clock CLK to DOUT output (without output register)	0.797	0.797	0.901	0.967	1.141	1.233	ns, Max
$T_{RCKO\_DO\_REG}$	Clock CLK to DOUT output (with output register)	0.234	0.234	0.262	0.280	0.333	0.362	ns, Max

Notes:

1. The block RAM is power by the V_{CC_RAM} supply that operates at 0.80V in low (L) voltage operation, see Table 4.

UltraRAM Switching Characteristics

Table 61: **UltraRAM Switching Characteristics**

Symbol	Description	Performance as a Function of Speed Grade and Operating Voltage (V_{CC_RAM})						Units
		0.88V (H)		0.80V (M)		0.80V (L)[1]		
		-3	-2	-2	-1	-2	-1	
Maximum Frequency								
F_{MAX}	UltraRAM maximum frequency with output register	738	738	664	645	530	500	MHz

Notes:

1. The UltraRAM is power by the V_{CC_RAM} supply that operates at 0.80V in low (L) voltage operation, see Table 4.

Accelerator RAM Switching Characteristics

The *Versal Architecture and Product Data Sheet: Overview* (DS950) lists the Versal Prime devices that include the accelerator RAM (XRAM).

Table 62: **Accelerator RAM Switching Characteristics**

Symbol	Description	Performance as a Function of Speed Grade and Operating Voltage (V_{CC_PSLP})						Units
		0.88V (H)		0.80V (M)		0.80V (L)		
		-3	-2	-2	-1	-2	-1	
F_{MAX_XRAM}	Maximum accelerator RAM (XRAM) clock frequency	750	725	625	600	500	450[1]	MHz
F_{PL_XRAM}	Maximum accelerator RAM PL interface frequency	390	375	325	300	270	250[2]	MHz

Notes:

1. The -1LLI and -1LSI low-power devices support an overdrive voltage where the maximum clock frequency is 800 MHz when V_{CC_PSLP} = 0.88V.
2. The -1LLI and -1LSI low-power devices support an overdrive voltage where the maximum clock frequency is 350 MHz when V_{CC_PSLP} = 0.88V.

Input/Output Delay Switching Characteristics

Table 63: **Input/Output Delay Switching Characteristics**

Symbol	Description	Performance as a Function of Speed Grade and Operating Voltage (V_{CCINT})						Units
		0.88V (H)		0.80V (M)		0.70V (L)		
		-3	-2	-2	-1	-2	-1	
$T_{IDELAY\_RESOLUTION}$/ $T_{ODELAY\_RESOLUTION}$	XPHY IDELAY/ODELAY delay tap resolution	1.22 to 4.00						ps
T_{IDELAY_ERROR}/ T_{ODELAY_ERROR}	XPHY calibrated delay line error (DELAY_VALUE) (REFCLK_FREQUENCY = 500 to 1800 MHz)[1]	–10 to +10						Delay Taps
$T_{IOL\_IDELAY\_RESOLUTION}$/ $T_{IOL\_ODELAY\_RESOLUTION}$	IOL IDELAY/ODELAY uncalibrated delay tap resolution for both HD and XP IOL resources	60 to 173						ps

Notes:

1. For REFCLK_FREQUENCY < 500 MHz, BISC calibration of the DELAY_VALUE_<0-5> is not guaranteed. Use the $T_{IDELAY\_RESOLUTION}$/ $T_{ODELAY\_RESOLUTION}$ for delay calculations. Refer to the *Versal ACAP SelectIO Resources Architecture Manual* (AM010). IDELAY is used for alignment and ALIGN_DELAY effects the programmed DELAY_VALUE programming.

DSP58 Switching Characteristics

Table 64: **DSP58 Switching Characteristics**

Symbol	Description	Performance as a Function of Speed Grade and Operating Voltage (V_{CCINT})						Units
		0.88V (H)		0.80V (M)		0.70V (L)		
		-3	-2	-2	-1	-2	-1	
Fixed Point Arithmetic								
$F_{MAX\_INT\_MULT}$	27 × 24 two's complement multiply	1150	1150	1070	984	760	680	MHz
F_{MAX_SIMD}	Single-instruction multiple-data (SIMD) arithmetic	1150	1150	1070	984	760	680	MHz
Complex Arithmetic								
$F_{MAX\_COMPLEX\_MULT}$	18 × 18 two's complement complex multiply	984	984	909	850	646	578	MHz
Floating Point Arithmetic								
F_{MAX_FP}	Floating-point operations	805	805	750	700	532	476	MHz

Clock Buffers and Networks

Table 65: **Clock Buffers Switching Characteristics (including Multi-clock Buffers)**

Symbol	Description	Performance as a Function of Speed Grade and Operating Voltage (V_{CCINT})						Units
		0.88V (H)		0.80V (M)		0.70V (L)		
		-3	-2	-2	-1	-2	-1	
Global Clock Switching Characteristics (Including BUFGCTRL and MBUFGCTRL)								
F_{MAX}	Maximum frequency of a global clock tree (BUFG)	1150	1150	1070	984	800	680	MHz
Global Clock Buffer with Input Divide Capability (BUFGCE_DIV and MBUFGCE_DIV)								
F_{MAX}	Maximum frequency of a global clock buffer with input divide capability	1150	1150	1070	984	800	680	MHz
Global Clock Buffer with Clock Enable (BUFGCE)								
F_{MAX}	Maximum frequency of a global clock buffer with clock enable	1150	1150	1070	984	800	680	MHz
Global Clock Buffer with for the Processing System (BUFG_PS and MBUFG_PS)								
F_{MAX}	Maximum frequency of a global clock buffer with clock enable	1150	1150	1070	984	800	680	MHz
GTY or GTM Clock Buffer with Clock Enable and Clock Input Divide Capability (BUFG_GT and MBUFG_GT)								
F_{MAX}	Maximum frequency of a serial transceiver clock buffer with clock enable and clock input divide capability	1150	1150	1070	984	1000	680	MHz

MMCM Switching Characteristics

Table 66: **MMCM Specification**

Symbol	Description	Performance as a Function of Speed Grade and Operating Voltage (V_{CC_RAM})						Units
		0.88V (H)		0.80V (M)		0.80V (L)[1]		
		-3	-2	-2	-1	-2	-1	
F_{INMAX_MMCM}	Maximum input clock frequency[2]	1150	1150	1070	984	800	680	MHz
F_{INMIN_MMCM}	Minimum input clock frequency	10	10	10	10	10	10	MHz
$F_{INJITTER\_MMCM}$	Maximum input clock period jitter[3]	< 20% of clock input period or 1 ns Max						
F_{INDUTY_MMCM}	Input duty cycle range: 10–49 MHz	25–75						%
	Input duty cycle range: 50–199 MHz	30–70						%
	Input duty cycle range: 200–399 MHz	35–65						%
	Input duty cycle range: 400–499 MHz	40–60						%
	Input duty cycle range: >500 MHz	45–55						%
$F_{MAX\_PSCLK\_MMCM}$	Maximum dynamic phase shift clock frequency	550	500	500	450	500	450	MHz
$F_{MIN\_PSCLK\_MMCM}$	Minimum dynamic phase shift clock frequency	0.01	0.01	0.01	0.01	0.01	0.01	MHz
F_{VCOMAX_MMCM}	Maximum MMCM VCO frequency	4320	4320	4320	4320	4320	4320	MHz
F_{VCOMIN_MMCM}	Minimum MMCM VCO frequency	2160	2160	2160	2160	2160	2160	MHz
$F_{BANDWIDTH\_MMCM}$	Low MMCM bandwidth at typical[4]	1.00	1.00	1.00	1.00	1.00	1.00	MHz
	High MMCM bandwidth at typical[4]	4.00	4.00	4.00	4.00	4.00	4.00	MHz
$T_{STATPHAOFFSET\_MMCM}$	Static phase offset of the MMCM outputs[5]	0.12	0.12	0.12	0.12	0.12	0.12	ns
$T_{OUTJITTER\_MMCM}$	MMCM output jitter	Note 6						
$T_{OUTDUTY\_MMCM}$	MMCM output clock duty cycle precision[7]	0.165	0.20	0.20	0.20	0.20	0.20	ns
$T_{LOCKMAX\_MMCM}$	MMCM maximum lock time (non deskew mode)	100	100	100	100	100	100	µs
$T_{LOCKDESKEWMAX\_MMCM}$	MMCM maximum lock time in deskew mode	Note 8						
F_{OUTMAX_MMCM}	MMCM maximum output clock frequency[2]	1150	1150	1070	984	800	680	MHz
F_{OUTMIN_MMCM}	MMCM minimum output clock frequency	5	5	5	5	5	5	MHz
$T_{EXTFDVAR\_MMCM}$	External clock feedback variation	< 20% of clock input period or 1 ns Max						
$T_{PWRDWNMINPULSE\_MMCM}$	Minimum power-down pulse width	5.00	5.00	5.00	5.00	5.00	5.00	ns
F_{PFDMAX_MMCM}	Maximum frequency at the phase frequency detector with bandwidth set to High or optimized	550	500	500	450	500	450	MHz
	Maximum frequency at the phase frequency detector with bandwidth set to Low	550	500	500	450	500	450	MHz
F_{PFDMIN_MMCM}	Minimum frequency at the phase frequency detector	10	10	10	10	10	10	MHz
$T_{FBDELAY\_MMCM}$	Maximum delay in the feedback path[9]	3 ns Max or one clock cycle						

Table 66: **MMCM Specification** *(cont'd)*

Symbol	Description	Performance as a Function of Speed Grade and Operating Voltage (V_{CC_RAM})						Units
		0.88V (H)		0.80V (M)		0.80V (L)[1]		
		-3	-2	-2	-1	-2	-1	
$T_{DESKEWTAPDELAY\_MMCM}$	Nominal tap-delay of the programmable delay in the PD based deskew scheme	Note 10						

Notes:

1. The MMCM is powered by the V_{CC_RAM} supply that operates at 0.80V in low (L) voltage operation, see Table 4.
2. The maximum input and output clock frequencies are limited by the global clock buffers. See Table 65.
3. CLKIN jitter also applies to CLKIN_DESKEW and CLKFB_DESKEW in digital compensation. CLKFBIN applies only to analog compensation. This parameter is in regards to the functionality of the MMCM. Input jitter above ~1 MHz is reduced by the filtering properties of the MMCM. The magnitude of the reduction is found in the Vivado® timing report.
4. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
5. The static offset is measured between any MMCM outputs with identical phase.
6. Values for this parameter are available in the Vivado timing summary as part of the clock uncertainty equation.
7. Includes global clock buffer.
8. The maximum lock time in deskew mode is given by the following formula: Lock time in deskew mode in ms = (0.208 x (VCO_frequency in MHz) / (CLKIN_DESKEW_frequency in MHz)^2) + 0.1.
9. The parameter only applies to analog compensation.
10. The value for this parameter is included in compensation delay calculations.

DPLL Switching Characteristics

Table 67: **DPLL Specification**

Symbol	Description[1]	Performance as a Function of Speed Grade and Operating Voltage (V_{CC_RAM})[2]						Units
		0.88V (H)		0.80V (M)		0.80V (L)[2]		
		-3	-2	-2	-1	-2	-1	
F_{INMAX_DPLL}	Maximum input clock frequency[3]	1150	1150	1070	984	800	680	MHz
F_{INMIN_DPLL}	Minimum input clock frequency	50	50	50	50	50	50	MHz
$F_{INJITTER\_DPLL}$	Maximum input clock jitter[4]	< 20% of clock input period or 1 ns Max						
F_{INDUTY_DPLL}	Input duty cycle range: 50–399 MHz	35–65						%
	Input duty cycle range: 400–499 MHz	40–60						%
	Input duty cycle range: >500 MHz	45–55						%
$F_{PSCLKMAX\_DPLL}$	Maximum dynamic phase shift clock frequency	550	500	500	450	500	450	MHz
$F_{PSCLKMIN\_DPLL}$	Minimum dynamic phase shift clock frequency	0.01	0.01	0.01	0.01	0.01	0.01	MHz
F_{DCOMAX_DPLL}	Maximum DPLL DCO frequency	4000	4000	4000	4000	4000	4000	MHz
F_{DCOMIN_DPLL}	Minimum DPLL DCO frequency	2000	2000	2000	2000	2000	2000	MHz
$F_{BANDWIDTH\_DPLL}$	DPLL bandwidth at typical[5]	1.00	1.00	1.00	1.00	1.00	1.00	MHz
$T_{STATPHAOFFSET\_DPLL}$	Static phase offset of the DPLL outputs[6]	0.12	0.12	0.12	0.12	0.12	0.12	ns
$T_{OUTJITTER\_DPLL}$	DPLL output jitter	Note 7						
$T_{OUTDUTY\_DPLL}$	DPLL output clock duty cycle precision[8]	0.165	0.20	0.20	0.20	0.20	0.20	ns
$T_{LOCKMAX\_DPLL}$	DPLL maximum lock time (non-deskew mode)	Note 9						
$T_{LOCKDESKEWMAX\_DPLL}$	DPLL maximum lock time in deskew mode[10]	Note 11						
F_{OUTMAX_DPLL}	DPLL maximum output clock frequency[3]	1150	1150	1070	984	800	680	MHz
F_{OUTMIN_DPLL}	DPLL minimum output clock frequency	5	5	5	5	5	5	MHz
$T_{PWRDWNMINPULSE\_DPLL}$	Minimum power-down pulse width	5.00	5.00	5.00	5.00	5.00	5.00	ns
F_{TDCMAX_DPLL}	Maximum frequency at the time to digital converter	200	200	200	200	200	200	MHz
F_{TDCMIN_DPLL}	Minimum frequency at the time to digital converter	50	50	50	50	50	50	MHz

Table 67: **DPLL Specification** *(cont'd)*

Symbol	Description[1]	Performance as a Function of Speed Grade and Operating Voltage (V_{CC_RAM})[2]						Units
		0.88V (H)		0.80V (M)		0.80V (L)[2]		
		-3	-2	-2	-1	-2	-1	
$T_{DESKEWTAPDELAY\_DPLL}$	Nominal tap-delay of the programmable delay in the PD based deskew scheme[10]	Note 12						

Notes:

1. In the VM1802 device, the DPLLs (DPLL_X3Y7 and DPLL_X12Y7 sites) at the HDIO banks are not supported. Thus, DPLL ZHOLD mode for HDIO is not supported in these devices.
2. The DPLLs are powered by the V_{CC_RAM} supply, except for the DPLLs at HDIO banks are powered by the V_{CCINT} supply. The V_{CC_RAM} supply operates at 0.80V in low (L) voltage operation, see Table 4.
3. The maximum input and output clock frequencies are limited by the global clock buffers. See Table 65.
4. CLKIN jitter also applies to CLKIN_DESKEW and CLKFB_DESKEW in digital compensation. CLKFBIN applies only to analog compensation. This parameter is in regards to the functionality of the DPLL. Input jitter above ~1 MHz is reduced by the filtering properties of the DPLL. The magnitude of the reduction is found in the Vivado® timing report.
5. The DPLL does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
6. The static offset is measured between any DPLL outputs with identical phase.
7. Values for this parameter are available in the Vivado timing summary as part of the clock uncertainty equation.
8. Includes global clock buffer.
9. The maximum lock time in non-deskew mode is given by the given formula: Lock time in non-deskew mode in ms = 153.6 × DIVCLK_DIVIDE / (CLKIN_FREQUENCY in MHz).
10. In the VM1802 device, the DPLL deskew functions are not supported.
11. The maximum lock time in deskew mode is given by the following formula: Lock time in deskew mode in ms = (0.208 x (VCO_frequency in MHz) / (CLKIN_DESKEW_frequency in MHz)^2) + (maximum lock time in non-deskew mode in ms from Note 9).
12. The value for this parameter is included in compensation delay calculations.

XPLL Switching Characteristics

Table 68: **XPLL Specification**

Symbol	Description	Performance as a Function of Speed Grade and Operating Voltage (V_{CC_IO})						Units
		0.88V (H)		0.80V (M)		0.80V (L)[1]		
		-3	-2	-2	-1	-2	-1	
F_{INMAX_XPLL}	Maximum input clock frequency[2]	1150	1150	1070	984	800	680	MHz
F_{INMIN_XPLL}	Minimum input clock frequency	100	100	100	100	100	100	MHz
$F_{INJITTER\_XPLL}$	Maximum input clock jitter[3]	< 20% of clock input period or 1 ns Max						
F_{INDUTY_XPLL}	Allowable input duty cycle: 100–399 MHz	35–65						%
	Allowable input duty cycle: 400–499 MHz	40–60						%
	Allowable input duty cycle: >500 MHz	45–55						%
$F_{PSCLKMAX\_XPLL}$	Maximum dynamic phase shift clock frequency	300	300	300	300	300	300	MHz
$F_{PSCLKMIN\_XPLL}$	Minimum dynamic phase shift clock frequency	0.01	0.01	0.01	0.01	0.01	0.01	MHz
F_{VCOMAX_XPLL}	Maximum XPLL VCO frequency	4320	4320	4320	4320	4320	4320	MHz
F_{VCOMIN_XPLL}	Minimum XPLL VCO frequency	2160	2160	2160	2160	2160	2160	MHz
$F_{BANDWIDTH\_XPLL}$	XPLL bandwidth at typical[4]	14.00	14.00	14.00	14.00	14.00	14.00	MHz
$T_{STATPHAOFFSET\_XPLL}$	Static phase offset of the XPLL outputs[5]	0.12	0.12	0.12	0.12	0.12	0.12	ns
$T_{OUTJITTER\_XPLL}$	XPLL output jitter	Note 6						
$T_{OUTDUTY\_XPLL}$	XPLL CLKOUT0, CLKOUT1, CLKOUT2, CLKOUT3 duty-cycle precision[7]	0.125	0.15	0.15	0.15	0.15	0.15	ns
$T_{LOCKMAX\_XPLL}$	XPLL maximum lock time (in non-deskew mode)	100	100	100	100	100	100	µs
$T_{LOCKDESKEWMAX\_XPLL}$	XPLL maximum lock time in deskew mode	Note 8						
F_{OUTMAX_XPLL}	XPLL maximum output frequency at CLKOUT0, CLKOUT1, CLKOUT2, CLKOUT3[2,9]	1150	1150	1070	984	800	680	MHz
	XPLL maximum output frequency at CLKOUTPHY	4266	4266	3933	3733	3933	3733	MHz
F_{OUTMIN_XPLL}	XPLL minimum output frequency at CLKOUT0, CLKOUT1, CLKOUT2, CLKOUT3	16.875	16.875	16.875	16.875	16.875	16.875	MHz
	XPLL minimum output frequency at CLKOUTPHY	200	200	200	200	200	200	MHz
$T_{PWRDWNMINPULSE\_XPLL}$	Minimum power-down pulse width	5.00	5.00	5.00	5.00	5.00	5.00	ns
F_{PFDMAX_XPLL}	Maximum frequency at the phase frequency detector with bandwidth set to High optimized	667.5	667.5	667.5	667.5	667.5	667.5	MHz
F_{PFDMIN_XPLL}	Minimum frequency at the phase frequency detector	100	100	100	100	100	100	MHz

Table 68: **XPLL Specification** *(cont'd)*

Symbol	Description	Performance as a Function of Speed Grade and Operating Voltage (V_{CC_IO})						Units
		0.88V (H)		0.80V (M)		0.80V (L)[1]		
		-3	-2	-2	-1	-2	-1	
$T_{DESKEWTAPEDELAY\_XPLL}$	Nominal tap-delay of the programmable delay in the PD based deskew scheme	Note 10						

Notes:

1. The XPLL is powered by the V_{CC_IO} supply that operates at 0.80V in low (L) voltage operation, see Table 4.
2. The maximum input clock frequency and output clock frequency at CLKOUT0, CLKOUT1, CLKOUT2, and CLKOUT3 are limited by the global clock buffers. See Table 65.
3. CLKIN jitter also applies to CLKIN_DESKEW and CLKFB_DESKEW in digital compensation. CLKFBIN applies only to analog compensation. This parameter is in regards to the functionality of the XPLL. Input jitter above ~1 MHz is reduced by the filtering properties of the XPLL. The magnitude of the reduction is found in the Vivado® timing report.
4. The XPLL does not filter typical spread-spectrum input clocks because they are usually far below the loop filter frequencies.
5. The static offset is measured between any XPLL outputs with identical phase.
6. Values for this parameter are available in the Vivado timing summary as part of the clock uncertainty equation.
7. Includes global clock buffer.
8. The maximum lock time in deskew mode is given by the following formula: Lock time in deskew mode in µs = (208 x (VCO_frequency in MHz) / (CLKIN_DESKEW_frequency in MHz)^2 + 100.
9. XPLL CLKOUTs F_{MAX} is increased in the -1L/-2L speed grade when it directly drives the memory controller at a 1/4 x DDR bit rate. Refer to the DDR bit rate in Table 72.
10. The value for this parameter is included in compensation delay calculations.

Device Pin-to-Pin Output Parameter Guidelines

The pin-to-pin numbers in the following tables are based on the clock root placement in the center of the device. The actual pin-to-pin values will vary if the root placement selected is different. Consult the Vivado Design Suite timing report for the actual pin-to-pin values.

Table 69: **Global Clock Input to Output Delay With MMCM (Internal Mode)**

Symbol	Description[1, 2]	Device	Performance as a Function of Speed Grade and Operating Voltage (V_{CCINT})						Units
			0.88V (H)		0.80V (M)		0.70V (L)		
			-3	-2	-2	-1	-2	-1	
SSTL15 Global Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *with* MMCM									
$T_{ICKOFMMCM}$	Global clock input and output flip-flop *with* MMCM	XCVM1102							ns
		XCVM1302							ns
		XCVM1402							ns
		XCVM1502							ns
		XCVM1802	7.45	7.45	8.13	8.63	8.79	9.43	ns
		XCVM2502							ns
		XCVM2602							ns
		XCVM2902							ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

Device Pin-to-Pin Input Parameter Guidelines

The pin-to-pin numbers in the following tables are based on the clock root placement in the center of the device. The actual pin-to-pin values will vary if the root placement selected is different. Consult the Vivado Design Suite timing report for the actual pin-to-pin values.

Table 70: **Global Clock Input Setup and Hold With MMCM (Internal Mode)**

Symbol	Description		Device	Performance as a Function of Speed Grade and Operating Voltage (V_{CCINT})						Units
				0.88V (H)		0.80V (M)		0.70V (L)		
				-3	-2	-2	-1	-2	-1	
Input Setup and Hold Time Relative to Global Clock Input Signal using SSTL15 Standard.[1, 2, 3]										
T_{SUMMCM_VM1102}	Global clock input and input flip-flop (or latch) with MMCM	Setup	XCVM1102							ns
T_{HMMCM_VM1102}		Hold								ns
T_{SUMMCM_VM1302}		Setup	XCVM1302							ns
T_{HMMCM_VM1302}		Hold								ns
T_{SUMMCM_VM1402}		Setup	XCVM1402							ns
T_{HMMCM_VM1402}		Hold								ns
T_{SUMMCM_VM1502}		Setup	XCVM1502							ns
T_{HMMCM_VM1502}		Hold								ns
T_{SUMMCM_VM1802}		Setup	XCVM1802	–1.09	–1.09	–1.00	–1.00	–1.02	–1.02	ns
T_{HMMCM_VM1802}		Hold		4.14	4.14	5.00	5.00	4.82	5.02	ns
T_{SUMMCM_VM2502}		Setup	XCVM2502							ns
T_{HMMCM_VM2502}		Hold								ns
T_{SUMMCM_VM2602}		Setup	XCVM2602							ns
T_{HMMCM_VM2602}		Hold								ns
T_{SUMMCM_VM2902}		Setup	XCVM2902							ns
T_{HMMCM_VM2902}		Hold								ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, slowest temperature, and slowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, fastest temperature, and fastest voltage.
2. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net.
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Package Parameter Guidelines

The parameters in this section provide the necessary values for calculating timing budgets for clock transmitter and receiver data-valid windows.

Table 71: **Package Skew**

Symbol	Description	Device	Package	Value	Units
PKGSKEW	Package Skew[1, 2]	XCVM1102	SFVBB625		ps
			VFVB1024		ps
		XCVM1302	VFVB1024		ps
			VFVB1369		ps
			VFVF1369		ps
			VFVA1760		ps
			VSVD1760		ps
		XCVM1402	VFVB1024		ps
			VFVB1369		ps
			VFVF1369		ps
			VFVA1760		ps
			VSVD1760		ps
		XCVM1502	VFVB1369		ps
			VFVC1760		ps
		XCVM1802	VFVC1760	214	ps
			VSVD1760	211	ps
			VSVA2197	111	ps
		XCVM2502	VSVA2197		ps
		XCVM2602	VFVA1760		ps
			VFVC1760		ps
		XCVM2902	VFVC1760		ps

Notes:

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from die pad to ball.
2. Package delay information is available for these device/package combinations. This information can be used to deskew the package.

Memory Interface Controller

The following table provides the maximum data rates for applicable memory standards using the Versal Prime device memory PHY. Refer to *Versal ACAP Programmable Network on Chip and Integrated Memory Controller LogiCORE IP Product Guide* (PG313) for the complete list of memory interface standards supported and detailed specifications. The final performance of the memory interface is determined through a complete design implemented in the Vivado Design Suite, following guidelines in the *Versal ACAP PCB Design User Guide* (UG863), electrical analysis, and characterization of the system.

Table 72: **Maximum Physical Interface (PHY) Rate for Integrated Memory Interface Controller**

Memory Standard	DRAM Type	DIMM Slots	XPIO Bank Performance [1]	Performance as a Function of Speed Grade and Operating Voltage (V_{CC_SOC})						Units
				0.88V (H)		0.80V (M)		0.80V (L)[2]		
				-3	-2	-2	-1	-2	-1	
DDR4	Single rank component[3]		All	3200	3200	3200	3200	3200	3200	Mb/s
	1 rank DIMM[4], LRDIMM[5]	1	All	3200	3200	3200	3200	3200	3200	Mb/s
	2 rank DIMM[4]	1	All	2933	2933	2933	2933	2933	2933	Mb/s
	1 rank RDIMM, 2 rank LRDIMM	2	All	2667	2667	2667	2667	2667	2667	Mb/s
	2 rank RDIMM	2	All	2133	2133	2133	2133	2133	2133	Mb/s
LPDDR4 LPDDR4X	Single rank component[6]		High, Medium	4266	4266	3933	3733	3933	3733	Mb/s
	Dual rank component		High, Medium	3733	3733	3733	3733	3733	3733	Mb/s
	Single rank component		All	3200	3200	3200	3200	3200	3200	Mb/s
	Dual rank component		All	2933	2933	2933	2933	2933	2933	Mb/s

Notes:

1. The Versal ACAP package pinout files specify XPIO bank performance (XPIOperf). See the ASCII package files information in the *Versal ACAP Packaging and Pinouts Architecture Manual* (AM013).
2. The integrated DDRMC is powered by the V_{CC_SOC} supply that operates at 0.80V in low (L) voltage operation, see Table 4.
3. For DDR4 DDP deep components, the maximum data rate is 2933 Mb/s for five or less DDP devices across all speed grades and temperature grades. For six or more DDP deep devices, the maximum data rate is 2133 Mb/s across all speed grades and temperature grades. For DDR4 DDP wide components, use single rank component data rates.
4. Dual in-line memory module (DIMM) includes RDIMM, SODIMM, and UDIMM.
5. Includes 1 and 2 rank LRDIMM.
6. The LPDDR4/4X pin efficient component interface is limited to 3733 Mb/s. See *Versal ACAP Programmable Network on Chip and Integrated Memory Controller LogiCORE IP Product Guide* (PG313) for pin efficient component interfaces.

GTY and GTYP Transceiver Specifications

The *Versal Architecture and Product Data Sheet: Overview* (DS950) lists the Versal Prime devices that include the GTY and GTYP transceivers.

GTY and GTYP Transceiver DC Input and Output Levels

Table 73 summarizes the DC specifications of the GTY and GTYP transceivers in Versal Prime devices. Consult the *Versal ACAP GTY and GTYP Transceivers Architecture Manual* (AM002) for further details.

Table 73: **GTY and GTYP Transceiver DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV_{PPIN}	Differential peak-to-peak input voltage (external AC coupled)	>10.3125 Gb/s	150	–	1250	mV
		6.6 Gb/s to 10.3125 Gb/s	150	–	1250	mV
		≤ 6.6 Gb/s	150	–	2000	mV
V_{IN}	Single-ended input voltage. Voltage measured at the pin referenced to GND.	DC coupled V_{GTY_AVTT} = 1.2V	–200	–	V_{GTY_AVTT}	mV
V_{CMIN}	Common mode input voltage	DC coupled V_{GTY_AVTT} = 1.2V	–	2/3 V_{GTY_AVTT}	–	mV
D_{VPPOUT}	Differential peak-to-peak output voltage[1]	Transmitter output swing is set to 11111	800	–	–	mV
$V_{CMOUTDC}$	Common mode output voltage: DC coupled (equation based)	When remote RX is terminated to GND	$V_{GTY\_AVTT}/2 - D_{VPPOUT}/4$			mV
		When remote RX termination is floating	$V_{GTY\_AVTT} - D_{VPPOUT}/2$			mV
		When remote RX is terminated to V_{RX_TERM}[2]	$V_{GTY\_AVTT} - \frac{D_{VPPOUT}}{4} - \left(\frac{V_{GTY\_AVTT} - V_{RX\_TERM}}{2}\right)$			mV
$V_{CMOUTAC}$	Common mode output voltage: AC coupled	Equation based	$V_{GTY\_AVTT} - D_{VPPOUT}/2$			mV
R_{IN}	Differential input resistance		–	100	–	Ω
R_{OUT}	Differential output resistance		–	100	–	Ω
T_{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew		–	–	10	ps
C_{EXT}	Recommended external AC coupling capacitor[3]		–	100	–	nF

Notes:

1. The output swing and pre-emphasis levels are programmable using the GTY and GTYP transceiver attributes discussed in the *Versal ACAP GTY and GTYP Transceivers Architecture Manual* (AM002) and can result in values lower than reported in this table.
2. V_{RX_TERM} is the remote RX termination voltage.
3. Other values can be used as appropriate to conform to specific protocols and standards.

Figure 1: **Single-Ended Peak-to-Peak Voltage**

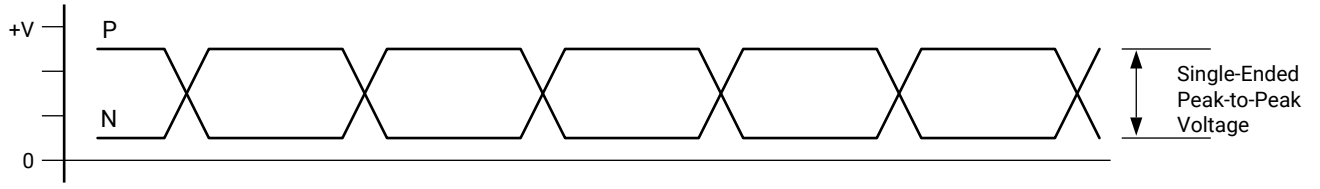

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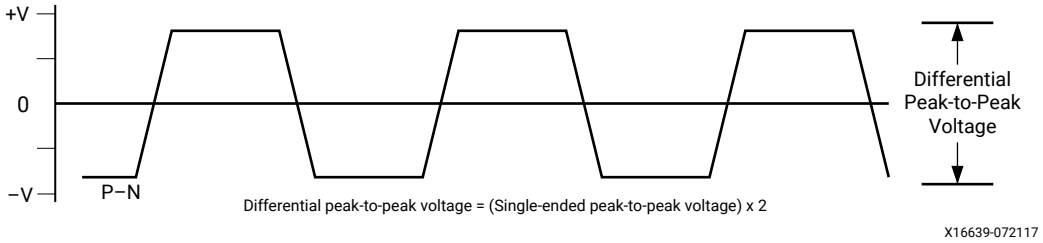
Figure 2: **Differential Peak-to-Peak Voltage**



The following tables summarize the DC specifications of the clock input/output levels of the GTY and GTYP transceivers in Versal Prime devices. Consult the *Versal ACAP GTY and GTYP Transceivers Architecture Manual* (AM002) for further details.

Table 74: **GTY and GTYP Transceiver Clock DC Input Level Specification**

Symbol	DC Parameter	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage	250	–	2000	mV
R_{IN}	Differential input resistance	–	100	–	Ω
C_{EXT}	Required external AC coupling capacitor	–	10	–	nF

Table 75: **GTY and GTYP Transceiver Clock Output Level Specification**

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{OL}	Output Low voltage for P and N	R_T = 100Ω across P and N signals	–100	–	100	mV
V_{OH}	Output High voltage for P and N	R_T = 100Ω across P and N signals	250	–	450	mV
V_{DDOUT}	Differential output voltage (P–N), P = High (N–P), N = High	R_T = 100Ω across P and N signals	300	–	430	mV
V_{CMOUT}	Common mode voltage	R_T = 100Ω across P and N signals	100	–	250	mV

GTY and GTYP Transceiver Switching Characteristics

Consult the *Versal ACAP GTY and GTYP Transceivers Architecture Manual* (AM002) for further information.

GTY and GTYP Transceiver Performance

Table 76: **GTY Transceiver Performance**

Symbol	Description	Subrate Divider	Output Divider	Performance as a Function of Speed Grade and Operating Voltage (V_{CCINT})												Units
				0.88V (H)				0.80V (M)				0.70V (L)				
				-3		-2		-2		-1		-2		-1		
F_{GTYMAX}	GTY maximum line rate			32.75 (LPM) 30.5 (DFE)		28.21		28.21		26.5625		28.21		25.78125		Gb/s
F_{GTYMIN}	GTY minimum line rate			1.2		1.2		1.2		1.2		1.2		1.2		Gb/s
				Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
$F_{GTYRRANGE}$	RINGPLL line rate range[1, 2]		1	8	12.5	8	12.5	8	12.5	8	12.5	8	12.5	8	12.5	Gb/s
			2	4	8	4	8	4	8	4	8	4	8	4	8	Gb/s
			4	2	4	2	4	2	4	2	4	2	4	2	4	Gb/s
			8	1.2	2	1.2	2	1.2	2	1.2	2	1.2	2	1.2	2	Gb/s
				Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
$F_{GTYLRANGE}$	LCPLL line rate range[3]	1	1	16	32.75 (LPM) 30.5 (DFE)	16	28.21	16	28.21	16	26.5625	16	28.21	16	25.78125	Gb/s
		2		8	16.375	8	16.375	8	16.375	8	16.375	8	16.375	8	16.375	Gb/s
		1	2	8	16.375	8	14.105	8	14.105	8	13.28125	8	14.105	8	12.891	Gb/s
		2		4	8.1875	4	8.1875	4	8.1875	4	8.1875	4	8.1875	4	8.1875	Gb/s
		1	4	4	8.1875	4	7.0525	4	7.0525	4	6.640625	4	7.0525	4	6.4453125	Gb/s
		2		2	4.09375	2	4.09375	2	4.09375	2	4.09375	2	4.0938	2	4.09375	Gb/s
		1	8	2	4.09375	2	3.52625	2	3.52625	2	3.3203125	2	3.5263	2	3.2226563	Gb/s
		2		1.2	2.046875	1.2	2.046875	1.2	2.046875	1.2	1.66015625	1.2	1.7631	1.2	2.046875	Gb/s
				Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
$F_{RPLLRANGE}$	RINGPLL frequency range			4	8	4	8	4	8	4	8	4	8	4	8	GHz
$F_{LCPLLRANGE}$	LCPLL frequency range			8	16.375	8	16.375	8	16.375	8	16.375	8	16.375	8	16.375	GHz

Notes:

1. The values listed are the rounded results of the calculated equation (2 × RINGPLL_Frequency)/Subrate_Divider.
2. The highest supported line rate when using the RPLL to drive the datapath is 12.5 Gb/s.
3. The values listed are the rounded results of the calculated equation (2 × LCPLL_Frequency)/(Output_Divider × Subrate_Divider).

Table 77: **GTYP Transceiver Performance**

Symbol	Description	Subrate Divider	Output Divider	Performance as a Function of Speed Grade and Operating Voltage (V_{CCINT})												Units
				0.88V (H)				0.80V (M)				0.70V (L)				
				-3		-2		-2		-1		-2		-1		
$F_{GTYPMAX}$	GTYP maximum line rate			32.75 (LPM) 32 (DFE)		32		32		32		32		25.78125		Gb/s
$F_{GTYPMIN}$	GTYP minimum line rate			1.2		1.2		1.2		1.2		1.2		1.2		Gb/s
				Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
$F_{GTYPRRANGE}$	RINGPLL line rate range[1, 2]		1	8	12.5	8	12.5	8	12.5	8	12.5	8	12.5	8	12.5	Gb/s
			2	4	8	4	8	4	8	4	8	4	8	4	8	Gb/s
			4	2	4	2	4	2	4	2	4	2	4	2	4	Gb/s
			8	1.2	2	1.2	2	1.2	2	1.2	2	1.2	2	1.2	2	Gb/s
				Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
$F_{GTYPLRANGE}$	LCPLL line rate range[3]	1	1	16	32.75 (LPM) 32 (DFE)	16	32	16	32	16	32	16	32	16	25.78125	Gb/s
			2	8	16.375	8	16.375	8	16.375	8	16.375	8	16.375	8	16.375	Gb/s
		2	1	8	16.375	8	16.375	8	16.375	8	16.375	8	16.375	8	16.375	Gb/s
			2	4	8.1875	4	8.1875	4	8.1875	4	8.1875	4	8.1875	4	8.1875	Gb/s
		4	1	4	8.1875	4	8.1875	4	8.1875	4	8.1875	4	8.1875	4	8.1875	Gb/s
			2	2	4.09375	2	4.09375	2	4.09375	2	4.09375	2	4.09375	2	4.09375	Gb/s
		8	1	2	4.09375	2	4.09375	2	4.09375	2	4.09375	2	4.09375	2	4.09375	Gb/s
			2	1.2	2.046875	1.2	2.046875	1.2	2.046875	1.2	2.046875	1.2	2.046875	1.2	2.046875	Gb/s
				Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
$F_{RPLLRANGE}$	RINGPLL frequency range			4	8	4	8	4	8	4	8	4	8	4	8	GHz
$F_{LCPLLRANGE}$	LCPLL frequency range			8	16.375	8	16.375	8	16.375	8	16.375	8	16.375	8	16.375	GHz

Notes:

1. The values listed are the rounded results of the calculated equation (2 × RINGPLL_Frequency)/Subrate_Divider.
2. The highest supported line rate when using the RPLL to drive the datapath is 12.5 Gb/s.
3. The values listed are the rounded results of the calculated equation (2 × LCPLL_Frequency)/(Output_Divider × Subrate_Divider).

GTY and GTYP Transceiver Configuration Interface Port Switching Characteristics

Table 78: **GTY and GTYP Transceiver Configuration Interface Port (APB3) Switching Characteristics**

Symbol	Description	All Speed Grades		Units
		Min	Max	
$F_{GTYAPB3}$	GTYAPB3CLK frequency	100	350	MHz

GTY and GTYP Transceiver Reference Clock Switching Characteristics

Table 79: **GTY and GTYP Transceiver Reference Clock Switching Characteristics**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GTY_REFCLK}	Reference clock frequency range		60	–	820	MHz
T_{RCLK}	Reference clock rise time	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle	Transceiver PLL only	40	50	60	%

GTY and GTYP Transceiver Reference Clock Oscillator Selection Phase Noise Mask

Table 80: **GTY and GTYP Transceiver Reference Clock Oscillator Selection Phase Noise Mask**

Symbol	Description[1, 2]	Offset Frequency	Min	Typ	Max	Units
$RINGPLL_{REFCLKMASK}$	RINGPLL reference clock select phase noise mask at GTY_REFCLK frequency = 156.25 MHz	10 kHz	–	–	–112	dBc/Hz
		100 kHz	–	–	–128	
		1 MHz	–	–	–145	
	RINGPLL reference clock select phase noise mask at GTY_REFCLK frequency = 312.5 MHz	10 kHz	–	–	–103	dBc/Hz
		100 kHz	–	–	–123	
		1 MHz	–	–	–143	
	RINGPLL reference clock select phase noise mask at GTY_REFCLK frequency = 625 MHz	10 kHz	–	–	–98	dBc/Hz
		100 kHz	–	–	–117	
		1 MHz	–	–	–140	
$LCPLL_{REFCLKMASK}$	LCPLL reference clock select phase noise mask at GTY_REFCLK frequency = 156.25 MHz	10 kHz	–	–	–112	dBc/Hz
		100 kHz	–	–	–128	
		1 MHz	–	–	–145	
		50 MHz	–	–	–145	
	LCPLL reference clock select phase noise mask at GTY_REFCLK frequency = 312.5 MHz	10 kHz	–	–	–103	dBc/Hz
		100 kHz	–	–	–123	
		1 MHz	–	–	–143	
		50 MHz	–	–	–145	
	LCPLL reference clock select phase noise mask at GTY_REFCLK frequency = 625 MHz	10 kHz	–	–	–98	dBc/Hz
		100 kHz	–	–	–117	
		1 MHz	–	–	–140	
		50 MHz	–	–	–144	

Notes:

1. For reference clock frequencies not in this table, use the phase-noise mask for the nearest reference clock frequency.
2. This reference clock phase-noise mask is superseded by any reference clock phase-noise mask that is specified in a supported protocol, e.g., PCIe.

GTY and GTYP Transceiver PLL/Lock Time Adaptation

Table 81: **GTY and GTYP Transceiver PLL/Lock Time Adaptation**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
T_{LOCK}	Initial PLL lock	Reference clock frequency ≥ 150MHz	–	–	3	ms
		Reference clock frequency < 150MHz	–	–	5.7	ms
T_{DLOCK}	Clock recovery phase acquisition and adaptation time for decision feedback equalizer (DFE)	After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input.	–	50,000	37×10^6	UI
	Clock recovery phase acquisition and adaptation time for low-power mode (LPM) when the DFE is disabled		–	50,000	2.3×10^6	UI

GTY and GTYP Transceiver User Clock Switching Characteristics

Table 82: **GTY Transceiver User Clock Switching Characteristics**

Symbol	Description[1]	Data Width Conditions (Bit)		Performance as a Function of Speed Grade and Operating Voltage (V_{CCINT})						Units
				0.88V (H)		0.80V (M)		0.70V (L)		
		Internal Logic	Interconnect Logic	-3	-2	-2	-1	-2	-1	
$F_{TXOUTPMA}$	TXOUTCLK maximum frequency sourced from OUTCLKPMA			664.063	664.063	664.063	664.063	664.063	644.531	MHz
$F_{RXOUTPMA}$	RXOUTCLK maximum frequency sourced from OUTCLKPMA			664.063	664.063	664.063	664.063	664.063	644.531	MHz
$F_{TXOUTPROGDIV}$	TXOUTCLK maximum frequency sourced from OUTPROGDIV			1024.000	1024.000	1024.000	664.063	664.063	644.531	MHz
$F_{RXOUTPROGDIV}$	RXOUTCLK maximum frequency sourced from OUTPROGDIV			1024.000	1024.000	1024.000	664.063	664.063	644.531	MHz
F_{TXIN}	TXUSRCLK maximum frequency	16	16	511.719	440.781	440.781	415.040	402.832	402.832	MHz
			32	255.859	220.391	220.391	207.520	201.416	201.416	MHz
		32	32	511.719	440.781	440.781	415.040	402.832	402.832	MHz
			64	255.859	220.391	220.391	207.520	201.416	201.416	MHz
		64	64	511.719 (LPM)	440.781	440.781	415.039	402.832	402.832	MHz
				476.563 (DFE)						
			128	255.859 (LPM)	220.391	220.391	207.520	201.416	201.416	MHz
				238.281 (DFE)						
		20	20	409.375	352.625	352.625	332.032	352.625	322.266	MHz
			40	204.688	176.313	176.313	166.016	176.313	161.133	MHz
		40	40	664.063	664.063	664.063	664.063	664.063	644.531	MHz
			80	204.688	176.313	176.313	166.016	176.313	161.133	MHz
		80	80	409.375 (LPM)	352.625	352.625	332.032	352.625	322.266	MHz
				381.250 (DFE)						
			160	204.688 (LPM)	176.313	176.313	166.016	176.313	161.133	MHz
				190.625 (DFE)						

Table 82: **GTY Transceiver User Clock Switching Characteristics** *(cont'd)*

Symbol	Description[1]	Data Width Conditions (Bit)		Performance as a Function of Speed Grade and Operating Voltage (V_{CCINT})						Units
				0.88V (H)		0.80V (M)		0.70V (L)		
		Internal Logic	Interconnect Logic	-3	-2	-2	-1	-2	-1	
F_{RXIN}	RXUSRCLK maximum frequency	16	16	511.719	440.781	440.781	415.040	402.832	402.832	MHz
			32	255.859	220.391	220.391	207.520	201.416	201.416	MHz
		32	32	511.719	440.781	440.781	415.040	402.832	402.832	MHz
			64	255.859	220.391	220.391	207.520	201.416	201.416	MHz
		64	64	511.719 (LPM)	440.781	440.781	415.039	402.832	402.832	MHz
				476.563 (DFE)						
			128	255.859 (LPM)	220.391	220.391	207.520	201.416	201.416	MHz
				238.281 (DFE)						
		20	20	409.375	352.625	352.625	332.032	352.625	322.266	MHz
			40	204.688	176.313	176.313	166.016	176.313	161.133	MHz
		40	40	664.063	664.063	664.063	664.063	664.063	644.531	MHz
			80	204.688	176.313	176.313	166.016	176.313	161.133	MHz
		80	80	409.375 (LPM)	352.625	352.625	332.031	352.625	322.266	MHz
				381.250 (DFE)						
			160	204.688 (LPM)	176.313	176.313	166.016	176.313	161.133	MHz
				190.625 (DFE)						

Notes:

1. Clocking must be implemented as described in the *Versal ACAP GTY and GTYP Transceivers Architecture Manual* (AM002).

Table 83: **GTYP Transceiver User Clock Switching Characteristics**

Symbol	Description[1]	Data Width Conditions (Bit)		Performance as a Function of Speed Grade and Operating Voltage (V_{CCINT})						Units
				0.88V (H)		0.80V (M)		0.70V (L)		
		Internal Logic	Interconnect Logic	-3	-2	-2	-1	-2	-1	
$F_{TXOUTPMA}$	TXOUTCLK maximum frequency sourced from OUTCLKPMA			664.063	664.063	664.063	664.063	664.063	644.531	MHz
$F_{RXOUTPMA}$	RXOUTCLK maximum frequency sourced from OUTCLKPMA			664.063	664.063	664.063	664.063	664.063	644.531	MHz
$F_{TXOUTPROGDIV}$	TXOUTCLK maximum frequency sourced from OUTPROGDIV			1024.000	1024.000	1024.000	1000	664.063	644.531	MHz
$F_{RXOUTPROGDIV}$	RXOUTCLK maximum frequency sourced from OUTPROGDIV			1024.000	1024.000	1024.000	1000	664.063	644.531	MHz

Table 83: **GTYP Transceiver User Clock Switching Characteristics** *(cont'd)*

Symbol	Description[1]	Data Width Conditions (Bit)		Performance as a Function of Speed Grade and Operating Voltage (V_{CCINT})						Units
				0.88V (H)		0.80V (M)		0.70V (L)		
		Internal Logic	Interconnect Logic	-3	-2	-2	-1	-2	-1	
F_{TXIN}	TXUSRCLK maximum frequency	16	16	511.719	440.781	440.781	415.039	402.832	402.832	MHz
			32	255.859	220.391	220.391	207.520	201.416	201.416	MHz
		32	32	511.719	440.781	440.781	415.039	402.832	402.832	MHz
			64	255.859	220.391	220.391	207.520	201.416	201.416	MHz
		64	64	511.719 (LPM)	500	500	415.039	402.832	402.832	MHz
				500 (DFE)						
			128	255.859 (LPM)	220.391	220.391	207.520	201.416	201.416	MHz
				238.281 (DFE)						
		20	20	409.375	352.625	352.625	332.032	352.625	322.266	MHz
			40	204.688	176.313	176.313	166.016	176.313	161.133	MHz
		40	40	664.063	664.063	664.063	664.063	664.063	644.531	MHz
			80	204.688	176.313	176.313	166.016	176.313	161.133	MHz
		80	80	409.375 (LPM)	400	400	332.031	352.625	322.266	MHz
				400 (DFE)						
			160	204.688 (LPM)	176.313	176.313	166.016	176.313	161.133	MHz
				190.625 (DFE)						

Table 83: **GTYP Transceiver User Clock Switching Characteristics** *(cont'd)*

Symbol	Description[1]	Data Width Conditions (Bit)		Performance as a Function of Speed Grade and Operating Voltage (V_{CCINT})						Units
				0.88V (H)		0.80V (M)		0.70V (L)		
		Internal Logic	Interconnect Logic	-3	-2	-2	-1	-2	-1	
F_{RXIN}	RXUSRCLK maximum frequency	16	16	511.719	440.781	440.781	415.039	402.832	402.832	MHz
			32	255.859	220.391	220.391	207.520	201.416	201.416	MHz
		32	32	511.719	440.781	440.781	415.039	402.832	402.832	MHz
			64	255.859	220.391	220.391	207.520	201.416	201.416	MHz
		64	64	511.719 (LPM)	500	500	415.039	402.832	402.832	MHz
				500 (DFE)						
			128	255.859 (LPM)	220.391	220.391	207.520	201.416	201.416	MHz
				238.281 (DFE)						
		20	20	409.375	352.625	352.625	332.032	352.625	322.266	MHz
			40	204.688	176.313	176.313	166.016	176.313	161.133	MHz
		40	40	664.063	664.063	664.063	664.063	664.063	644.531	MHz
			80	204.688	176.313	176.313	166.016	176.313	161.133	MHz
		80	80	409.375 (LPM)	400	400	332.031	352.625	322.266	MHz
				400 (DFE)						
			160	204.688 (LPM)	176.313	176.313	166.016	176.313	161.133	MHz
				190.625 (DFE)						

Notes:

1. Clocking must be implemented as described in the *Versal ACAP GTY and GTYP Transceivers Architecture Manual* (AM002).

GTY and GTYP Transceiver Transmitter and Receiver Switching Characteristics

Table 84: **GTY and GTYP Transceiver Transmitter Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTYTX}	Serial data rate range		1.2	–	F_{GTYMAX}	Gb/s
T_{RTX}	TX rise time	20%–80%	–	21	–	ps
T_{FTX}	TX fall time	80%–20%	–	21	–	ps
T_{LLSKEW}	TX lane-to-lane skew[1]		–	–	500.00	ps
$T_{J32.75}$	Total jitter[2, 4]	32.75 Gb/s	–	–	0.35	UI
$D_{J32.75}$	Deterministic jitter[2, 4]		–	–	0.19	UI
$T_{J28.21}$	Total jitter[2, 4]	28.21 Gb/s	–	–	0.28	UI
$D_{J28.21}$	Deterministic jitter[2, 4]		–	–	0.17	UI
$T_{J16.375}$	Total jitter[2, 4]	16.375 Gb/s	–	–	0.28	UI
$D_{J16.375}$	Deterministic jitter[2, 4]		–	–	0.17	UI

Table 84: **GTY and GTYP Transceiver Transmitter Switching Characteristics** *(cont'd)*

Symbol	Description	Condition	Min	Typ	Max	Units
$T_{J15.0}$	Total jitter[2, 4]	15.0 Gb/s	–	–	0.28	UI
$D_{J15.0}$	Deterministic jitter[2, 4]		–	–	0.17	UI
$T_{J14.1}$	Total jitter[2, 4]	14.1 Gb/s	–	–	0.28	UI
$D_{J14.1}$	Deterministic jitter[2, 4]		–	–	0.17	UI
$T_{J14.1}$	Total jitter[2, 4]	14.025 Gb/s	–	–	0.28	UI
$D_{J14.1}$	Deterministic jitter[2, 4]		–	–	0.17	UI
$T_{J13.1}$	Total jitter[2, 4]	13.1 Gb/s	–	–	0.28	UI
$D_{J13.1}$	Deterministic jitter[2, 4]		–	–	0.17	UI
$T_{J12.5\_LCPLL}$	Total jitter[2, 4]	12.5 Gb/s	–	–	0.28	UI
$D_{J12.5\_LCPLL}$	Deterministic jitter[2, 4]		–	–	0.17	UI
$T_{J12.5\_RPLL}$	Total jitter[3, 4]	12.5 Gb/s	–	–	0.33	UI
$D_{J12.5\_RPLL}$	Deterministic jitter[3, 4]		–	–	0.17	UI
$T_{J11.3\_LCPLL}$	Total jitter[2, 4]	11.3 Gb/s	–	–	0.28	UI
$D_{J11.3\_LCPLL}$	Deterministic jitter[2, 4]		–	–	0.17	UI
$T_{J10.3125\_LCPLL}$	Total jitter[2, 4]	10.3125 Gb/s	–	–	0.28	UI
$D_{J10.3125\_LCPLL}$	Deterministic jitter[2, 4]		–	–	0.17	UI
$T_{J10.3125\_RPLL}$	Total jitter[3, 4]	10.3125 Gb/s	–	–	0.33	UI
$D_{J10.3125\_RPLL}$	Deterministic jitter[3, 4]		–	–	0.17	UI
$T_{J9.953\_LCPLL}$	Total jitter[2, 4]	9.953 Gb/s	–	–	0.28	UI
$D_{J9.953\_LCPLL}$	Deterministic jitter[2, 4]		–	–	0.17	UI
$T_{J9.953\_RPLL}$	Total jitter[3, 4]	9.953 Gb/s	–	–	0.33	UI
$D_{J9.953\_RPLL}$	Deterministic jitter[3, 4]		–	–	0.17	UI
$T_{J8.0}$	Total jitter[3, 4]	8.0 Gb/s	–	–	0.32	UI
$D_{J8.0}$	Deterministic jitter[3, 4]		–	–	0.17	UI
$T_{J6.6}$	Total jitter[3, 4]	6.6 Gb/s	–	–	0.30	UI
$D_{J6.6}$	Deterministic jitter[3, 4]		–	–	0.15	UI
$T_{J5.0}$	Total jitter[3, 4]	5.0 Gb/s	–	–	0.30	UI
$D_{J5.0}$	Deterministic jitter[3, 4]		–	–	0.15	UI
$T_{J4.25}$	Total jitter[3, 4]	4.25 Gb/s	–	–	0.30	UI
$D_{J4.25}$	Deterministic jitter[3, 4]		–	–	0.15	UI
$T_{J3.20}$	Total jitter[3, 4]	3.20 Gb/s	–	–	0.20	UI
$D_{J3.20}$	Deterministic jitter[3, 4]		–	–	0.10	UI
$T_{J2.5}$	Total jitter[3, 4]	2.5 Gb/s	–	–	0.20	UI
$D_{J2.5}$	Deterministic jitter[3, 4]		–	–	0.10	UI
$T_{J1.25}$	Total jitter[3, 4]	1.25 Gb/s	–	–	0.15	UI
$D_{J1.25}$	Deterministic jitter[3, 4]		–	–	0.06	UI

Notes:

1. Using same REFCLK input with TX phase alignment enabled for up to four consecutive transmitters (one fully populated GTY or GTYP Quad) at maximum line rate.
2. Using LCPLL_FBDIV = 40, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
3. Using RPLL_FBDIV = 10, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
4. All jitter values are based on a bit-error ratio of 10^{-12}.

Table 85: **GTY and GTYP Transceiver Receiver Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTYRX}	Serial data rate		1.2	–	F_{GTYMAX}	Gb/s
R_{XSST}	Receiver spread-spectrum tracking	Modulated at 33 kHz	–5000	–	0	ppm
R_{XRL}	Run length (CID)		–	–	256	UI
$R_{XPPMTOL}$	Data/REFCLK PPM offset tolerance	Bit rates ≤ 6.6 Gb/s	–1250	–	1250	ppm
		Bit rates > 6.6 Gb/s and ≤ 8.0 Gb/s	–700	–	700	ppm
		Bit rates > 8.0 Gb/s and ≤ 16.3 Gb/s	–600	–	600	ppm
		Bit rates > 16.3 Gb/s and ≤ 24.0 Gb/s	–350	–	350	ppm
		Bit rates > 24.0 Gb/s	–200	–	200	ppm
SJ Jitter Tolerance[1]						
$J_{T\_SJ32.75}$	Sinusoidal jitter (LCPLL)[2]	32.75 Gb/s	0.25	–	–	UI
$J_{T\_SJ28.21}$	Sinusoidal jitter (LCPLL)[2]	28.21 Gb/s	0.30	–	–	UI
$J_{T\_SJ16.375}$	Sinusoidal jitter (LCPLL)[2]	16.375 Gb/s	0.30	–	–	UI
$J_{T\_SJ15.0}$	Sinusoidal jitter (LCPLL)[2]	15.0 Gb/s	0.30	–	–	UI
$J_{T\_SJ14.1}$	Sinusoidal jitter (LCPLL)[2]	14.1 Gb/s	0.30	–	–	UI
$J_{T\_SJ13.1}$	Sinusoidal jitter (LCPLL)[2]	13.1 Gb/s	0.30	–	–	UI
$J_{T\_SJ12.5}$	Sinusoidal jitter (LCPLL)[2]	12.5 Gb/s	0.30	–	–	UI
$J_{T\_SJ11.3}$	Sinusoidal jitter (LCPLL)[2]	11.3 Gb/s	0.30	–	–	UI
$J_{T\_SJ10.32\_LCPLL}$	Sinusoidal jitter (LCPLL)[2]	10.32 Gb/s	0.30	–	–	UI
$J_{T\_SJ10.32\_RPLL}$	Sinusoidal jitter (RPLL)[2]	10.32 Gb/s	0.30	–	–	UI
$J_{T\_SJ9.953\_LCPLL}$	Sinusoidal jitter (LCPLL)[2]	9.953 Gb/s	0.30	–	–	UI
$J_{T\_SJ9.953\_RPLL}$	Sinusoidal jitter (RPLL)[2]	9.953 Gb/s	0.30	–	–	UI
$J_{T\_SJ8.0}$	Sinusoidal jitter (RPLL)[2]	8.0 Gb/s	0.42	–	–	UI
$J_{T\_SJ6.6}$	Sinusoidal jitter (RPLL)[2]	6.6 Gb/s	0.42	–	–	UI
$J_{T\_SJ5.0}$	Sinusoidal jitter (RPLL)[2]	5.0 Gb/s	0.42	–	–	UI
$J_{T\_SJ4.25}$	Sinusoidal jitter (RPLL)[2]	4.25 Gb/s	0.44	–	–	UI
$J_{T\_SJ3.2}$	Sinusoidal jitter (RPLL)[2]	3.2 Gb/s	0.45	–	–	UI
$J_{T\_SJ2.5}$	Sinusoidal jitter (RPLL)[2]	2.5 Gb/s	0.30	–	–	UI
$J_{T\_SJ1.25}$	Sinusoidal jitter (RPLL)[2]	1.25 Gb/s	0.30	–	–	UI

Notes:

1. All jitter values are based on a bit error ratio of 10^{-12}.
2. The frequency of the injected sinusoidal jitter is 10 MHz.

GTY and GTYP Transceiver Electrical Compliance

The *Versal ACAP GTY and GTYP Transceivers Architecture Manual* (AM002) contains recommended use modes that ensure compliance for the protocols listed in the following table. The transceiver wizard provides the recommended settings for those use cases and for protocol specific characteristics.

Table 86: **GTY and GTYP Transceiver Protocol List**

Protocol	Specification	Serial Rate (Gb/s)	Electrical Compliance
CAUI-4	IEEE 802.3-2012	25.78125	Compliant
28 Gb/s backplane	CEI-25G-LR	25–28.05	Compliant
Interlaken	OIF-CEI-6G, OIF-CEI-11GSR, OIF-CEI-28G-MR	4.25–25.78125	Compliant
100GBASE-KR4	IEEE 802.3bj-2014, CEI-25G-LR	25.78125	Compliant[1]
100GBASE-CR4	IEEE 802.3bj-2014, CEI-25G-LR	25.78125	Compliant[1]
50GBASE-KR4	IEEE 802.3by-2014, CEI-25G-LR	25.78125	Compliant[1]
50GBASE-CR4	IEEE 802.3by-2014, CEI-25G-LR	25.78125	Compliant[1]
25GBASE-KR4	IEEE 802.3by-2014, CEI-25G-LR	25.78125	Compliant[1]
25GBASE-CR4	IEEE 802.3by-2014, CEI-25G-LR	25.78125	Compliant[1]
OTU4 (OTL4.4) CFP2	OIF-CEI-28G-VSR	27.952493–32.75	Compliant
OTU4 (OTL4.4) CFP	OIF-CEI-11G-MR	11.18–13.1	Compliant
CAUI-10	IEEE 802.3-2012	10.3125	Compliant
nPPI	IEEE 802.3-2012	10.3125	Compliant
10GBASE-KR[2]	IEEE 802.3-2012	10.3125	Compliant
SFP+	SFF-8431 (SR and LR)	9.95328–11.10	Compliant
XFP	INF-8077i, revision 4.5	10.3125	Compliant
RXAUI	CEI-6G-SR	6.25	Compliant
XAUI	IEEE 802.3-2012	3.125	Compliant
1000BASE-X	IEEE 802.3-2012	1.25	Compliant
5.0G Ethernet	IEEE 802.3bx (PAR)	5	Compliant
2.5G Ethernet	IEEE 802.3bx (PAR)	2.5	Compliant
HiGig, HiGig+, HiGig2	IEEE 802.3-2012	3.74, 6.6	Compliant
QSGMII	QSGMII v1.2 (Cisco System, ENG-46158)	5	Compliant
OTU2	ITU G.8251	10.709225	Compliant
OTU4 (OTL4.10)	OIF-CEI-11G-SR	11.180997	Compliant
OC-3/12/48/192	GR-253-CORE	0.1555–9.956	Compliant
PCIe Gen1, 2, 3	PCI Express base 3.0	2.5, 5.0, and 8.0	Compliant
SDI[3]	SMPTE 424M-2006	0.27–2.97	Compliant
UHD-SDI[3]	SMPTE ST-2081 6G, SMPTE ST-2082 12G	6 and 12	Compliant
Hybrid memory cube (HMC)	HMC-15G-SR	10, 12.5, and 15.0	Compliant
MoSys bandwidth engine	CEI-11-SR and CEI-11-SR (overclocked)	10.3125, 15.5	Compliant
CPRI	CPRI_v_6_1_2014-07-01	0.6144–12.165	Compliant
Passive optical network (PON)	10G-EPON, 1G-EPON, NG-PON2, XG-PON, and 2.5G-PON	0.155–10.3125	Compliant
JESD204a/b	OIF-CEI-6G, OIF-CEI-11G	3.125–12.5	Compliant
Serial RapidIO	RapidIO specification 3.1	1.25–10.3125	Compliant
DisplayPort	DP 1.2B CTS	1.62–5.4	Compliant[3]
Fibre channel	FC-PI-4	1.0625–14.025	Compliant
SATA Gen1, 2, 3	Serial ATA revision 3.0 specification	1.5, 3.0, and 6.0	Compliant
SAS Gen1, 2, 3	T10/BSR INCITS 519	3.0, 6.0, and 12.0	Compliant
SFI-5	OIF-SFI5-01.0	0.625 - 12.5	Compliant

Table 86: **GTY and GTYP Transceiver Protocol List** *(cont'd)*

Protocol	Specification	Serial Rate (Gb/s)	Electrical Compliance
Aurora	CEI-6G, CEI-11G-LR	All rates	Compliant

Notes:

1. 25 dB loss at Nyquist without FEC.
2. The transition time of the transmitter is faster than the IEEE Std 802.3-2012 specification.
3. This protocol requires external circuitry to achieve compliance.

Integrated Block for MRMAC

More information and documentation on solutions using the multirate Ethernet MAC (MRMAC) can be found at *Versal Devices Integrated 100G Multirate Ethernet MAC (MRMAC) LogiCORE IP Product Guide* (PG314). The *Versal Architecture and Product Data Sheet: Overview* (DS950) lists how many blocks are in each Versal Prime device.

Table 87: **Maximum Performance for MRMAC Designs**

Symbol	Description[1]	Performance as a Function of Speed Grade and Operating Voltage (V_{CCINT})						Units
		0.88V (H)		0.80V (M)		0.70V (L)		
		-3	-2	-2	-1	-2	-1	
$F_{RX\_CORE\_CLK}$	Receive core clock	725.000	705.250	705.250	664.063	705.250	644.531	MHz
$F_{TX\_CORE\_CLK}$	Transmit core clock	725.000	705.250	705.250	664.063	705.250	644.531	MHz
$F_{RX\_AXIS\_CLK}$	Receive AXI4-Stream interface clock	431.762	420.000	420.000	420.000	420.000	322.266	MHz
$F_{TX\_AXIS\_CLK}$	Transmit AXI4-Stream interface clock	431.762	420.000	420.000	420.000	420.000	322.266	MHz
$F_{RX\_SERDES\_CLK}$	Serializer/deserializer clock	725.000	664.063	664.063	664.063	664.063	644.531	MHz
$F_{RX\_ALT\_SERDES\_CLK}$[2]	Receive alternate serializer/ deserializer clock	362.500	352.625	352.625	332.031	352.625	322.266	MHz
$F_{TX\_ALT\_SERDES\_CLK}$[2]	Transmit alternate serializer/deserializer clock	362.500	352.625	352.625	332.031	352.625	322.266	MHz
$F_{RX\_TS\_CLK}$	Receive timestamp clock	350.000	350.000	350.000	350.000	350.000	350.000	MHz
$F_{TX\_TS\_CLK}$	Transmit timestamp clock	350.000	350.000	350.000	350.000	350.000	350.000	MHz
$F_{RX\_FLEXIF\_CLK}$	Receive flex interface clock	431.762	420.000	420.000	420.000	420.000	322.266	MHz
$F_{TX\_FLEXIF\_CLK}$	Transmit flex interface clock	431.762	420.000	420.000	420.000	420.000	322.266	MHz
F_{APB3_CLK}	AMBA® advance peripheral bus (APB3) clock	300.000	300.000	300.000	300.000	300.000	300.000	MHz

Notes:

1. Overclocking is only supported in 100 GbE (with $F_{RX\_CORE\_CLK}$ and $F_{TX\_CORE\_CLK}$ running at 706 MHz, and the $F_{RX\_SERDES\_CLK}$ running at 353 MHz) by faster speed grade devices (-3H, -2H, -2M, -2L).
2. The ALT_SERDES_CLKs run at half the speed of the primary SERDES_CLK. See *Versal Devices Integrated 100G Multirate Ethernet MAC (MRMAC) LogiCORE IP Product Guide* (PG314) for more information.

Programmable Logic Integrated Block for PCIe

More information and documentation on solutions for PCI Express® designs can be found at PCI Express. The *Versal Architecture and Product Data Sheet: Overview* (DS950) lists how many blocks are in each Versal device.

Table 88: **Maximum Performance for Programmable Logic Integrated Block for PCIe Rev. 4.0**

Symbol	Description[1]	Performance as a Function of Speed Grade and Operating Voltage (V_{CCINT})						Units
		0.88V (H)		0.80V (M)		0.70V (L)		
		-3	-2	-2	-1	-2	-1	
$F_{PIPECLK}$	Pipe clock maximum frequency	500	500	500	500	500	500	MHz
$F_{CORECLK}$	Core clock maximum frequency	500	500	500	500	500	500	MHz
F_{APBCLK}	APB clock maximum frequency	250	250	250	250	250	250	MHz

Notes:

1. PCI Express Gen4 operation is supported for x1, x2, x4, and x8 widths.

Integrated Blocks for PCIe with DMA and Cache Coherent Interconnect (CPM)

More information and documentation on solutions for PCI Express® designs can be found at PCI Express. The *Versal Architecture and Product Data Sheet: Overview* (DS950) lists how many blocks are in each Versal device.

Table 89: **Maximum Performance for Streaming Mode Interface of Integrated Block for PCIe Rev. 4.0 with DMA and CCIX Rev. 1.0 (CPM4)**

Symbol	Description	Performance as a Function of Speed Grade and Operating Voltage (V_{CCINT})						Units
		0.88V (H)		0.80V (M)		0.70V (L)		
		-3	-2	-2	-1	-2	-1	
PCIe Up To Gen3x16 With One Link With 512-bit Interface								
$F_{CPM\_USERCLK\_MAX}$	CPM user clock maximum frequency	250	250	250	250	250	250	MHz
PCIe Up To Gen4x8 With Two Links With 512-bit Interface								
$F_{CPM\_USERCLK\_MAX}$	CPM user clock maximum frequency	250	250	250	250	250	250	MHz
CCIX Up To Gen3x16 With One Link With 512-bit Interface								
$F_{CPM\_USERCLK\_MAX}$	CPM user clock maximum frequency	250	250	250	250	250	250	MHz
$F_{CPM\_CHICLK\_MAX}$	CPM AMBA® coherent hub interface (CHI) clock maximum frequency[1]	390	390	390	312	312	250	MHz
CCIX Up To Gen4x8 With Two Links With 512-bit Interface								
$F_{CPM\_USERCLK\_MAX}$	CPM user clock maximum frequency	250	250	250	250	250	250	MHz
$F_{CPM\_CHICLK\_MAX}$	CPM CHI clock maximum frequency[1]	390	390	390	312	312	250	MHz
CCIX Up To 20 Gb/s x8 With Two Links								
$F_{CPM\_USERCLK\_MAX}$	CPM user clock maximum frequency	156.125	156.125	156.125	156.125	156.125	N/A	MHz
$F_{CPM\_CHICLK\_MAX}$	CPM CHI clock maximum frequency[1]	390	390	390	312	312	N/A	MHz
CCIX Up To 25 Gb/s x8 With Two Links								
$F_{CPM\_USERCLK\_MAX}$	CPM user clock maximum frequency	195.312	195.312	195.312	N/A	N/A	N/A	MHz
$F_{CPM\_CHICLK\_MAX}$	CPM CHI clock maximum frequency[1]	390	390	390	N/A	N/A	N/A	MHz

Notes:

1. The CHI clock domain is for the CHI interface that connects the coherent hub to the programmable logic.

Table 90: **Maximum Performance for DMA Streaming Mode Interface of Integrated Block for PCIe Rev. 4.0 with DMA and CCIX Rev. 1.0 (CPM4)**

Symbol	Description	Performance as a Function of Speed Grade and Operating Voltage (V_{CCINT})						Units
		0.88V (H)		0.80V (M)		0.70V (L)		
		-3	-2	-2	-1	-2	-1	
PCIe Up To Gen3x16 With One Link With 512-bit Interface								
$F_{CPM\_USERCLK\_MAX}$	CPM user clock maximum frequency	250	250	250	250	250	250	MHz
PCIe Up To Gen4x8 With One Link With 512-bit Interface								
$F_{CPM\_USERCLK\_MAX}$	CPM user clock maximum frequency	250	250	250	250	250	250	MHz

Table 91: **Maximum Performance for DMA Memory-Mapped AXI4 Mode Interface of Integrated Block for PCIe Rev. 4.0 with DMA and CCIX Rev. 1.0 (CPM4)**

Symbol	Description[1]	Performance as a Function of Speed Grade and Operating Voltage (V_{CCINT})						Units
		0.88V (H)		0.80V (M)		0.70V (L)		
		-3	-2	-2	-1	-2	-1	
PCIe® Gen4x16 With One Link								
$F_{CPM\_USERCLK\_MAX}$	CPM user clock maximum frequency	500	500	N/A	N/A	N/A	N/A	MHz
PCIe Up To Gen4x8 With One Link								
$F_{CPM\_USERCLK\_MAX}$	CPM user clock maximum frequency	250	250	250	250	250	250	MHz

Notes:

1. All clock frequencies shown are for informational purposes only. The CPM user clock is actually internal to the CPM block and cannot be set by the PL because the DMA is operating through hard memory-mapped AXI4 interfaces to the NoC.

Revision History

The following table shows the revision history for this document.

Section	Revision Summary
7/01/2021 Version 1.2	
Recommended Operating Conditions	Added Note 9.
AC Switching Characteristics	Updated the speed file versions to Vivado Design Suite 2021.1 v2.01.
Speed Grade Designations	Moved the XCVM1802 to production for the following speed grades: • -2MSE, -2MLE, -2MSI, -2MLI (V_{CCINT} = 0.80V) • -1MSE, -1MLE, -1MSI, -1MLI (V_{CCINT} = 0.80V)
Production Silicon and Software Status	Updated the software status for the following speed grades to Vivado Design Suite 2021.1 v2.01. • -2MSE, -2MLE, -2MSI, -2MLI (V_{CCINT} = 0.80V) • -1MSE, -1MLE, -1MSI, -1MLI (V_{CCINT} = 0.80V)
Processing System Performance Characteristics	In Table 24: Processor Performance, updated F_{RPUMAX} for the -3/-2 (0.88V (H)) speed grades.
	Added F_{PLATB_CLK} to Table 25: PS-PL Interface Performance.
PS CAN FD Controller Interface	Added Note 2.
PS Trace Interface	Updated Note 2 and added Note 4.
Programmable Logic Performance Characteristics	Updated Table 58: MIPI D-PHY Performance for -2/-1 (0.80V (M) and 0.70V (L)) speed grades.
	In Table 59: Maximum Physical Interface (PHY) Rate for Soft Memory Interface Controller: • Removed Note 4: Maximum performance for interfaces using more than one bank. • Added Note 1. • Revised the -1 performance values for DRAM type DDR4 single rank component. • Revised the -1M performance value for DRAM type 1 rank RDIMM, DIMM.
Accelerator RAM Switching Characteristics	Added the section because the accelerator RAM is available in the VM1102 device.

Section	Revision Summary
Device Pin-to-Pin Output Parameter Guidelines	Updated the $T_{ICKOFMMCM}$ values to the speed specifications in Vivado Design Suite 2021.1.
Device Pin-to-Pin Input Parameter Guidelines	Updated the setup and hold values to the speed specifications in Vivado Design Suite 2021.1.
Memory Interface Controller	Added Note 1 to Table 72: Maximum Physical Interface (PHY) Rate for Integrated Memory Interface Controller, and updated Note 5.
GTY and GTYP Transceiver User Clock Switching Characteristics	Updated values in Table 83: GTYP Transceiver User Clock Switching Characteristics.
4/14/2021 Version 1.1	
General	Added GTYP transceiver specifications.
Summary	Added V_{CC_PMC} overdrive support.
Table 1: Absolute Maximum Ratings—Power, Voltages, and Current	Updated the notes.
Table 3: Recommended Operating Conditions	Revised maximum V_{CCBATT}, added minimum CFU reference clock frequency to F_{CFU_REFCLK}, added overdrive conditions to V_{CC_PMC}, added Notes 2, 3, 4, 8, 12, and updated Note 15.
Available Speed Grades and Operating Voltages	Updated table with standard and overdrive modes. Added note 2.
Table 5: DC Characteristics Over Recommended Operating Conditions	Added table.
V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot	Added note 3 to Table 7: VIN Maximum Allowed AC Voltage Overshoot and Undershoot for XPIO Banks.
Table 11: DC Input Levels for Single-ended POD10, POD12, LVSTL06_12, and LVSTL_11 I/O Standards	Updated V_{IL} maximum and V_{IH} minimum for LVSTL06_12 and LVSTL_11.
Table 16: DC Output Levels for Single-ended and Differential POD10, POD12, LVSTL06_12, and LVSTL_11 I/O Standards	Removed LVSTL_11 (V_{OH} = 33). Added Note 2.
Table 17: Definitions for DC Output Levels for Single-ended and Differential POD10, POD12, LVSTL06_12, and LVSTL_11 I/O Standards	Removed LVSTL_11 (V_{OH} = 33).
LVDS DC Specifications (LVDS15)	Added V_{ICM_AC} and Note 5.
AC Switching Characteristics	Updated the speed file versions and the definitions for engineering sample, pre-production, and production product specification.
Speed Grade Designations	Moved the XCVM1802 to production for the following speed grades: • -2LSE, -2LLE (V_{CCINT} = 0.70V) • -1LSE, -1LLE, -1LSI, -1LLI (V_{CCINT} = 0.70V)
Production Silicon and Software Status	The XCVM1802 is production released using Vivado Design Suite 2020.3 v2.00.
Device Identification	Updated the IDCODE for the XCVM1802, and added notes to explain the table fields.
Processing System Performance Characteristics	Updated Table 24: Processor Performance.
	Added $F_{PSFCIDMA\_CLK}$ and Note 3 to Table 25: PS-PL Interface Performance.
Clocks and Reset	Added $T_{MODEPOR}$, and $T_{PORMODE}$ to Table 28: Power-on Reset Assertion Timing Requirements.
	Added $F_{FPD\_LSBUS\_CLK}$ and Note 1 to Table 29: PS FPD Clocks Switching Characteristics.
	Added $F_{RPLL\_TO\_XPD\_CLK}$, $F_{LPD\_LSBUS\_CLK}$, F_{TS_REFCLK}, F_{PSM_REFCLK}, $F_{DBG\_LPD\_CLK}$, F_{USB_REFCLK}, $F_{DBG\_TS\_CLK}$, and Notes 1, 3, 4, and 6 to Table 30: PS LPD Clocks Switching Characteristics.
	In Table 31: PMC IRO Clock Switching Characteristics, updated the IRO tolerance range.
	In Table 32: PMC Clocks Switching Characteristics, added F_{EFUSE_REFCLK}, F_{SMON_REFCLK}, F_{NPI_REFCLK}, $F_{PPLL\_TO\_XPD\_CLK}$, $F_{NPLL\_TO\_XPD\_CLK}$, F_{LSBUS_REFCLK}, $F_{AXI\_TO\_REFCLK}$, $F_{USB\_SREFCLK}$, and F_{HSM0_REFCLK}. Revised the -3 specifications for F_{PL0_REFCLK}, F_{PL1_REFCLK}, F_{PL2_REFCLK}, and F_{PL3_REFCLK}. Updated the Notes 1 and 3.
	Added Note 1 to Table 33: PMC PLL Switching Characteristics.

Section	Revision Summary
PMC JTAG and SelectMAP	Extensive updates to Table 38: JTAG/Boundary-Scan Port Switching Characteristics and Table 39: SelectMap Interface Switching Characteristics.
PMC Quad-SPI Controller Interface	Extensive changes to the table. Updated Note 1 and added Note 2 and 5.
PMC Octal-SPI Controller Interface	Removed load condition column. Updated Note 1.
PS USB Controller Interface	Added $T_{ULPIDCK}$, $T_{ULPICKD}$, and $T_{ULPICKO}$.
PS Gigabit Ethernet MAC Controller Interface	Added $F_{GEMTSUREFCLK}$.
PS Trace Interface	Updated F_{TCECLK} and Note 3.
Network on Chip Switching Characteristics	Updated the performance values in the table.
Programmable Logic Performance Characteristics	Updated values in Table 56: I/O Logic Performance. Updated values in Table 57: XPHY I/O Performance and added Notes 3 and 4. Updated the values in Table 58: MIPI D-PHY Performance. Updated the values in Table 59: Maximum Physical Interface (PHY) Rate for Soft Memory Interface Controller and added Note 4: Maximum performance for interfaces using more than one bank. Removed the *LVDS Native-Mode 1000BASE-X Support* table.
Block RAM Switching Characteristics	Updated T_{RCKO_DO} and $T_{RCKO\_DO\_REG}$.
Input/Output Delay Switching Characteristics	Added $T_{IOL\_IDELAY\_RESOLUTION}$.
MMCM Switching Characteristics	Extensive updates to table and notes including removal of $T_{DESKEWMISMATCH\_MMCM}$.
DPLL Switching Characteristics	Extensive updates to table and notes including removal of $T_{DESKEWMISMATCH\_DPLL}$.
XPLL Switching Characteristics	Extensive updates to table and notes including removal of $T_{DESKEWMISMATCH\_XPLL}$.
Device Pin-to-Pin Output Parameter Guidelines	Updated the XCVM1802 parameters in Vivado Design Suite 2020.3 v2.00.
Device Pin-to-Pin Input Parameter Guidelines	Updated the XCVM1802 parameters in Vivado Design Suite 2020.3 v2.00.
Package Parameter Guidelines	Updated the XCVM1802 package skew in Vivado Design Suite 2020.3 v2.00.
Memory Interface Controller	Added Notes 2 and 3. Updated 6.
GTY and GTYP Transceiver DC Input and Output Levels	Revised V_{IN} in Table 73: GTY and GTYP Transceiver DC Specifications. Updated the specifications in Table 75: GTY and GTYP Transceiver Clock Output Level Specification.
GTY and GTYP Transceiver Performance	Updated the $F_{GTYLRANGE}$ values.
GTY and GTYP Transceiver PLL/Lock Time Adaptation	Added conditions to T_{LOCK}.
GTY and GTYP Transceiver Transmitter and Receiver Switching Characteristics	Removed legacy content and updated the applicable symbols, conditions, and values in both the Transmitter and Receiver tables.
GTY and GTYP Transceiver Electrical Compliance	Added the table.
PMC Quad-SPI Controller Interface	Added additional load information to the table.
Integrated Block for MRMAC	Changed title and added specifications.
Programmable Logic Integrated Block for PCIe	Added Table 88: Maximum Performance for Programmable Logic Integrated Block for PCIe Rev. 4.0.
7/16/2020 Version 1.0	
Initial release.	N/A

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