LogiCORE IP Aurora 64B/66B v7.1

DS815 April 24, 2012 **Product Specification**

Introduction

The LogiCORE™ IP Aurora 64B/66B core supports the AMBA® protocol AXI4-Stream user interface. It implements the Aurora 64B/66B protocol using the high-speed serial GTX or GTH transceivers in applicable Virtex®-6 LXT, SXT, and HXT, Kintex™-7, and Virtex-7 devices. The core can use up to 16 Virtex-6, Kintex-7, or Virtex-7 FPGA GTX or GTH transceivers and up to 12 GTH transceivers in a Virtex-6 HXT device running at any supported line rate to provide a low-cost, general-purpose, data channel with throughput from 600 Mb/s to over 200 Gb/s.

Aurora 64B/66B is a scalable, lightweight, high data rate, link-layer protocol for high-speed serial communication. The protocol is open and can be implemented using Xilinx FPGA technology.

The CORE Generator™ tool produces source code for Aurora 64B/66B cores. The cores can be simplex or full-duplex, and feature one of two simple user interfaces and optional flow control.

Aurora 64B/66B cores are verified for protocol compliance using an array of automated simulation tests.

Features

- General-purpose data channels with throughput range from 600 Mb/s to over 200 Gb/s
- Supports up to 16 GTX transceivers, 12 Virtex-6 FPGA GTH transceivers, or 16 Virtex-7 FPGA GTH transceivers
- Aurora 64B/66B protocol specification v1.2 compliant (64B/66B encoding)
- Low resource cost with very low (3%) transmission overhead
- Easy-to-use AXI4-Stream (framing) or streaming interface and optional flow control
- Automatically initializes and maintains the channel
- Full-duplex or simplex operation

LogiCORE IP Facts Table					
Core Specifics					
Supported Device Family(1)	Virtex-7, Kintex-7(2) Virtex-6 LXT/SXT/HXT(3)				
Supported User Interfaces	AXI4-Stream				
	Resources(4)				**Frequency**
	LUTs	**FFs**	**DSP Slices**	**Block RAMs**	**Max. Freq.(5)**
Config(6)	6247	10536	0	16	325 MHz
Provided with Core					
Documentation	Product Specification User Guide				
Design Files	Verilog and VHDL				
Example Design	Verilog and VHDL				
Test Bench	Verilog and VHDL				
Constraints File	Xilinx Constraints File				
Simulation Model	Not Provided				
Tested Design Tools					
Design Entry Tools	CORE Generator tool				
Simulation(5)	Mentor Graphics ModelSim(7) Xilinx ISim v14.1 Cadence Incisive Enterprise Simulator(7)				
Synthesis Tools	XST v14.1 Synopsys Synplify Pro(5)				
Support					
Provided by Xilinx @ www.xilinx.com/support					

Notes:

1. For a complete listing of supported devices, see the release notes for this core.
2. For more information, see DS180, *7 Series FPGAs Overview*.
3. For more information, see DS150, *Virtex-6 Family Overview*.
4. For device performance numbers, see Table 2 through Table 7.
5. For more complete performance data, see Performance, page 11.
6. Running at 325 MHz in a Virtex-6 XC6LX240T-FF1156 -2 device. Config1 is a 16-lane Aurora 64B/66B core with Streaming interface and Duplex dataflow targeting a 6.6 Gb/s line rate.
7. For the supported versions of these tools, see the ISE Design Suite 14: Release Notes Guide.

Functional Overview

Aurora 64B/66B is a lightweight, serial communications protocol for multi-gigabit links (Figure 1). It is used to transfer data between devices using one or many GTX/GTH transceivers. Connections can be *full-duplex* (data in both directions) or *simplex* (data in either one of the directions).

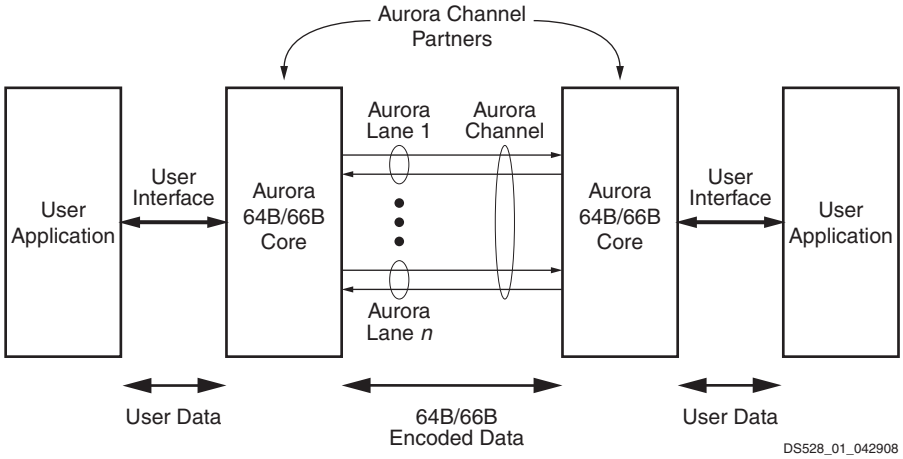

Figure 1: **Aurora 64B/66B Channel Overview**

Aurora 64B/66B cores automatically initialize a channel when they are connected to an Aurora 64B/66B channel partner. After initialization, applications can pass data across the channel as *frames* or *streams* of data. Aurora 64B/66B *frames* can be of any size, and can be interrupted any time by high priority requests. Gaps between valid data bytes are automatically filled with *idles* to maintain lock and prevent excessive electromagnetic interference. *Flow control* is optional in Aurora 64B/66B, and can be used to throttle the link partner's transmit data rate, or to send brief, high-priority messages through the channel.

Streams are implemented in Aurora 64B/66B as a single, unending frame. Whenever data is not being transmitted, idles are transmitted to keep the link alive. Excessive bit errors, disconnections, or equipment failures cause the core to reset and attempt to initialize a new channel. The Aurora 64B/66B core can support a maximum of two symbols skew in the receive of a multi-lane channel. The Aurora 64B/66B protocol uses 64B/66B encoding. The 64B/66B encoding offers improved performance because of its very low (3%) transmission overhead, compared to 25% overhead for 8B/10B encoding.

Applications

Aurora 64B/66B cores can be used in a wide variety of applications because of their low resource cost, scalable throughput, and flexible data interface. Examples of Aurora 64B/66B core applications include:

- **Chip-to-chip links:** Replacing parallel connections between chips with high-speed serial connections can significantly reduce the number of traces and layers required on a PCB. The Aurora 64B/66B core provides the logic needed to use GTX/GTH transceivers, with minimal FPGA resource cost.
- **Board-to-board and backplane links:** Aurora 64B/66B uses standard 64B/66B encoding, which is the preferred encoding scheme for 10-Gigabit Ethernet making it compatible with many existing hardware standards for cables and backplanes. Aurora 64B/66B can be scaled, both in line rate and channel width, to allow inexpensive legacy hardware to be used in new, high-performance systems.
- **Simplex connections (unidirectional):** In some applications there is no need for a high-speed back channel. The Aurora 64B/66B simplex protocol provides several ways to perform unidirectional channel initialization, making it possible to use the GTX/GTH transceivers when a back channel is not available, and to reduce costs due to unused full-duplex resources.
- **ASIC applications:** Aurora 64B/66B is not limited to FPGAs, and can be used to create scalable, high-performance links between programmable logic and high-performance ASICs. The simplicity of the Aurora 64B/66B protocol leads to low resource costs in ASICs as well as in FPGAs, and design resources like the Aurora 64B/66B bus functional model (BFM) with automated compliance testing make it easy to get an Aurora 64B/66B connection up and running. Contact Xilinx Sales or Auroramkt@xilinx.com for information on licensing Aurora for ASIC applications.

Functional Blocks

Figure 2 shows a block diagram of the implementation of the Aurora 64B/66B core.

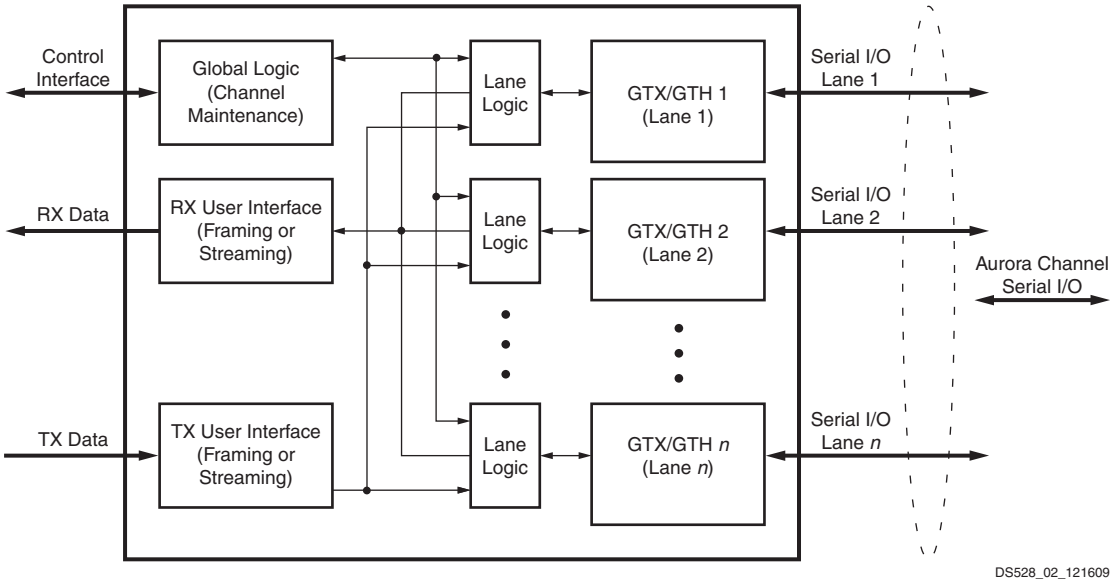

Figure 2: **Aurora 64B/66B Core Block Diagram**

The major functional modules of the Aurora 64B/66B core are:

- **Lane logic:** Each GTX/GTH transceiver is driven by an instance of the lane logic module, which initializes each individual GTX/GTH transceiver and handles the encoding and decoding of control characters and error detection.
- **Global logic:** The global logic module in the Aurora 64B/66B core performs the channel bonding for channel initialization. While the channel is operating, it keeps track of the Not Ready idle characters defined by the Aurora 64B/66B protocol and monitors all the lane logic modules for errors.
- **RX user interface:** The receive (RX) user interface moves data from the channel to the application. Streaming data is presented using a simple stream interface equipped with a data bus and *valid* and *ready* signals for flow control operation. Frames are presented using a standard AXI4-Stream interface. This module also performs flow control functions.
- **TX user interface:** The transmit (TX) user interface moves data from the application to the channel. A stream interface with valid and ready signals are used for streaming data. A standard AXI4-Stream interface is used for data frames. The module also performs flow control TX functions. The module has an interface for controlling clock compensation (the periodic transmission of special characters to prevent errors due to small clock frequency differences between connected Aurora 64B/66B cores). Normally, this interface is driven by a standard clock compensation manager module provided with the Aurora 64B/66B core, but it can be turned off, or driven by custom logic to accommodate special needs.

Core Parameters

The users can customize Aurora 64B/66B cores by setting the parameters for the core using the CORE Generator tool. It is not advisable to change core settings after the core is generated using a set of parameters. Table 1 describes the customizable parameters.

Table 1: **Core Parameters**

Parameter	Description	Supported Values
Lanes	The number of GTX or GTH transceivers used in the channel.	1 to a maximum of 16 GTX transceivers, 12 Virtex-6 FPGA GTH transceivers, or 16 Virtex-7 FPGA GTH transceivers depending on the chosen device
Direction	The type of channel the core will create. Can be full-duplex, simplex in the TX direction, or simplex in the RX direction using a GTX or GTH transceiver.	Full-Duplex Simplex-TX Simplex-RX
Flow Control	Enables optional Aurora 64B/66B flow control. There are two types of flow control: • **Native Flow Control (NFC):** NFC allows full-duplex receivers to control the rate of incoming data. Completion mode NFC forces idles when frames are complete. Immediate mode NFC forces idles as soon as the flow control message arrives. • **User Flow Control (UFC):** UFC allows applications to send each other brief high priority messages through the channel.	None NFC Immediate NFC Completion UFC UFC and NFC Immediate UFC and NFC Completion
User K-Blocks	Aurora 64B/66B includes several control blocks that are not decoded by the Aurora interface, but are instead passed directly to the user. These blocks can be used to implement application specific control functions. There are 9 available User K-blocks.	Enable/Disable

Table 1: **Core Parameters *(Cont'd)***

Parameter	Description	Supported Values
Interface	The user can specify one of two types of interfaces: • **Framing:** The framing user interface is AXI4-Stream compliant. After initialization, it allows framed data to be sent across the Aurora 64B/66B channel. Framing interface cores tend to be larger because of their comprehensive word alignment and control character stripping logic. • **Streaming:** The streaming user interface allows users to start a single, infinite frame. After initialization, the user writes words to the frame using a simple register style interface that has data valid and ready signals. User data has to be integral multiple of 8 bytes.	Framing (AXI4-Stream) Streaming
CRC	Enables optional CRC insertion for data interface. The user can select the following: • **None:** No CRC included in the data interface. • **CRC32:** CRC calculated in the data interface from the standard CRC32 polynomial. The calculated CRC is verified at the RX side, and the status is reported	None/CRC32
DRP	DRP interface to control or monitor the Transceiver interface. The user can select the following: • **AXI4_LITE:** This interface allows reads/writes to serial transceiver parameters based on the AXI4 Lite interface • **Native:** This interface allows reads/writes to serial transceiver parameters based on the Native DRP interface.	AXI4_LITE/Native
Line Rate	The line rate for Virtex-7, Kintex-7, and Virtex-6 FPGA cores can be set from 600 Mb/s to 12.5 Gb/s for GTX transceivers and 600 Mb/s to 13.1(1) Gb/s for GTH transceivers using the CORE Generator tool. See the *LogiCORE IP Aurora 64B/66B v7.1 User Guide* for detailed instructions.	600 Mb/s to 12.5 Gb/s for GTX transceivers 600 Mb/s to 13.1(1) Gb/s for GTH transceivers
Reference Clock Frequency	The CORE Generator tool accepts parameters to set the reference clock rate for Virtex-7, Kintex-7, and Virtex-6 devices. See the *LogiCORE IP Aurora 64B/66B v7.1 User Guide* for detailed instructions.	A selection of legal rates based on the selected line rate and available clock multipliers in the Virtex-7, Kintex-7, and Virtex-6 FPGA GTX/GTH transceivers
Reference Clock	The GTX/GTH transceivers can be fed a reference clock from a variety of dedicated and non-dedicated clock networks. See the *LogiCORE IP Aurora 64B/66B v7.1 User Guide* for instructions to select the best reference clock network for a given application.	GTXQ/GTHQ
GTX/GTH Transceiver Placement	The CORE Generator tool provides a graphical interface that allows users to assign lanes to specific GTX/GTH transceivers. See the *LogiCORE IP Aurora 64B/66B v7.1 User Guide* for guidelines to place GTX/GTH transceivers for best timing results and for details on north-south clocking.	Any combination of GTX/GTH transceivers can be selected. GTX/GTH transceivers should be selected such that transceiver's north-south clocking criteria is met.

Notes:

1. The line rate range for GTH transceivers is not continuous. See DS183, *Virtex-7 FPGAs Data Sheet: DC and Switching Characteristics*, DS182, *Kintex-7 FPGAs Data Sheet: DC and Switching Characteristics*, and DS152, *Virtex-6 FPGA Data Sheet: DC and Switching Characteristics*, for more details on supported line rates.

Core Interfaces

The parameters used to generate each Aurora 64B/66B core determine the interfaces available (Figure 3, page 6) for that specific core. The Aurora 64B/66B cores have three to six interfaces:

- User Interface, page 7
- User Flow Control Interface, page 7
- Native Flow Control Interface, page 7
- GTX/GTH Transceiver Interface, page 7
- Clock Interface, page 8
- Clock Compensation Interface, page 8

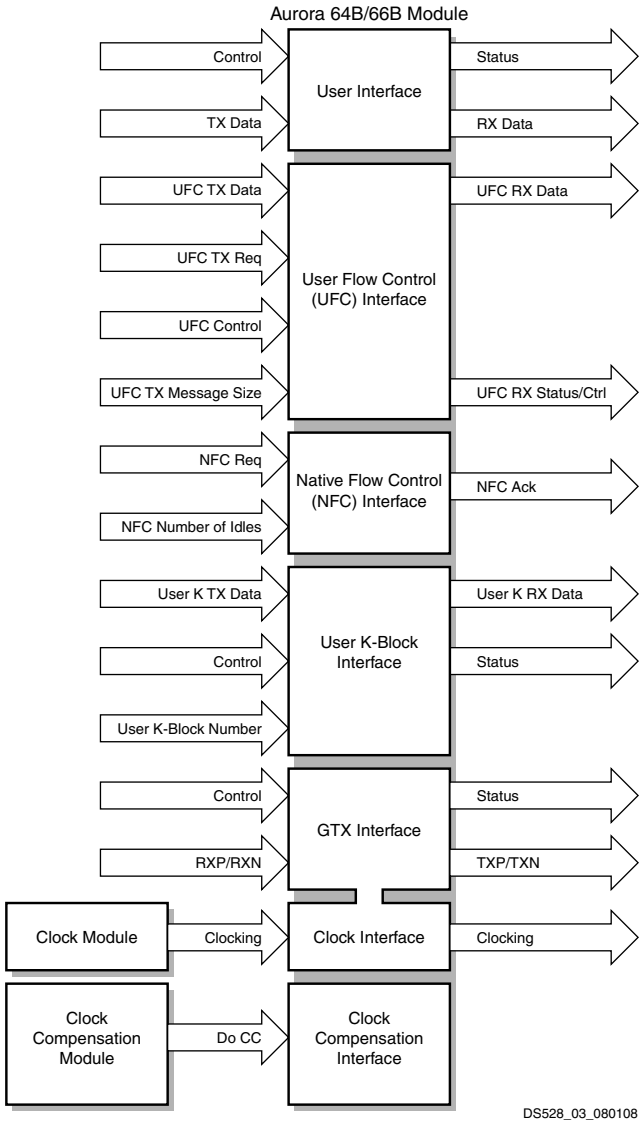

Figure 3: **Top-Level Interface**

User Interface

This interface includes all the ports needed to read and write *streaming* or *framed* data to and from the Aurora 64B/66B core. AXI4-Stream ports are used if the Aurora 64B/66B core is generated with a framing interface; for streaming modules, the interface consists of a simple set of data ports with data valid and ready ports. Full-duplex cores include ports for both transmit (TX) and receive (RX); simplex cores use only the ports they require in the direction they support. The width of the data ports in all interfaces depends on the number of GTX/GTH transceivers used by the core. CRC is computed on the data interface for every frame in the framing interface, if the CRC32 option is selected.

User Flow Control Interface

If the core is generated with user flow control (UFC) enabled, a UFC interface is created. The TX side of the UFC interface consists of a request, valid, and ready ports that are used to start a UFC message, and a port to specify the length of the message. The user supplies the message data to the UFC data port immediately after a UFC request, depending on valid and ready ports of the UFC interface; this in turn deasserts the ready port of the user data interface indicating that the core is no longer ready for normal data, thereby allowing UFC data to be written to the UFC data port.

The RX side of the UFC interface consists of a set of AXI4-Stream ports that allows the UFC message to be read as a frame. Full-duplex modules include both TX and RX UFC ports; simplex modules retain only the interface they need to send data in the direction they support.

Native Flow Control Interface

If the core is generated with native flow control (NFC) enabled, an NFC interface is created. This interface includes a request and an acknowledge port that are used to send NFC messages, an NFC XOFF bit that when asserted sends XOFF code to the lane partner to stop transmission, and a 16-bit port to specify the NFC PAUSE count (number of idle cycles requested) and NFC XOFF.

Note: NFC completion mode is not applicable to streaming designs.

User K-Block Interface

If the core is generated with User K-block feature enabled, a User K interface is created. User K-blocks are special single block codes that includes control blocks that are not decoded by the Aurora interface, but are instead passed directly to the user. These blocks can be used to implement application specific control functions. The TX side consists of valid and ready ports that are used to start a User K transmission along with the block number port to indicate which of the nine User K-blocks needs to be transmitted. The User K data is transmitted after the core provides a ready for the User K interface. It also indicates to the user interface that it is no longer ready for normal data, thereby allowing User K data to be written to the User K data port. The User K blocks are single block codes.

The receive side of the User K interface consists of an RX valid signal to indicate the reception of User K-block. Full-duplex modules include both TX and RX User K ports; simplex modules retain only the interface they need to send data in the direction they support.

GTX/GTH Transceiver Interface

This interface includes the serial I/O ports of the GTX/GTH transceivers and the control and status ports of the Aurora 64B/66B core. This interface is the user's access to control functions such as reset,

loopback, and powerdown. The DRP interface can be used to access or update the serial transceiver parameters and settings through the AXI4 Lite or Native DRP interface.

Clock Interface

This interface is most critical for correct Aurora 64B/66B core operation. The clock interface has ports for the reference clocks that drive the GTX/GTH transceivers, and ports for the parallel clocks that the Aurora 64B/66B core shares with application logic. For more details on the clock interface, see the *LogiCORE IP Aurora 64B/66B v7.1 User Guide*.

Clock Compensation Interface

This interface is included in modules that transmit data, and is used to manage clock compensation. Whenever the DO_CC port is driven High, the core stops the flow of data and flow control messages, then sends clock compensation sequences. Each Aurora 64B/66B core is accompanied by a clock compensation management module that is used to drive the clock compensation interface in accordance with the *Aurora 64B/66B Protocol Specification*. When the same physical clock is used on both sides of the channel, DO_CC should be tied Low. For more details on the clock compensation interface, see the *LogiCORE IP Aurora 64B/66B v7.1 User Guide*.

Resource Utilization

Table 2 through Table 7, page 10 show the number of look-up tables (LUTs) and flip-flops (FFs) used in selected Aurora 64B/66B *framing* and *streaming* modules. The Aurora 64B/66B core is also available in configurations not shown in the tables. The tables do not include the additional resource usage for flow controls.

Table 2: **Virtex-7 Family GTX Transceiver Resource Usage for Streaming**

Virtex-7 Family (GTX Transceiver)		Streaming		
		Duplex	Simplex	
Lanes	Resource Type	Full-Duplex	TX-Only	RX-Only
1	LUTs	410	190	339
	FFs	697	229	519
2	LUTs	781	195	698
	FFs	1216	229	1037
4	LUTs	1450	253	1301
	FFs	2193	231	2011
8	LUTs	2736	156	2606
	FFs	4144	235	3959
16	LUTs	5321	164	5091
	FFs	8049	244	7855

Table 3: **Virtex-7 Family GTX Transceiver Resource Usage for Framing**

Virtex-7 Family (GTX Transceiver)		Framing		
		Duplex	Simplex	
Lanes	Resource Type	Full-Duplex	TX-Only	RX-Only
1	LUTs	448	190	345
	FFs	697	229	519
2	LUTs	779	194	708
	FFs	1218	229	1039
4	LUTs	1448	253	1300
	FFs	2196	231	2014
8	LUTs	2750	148	2681
	FFs	4144	235	3959
16	LUTs	5416	162	5146
	FFs	8048	244	7855

Table 4: **Virtex-6 LXT/SXT/HXT Family GTX Transceiver Resource Usage for Streaming**

Virtex-6 LXT/SXT/HXT Family (GTX Transceiver)		Streaming		
		Duplex	Simplex	
Lanes	Resource Type	Full-Duplex	TX-Only	RX-Only
1	LUTs	474	147	395
	FFs	804	244	613
2	LUTs	921	153	810
	FFs	1411	245	1217
4	LUTs	1722	152	1558
	FFs	2785	247	2363
8	LUTs	3327	158	3123
	FFs	5386	251	4655
16	LUTs	6247	566	5773
	FFs	10536	1369	9239

Table 5: **Virtex-6 LXT/SXT/HXT Family GTX Transceiver Resource Usage for Framing**

Virtex-6 LXT/SXT/HXT Family (GTX Transceiver)		Framing		
		Duplex	Simplex	
Lanes	Resource Type	Full-Duplex	TX-Only	RX-Only
1	LUTs	514	153	402
	FFs	804	244	613
2	LUTs	935	144	435
	FFs	1411	247	813

Table 5: **Virtex-6 LXT/SXT/HXT Family GTX Transceiver Resource Usage for Framing *(Cont'd)***

Virtex-6 LXT/SXT/HXT Family (GTX Transceiver)		Framing		
		Duplex	Simplex	
Lanes	Resource Type	Full-Duplex	TX-Only	RX-Only
4	LUTs	1705	151	1562
	FFs	2785	247	2363
8	LUTs	3510	142	3145
	FFs	5386	251	4655
16	LUTs	6363	575	5867
	FFs	10586	1369	9239

Table 6: **Virtex-6 HXT Family GTH Transceiver Resource Usage for Framing**

Virtex-6 HXT Family GTH Transceiver		Framing		
		Duplex	Simplex	
Lanes	Resource Type	Full-Duplex	TX Only	RX Only
1	LUTs	2698	1691	1066
	FFs	1320	571	909
2	LUTs	4946	3187	2035
	FFs	2485	967	1705
4	LUTs	9637	6051	3927
	FFs	4773	1780	3237
8	LUTs	19254	12099	7859
	FFs	9481	3550	6430

Table 7: **Virtex-6 HXT Family GTH Transceiver Resource Usage for Streaming**

Virtex-6 HXT Family GTH Transceiver		Streaming		
		Duplex	Simplex	
Lanes	Resource Type	Full-Duplex	TX Only	RX Only
1	LUTs	2703	1690	1137
	FFs	1311	585	909
2	LUTs	4993	3126	2019
	FFs	2485	996	1705
4	LUTs	9589	6009	3886
	FFs	4773	1827	3237
8	LUTs	18836	12675	7729
	FFs	9482	3500	6430

Performance

The Aurora 64B/66B cores listed in Table 2, page 8 through Table 5, page 9 were run at 156.25 MHz in devices with speed grades ranging from -1 to -3. For more details on core performance, see the *LogiCORE IP Aurora 64B/66B v7.1 User Guide*.

Verification

The Aurora 64B/66B core is verified using the Aurora 64B/66B BFM and proprietary custom test benches. The Aurora 64B/66B BFM verifies the protocol compliance along with interface level checks and error scenarios. An automated test system runs a series of simulation tests on the most widely used set of design configurations chosen at random. Aurora 64B/66B cores are also tested in hardware for functionality, performance, and reliability using Xilinx GTX/GTH transceiver demonstration boards. Aurora 64B/66B verification test suites for all possible modules are continuously being modified to increase test coverage across the range of possible parameters for each individual module.

Two boards can be used for verification:

- ML623
- KC724

Support

Xilinx provides technical support for this LogiCORE IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled DO NOT MODIFY.

Ordering Information

This Xilinx LogiCORE IP module is included at no additional charge with the Xilinx ISE® Design Suite and is provided under the terms of the Xilinx End User License Agreement. The core is generated using the CORE Generator tool, which is a standard component of the Xilinx ISE tool. For more information, visit the Aurora 64B/66B product page.

Information about additional LogiCORE IP modules can be found on the Xilinx.com Intellectual Property page. Contact your local Xilinx sales representative for pricing and availability.

References

1. Xilinx Aurora website: www.xilinx.com/aurora
   - UG775, *LogiCORE IP Aurora 64B/66B v7.1 User Guide*
   - SP011, *Aurora 64B/66B Protocol Specification*
2. *AMBA AXI4-Stream Protocol Specification*
3. These Xilinx documents can be located from the Xilinx Support website:
   - UG761, *AXI Reference Guide*
   - UG366, *Virtex-6 FPGA GTX Transceivers User Guide*
   - UG371, *Virtex-6 FPGA GTH Transceivers User Guide*

- UG476, *7 Series FPGAs GTX Transceivers User Guide*
- DS152, *Virtex-6 FPGA Data Sheet: DC and Switching Characteristics*
- DS182, *Kintex-7 FPGAs Data Sheet: DC and Switching Characteristics*
- DS183, *Virtex-7 FPGAs Data Sheet: DC and Switching Characteristics*

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
12/14/10	1.0	First release of the core with AXI interface support. The previous release of this document was DS528.
06/22/11	2.0	ISE 13.2 release for core version 6.1. Removed Virtex-5 devices and added Virtex-7 and Kintex-7 device support. Extended the number of GTH transceivers to 12. Removed references to Simplex Both.
01/18/12	2.1	ISE 13.4 release for core version 6.2.
04/24/12	2.2	ISE 14.1 release for core version 7.1. • Updated the maximum supported line rate to 200 Gb/s. • Updated the number of transceivers supported per device. • Revised the Resource Usage tables. • Added CRC and DRP parameters to Table 1 and to interface descriptions.

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