LogiCORE IP Aurora 64B/66B v4.1

DS528 April 19, 2010 **Product Specification**

Introduction

The LogiCORE™ IP Aurora 64B/66B core implements the Aurora 64B/66B protocol using the high-speed serial GTX or GTH transceivers in applicable Virtex®-5 FXT and TXT and Virtex-6 LXT, SXT, and HXT devices. The core can use up to 16 Virtex-5 or Virtex-6 FPGA GTX transceivers and up to 8[1] GTH transceivers in an HXT device running at any supported line rate to provide a low cost, general purpose, data channel with throughput from 750 Mbps to over 86.78 Gbps.

Aurora 64B/66B is a scalable, lightweight, high data rate, link-layer protocol for high-speed serial communication. The protocol is open and can be implemented using Xilinx® FPGA technology.

The CORE Generator™ software produces source code for Aurora 64B/66B cores. The cores can be simplex or full-duplex, and feature one of two simple user interfaces and optional flow control.

Aurora 64B/66B cores are verified for protocol compliance using an array of automated simulation tests.

Features

- General purpose data channels with throughput range from 750 Mbps to over 86.78 Gbps
- Supports up to 16 GTX or 8 GTH transceivers
- Aurora 64B/66B protocol specification v1.1 compliant (64B/66B encoding)
- Low resource cost with very low transmission overhead (3%)
- Easy-to-use LocalLink (framing) or streaming interface and optional flow control
- Automatically initializes and maintains the channel
- Full-duplex or simplex operation

LogiCORE IP Facts				
Core Specifics				
Supported Device Family (1)	Virtex-5 FXT/TXT (2) Virtex-6 LXT/SXT/HXT (3)			
Resources Used	I/O	LUTs	FFs	Block RAMs
	Varies with the channel size See "Resource Utilization," page 8			1 per Aurora Lane
Special Features	Open source; core is free to use with Xilinx devices			
Provided with Core				
Documentation	Product Specification Getting Started Guide User Guide			
Design File Formats	Verilog and VHDL			
Constraints File	.ucf (user constraints file)			
Verification	Example Design and Test Bench			
Design Tool Requirements				
Xilinx Implementation Tools	ISE®(4) 12.1 or later			
Verification	Mentor Graphics ModelSim 6.5c and above			
Simulation	Mentor Graphics ModelSim 6.5c and above			
Synthesis	XST 12.1			
Support				
Provided by Xilinx, Inc. www.xilinx.com/support				

1. For the complete list of supported devices, see the 12.1 release notes for this core.
2. For more information on the Virtex-5 FPGAs, see DS100: *Virtex-5 Family Overview*
3. For more information on the Virtex-6 FPGAs, see DS150: *Virtex-6 Family Overview*
4. ISE Service Packs can be downloaded at www.xilinx.com/support/download.htm

1. Contact Aurora Marketing for further information.

Functional Overview

Aurora 64B/66B is a lightweight, serial communications protocol for multi-gigabit links (Figure 1). It is used to transfer data between devices using one or many GTX/GTH transceivers. Connections can be *full-duplex* (data in both directions) or *simplex* (data in either one of the directions).

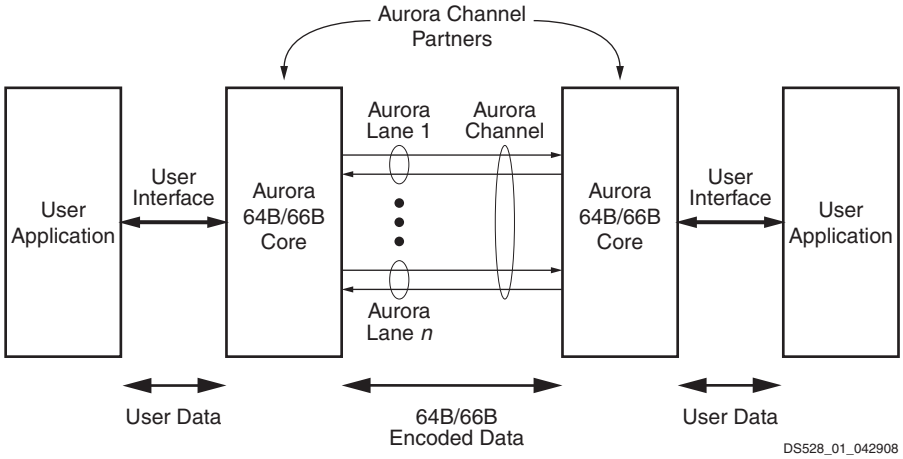

Figure 1: **Aurora 64B/66B Channel Overview**

Aurora 64B/66B cores automatically initialize a channel when they are connected to an Aurora 64B/66B channel partner. After initialization, applications can pass data across the channel as *frames* or *streams* of data. Aurora 64B/66B *frames* can be of any size, and can be interrupted any time by high priority requests. Gaps between valid data bytes are automatically filled with *idles* to maintain lock and prevent excessive electromagnetic interference. *Flow control* is optional in Aurora 64B/66B, and can be used to throttle the link partner's transmit data rate, or to send brief, high-priority messages through the channel.

Streams are implemented in Aurora 64B/66B as a single, unending frame. Whenever data is not being transmitted, idles are transmitted to keep the link alive. Excessive bit errors, disconnections, or equipment failures cause the core to reset and attempt to initialize a new channel. The Aurora 64B/66B core can support a maximum of two symbols skew in the receive of a multi-lane channel. The Aurora 64B/66B protocol uses 64B/66B encoding. The 64B/66B encoding offers improved performance because of its very low (3%) transmission overhead, compared to 25% overhead for 8B/10B encoding.

Applications

Aurora 64B/66B cores can be used in a wide variety of applications because of their low resource cost, scalable throughput, and flexible data interface. Examples of Aurora 64B/66B core applications include:

- **Chip-to-chip links:** Replacing parallel connections between chips with high-speed serial connections can significantly reduce the number of traces and layers required on a PCB. The Aurora 64B/66B core provides the logic needed to use GTX/GTH transceivers, with minimal FPGA resource cost.
- **Board-to-board and backplane links:** Aurora 64B/66B uses standard 64B/66B encoding, which is the preferred encoding scheme for 10-Gigabit Ethernet making it compatible with many existing hardware standards for cables and backplanes. Aurora 64B/66B can be scaled, both in line rate and channel width, to allow inexpensive legacy hardware to be used in new, high-performance systems.
- **Simplex connections (unidirectional):** In some applications there is no need for a high-speed back channel. The Aurora 64B/66B simplex protocol provides several ways to perform unidirectional channel initialization, making it possible to use the GTX/GTH transceivers when a back channel is not available, and to reduce costs due to unused full-duplex resources.
- **ASIC applications:** Aurora 64B/66B is not limited to FPGAs, and can be used to create scalable, high-performance links between programmable logic and high-performance ASICs. The simplicity of the Aurora 64B/66B protocol leads to low resource costs in ASICs as well as in FPGAs, and design resources like the Aurora 64B/66B bus functional model (BFM) with automated compliance testing make it easy to get an Aurora 64B/66B connection up and running. Contact Xilinx Sales or Auroramkt@xilinx.com for information on licensing Aurora for ASIC applications.

Functional Blocks

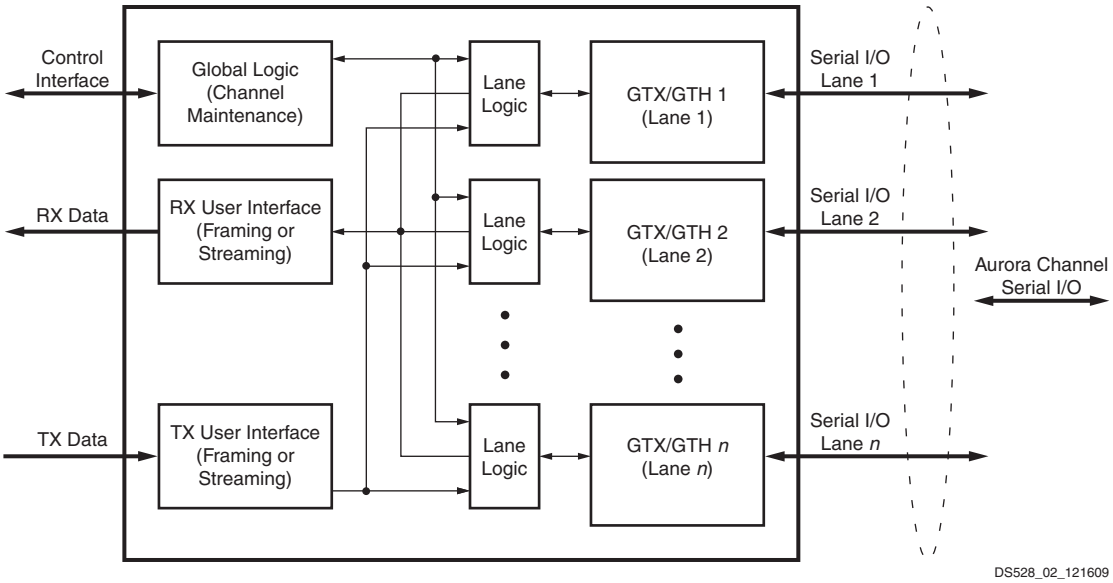

Figure 2: **Aurora 64B/66B Core Block Diagram**

Figure 2 shows a block diagram of the implementation of the Aurora 64B/66B core. The major functional modules of the Aurora 64B/66B core are:

- **Lane logic:** Each GTX/GTH transceiver is driven by an instance of the lane logic module, which initializes each individual GTX/GTH transceiver and handles the encoding and decoding of control characters and error detection.
- **Global logic:** The global logic module in the Aurora 64B/66B core performs the channel bonding for channel initialization. While the channel is operating, it keeps track of the Not Ready idle characters defined by the Aurora 64B/66B protocol and monitors all the lane logic modules for errors.
- **RX user interface:** The receive (RX) user interface moves data from the channel to the application. Streaming data is presented using a simple stream interface equipped with a data bus and *source ready* and *destination ready* signals for flow control operation. Frames are presented using a standard LocalLink interface. This module also performs flow control functions.
- **TX user interface:** The transmit (TX) user interface moves data from the application to the channel. A stream interface with source ready and destination ready signals are used for streaming data. A standard LocalLink interface is used for data frames. The module also performs flow control TX functions. The module has an interface for controlling clock compensation (the periodic transmission of special characters to prevent errors due to small clock frequency differences between connected Aurora 64B/66B cores). Normally, this interface is driven by a standard clock compensation manager module provided with the Aurora 64B/66B core, but it can be turned off, or driven by custom logic to accommodate special needs.

Core Parameters

The users can customize Aurora 64B/66B cores by setting the parameters for the core using the CORE Generator software. It is not advisable to change core settings once the core is generated using a set of parameters. Table 1 describes the customizable parameters.

Table 1: **Core Parameters**

Parameter	Description	Values Supported by Aurora 64B/66B Core
Lanes	The number of GTX or GTH transceivers used in the channel.	1 to a maximum of 16 GTX or 8 GTH transceivers depending on the chosen device
Direction	The type of channel the core will create. Can be full-duplex, simplex in the TX direction, simplex in the RX direction, or two separate simplex modules (one TX and one RX) sharing the same GTX or GTH transceiver.	Full-Duplex Simplex-TX Simplex-RX Simplex-Both
Flow Control	Enables optional Aurora 64B/66B flow control. There are two types of flow control: • **Native Flow Control (NFC):** NFC allows full-duplex receivers to control the rate of incoming data. Completion mode NFC forces idles when frames are complete. Immediate mode NFC forces idles as soon as the flow control message arrives. • **User Flow Control (UFC):** UFC allows applications to send each other brief high priority messages through the channel.	None NFC Immediate NFC Completion UFC UFC and NFC Immediate UFC and NFC Completion
User K-Blocks	Aurora 64B/66B includes several control blocks that are not decoded by the Aurora interface, but are instead passed directly to the user. These blocks can be used to implement application specific control functions. There are 9 available User K-blocks.	Enable/Disable

Table 1: **Core Parameters *(Cont'd)***

Parameter	Description	Values Supported by Aurora 64B/66B Core
Interface	The user can specify one of two types of interfaces: • **Framing:** The framing user interface is LocalLink compliant. After initialization, it allows framed data to be sent across the Aurora 64B/66B channel. Framing interface cores tend to be larger because of their comprehensive word alignment and control character stripping logic. • **Streaming:** The streaming user interface allows users to start a single, infinite frame. After initialization, the user writes words to the frame using a simple register style interface that has source ready and destination ready signals. User data has to be integral multiple of 8 bytes.	Framing (LocalLink) Streaming
Line Rate	The line rate for Virtex-5 and Virtex-6 FPGA cores can be set from 750 Mbps to 6.6 Gbps for GTX transceivers and 2.488 Gbps to 11.18(1) Gbps for GTH transceivers using the CORE Generator software. See the *LogiCORE IP Aurora 64B/66B User Guide* for detailed instructions.	750 Mbps to 6.6 Gbps for GTX 2.488 Gbps to 11.18(1) Gbps for GTH
Reference Clock Frequency	The CORE Generator software accepts parameters to set the reference clock rate for Virtex-5 and Virtex-6 devices. See the *LogiCORE IP Aurora 64B/66B User Guide* for detailed instructions.	A selection of legal rates based on the selected line rate and available clock multipliers in the Virtex-5 and Virtex-6 FPGA GTX/GTH transceivers
Reference Clock	The GTX/GTH transceivers can be fed a reference clock from a variety of dedicated and non-dedicated clock networks. See the *LogiCORE IP Aurora 64B/66B User Guide* for instructions to select the best reference clock network for a given application.	GTXD/GTXQ/GTHQ
GTX/GTH Transceiver Placement	The CORE Generator software provides a graphical interface that allows users to assign lanes to specific GTX/GTH transceivers. See the *LogiCORE IP Aurora 64B/66B User Guide* for guidelines to place GTX/GTH transceivers for best timing results and for details on north-south clocking.	Any combination of GTX/GTH transceivers can be selected GTX/GTH transceivers should be selected such that transceiver's north-south clocking criteria is met

1. The line rate range for GTH transceivers is not continuous. See DS152,See the *Virtex-6 FPGA Data Sheet: DC and Switching Characteristics* for more details on supported line rates

Core Interfaces

The parameters used to generate each Aurora 64B/66B core determine the interfaces available (Figure 3, page 6) for that specific core. The Aurora 64B/66B cores have three to six interfaces:

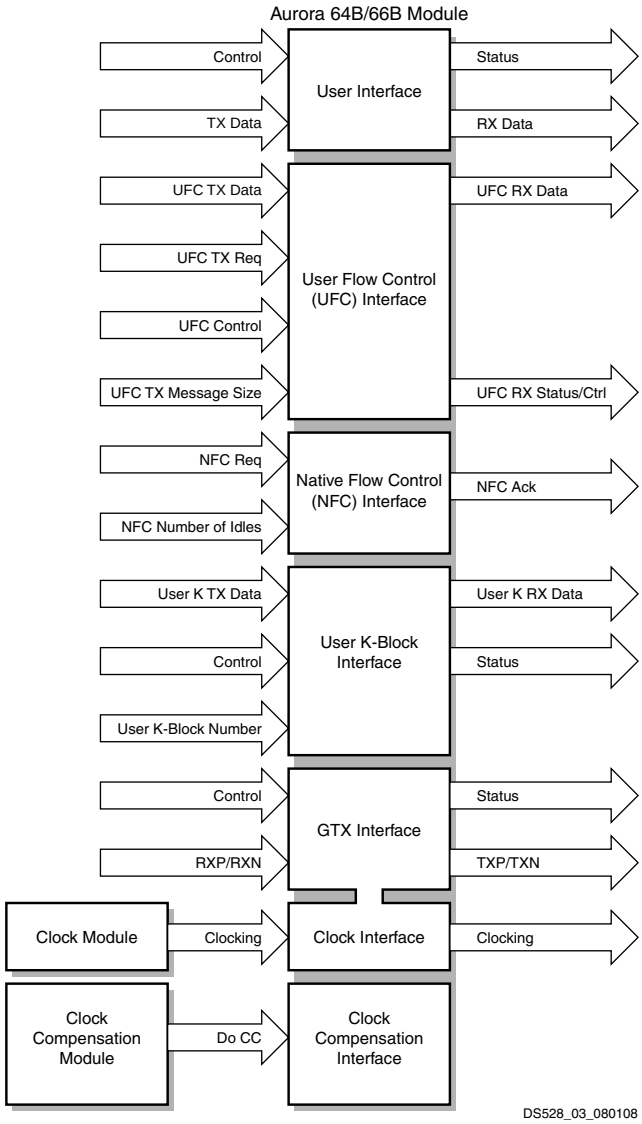

Figure 3: **Top-Level Interface**

User Interface

This interface includes all the ports needed to read and write *streaming* or *framed* data to and from the Aurora 64B/66B core. LocalLink ports are used if the Aurora 64B/66B core is generated with a framing interface; for streaming modules, the interface consists of a simple set of data ports and source ready and destination ready ports. Full-duplex cores include ports for both transmit (TX) and receive (RX); simplex cores use only the ports they require in the direction they support. The width of the data ports in all interfaces depends on the number of GTX/GTH transceivers used by the core.

User Flow Control Interface

If the core is generated with user flow control (UFC) enabled, a UFC interface is created. The TX side of the UFC interface consists of a request, source ready, and destination ready ports that are used to start a UFC message, and a port to specify the length of the message. The user supplies the message data to the UFC data port immediately after a UFC request, depending on source ready and destination ready

ports of the UFC interface; this in turn deasserts the destination ready port of the user interface indicating that the core is no longer ready for normal data, thereby allowing UFC data to be written to the UFC data port.

The RX side of the UFC interface consists of a set of LocalLink ports that allows the UFC message to be read as a frame. Full-duplex modules include both TX and RX UFC ports; simplex modules retain only the interface they need to send data in the direction they support.

Native Flow Control Interface

If the core is generated with native flow control (NFC) enabled, an NFC interface is created. This interface includes a request and an acknowledge port that are used to send NFC messages, an NFC XOFF port that when asserted sends XOFF code to the lane partner to stop transmission, and an 8-bit port to specify the NFC PAUSE count (number of idle cycles requested).

Note: NFC completion mode is not applicable to streaming designs.

User K-Block Interface

If the core is generated with User K-block feature enabled, a User K interface is created. User K-blocks are special single block codes that includes control blocks that are not decoded by the Aurora interface, but are instead passed directly to the user. These blocks can be used to implement application specific control functions. The TX side consists of source ready and destination ready ports that are used to start a User K transmission along with the block number port to indicate which of the nine User K-blocks needs to be transmitted. The User K data is transmitted once the core provides a destination ready for the User K interface. It also indicates to the user interface that it is no longer ready for normal data, thereby allowing User K data to be written to the User K data port. The User K-blocks are single block codes.

The receive side of the User K interface consists of an RX source ready signal to indicate the reception of User K-block. Full-duplex modules include both TX and RX User K ports; simplex modules retain only the interface they need to send data in the direction they support.

GTX/GTH Transceiver Interface

This interface includes the serial I/O ports of the GTX/GTH transceivers and the control and status ports of the Aurora 64B/66B core. This interface is the user's access to control functions such as reset, loopback, and powerdown.

Clock Interface

This interface is most critical for correct Aurora 64B/66B core operation. The clock interface has ports for the reference clocks that drive the GTX/GTH transceivers, and ports for the parallel clocks that the Aurora 64B/66B core shares with application logic. For more details on the clock interface, see the *LogiCORE IP Aurora 64B/66B User Guide*.

Clock Compensation Interface

This interface is included in modules that transmit data, and is used to manage clock compensation. Whenever the DO_CC port is driven High, the core stops the flow of data and flow control messages, then sends clock compensation sequences. Each Aurora 64B/66B core is accompanied by a clock compensation management module that is used to drive the clock compensation interface in accordance

with the *Aurora 64B/66B Protocol Specification*. When the same physical clock is used on both sides of the channel, DO_CC should be tied Low. For more details on the clock compensation interface, see the *LogiCORE IP Aurora 64B/66B User Guide*.

Resource Utilization

Table 2 through Table 9, page 11 show the number of look-up tables (LUTs) and flip-flops (FFs) used in selected Aurora 64B/66B *framing* and *streaming* modules. The Aurora 64B/66B core is also available in configurations not shown in the tables. These tables do not include the additional resource usage for flow controls.

Table 2: **Virtex-5 FXT/TXT Family Resource Usage for Framing**

Virtex 5 FXT/TXT Family		Framing			
		Duplex	Simplex		
Lanes	Resource Type	Full-Duplex	TX Only	RX Only	RX/TX
1	LUTs	475	169	356	476
	FFs	656	217	479	656
2	LUTs	955	247	779	955
	FFs	1280	353	973	1280
4	LUTs	1725	403	1397	1723
	FFs	2474	625	1907	2474
8	LUTs	3184	710	2582	3176
	FFs	4856	1163	3775	4856
16	LUTs	6287	1328	5144	6285
	FFs	9624	2243	7511	9624

Table 3: **Virtex-5 FXT/TXT Family Resource Usage for Streaming**

Virtex 5 FXT/TXT Family		Streaming			
		Duplex	Simplex		
Lanes	Resource Type	Full-Duplex	TX Only	RX Only	RX/TX
1	LUTs	391	152	283	391
	FFs	570	201	409	570
2	LUTs	790	219	623	790
	FFs	1112	325	833	1112
4	LUTs	1504	353	1215	1503
	FFs	2142	573	1627	2142
8	LUTs	2949	620	2402	2941
	FFs	4202	1069	3215	4202
16	LUTs	5732	1153	4785	5736
	FFs	8324	2061	6391	8324

Table 4: **Virtex-6 LXT/SXT Family Resource Usage for Framing**

Virtex-6 LXT/SXT Family		Framing			
		Duplex	Simplex		
Lanes	Resource Type	Full-Duplex	TX Only	RX Only	RX/TX
1	LUTs	533	206	377	535
	FFs	659	223	481	659
2	LUTs	1062	336	786	1059
	FFs	1281	364	971	1281
4	LUTs	1998	548	1527	1995
	FFs	2469	640	1897	2469
8	LUTs	3952	987	3026	3947
	FFs	4838	1176	3749	4838
16	LUTs	7753	1909	6001	7784
	FFs	9582	2267	7453	9582

Table 5: **Virtex-6 LXT/SXT Family Resource Usage for Streaming**

Virtex-6 LXT/SXT Family		Streaming			
		Duplex	Simplex		
Lanes	Resource Type	Full-Duplex	TX Only	RX Only	RX/TX
1	LUTs	470	190	332	472
	FFs	572	206	411	572
2	LUTs	925	282	691	922
	FFs	1110	330	831	1110
4	LUTs	1759	469	1349	1743
	FFs	2132	578	1617	2132
8	LUTs	3420	852	2669	3414
	FFs	4176	1074	3189	4176
16	LUTs	6739	1617	5274	6748
	FFs	8264	2066	6333	8264

Table 6: **Virtex-6 HXT Family GTX Transceiver Resource Usage for Framing**

Virtex-6 HXT Family		Framing			
		Duplex	Simplex		
Lanes	Resource Type	Full-Duplex	TX Only	RX Only	RX/TX
1	LUTs	541	206	378	536
	FFs	659	223	481	659
2	LUTs	1058	331	783	1058
	FFs	1281	364	971	1281
4	LUTs	2014	565	1534	2017
	FFs	2469	640	1897	2469
8	LUTs	3948	988	3018	3949
	FFs	4838	1176	3749	4838
16	LUTs	8456	1897	5992	8454
	FFs	9583	2268	7453	9583

Table 7: **Virtex-6 HXT Family GTX Transceiver Resource Usage for Streaming**

Virtex-6 HXT Family		Streaming			
		Duplex	Simplex		
Lanes	Resource Type	Full-Duplex	TX Only	RX Only	RX/TX
1	LUTs	474	190	332	474
	FFs	572	206	411	572
2	LUTs	927	293	695	923
	FFs	1110	330	831	1110
4	LUTs	1752	479	1347	1754
	FFs	2132	578	1617	2132
8	LUTs	3427	869	2656	3415
	FFs	4176	1074	3189	4176
16	LUTs	7443	2295	5288	7443
	FFs	8265	2067	6333	8265

Table 8: **Virtex-6 HXT Family GTH Transceiver Resource Usage for Framing**

Virtex-6 HXT Family		Framing			
		Duplex	Simplex		
Lanes	Resource Type	Full-Duplex	TX Only	RX Only	RX/TX
1	LUTs	2637	1684	1155	2637
	FFs	1395	561	974	1395
2	LUTs	5203	3039	2236	5197
	FFs	2657	970	1841	2657
4	LUTs	9876	6122	4341	9883
	FFs	5125	1782	3521	5125
8	LUTs	19694	12808	8677	19707
	FFs	10182	3486	7009	10182
Note: Resource numbers are preliminary and subject to change.					

Table 9: **Virtex-6 HXT Family GTH Transceiver Resource Usage for Streaming**

Virtex-6 HXT Family		Streaming			
		Duplex	Simplex		
Lanes	Resource Type	Full-Duplex	TX Only	RX Only	RX/TX
1	LUTs	2583	1678	1168	2584
	FFs	1314	550	904	1314
2	LUTs	5122	3248	2118	5123
	FFs	2498	948	1701	2498
4	LUTs	9687	6410	4087	9683
	FFs	4812	1744	3241	4812
8	LUTs	19465	12791	8205	19466
	FFs	9568	3432	6449	9568
Note: Resource numbers are preliminary and subject to change.					

Performance

Virtex-5 and Virtex-6 FPGA GTX/GTH transceivers have fewer restrictions on line rate, so the speed of Aurora 64B/66B cores in those devices is typically limited by the f_{MAX} of the FPGA design. The maximum line rate is 6.6 Gbps per GTX transceiver and 11.18 Gbps per GTH transceiver. For more details on core performance, see the *LogiCORE IP Aurora 64B/66B User Guide*.

Verification

The Aurora 64B/66B core is verified using the Aurora 64B/66B BFM and proprietary custom test benches. The Aurora 64B/66B BFM verifies the protocol compliance along with interface level checks

and error scenarios. An automated test system runs a series of simulation tests on the most widely used set of design configurations chosen at random. Aurora 64B/66B cores are also tested in hardware for functionality, performance, and reliability using Xilinx GTX/GTH demonstration boards. Aurora 64B/66B verification test suites for all possible modules are continuously being modified to increase test coverage across the range of possible parameters for each individual module.

Table 10: **Board Used for Verification**

Test Board
ML523
ML623

Support

Xilinx provides technical support for this LogiCORE IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled DO NOT MODIFY.

References

1. Xilinx Aurora Web site: www.xilinx.com/aurora
   - UG237, *LogiCORE IP Aurora 64B/66B User Guide*
   - SP011, *Aurora 64B/66B Protocol Specification*
2. SP006, *LocalLink Interface Specification, v2.0*
3. UG198, *Virtex-5 FPGA RocketIO GTX Transceiver User Guide*
4. UG366, *Virtex-6 FPGA GTX Transceivers User Guide*
5. UG371, *Virtex-6 FPGA GTH Transceivers User Guide*
6. DS152, *Virtex-6 FPGA Data Sheet: DC and Switching Characteristics*

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
03/24/08	1.1	LogiCORE IP Aurora 64B/66B v1.1 release.
03/24/08	1.1.1	Miscellaneous typographical edits.
06/27/08	1.2	Virtex-5 Aurora 64B/66B v1.2 release. Updated Figure 3, page 6. Updated throughput speed range. Expanded definition of User K-blocks in "User K-Block Interface," page 7. Added introductory paragraph to "Resource Utilization," page 8. Replaced *Both* simplex with *RX/TX* simplex. Miscellaneous typographical edits.
09/19/08	1.3	LogiCORE IP Aurora 64B/66B v1.3 release. Added support for VHDL to design format and to HDL Parameter inTable 1, page 4. Added Note to "Native Flow Control Interface," page 7. Updated resource usage inTable 2, page 8 and Table 3, page 8.
04/24/09	2.1	Updated core to v2.1 and tools to 11.1. Added support for the Virtex-5 TXT platform.
09/16/09	3.1	Updated core to v3.1 and tools to 11.3. Added support for the Virtex-6 LXT/SXT/-1L devices.
04/19/10	4.1	LogiCORE IP Aurora 64B/66B v4.1release. Added support for Virtex-6 FPGA HXT sub-family and GTH transceivers. Removed Ordering Information section.

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