LogiCORE IP AXI Thin Film Transistor (TFT) Controller v1.00a

Product Guide

PG095 December 18, 2012

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Appendix C: Additional Resources

Introduction

The Xilinx LogiCORE™ IP Advanced eXtensible Interface (AXI) Thin Film Transistor (TFT) controller is a hardware display controller IP core capable of displaying 256k colors. The AXI TFT Controller connects as a master on the AXI4 and reads the video pixel data from the attached video memory. This core also connects as a slave to the AXI4 bus for the register access. This core is capable of configuring Chrontel CH-7301 DVI Transmitter Chip through I2C interface.

Features

- Connects as 64-bit master on AXI4 bus of 32, 64, or 128 bits data width
- Connects as a 32-bit slave on the AXI4-Lite bus of 32 bits data width
- Parameterizable TFT interface for 18-bit VGA or 24-bit DVI
- Supports 25 MHz TFT clock for display resolution of 640 × 480 pixels at 60Hz refresh rate
- Supports configuration of external Chrontel DVI Transmitter Chip through I2C interface
- Supports separate clock domain for AXI4 interface and TFT interface
- Supports VSYNC Interrupt and Status

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family[1]	Zynq™-7000[2], Virtex®-7, Kintex™-7, Artix™-7
Supported User Interfaces	AXI4, AXI4-Lite
Resources	See Table 2-1 and Table 2-2.
Provided with Core	
Design Files	Vivado™: RTL
Example Design	Not Provided
Test Bench	Not Provided
Constraints File	Vivado: XDC
Simulation Model	Not Provided
Supported S/W Driver	N/A
Tested Design Flows[3]	
Design Entry	Vivado Design Suite 2012.4[4]
Simulation	Mentor Graphics ModelSim
Synthesis	Vivado Synthesis
Support	
Provided by Xilinx @ www.xilinx.com/support	

Notes:

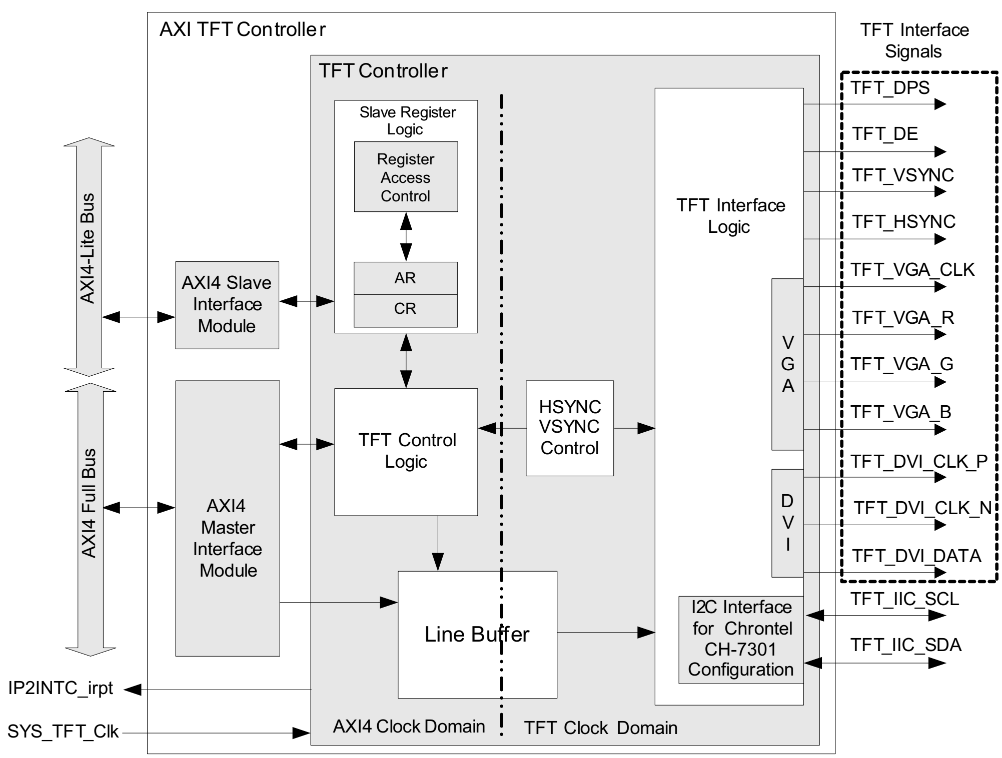
1. For a complete list of supported derivative devices, see Embedded Edition Derivative Device Support.
2. Supported in ISE Design Suite implementations only.
3. For the supported versions of the tools, see the Xilinx Design Tools: Release Notes Guide.
4. Supports only 7 series devices.

Overview

Functional Description

The AXI TFT Controller core IP is a hardware display controller for a 640 × 480 resolution display screen. This core is capable of displaying up to 256K colors through VGA or DVI interface. The design contains an AXI4 master interface that reads video data from an attached memory device and displays the data onto the TFT screen. The design also contains an AXI4 slave interface for register access.

This controller also provides an I2C interface to configure Chrontel CH-7301 video encoder chip when the DVI interface is selected. Figure 1-1 shows the AXI TFT Controller block diagram.



Notes:
1. DVI interface is included in the design if the parameter C_TFT_INTERFACE = 1.
2. VGA interface is included in the design if the parameter C_TFT_INTERFACE = 0.
3. This logic is included in the design if C _TFT_INTERFACE = 1.

Figure 1-1: **AXI TFT Controller Block Diagram**

The major modules of AXI TFT Controller are described in the following sections. These modules include:

- AXI4 Master Interface Module
- AXI4 Slave Interface Module
- Slave Register Logic
- TFT Control Logic
- Line Buffer
- HSYNC/VSYNC Control
- TFT Interface Logic

AXI4 Master Interface Module

The AXI4 Master Interface module provides a master interface between the AXI TFT Controller and the AXI4 bus. The AXI TFT Controller reads pixel data from an external AXI4 memory device through the AXI4 Master Interface module. This addresses bus interface signals, bus protocol, and other interface issues. The master interface supports 32, 64, and 128-bit data width, and 32-bit address width.

AXI4 Slave Interface Module

The AXI4 Slave Interface module provides an interface between Slave Register Logic and AXI4-Lite bus. The AXI TFT Controller registers can be accessed through AXI4 using this interface. This module generates signals that are required for the AXI4-Lite interface and IPIF interface on the TFT side.

Slave Register Logic

The Slave Register Logic module consists of the Address register (AR), Control register (CR), and logic that provide the access to these registers using the AXI4 interface. The Address register allows you to change the base address of video memory to be read from. This allows video frames to be fetched from other memory locations without being seen on the display. You can change the video memory base address to display a different frame when it is ready. The Control register allows the display to be rotated by 180 degrees or to be turned off by configuring the control bits.

TFT Control Logic

The TFT Control Logic module generates read request to AXI4 Master Interface module to get pixel data from an external AXI4 memory device. This module synchronizes the signals crossing the different clock domains. The TFT control logic generates master read request, address for the video memory, and reads the pixel data for each display line using a series of 16-double word burst transactions. The pixel data is stored in an internal line buffer and then sent out to the TFT display with the necessary timing to correctly display the image. This process repeats continuously over every line and frame to be displayed on the 640 × 480 TFT screen.

Figure 1-2 shows the data flow diagram from the AXI4 clock domain to the TFT clock domain. The display is turned off by clearing the display enable bit in the Control register. The TFT controller then issues a reset to all the counters. It stops requesting data from the video memory by applying reset to the Master Interface module. In the reset state, the controller sets the HSYNC and VSYNC to their default value causing the display to enter in sleep mode.

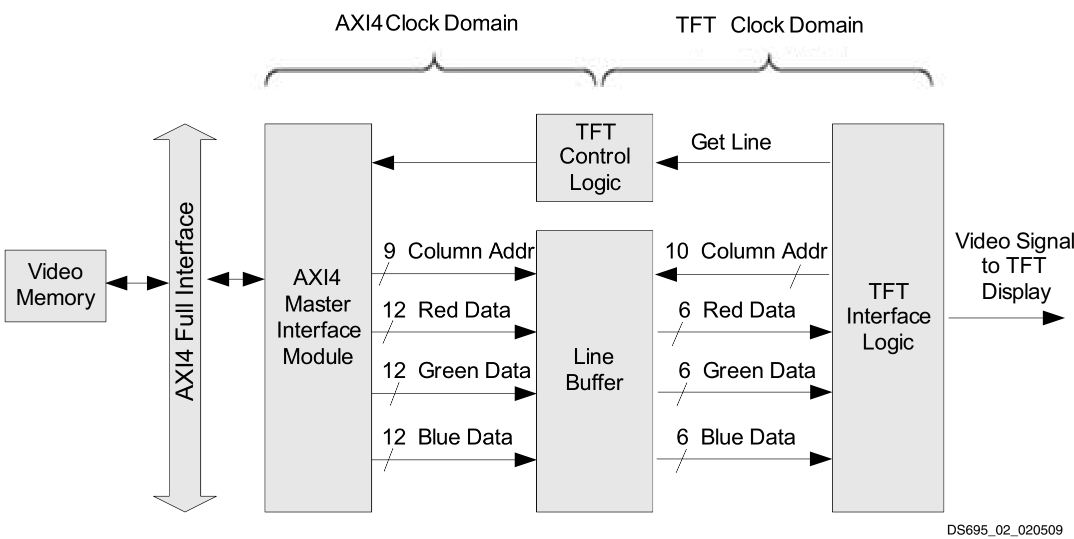


Figure 1-2: **Data Flow Diagram**

Line Buffer

The AXI TFT Controller allows the AXI4 clock and TFT video clock to be asynchronous to each other. The line buffer module includes synchronization logic to allow the passing of control signals to be passed between asynchronous AXI4 and TFT clock domains. This module consists of a dual port 1 KB × 18-bit block RAM which is used as the line buffer to pass video data between the two clock domains. Out of 64-bit AXI4 data, the 36-bit of RGB data is written to the block RAM.

HSYNC/VSYNC Control

This module generates the timing necessary for the video synchronization signals including back porch and front porch timing for HSYNC and VSYNC. For more information, see Chapter 3, Video Timing.

TFT Interface Logic

The TFT interface logic driving the TFT display operates in the same clock domain as the video clock. It reads out the pixel data from the dual port line buffer and transmits it to the TFT. This module consists of logic to transmit the pixel data in either VGA or DVI format based on the parameter C_TFT_INTERFACE and the logic to configure the Chrontel CH-7301 video encoder chip. The HSYNC, VSYNC, and DE signals are common for both the interfaces. The following VGA, DVI, and Chrontel I2C interfaces are described in the following sections.

VGA Interface

The VGA interface logic is included in the design if the parameter C_TFT_INTERFACE is set to 0. The 18-bit RGB pixel data is transmitted to the VGA ports and logic 0 is transmitted to all DVI ports.

DVI Interface

The DVI interface logic is included in the design if the parameter C_TFT_INTERFACE is set to 1. The 18-bit RGB data is converted into 24-bit pixel data by padding zeroes in between the RGB data. This 24-bit pixel data is transmitted to the 12-bit DVI data port by clocking the data on both edges using the double data rate registers shown in Figure 1-3. The 18-bit RGB pixel data translation to 24-bit DVI data is shown in Table 1-1.

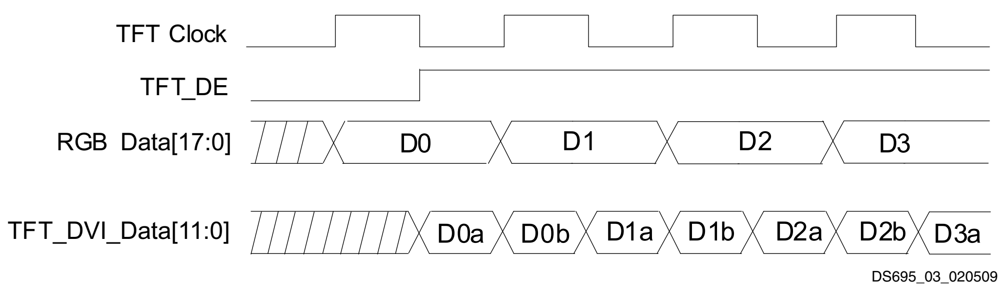


Figure 1-3: **RGB to DVI Data**

Table 1-1: **RGB to DVI Data Conversion**

DVI Data	Data A	Data B
TFT_DVI_DATA[0]	0	G[2]
TFT_DVI_DATA[1]	0	G[3]
TFT_DVI_DATA[2]	B[0]	G[4]
TFT_DVI_DATA[3]	B[1]	G[5]
TFT_DVI_DATA[4]	B[2]	0
TFT_DVI_DATA[5]	B[3]	0
TFT_DVI_DATA[6]	B[4]	R[0]
TFT_DVI_DATA[7]	B[5]	R[1]
TFT_DVI_DATA[8]	0	R[2]

Table 1-1: **RGB to DVI Data Conversion *(Cont'd)***

DVI Data	Data A	Data B
TFT_DVI_DATA[9]	0	R[3]
TFT_DVI_DATA[10]	G[0]	R[4]
TFT_DVI_DATA[11]	G[1]	R[5]

Chrontel I2C Interface

The Chrontel I2C interface logic is included in the design if the parameter C_TFT_INTERFACE is set to 1. This module consists of logic to configure the Chrontel CH-7301 video encoder chip. The configuration sequence logic is hard coded in this module and the data is sent over I2C interface. This core configures only the basic registers of the CH-7301 chip for DVI interface. The AXI TFT Controller remains in the reset state until the controller completes configuration of the Chrontel chip.

The description of these register addresses and the configuration data is shown in Table 1-2. If you want a different configuration for the Chrontel chip, you can configure the device using the Chrontel Chip Configuration register (CCR). For more information on the Chrontel DVI transmitter, see the *Chrontel CH-7301 DVI Transmitter Device Specification* [Ref 5].

Table 1-2: **Chrontel CH-7301 Configuration Register Descriptions**

Register Address	Register Name	Configuration Data	Access	Description
0x49	PM	0xC0	Write	Power Management Register
0x21	DC	0x09	Write	DAC Control Register
0x33	TPCP	0x08	Write	PLL Charge Pump Control Register
0x34	TPD	0x16	Write	PLL Divider Register
0x36	TPF	0x60	Write	PLL Filter Register

Applications

This core is used for VGA or DVI LCD panel applications. This core supports 640 × 480 resolution display screen.

Unsupported Features

The AXI TFT Controller is configured to the Chrontel CH-7301 chip only. If the system has a video encoder chip other than Chrontel CH-7301, you must take care of the chip configuration.

Licensing and Ordering Information

This Xilinx LogiCORE IP module is provided at no additional cost with the Xilinx Vivado Design Suite tool under the terms of the Xilinx End User License.

Information about this and other Xilinx LogiCORE IP modules is available at the Xilinx Intellectual Property page. For information on pricing and availability of other Xilinx LogiCORE IP modules and tools, contact your local Xilinx sales representative.

Product Specification

Standards

The AXI TFT Controller IP core is AXI4 and AXI4-Lite compliant.

Resource Utilization

Because the AXI TFT Controller core is used with other design modules in the FPGA, the utilization and timing numbers reported in this section are estimates only. When the AXI TFT Controller core is combined with other designs in the system, the utilization of FPGA resources and timing of the AXI TFT Controller design varies from the results reported here.

The AXI TFT Controller resource utilization for various parameter combinations measured with the 7 series and Zynq-7000 as the target devices are detailed in Table 2-1 and Table 2-2.

Table 2-1: **Performance and Resource Utilization Benchmarks on the Virtex-7 FPGA**

Parameter Values		Device Resources			Performance
C_M_AXI_DATA_WIDTH	**C_TFT_INTERFACE**	**Slices**	**Slice Flip-Flops**	**LUTs**	**F_{MAX} (MHz)**
32	0	295	699	476	200
32	1	314	763	547	200
64	0	271	718	499	200
64	1	287	782	571	200
128	0	261	719	536	200
128	1	305	783	608	200

Table 2-2: **Performance and Resource Utilization Benchmarks on the Kintex-7, Artix-7, and Zynq-7000 Devices**

Parameter Values		Device Resources			Performance
C_M_AXI_DATA_WIDTH	**C_TFT_INTERFACE**	**Slices**	**Slice Flip-Flops**	**LUTs**	**F_{MAX} (MHz)**
32	0	260	699	728	200
32	1	290	763	843	200
64	0	260	718	751	200
64	1	304	782	872	200
128	0	255	719	759	200
128	1	307	783	864	200

Port Descriptions

The AXI TFT Controller I/O signals are described in Table 2-3.

Table 2-3: **AXI TFT Controller I/O Signal Description**

Port	Signal Name	Interface	I/O	Initial State	Description
System Signals					
P1	M_AXI_ACLK	System	I	–	AXI4 Master Clock
P2	M_AXI_ARESETN	System	I	–	AXI4 Master Reset
P3	S_AXI_ACLK(1)	System	I	–	AXI4 Slave Clock
P4	S_AXI_ARESETN	System	I	–	AXI4 Slave Reset
P5	MD_ERROR	System	O	0	Master Error Detection Indicator (Active-High)
P6	IP2INTC_Irpt	System	O	0	VSYNC Pulse Interrupt
AXI4 Master Interface Signals					
AXI4 Master Burst Read Address Channel					
P7	M_AXI_ARREADY	MAXI	I	–	Read Address Ready. Indicates target is ready to accept the read address. 0 = Target not ready to accept address 1 = Target read to accept address
P8	M_AXI_ARVALID	MAXI	O	0	AXI4 Master Burst Read Address Channel Read Address Valid. Indicates if m_axi_araddr is valid. 0 = Read Address is not valid 1 = Read Address is valid

Table 2-3: **AXI TFT Controller I/O Signal Description *(Cont'd)***

Port	Signal Name	Interface	I/O	Initial State	Description
P9	M_AXI_ARADDR[C_M_AXI_ ADDR_WIDTH - 1: 0]	MAXI	O	0	AXI4 Master Burst Read Address Channel Address Bus. The starting address for the requested read transaction.
P10	M_AXI_ARLEN[7:0]	MAXI	O	0	AXI4 Master Burst Read Address Channel Burst Length. This qualifier specifies the requested AXI4 Read transaction length In data beats - 1.
P11	M_AXI_ARSIZE[2:0]	MAXI	O	0	AXI4 Master Burst Read Address Channel Burst Size. Indicates the data transaction width of each burst data beat. 000 = Not supported by AXI4 Master burst 001 = Not supported by AXI4 Master burst 010 = 4 bytes (32-bit wide burst) 011 = 8 bytes (64-bit wide burst) 100 = 16 bytes (128-bit wide burst) 101 = Not supported by AXI4 Master burst 110 = Not supported by AXI4 Master burst 111 = Not supported by AXI4 Master burst
P12	M_AXI_ARBURST[1:0]	MAXI	O	0	AXI4 Master Burst Read Address Channel Burst Type. Indicates type of burst. 00 = FIXED – Not supported 01 = INCR – Incrementing address 10 = WRAP – Not supported 11 = Reserved
P13	M_AXI_ARPROT[2:0]	MAXI	O	000	AXI4 Master Burst Read Address Channel Protection. This is always driven with a constant output of 000b.
P14	M_AXI_ARCACHE[3:0]	MAXI	O	0011	AXI4 Master Burst Read Address Channel Cache. This is always driven with a constant output of 0011.
AXI4 Master Read Data Channel					
P15	M_AXI_RREADY	MAXI	O	0	AXI4 Master Burst Read Data Channel Ready. Indicates the read channel is ready to accept read data. 0 = Is not ready 1 = Is ready

Table 2-3: **AXI TFT Controller I/O Signal Description *(Cont'd)***

Port	Signal Name	Interface	I/O	Initial State	Description
P16	M_AXI_RVALID	MAXI	I	–	AXI4 Master Burst Read Data Channel Data Valid. Indicates m_axi_rdata is valid. 0 = Not valid read data 1 = Valid read data
P17	M_AXI_RDATA[C_M_AXI_ DATA_WIDTH - 1: 0]	MAXI	I	–	AXI4 Master Burst Read Data Channel Read Data. Read data bus for the requested read transaction.
P18	M_AXI_RRESP[1:0]	MAXI	I	–	AXI4 Master Burst Read Data Channel Response. Indicates results of the read transaction. 00 = OKAY – Normal access has been successful 01 = EXOKAY – Not supported 10 = SLVERR – Slave returned error on transaction 11 = DECERR – Decode error, transaction targeted unmapped address
P19	M_AXI_RLAST	MAXI	I	–	AXI4 Master Burst Read Data Channel Last. Indicates the last data beat of a burst transaction. 0 = Not last data beat 1 = Last data beat
AXI4 Master Write Address Channel					
P20	M_AXI_AWREADY	MAXI	I	–	AXI4 Master Burst Write Address Channel Write Address Ready. Indicates target is ready to accept the write address. 0 = Target not ready to accept address 1 = Target ready to accept address
P21	M_AXI_AWVALID	MAXI	O	0	AXI4 Master Burst Write Address Channel Write Address Valid. Indicates if m_axi_awaddr is valid. 0 = Write Address is not valid 1 = Write Address is valid
P22	M_AXI_AWADDR[C_M_AXI_ ADDR_WIDTH - 1: 0]	MAXI	O	0	AXI4 Master Burst Write Address Channel Address Bus. The starting address for the requested write transaction.
P23	M_AXI_AWLEN[7:0]	MAXI	O	0	AXI4 Master Burst Write Address Channel Burst Length. This qualifier specifies the requested AXI4 Write transaction length In data beats - 1.

Table 2-3: **AXI TFT Controller I/O Signal Description *(Cont'd)***

Port	Signal Name	Interface	I/O	Initial State	Description
P24	M_AXI_AWSIZE[2:0]	MAXI	O	0	AXI4 Master Burst Write Address Channel Burst Size. Indicates the data transaction width of each burst data beat. 000 = Not supported by AXI4 Master burst 001 = Not supported by AXI4 Master burst 010 = 4 bytes (32-bit wide burst) 011 = 8 bytes (64-bit wide burst) 100 = 16 bytes (128-bit wide burst) 101 = Not supported by AXI4 Master burst 110 = Not supported by AXI4 Master burst 111 = Not supported by AXI4 Master burst
P25	M_AXI_AWBURST[1:0]	MAXI	O	0	AXI4 Master Burst Write Address Channel Burst Type. Indicates type of burst. 00 = FIXED – Not supported 01 = INCR – Incrementing address 10 = WRAP – Not supported 11 = Reserved
P26	M_AXI_AWPROT[2:0]	MAXI	O	000	AXI4 Master Burst Write Address Channel Protection. This is always driven with a constant output of 000.
P27	M_AXI_AWCACHE[3:0]	MAXI	O	0011	AXI4 Master Burst Write Address Channel Cache. This is always driven with a constant output of 0011.
AXI4 Master Write Data Channel					
P28	M_AXI_WREADY	MAXI	I	–	AXI4 Master Burst Write Data Channel Ready. Indicates the SG Write Data Channel target slave is ready to accept write data. 0 = Target slave is not ready 1 = Target slave is ready
P29	M_AXI_WVALID	MAXI	O	0	AXI4 Master Burst Write Data Channel Data Valid. Indicates the Write Data Channel has a valid data beat on the bus. 0 = Not valid write data 1 = Valid write data
P30	M_AXI_WDATA[C_M_AXI_ DATA_WIDTH - 1: 0]	MAXI	O	0	AXI4 Master Burst Write Data Channel Write Data Bus
P31	M_AXI_WSTRB[C_M_AXI_ DATA_WIDTH/8 - 1: 0]	MAXI	O	0	AXI4 Master Burst Write Data Channel Write Strobe Bus

Table 2-3: **AXI TFT Controller I/O Signal Description *(Cont'd)***

Port	Signal Name	Interface	I/O	Initial State	Description
P32	M_AXI_WLAST	MAXI	O	–	AXI4 Master Burst Write Data Channel Last. Indicates the last data beat of a burst transaction. 0 = Not last data beat 1 = Last data beat
AXI4 Master Write Response Channel					
P33	M_AXI_BRESP[1:0]	MAXI	I	–	AXI4 Master Burst Write Response Channel Response. Indicates results of the write transaction. 00 = OKAY – Normal access has been successful 01 = EXOKAY – Not supported 10 = SLVERR – Slave returned error on transaction 11 = DECERR – Decode error, transaction targeted unmapped address
P34	M_AXI_BVALID	MAXI	I	–	AXI4 Master Burst Write Response Channel Response Valid. Indicates response, m_axi_bresp, is valid. 0 = Response is not valid 1 = Response is valid
P35	M_AXI_BREADY	MAXI	O	0	AXI4 Master Burst Write Response Channel Ready. Indicates source is ready to receive response. 0 = Not ready to receive response 1 = Ready to receive response
AXI4 Slave Interface Signals					
SAXI Write Address Channel Signals					
P36	S_AXI_AWADDR[31:0]	SAXI	I	–	AXI4 Write Address. The write address bus gives the address of the write transaction.
P37	S_AXI_AWVALID	SAXI	I	–	Write Address Valid. This signal indicates that valid write address and control information are available.
P38	S_AXI_AWREADY	SAXI	O	0	Write Address Ready. This signal indicates that the slave is ready to accept an address and associated control signals.
SAXI Write Data Channel Signals					
P39	S_AXI_WDATA[31:0]	SAXI	I	–	Write Data
P40	S_AXI_WSTB[3:0]	SAXI	I	–	Write Strobes. This signal indicates which byte lanes to update in memory.

Table 2-3: **AXI TFT Controller I/O Signal Description *(Cont'd)***

Port	Signal Name	Interface	I/O	Initial State	Description
P41	S_AXI_WVALID	SAXI	I	–	Write Valid. This signal indicates that valid write data and strobes are available.
P42	S_AXI_WREADY	SAXI	O	0	Write Ready. This signal indicates that the slave can accept the write data.
SAXI Write Response Channel Signals					
P43	S_AXI_BRESP[1:0]	SAXI	O	0	Write Response. This signal indicates the status of the write transaction. 00 = OKAY 10 = SLVERR
P44	S_AXI_BVALID	SAXI	O	0	Write Response Valid. This signal indicates that a valid write response is available.
P45	S_AXI_BREADY	SAXI	I	–	Response Ready. This signal indicates that the master can accept the response information.
SAXI Read Address Channel Signals					
P46	S_AXI_ARADDR[31:0]	SAXI	I	–	Read Address. The read address bus gives the address of a read transaction.
P47	S_AXI_ARVALID	SAXI	I	–	Read Address Valid. This signal indicates, when high, that the read address and control information is valid and remains stable until the address acknowledgement signal, S_AXI_ARREADY, is high.
P48	S_AXI_ARREADY	SAXI	O	0	Read Address Ready. This signal indicates that the slave is ready to accept an address and associated control signals.
SAXI Read Data Channel Signals					
P49	S_AXI_RDATA[31:0]	SAXI	O	0	Read Data
P50	S_AXI_RRESP[1:0]	SAXI	O	0	Read Response. This signal indicates the status of the read transfer.
P51	S_AXI_RVALID	SAXI	O	0	Read Valid. This signal indicates that the required read data is available and the read transfer can complete.
P52	S_AXI_RREADY	SAXI	I	–	Read Ready. This signal indicates that the master can accept the read data and response information.
TFT Interface Signals					
P53	SYS_TFT_Clk	TFT	I	–	TFT Clock Input
P54	TFT_HSYNC	TFT	O	1	Horizontal Sync (Active-Low)
P53	TFT_VSYNC	TFT	O	1	Vertical Sync (Active-Low)

Table 2-3: **AXI TFT Controller I/O Signal Description *(Cont'd)***

Port	Signal Name	Interface	I/O	Initial State	Description
P54	TFT_DE	TFT	O	0	Data Enable
P55	TFT_DPS	TFT	O	0	TFT Display Scan
P56	TFT_VGA_CLK	TFT-VGA	O	0	TFT VGA Clock[1]
P57	TFT_VGA_R[5:0]	TFT-VGA	O	0	TFT VGA Red Pixel Data[1]
P58	TFT_VGA_G[5:0]	TFT-VGA	O	0	TFT VGA Green Pixel Data[1]
P59	TFT_VGA_B[5:0]	TFT-VGA	O	0	TFT VGA Blue Pixel Data[1]
P60	TFT_DVI_CLK_P	TFT-DVI	O	0	Differential TFT DVI Clock[2]
P61	TFT_DVI_CLK_N	TFT-DVI	O	0	Differential TFT DVI Clock[2]
P62	TFT_DVI_DATA[11:0]	TFT-DVI	O	0	TFT DVI Data[2]
P63	TFT_IIC_SCL_O	TFT-DVI	O	0	I2C Output Clock to Chrontel Chip[3]
P64	TFT_IIC_SCL_I	TFT-DVI	I	–	I2C input Clock from Chrontel Chip[3]
P65	TFT_IIC_SCL_T	TFT-DVI	O	1	3-State Control for I2C Clock[3]
P66	TFT_IIC_SDA_O	TFT-DVI	O	0	I2C Output Data to Chrontel Chip[3]
P67	TFT_IIC_SDA_I	TFT-DVI	I	–	I2C Input Data from Chrontel Chip[3]
P68	TFT_IIC_SDA_T	TFT-DVI	O	1	3-State Control for I2C Data[3]

Notes:
1. VGA interface signals.
2. DVI interface signals.
3. I2C signals are used to configure Chrontel Video Encoder chip. These ports are active when DVI interface is selected.

Register Space

There are four internal registers available in the AXI TFT Controller. The internal registers of the AXI TFT Controller are at a fixed offset from the base address on a 32-bit boundary. Writing into the reserved registers has no effect. Reading from the reserved registers returns 0.

All registers are defined for 32-bit access only. Any partial word write access (byte, half-word) has no effect on the registers and any partial word read access (byte, half-word) returns 0. All partial access to the core register returns bus error. The AXI TFT Controller internal registers and their offsets are listed in Table 2-4. The BASEADDR and HIGHADDR values for the IP are defined by the Vivado tool address mapping.

IMPORTANT: *The BASEADDR and HIGHADDR are not parameters.*

Table 2-4: **AXI TFT Controller Internal Register Map**

Base Address + Offset	Register Name	Access	Default Value (Hex)	Description
BASEADDR + 0x00	AR	R/W	C_DEFAULT_TFT_BASE_ADDR	TFT Address register which specifies the base address of the video memory from which the controller fetches the data.
BASEADDR + 0x04	CR	R/W	0x1	TFT Control Register
BASEADDR + 0x08	IESR	R/W	0x0	VSYNC Interrupt Enable and Status Register
BASEADDR + 0x0C	CCR	R/W	0x0	Chrontel Configuration Register

Address Register (AR)

TFT Base Address register specifies the upper 11 bits of base address of the video memory. This is the address of AXI4 accessible memory device that acts as a video memory. This address must be aligned on a 2 MB boundary (that is, only upper 11 bits are writable, the remaining address bits are always 0) as shown in Figure 2-1 and described in Table 2-5.

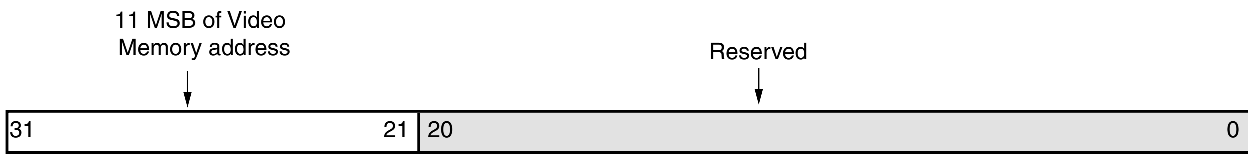


Figure 2-1: **Address Register**

Table 2-5: **Address**

Bits	Name	Reset Value	Core Access	Description
31:21	TFT base address	C_DEFAULT_TFT_BASE_ADDR [10:0]	R/W	Specifies the base address of the video memory from which the controller fetched the data.
20:0	Reserved	N/A	N/A	Reserved

Control Register (CR)

TFT Control register contains the control bits to configure the controller for TFT scanning mode and TFT display on/off. Writing a 0 in TFT display enable bit resets the TFT controller. In the reset state, controller stops requesting data from the video memory by applying reset to the Master Interface module and set the HSYNC and VSYNC to their default value causing the display to enter in sleep mode. The bit assignment in the TFT Control register is shown in Figure 2-2 and described in Table 2-6.

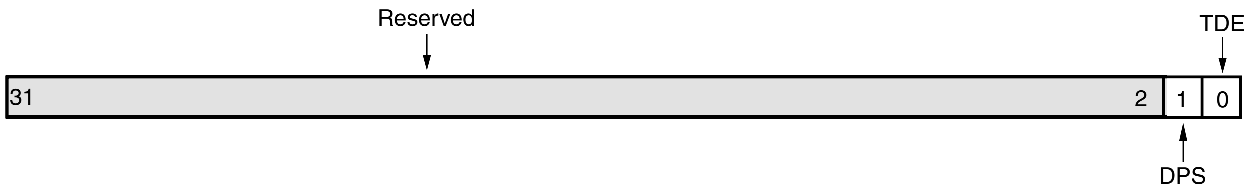


Figure 2-2: **Control Register**

Table 2-6: **Control**

Bits	Name	Reset Value	Core Access	Description
31:2	Reserved	N/A	N/A	Reserved
1	DPS	0	R/W	Display Scan Control Bit 0 = Set DPS output bit to 0. This sets the display to use normal scan direction. 1 = Set DPS output bit to 1. This sets the display to use reverse scan direction (rotates screen 180 degrees).
0	TDE	1	R/W	TFT Display Enable Bit 0 = Disable TFT display. This resets the TFT controller and stops VSYNC/HSYNC signals causing display to go in sleep mode. 1 = Enable TFT display. This causes the TFT controller to operate normally.

Interrupt Enable and Status Register (IESR)

TFT Interrupt Enable and Status register is a 32-bit read/write register. This register contains VSYNC interrupt enable bit and the status bit. If VSYNC interrupt is enabled, core generates interrupt for VSYNC pulse every frame. For every rising edge of VSYNC pulse, core set status bit to indicate that core has displayed the current frame completely and accepted the new address from the AR. This status bit gets cleared for every write access to the AR. The bit assignment in the IESR is shown in Figure 2-3 and described in Table 2-7.

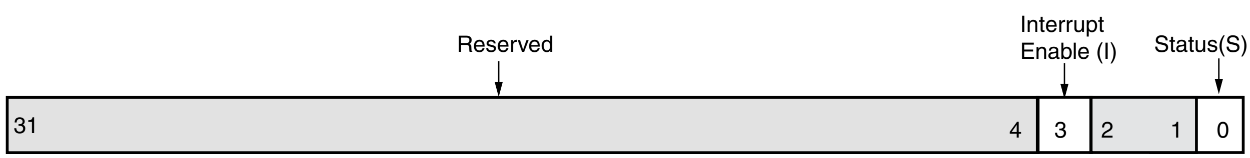


Figure 2-3: **Interrupt Enable and Status Register**

Table 2-7: **Interrupt Enable and Status**

Bits	Name	Reset Value	Core Access	Description
31:4	Reserved	N/A	N/A	Reserved
3	Interrupt Enable	0	R/W	VSYNC Interrupt Enable 0 = Disable VSYNC pulse interrupt 1 = Enable VSYNC pulse interrupt

Table 2-7: **Interrupt Enable and Status *(Cont'd)***

Bits	Name	Reset Value	Core Access	Description
2:1	Reserved	N/A	N/A	Reserved
0	Status	0	R/W	VSYNC and Address Latch Status Bit 0 = Core is displaying current frame. 1 = VSYNC pulse is active. Also indicate that previous frame is displayed completely and core has accepted new address from the AR.

Chrontel Chip Configuration Register (CCR)

The Chrontel Chip Configuration register is a 32-bit read/write register. This register contains IIC transmission start bit, Chrontel chip register address and Chrontel chip register data. This register enables the user to configure the Chrontel chip register on-the-fly. Setting Bit[0] of the this register initiates the IIC transmission to the Chrontel chip. This bit is cleared when the IIC transmission is complete. The bit assignment in the CCR is shown in Figure 2-4 and described in Table 2-8.

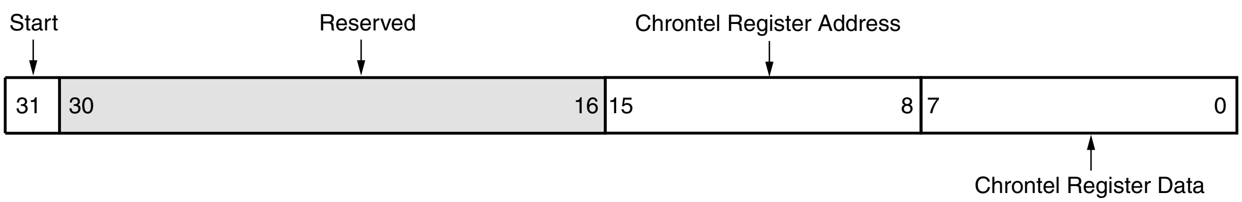


Figure 2-4: **Chrontel Chip Configuration Register**

Table 2-8: **Chrontel Chip Configuration**

Bits	Name	Reset Value	Core Access	Description
31	Start	0	R/W	Setting this bit starts IIC data transmission to the Chrontel chip.
30:16	Reserved	N/A	N/A	Reserved
15:8	ADDR	0	R/W	8-bit Chrontel Chip Register Address
7:0	DATA	0	R/W	8-bit Chrontel Chip Register Data

Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the core.

AXI TFT Controller Design Parameters

To create an AXI TFT Controller that is uniquely tailored for your system, certain features are parameterizable in the AXI TFT Controller design. This allows you to use only the resources required by the system and to achieve the best possible performance. The features that are parameterizable in the AXI TFT Controller core are shown in Table 3-1.

Table 3-1: **AXI TFT Controller Design Parameters**

Generic	Parameter Name	Allowable Values	Default Value	VHDL Type	Feature/ Description
AXI TFT Controller Parameter					
G1	C_FAMILY	Virtex7, Kintex7, Artix7, Zynq	virtex7	String	Target FPGA family
G2	C_DEFAULT_TFT_BASE_ADDR(1)	Valid address	0xF0000000	std_logic_ vector	Base address of AXI4 attached Video memory
G3	C_TFT_INTERFACE	0 = VGA interface 1 = DVI interface	1	Integer	TFT interface selection
G4	C_I2C_SLAVE_ADDR	Valid 7-bit I2C slave address	1110110	std_logic_ vector	I2C Slave address of external Chrontel DVI transmitter
AXI4 Master Interface Parameters					
G5	C_M_AXI_ADDR_WIDTH	32	32	Integer	Address bus width of AXI4 master interface
G6	C_M_AXI_DATA_WIDTH	32, 64, 128	64	Integer	Data bus width of the AXI4 master interface

Table 3-1: **AXI TFT Controller Design Parameters *(Cont'd)***

Generic	Parameter Name	Allowable Values	Default Value	VHDL Type	Feature/ Description
G7	C_MAX_BURST_LEN	16, 32, 64, 128, 256	16	Integer	Maximum number of burst for AXI4 master

Notes:

1. C_DEFAULT_TFT_BASE_ADDR specifies the base address of attached video memory. This base address of video memory must be aligned on a 2 MB boundary (that is, only upper 11 bits are valid, the remaining address bits must be always 0). The controller only uses 11 MSB of this base address to read data from the video memory.

Allowable Parameter Combinations

The address specified by C_DEFAULT_TFT_BASE_ADDR must be aligned on a 2 MB boundary. Only 11 MSB bits should have valid addresses, the remaining address bits must always be 0.

Optimal System Settings

RECOMMENDED: *Xilinx recommends having separate buses for the video memory access from the core and the rest of the system. There is sufficient bandwidth available between the AXI TFT Controller and AXI4 memory device to achieve this.*

The native data width of the AXI TFT Controller is fixed to 64 bits. Optimal performance is achieved when the video memory interface width is greater than or equal to native data width of AXI4 master interface.

AXI TFT Controller Parameter – I/O Signal Dependencies

The dependencies between the AXI TFT Controller core design parameters and I/O signals are described in Table 3-2. When certain features are parameterized out of the design, the related logic is no longer part of the design. The unused input signals and related output signals are set to a specified value.

Table 3-2: **AXI TFT Controller Parameter – I/O Signal Dependencies**

Generic or Port	Name	Affects	Depends	Relationship Description
Design Parameters				
G3	C_TFT_INTERFACE	P56–P68	–	Affects TFT interface ports. If C_TFT_INTERFACE = 0, all DVI ports are tied to 0. If C_TFT_INTERFACE = 1, all VGA ports are tied to 0.
G4	C_I2C_SLAVE_ADDR	–	G3	Depends on C_TFT_INTERFACE. Required only when DVI interface is selected.
G6	C_M_AXI_ADDR_WIDTH	P9,P22	–	Affects the number of bits in AXI4 master Address signals.
G6	C_M_AXI_DATA_WIDTH	P17, P30, P31	–	Affects the number of bits in AXI4 master data bus.
I/O Signals				
P9	m_axi_araddr[C_M_AXI_ ADDR_WIDTH - 1: 0]	–	G5	Width varies with the size of the AXI4 address bus.
P9	m_axi_awaddr[C_M_AXI_ ADDR_WIDTH - 1: 0]	–	G5	Width varies with the size of the AXI4 address bus.
P17	m_axi_rdata[C_M_AXI_ DATA_WIDTH - 1: 0]	–	G6	Width varies with the size of the AXI4 master data bus.
P30	m_axi_wdata[C_M_AXI_ DATA_WIDTH - 1: 0]	–	G6	Width varies with the size of the AXI4 master data bus.
P31	m_axi_wstrb[C_M_AXI_ DATA_WIDTH / 8 - 1: 0]	–	G6	Width varies with the size of the AXI4 master data bus.
P56	TFT_VGA_CLK	–	G3	Port tied to 0 when C_TFT_INTERFACE = 1
P57	TFT_VGA_R	–	G3	Ports tied to 0 when C_TFT_INTERFACE = 1
P58	TFT_VGA_G	–	G3	Ports tied to 0 when C_TFT_INTERFACE = 1
P59	TFT_VGA_B	–	G3	Ports tied to 0 when C_TFT_INTERFACE = 1
P60	TFT_DVI_CLK_P	–	G3	Port tied to 0 when C_TFT_INTERFACE = 0
P61	TFT_DVI_CLK_N	–	G3	Port tied to 0 when C_TFT_INTERFACE = 0
P62	TFT_DVI_DATA	–	G3	Ports tied to 0 when C_TFT_INTERFACE = 0
P63	TFT_IIC_SCL_O	–	G3	Port tied to 0 when C_TFT_INTERFACE = 0
P64	TFT_IIC_SCL_I	–	G3	Port is unused when C_TFT_INTERFACE = 0
P65	TFT_IIC_SCL_T	–	G3	Port tied to 0 when C_TFT_INTERFACE = 0
P66	TFT_IIC_SDA_O	–	G3	Port tied to 0 when C_TFT_INTERFACE = 0
P67	TFT_IIC_SDA_I	–	G3	Port is unused when C_TFT_INTERFACE = 0
P68	TFT_IIC_SDA_T	–	G3	Port tied to 0 when C_TFT_INTERFACE = 0

Clocking

The AXI TFT Controller has three clock domains each for AXI slave interface, AXI master interface, and TFT clock domain. The following clocks are provided as input to the core.

- **S_AXI_ACLK** – Associates with the AXI4 slave interface
- **M_AXI_ACLK** – Relates to the AXI4 master interface
- **SYS_TFT_Clk** – Applies with the TFT side interface (that is, VGA or DVI)

The AXI slave or master clocks can be operated up to 200 MHz frequency. The TFT clock is a slow operating clock with a constant frequency of 25 MHz.

Resets

The AXI TFT Controller has two external reset signals each associated with AXI slave and AXI master interface. The reset signal `S_AXI_ARESETN` is a synchronous reset input that resets the AXI slave interface and the register logic. The `M_AXI_ARESETN` signal is used to reset the AXI master interface, internal buffers, and TFT interface logic.

Protocol Description

Video Timing

The signal timings for 640 × 480 display using a 25 MHz pixel clock are shown in Table 3-3. The AXI TFT Controller takes 16.8 ms to display each 640 × 480 display frame at 60Hz refresh rate on the TFT. To display the complete frame on the TFT, you should not update the video memory start Address (AR) before this time frame.

Table 3-3: **640 × 480 Mode Display Timing**

Symbol	Parameter	Vertical Sync			Horizontal Sync	
		Time	Clocks	Lines	Time	Clocks
T_{PULSE}	Sync pulse time	16.8 ms	420000	525	32 µs	800
T_{Disp}	Display time	15.4 ms	384000	480	25.6 µs	640
T_{PW}	Pulse width time	64 µs	1600	2	3.84 µs	96
T_{BP}	Back porch time	992 µs	24800	31	1.92 µs	48
T_{FP}	Front porch time	384 µs	9600	12	640 ns	16

HSYNC Timing

The HSYNC is an active-Low signal and the complete time period of the HSYNC is 800 TFT clocks. Out of the 800 TFT clock period, the active pixel data qualified by the active-High DE signal is 640 TFT clocks. The HSYNC pulse period is 96 TFT clocks. The time period between the HSYNC pulse and start of the active data is called a back porch which is 48 TFT clocks. The time period between the end of active data and start of the new HSYNC pulse is called a front porch which is 16 TFT clocks. The HSYNC timing with respect to the TFT clock is shown in Figure 3-1.

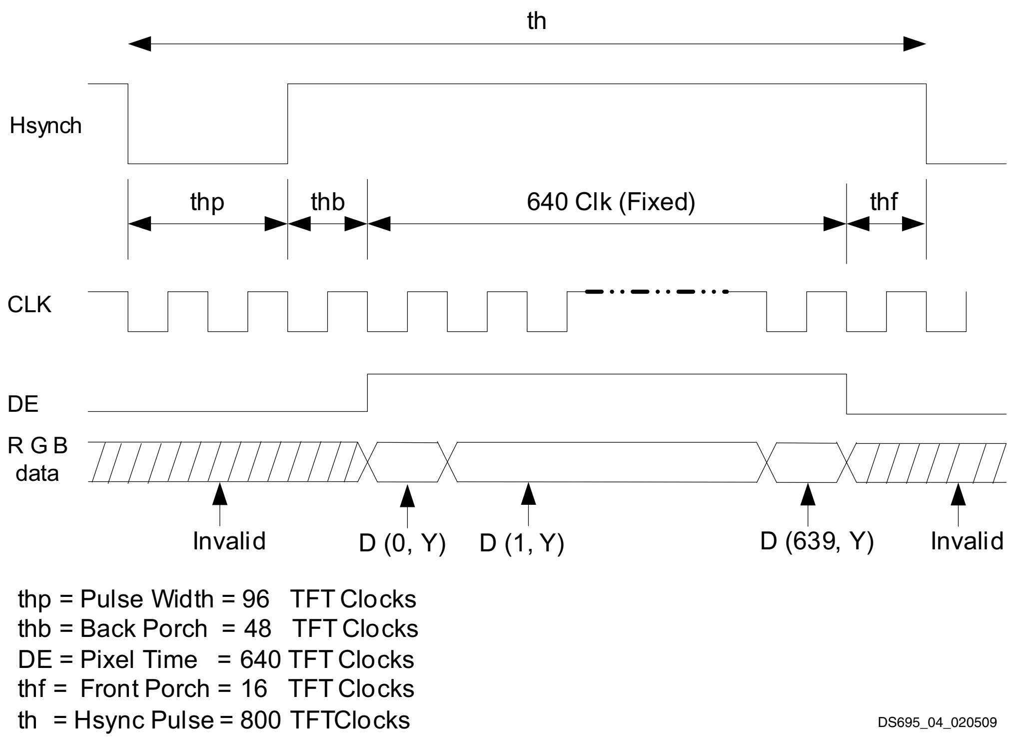


Figure 3-1: **Horizontal Data**

VSYNC Timing

The VSYNC is an active-Low signal and the complete time period of the VSYNC is 525 h_syncs. Out of the 525 h_syncs, the VSYNC pulse period is 2 h_syncs and the active display period is 480 h_syncs. The back porch period is 31 h_syncs and the front porch period is 12 h_syncs. The VSYNC timing with respect to the HSYNC is shown in Figure 3-2.

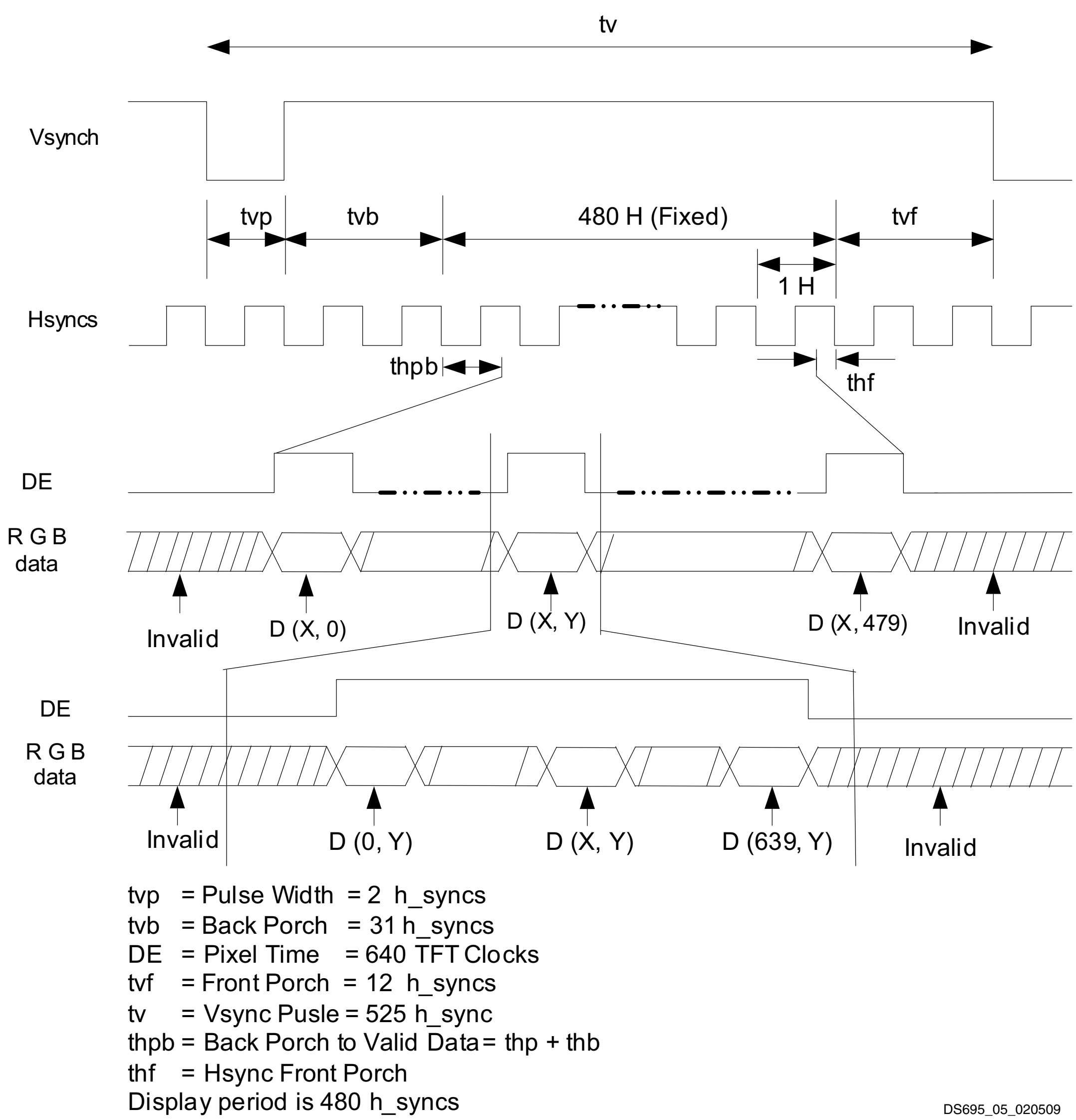


Figure 3-2: **Vertical Data**

Video Memory

IMPORTANT: *Design the system with sufficient bandwidth available between the AXI TFT Controller and the video memory device to meet the TFT video bandwidth requirements.*

There must be enough bandwidth available for the rest of the system. If the bandwidth requirement of the rest of the system is increased, the TFT clock frequency can be reduced. However, reducing the TFT clock frequency also lowers the refresh rate of the screen. This can lead to a noticeable flicker on the screen if the TFT clock is too slow.

The AXI4 master interface logic has the ability to skip reading a line of data if it fails to finish reading data from a previous line because of shortage of AXI4 bandwidth. This prevents the AXI TFT Controller losing synchronization between the AXI4 and the TFT interface logic.

CAUTION! *Extreme shortage of available bandwidth for the AXI TFT Controller can cause the screen to appear unstable as stale lines of video data are displayed on the screen.*

The video memory is expected to be arranged so that each RGB pixel is represented by a 32-bit word in memory. The video memory should be stored in a 2 MB region of memory consisting of 1024 data words (1 word = 32 bits) per line by 512 lines per frame. Out of this 1024 × 512 memory space, only the first 640 columns and 480 rows are displayed on the screen.

For a given row (0 to 479) and column (0 to 639), the pixel color information is encoded as shown in Table 3-4.

Table 3-4: **Pixel Color Encoding**

Pixel Address	Bits	Description
TFT Base Address + (4096 × row) + (4 × column)	31:24	Undefined
	23:18	Red Pixel Data: 000000 = darkest → 111111 = brightest
	17:16	Undefined
	15:10	Green Pixel Data: 000000 = darkest → 111111 = brightest
	9:8	Undefined
	7:2	Blue Pixel Data: 000000 = darkest → 111111 = brightest
	1:0	Undefined

AXI TFT Controller Timing Diagrams

AXI TFT Master Burst Read on AXI4 Attached Memory

The AXI TFT burst read transaction on AXI4 is shown in Figure 3-3.

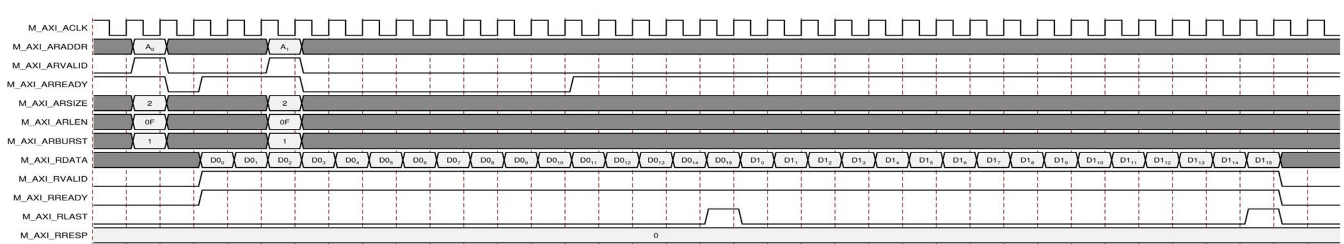


Figure 3-3: **AXI TFT Burst Read Transaction on AXI4 Master**

AXI TFT Register Read/Write through AXI4 Slave Interface

Figure 3-4 shows the AXI TFT Controller register access through AXI4 slave interface.

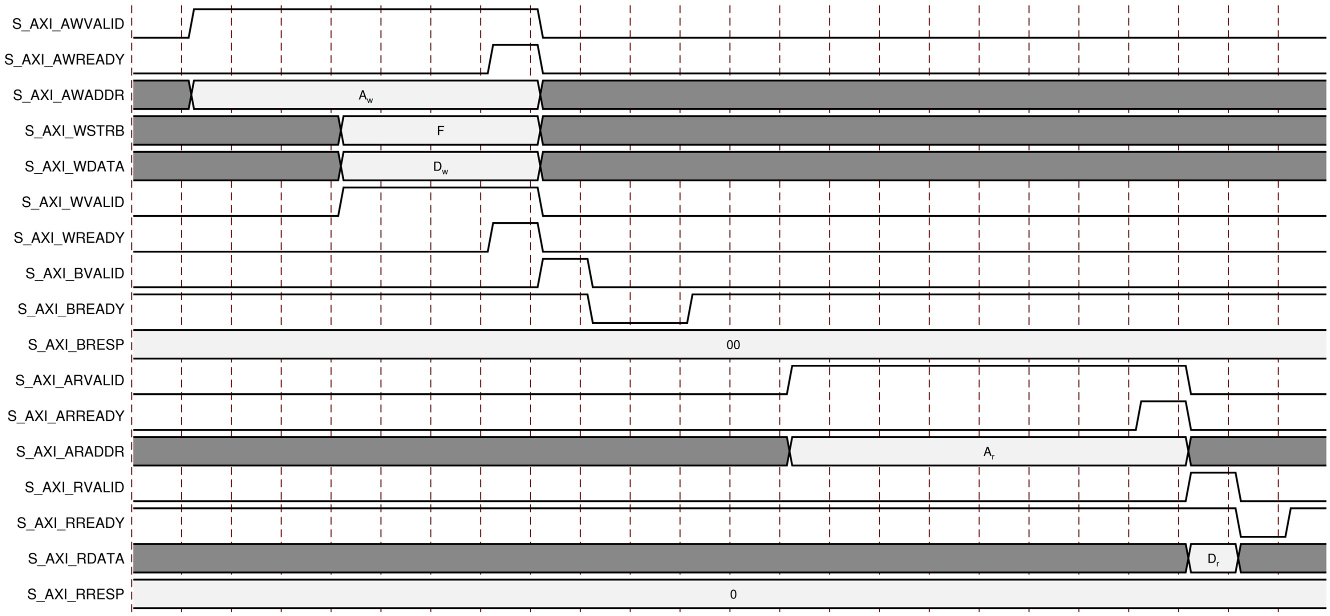


Figure 3-4: **AXI TFT Register Read/Write through AXI4 Slave Interface**

Customizing and Generating the Core

This chapter includes information about using Xilinx tools to customize and generate the core in the Vivado™ Design Suite environment.

GUI

The AXI TFT Controller can be found in `/Embedded_Processing/AXI_Peripheral/Low_Speed_Peripheral/` in the Vivado IP Catalog.

To access the core name, perform the following:

1. Open a project by selecting **File** then **Open Project** or create a new project by selecting **File** then **New Project** in Vivado.
2. Open the IP catalog and navigate to any of the taxonomies.
3. Double-click on **AXI TFT** to bring up the core name GUI.

Figure 4-1 shows the AXI TFT Controller Customize IP window GUI with information about customizing ports.

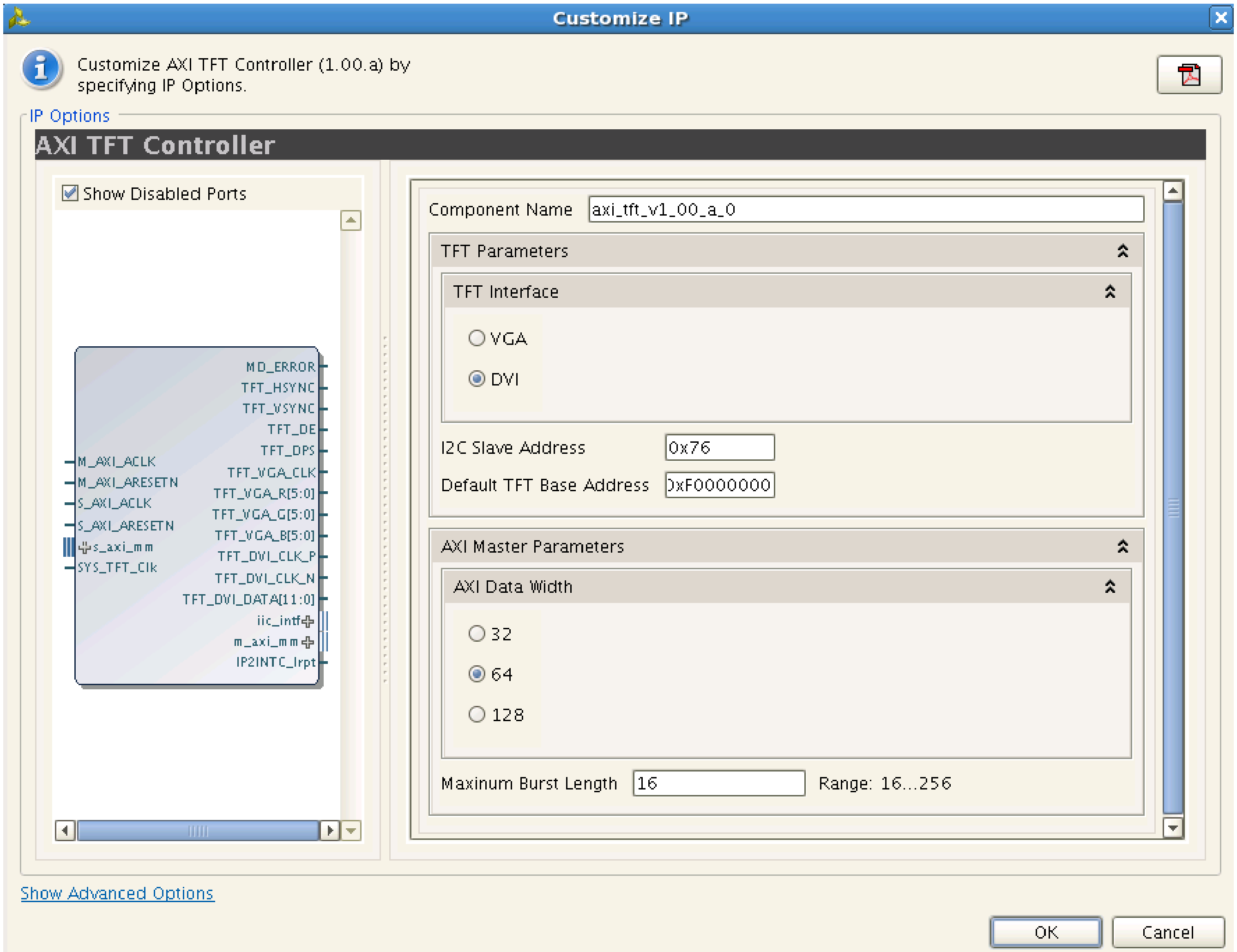


Figure 4-1: **Vivado Customize IP GUI**

- **Component Name** – The base name of the output files generated for the core. Names must begin with a letter and can be composed of any of the following characters: a to z, 0 to 9, and "_".

TFT Parameters

- **TFT Interface**
  - **VGA** – If C_TFT_INTERFACE = 1, all VGA ports are tied to 0.
  - **DVI** – If C_TFT_INTERFACE = 0, all DVI ports are tied to 0.
- **I2C Slave Address** – Depends on C_TFT_INTERFACE. Required only when DVI interface is selected.
- **Default TFT Base Address** – 0xF0000000

AXI Master Parameters

- **AXI Data Width** – Affects the number of bits in AXI4 master data bus. Set to 32, 64, or 128.
- **Maximum Burst Length** – Range of 16 to 256.

Output Generation

This section provides detailed information about the files and the directory structure generated by the Xilinx Vivado tool.

The output files generated from the Xilinx Vivado IP Catalog are placed in the project directory. The file output list might include some or all of the following files.

The component name of the IP generated is `axi_tft_v1_00_a`.

- **<project name>.srcs/sources_1/ip**
  Top-level project directory; name is user-defined
  - axi_tft_v1_00_a
    AXI TFT Controller folders and files
  - sim
    Simulation wrapper
  - synth
    Synthesis wrapper
  - axi_tft_v1_00_a.veo/.vho
    Instantiation template files
  - <axi_tft_v1_00_a>/axi_tft_v1_00_a/hdl/src
    AXI TFT Controller RTL files

<project name>.srcs/sources_1/ip

The `project` directory contains the `axi_tft` core RTL files.

axi_tft_v1_00_a

The `axi_tft_v1_00_a` name directory contains the following folders and files.

Table 4-1: **axi_tft_v1_00_a_0 Directory**

Name	Description
<project name.srcs/sources_1/ip/axi_tft_v1_00_a	
sim	Simulation wrapper folder

Table 4-1: **axi_tft_v1_00_a_0 Directory *(Cont'd)***

Name	Description
synth	Synthesis wrapper folder
axi_tft_v1_00_a.veo/.vho	Instantiation template files

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<axi_tft_v1_00_a>/axi_tft_v1_00_a/hdl/src

The `axi_tft` RTL files are delivered under `/ip/axi_tft_v1_00_a/hdl/src` directory.

Constraining the Core

This chapter contains information about constraining the core in the Vivado™ Design Suite environment.

Required Constraints

The IP generates the following false path constraints with respect to the clock domains:

```
set TFT_Clock [get_clocks -of_objects [get_ports SYS_TFT_Clk]]
set s_axi_clk [get_clocks -of_objects [get_ports S_AXI_ACLK]]
set m_axi_clk [get_clocks -of_objects [get_ports M_AXI_ACLK]]
set_false_path -from [all_registers -clock $s_axi_clk] -to [all_registers -clock
$TFT_Clock]
set_false_path -from [all_registers -clock $TFT_Clock] -to [all_registers -clock
$s_axi_clk]
set_false_path -from [all_registers -clock $s_axi_clk] -to [all_registers -clock
$m_axi_clk]
set_false_path -from [all_registers -clock $m_axi_clk] -to [all_registers -clock
$s_axi_clk]
set_false_path -from [all_registers -clock $m_axi_clk] -to [all_registers -clock
$TFT_Clock]
set_false_path -from [all_registers -clock $TFT_Clock] -to [all_registers -clock
$m_axi_clk]
```

All clock inputs need to be defined at the top-level in the system using create_clock command.

Migrating

This appendix describes migrating from older versions of the IP to the current IP release.

For information on migrating to the Vivado™ Design Suite, see UG911, *Vivado Design Suite Migration Methodology Guide* [Ref 3].

Debugging

This appendix includes details about resources available on the Xilinx Support website and debugging tools. In addition, this appendix provides a step-by-step process for debugging process and a flow diagram to guide you through debugging the AXI TFT Controller core.

Finding Help on Xilinx.com

To help in the design and debug process when using the AXI TFT Controller, the Xilinx Support web page contains key resources such as product documentation, release notes, answer records, information about known issues, and links for opening a Technical Support WebCase.

Documentation

This product guide is the main document associated with the AXI TFT Controller. This guide, along with documentation related to all products that aid in the design process, can be found on the Xilinx Support web page (www.xilinx.com/support) or by using the Xilinx Documentation Navigator.

Download the Xilinx Documentation Navigator from the Design Tools tab on the Downloads page (www.xilinx.com/download). For more information about this tool and the features available, open the online help after installation.

Release Notes

Known issues for all cores, including the AXI TFT are described in the IP Release Notes Guide (XTP025).

Known Issues

Answer Records include information about commonly encountered problems, helpful information on how to resolve these problems, and any known issues with a Xilinx product. Answer Records are created and maintained daily ensuring that users have access to the most accurate information available.

Answer Records for this core are listed below, and can also be located by using the Search Support box on the main Xilinx support web page. To maximize your search results, use proper keywords such as:

- Product name
- Tool message(s)
- Summary of the issue encountered

A filter search is available after results are returned to further target the results.

Answer Records for the AXI TFT Controller

The primary Answer Record for this core is 53104 where a write to the CCR register during initialization of Chrontel device affects pending IIC transactions.

Contacting Technical Support

Xilinx provides premier technical support for customers encountering issues that require additional assistance.

To contact Xilinx Technical Support:

1. Navigate to www.xilinx.com/support.
2. Open a WebCase by selecting the WebCase link located under Support Quick Links.

When opening a WebCase, include:

- Target FPGA including package and speed grade.
- All applicable Xilinx Design Tools and simulator software versions.
- Additional files based on the specific issue might also be required. See the relevant sections in this debug guide for guidelines about which file(s) to include with the WebCase.

Additional Resources

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Appendix B, Debugging and Xilinx Support website at:

www.xilinx.com/support.

For a glossary of technical terms used in Xilinx documentation, see:

www.xilinx.com/company/terms.htm.

References

Unless otherwise noted, IP references are for the product documentation page. These documents provide supplemental material useful with this product guide:

1. *LogiCORE IP AXI4-Lite IPIF Data Sheet* (DS765)
2. *LogiCORE IP AXI Master Burst Data Sheet* (DS844)
3. Vivado™ Design Suite user documentation (www.xilinx.com/cgi-bin/docs/rdoc?v=2012.4;t=vivado+docs)
4. *AXI4 AMBA® AXI Protocol v2.0 Specification*
5. *Chrontel CH-7301 DVI Transmitter Specification*, version 1.32
6. *I2C Bus Specification*, version 2.1

Technical Support

Xilinx provides technical support at www.xilinx.com/support for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled DO NOT MODIFY.

See the Embedded Edition Derivative Device Support web page (www.xilinx.com/ise/embedded/ddsupport.htm) for a complete list of supported derivative devices for this core.

See the IP Release Notes Guide (XTP025) for more information on this core. For each core, there is a master Answer Record that contains the Release Notes and Known Issues list for the core being used. The following information is listed for each version of the core:

- New Features
- Resolved Issues
- Known Issues

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
12/18/12	1.0	Initial Xilinx release.

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