LogiCORE IP CPRI v5.1

DS611 April 24, 2012 **Product Specification**

Introduction

The LogiCORE™ IP Common Packet Radio Interface (CPRI™) core is a high-performance, low-cost flexible solution for implementation of the CPRI interface. This core uses state-of-the-art Virtex®-5 Field Programmable Gate Array (FPGA) RocketIO™ GTP and GTX transceivers, Virtex-6 FPGA GTXE1 transceivers, Virtex-7 and Kintex™-7 FPGA GTXE2 and GTH2 transceivers or Spartan®-6 FPGA GTPA1 transceivers to implement the Physical Layer. A compact and customizable Data Link Layer is implemented in the FPGA logic.

Features

- Designs implemented on Virtex-7 and Kintex-7 devices operate at line rates of 614.4 Mb/s, 1228.8 Mb/s, 2457.6 and 3072 Mb/s, using GTXE2 transceivers. Optionally line rates of 4915.2 Mb/s, 6144 Mb/s and 9830.4 Mb/s are supported in these devices.
- Designs implemented on Virtex-6 devices operate at line rates of 614.4 Mb/s, 1228.8 Mb/s, 2457.6 and 3072 Mb/s, using GTXE1 transceivers. Optionally line rates of 4915.2 Mb/s and 6144 Mb/s are supported in these devices.
- Designs implemented on Virtex-5 LXT/SXT and Spartan-6 LXT devices operate at line rates of 614.4 Mb/s, 1228.8 Mb/s, 2457.6 and 3072 Mb/s, using GTP and GTPA1 transceivers.
- Designs implemented on Virtex-5 FXT/TXT devices operate at line rates of 1228.8 Mb/s, 2457.6 and 3072 Mb/s, using GTX transceivers.
- Suitable for use in both Radio Equipment Controllers (RECs) and Radio Equipment (RE), including multi-hop system
- UTRA-FDD I/Q module supporting 1 to 48 Antenna-Carriers per core
- Automatic speed negotiation
- Supports both Fast (Ethernet) and Slow High-Level Data Link Control (HDLC) Control and Management (C&M) channels per *CPRI Specification v4.2*. See References
- Designed to *CPRI Specification v4.2*

LogiCORE IP Facts				
Core Specifics				
Supported Device Family[1]	Virtex-7 [Ref 1][Ref 3], Kintex-7 [Ref 2][Ref 3], Virtex-6 [Ref 4], Spartan-6, Virtex-5 LXT[2]/SXT/FXT/TXT			
Supported User Interfaces	Generic data, status, configuration and management interfaces. AXI4-Lite management interface			
	Resources			
(3072.0 Mb/s default configuration)	**Slices**	**LUTs**	**FFs**	**Block RAMs**
	910	1460	1930	6
(6144.0 Mb/s default configuration)	1120	2050	2720	6
(9830.4 Mb/s default configuration)[3]	1110	2340	3030	6
Provided with Core				
Documentation	Product Specification User Guide			
Design Files	Native Generic Circuit (NGC) Netlist			
Example Design	VHDL			
Test Bench	VHDL			
Constraints File	User Constraints File (UCF)			
Simulation Models	VHDL, Verilog			
Supported S/W Drivers	N/A			
Tested Design Tools				
Design Entry Tools	Integrated Software Environment (ISE) v14.1 Design Suite			
Simulation[4]	Mentor Graphics ModelSim[5]			
Synthesis Tools	Xilinx Synthesis Technology (XST)			
Support				
Provided by Xilinx, Inc.				

1. For the complete list of supported devices, see the release notes for this core.
2. Excludes Virtex-5 LX20T FPGA.
3. Operation at 9.8 Gb/s is supported using a direct connection to a XFP using the XFI electrical specification or SFP+ optical module using SFI electrical specification.
4. Requires a Verilog LRM-IEEE 1364-2005 encryption-compliant simulator. For VHDL simulation, a mixed HDL license is required.
5. For the supported version of the tool, see the ISE Design Suite 14: Release Notes Guide.

Features (Continued)

- Can be configured as master or slave at generation time
- Master core can be switched to operate as a slave via a configuration port
- Easy-to-use interface for in-phase (I) and quadrature-phase (Q) data and synchronization
- Supports vendor-specific data transport
- Delay measurement capability meets CPRI Requirement 21 per *CPRI Specification v4.2*. See References.

Overview

The CPRI core implements Layer 1 and Layer 2 of the CPRI specification in Virtex-7, Kintex-7, Virtex-6, Spartan-6 and Virtex-5 LXT/SXT/FXT devices. The CPRI core provides these client-side interfaces.

- **I/Q Interface.** Consists of a stream of radio data (I/Q samples) that is synchronized to the Universal Mobile Telecommunications System (UMTS) radio frame pulse.
- **Synchronization Interface.** Provides the means for the client logic to synchronize to the network time by transmitting the UMTS radio frame pulse and clock frequency.
- **High-Level Data Link Control (HDLC) Interface.** Transports management information between master and slave. The HDLC interface is serialized and synchronous.
- **Ethernet Interface.** When configured to support speeds of up to 3072 Mb/s, the Ethernet interface is presented as a Media Independent Interface (MII); this allows a 100 Mbit Ethernet Media Access Controller (MAC) to be attached to the core to provide a high-speed channel for management information. When speeds of up to 4915.2 Mb/s, 6144 Mb/s or 9830.4 Mb/s are supported a Gigabit Media Independent Interface (GMII) option is available. This allows a 1 Gbit Ethernet MAC to be attached to the core. The core includes an Ethernet frame buffer in both transmit and receive directions.
- **Vendor-Specific Data Interface.** Provides client logic access to the vendor-specific sub-channels in the CPRI stream.
- **Management Interface.** Provides control and status registers that allow management of the entire design from a supervisory processor.

The architecture of the core is shown in Figure 1. In addition to the interfaces described previously, the core contains these blocks:

- **Status/Alarm Block.** Reflects the internal state of the core and the state of the link.
- **Start-up Sequencer.** Performs line-rate negotiation and Control and Management (C&M) parameter negotiation at link start-up. This block continuously monitors the state of the link and sends the status to the alarm block.
- **UMTS Terrestrial Radio Access - Frequency Division Duplexing (UTRA FDD) I/Q Module:** A pluggable I/Q module to support multiplexing and demultiplexing of I/Q samples in UTRA FDD systems (shown in Figure 1).
- **Legacy raw I/Q Module**: A pluggable I/Q Module for backward compatibility with the raw interfacing timing for v1.x CPRI cores (not shown in Figure 1).

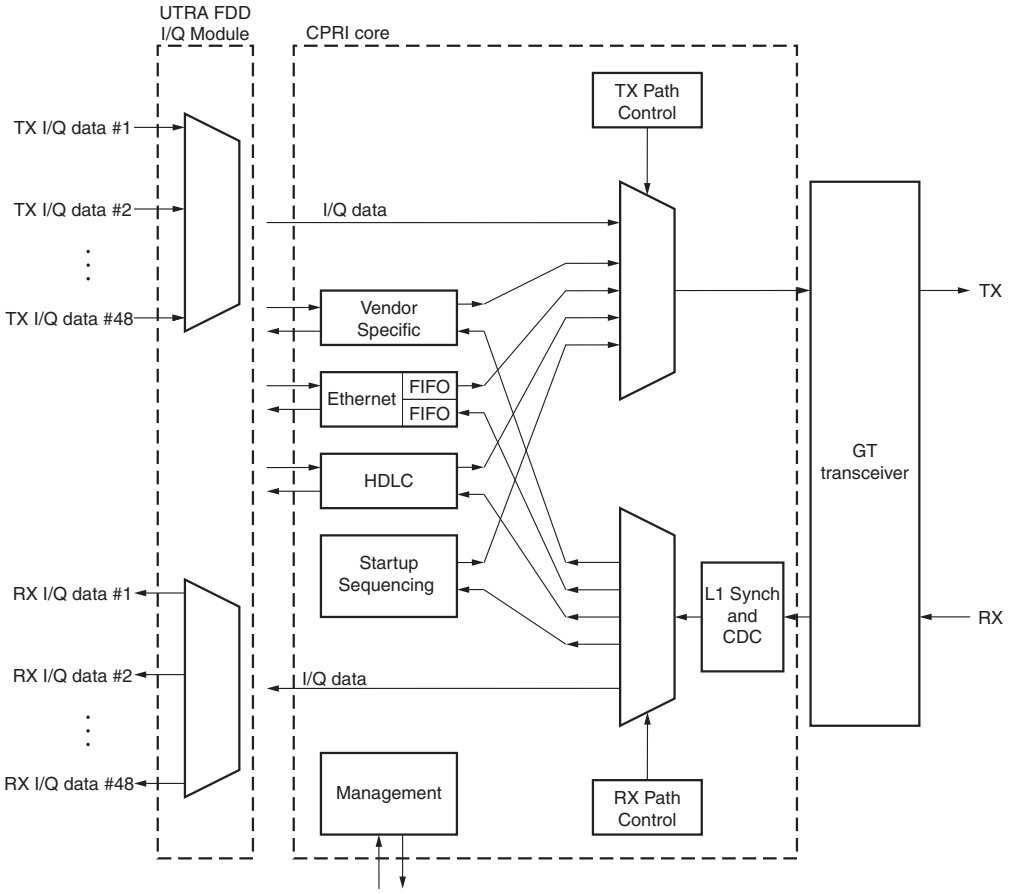

Figure 1: **CPRI Top-Level Block Diagram**

Applications

CPRI is an emerging standard for communication between a Radio Equipment Controller (REC) or Base Station and one or more Radio Equipment (RE) units in a 3 G cellular network. The concept is to foster an independent technology evolution for cellular equipment products by defining a publicly available specification for the key internal interface between these units. Figure 2 shows the position of the interface in a cellular system.

The goal of the CPRI interface is to use one physical connection for the radio data (I/Q data), radio unit management (for example, Automatic Gain Control, alarms) and synchronization (clock frequency control, frame synchronization). Table 1 shows the data rates supported by each Xilinx device. Data is transferred over a single serial link. This link is defined to be electrically compliant with existing high speed serial link standards such as the Gigabit Ethernet and 10 Gigabit eXtended Attachment Unit Interface (XAUI) standards

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Table 1: **Supported Data Rates**

	614.4 Mb/s	1228.8 Mb/s	2457.6 Mb/s	3072.0 Mb/s	4915.2 Mb/s	6144.0 Mb/s	9830.4 Mb/s
Virtex-5							
LXT/SXT	Supported	Supported	Supported	Supported	Not supported	Not supported	Not supported
FXT/TXT	Not supported	Supported	Supported	Supported	Not supported	Not supported	Not supported
Virtex-6							
LXT/SXT (-1/-1L speed grade)	Supported	Supported	Supported	Supported	Supported	Not supported	Not supported
LXT/SXT (-2/-3 speed grade)	Supported	Supported	Supported	Supported	Supported	Supported	Not supported
CXT	Supported	Supported	Supported	Supported	Not supported	Not supported	Not supported
Spartan-6	Supported	Supported	Supported	Supported	Not supported	Not supported	Not supported
Kintex-7							
-1 speed grade	Supported	Supported	Supported	Supported	Supported	Supported(1)	Not supported(1)
-2/-3 speed grade	Supported	Supported	Supported	Supported	Supported	Supported	Supported(1)
Virtex-7							
-1 speed grade	Supported	Supported	Supported	Supported	Supported	Supported	Not supported
-2/-3 speed grade	Supported	Supported	Supported	Supported	Supported	Supported	Supported

1. Not supported on non FFG packages.

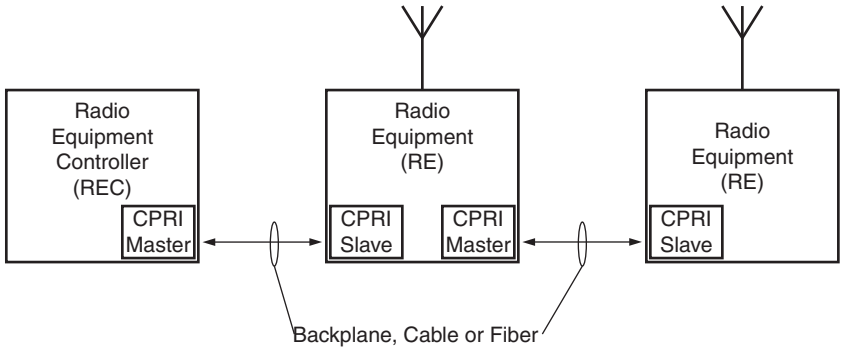

Figure 2: **Location of CPRI in a Cellular System**

Device Utilization

Virtex-7 Devices (Supporting Speeds of up to 3072.0 Mb/s)

Table 2 provides approximate device utilization figures for example configurations of the 3072.0 Mb/s core in Virtex-7 devices. The values include GTXE2 control logic and the clock control logic.

Table 2: **Virtex-7 Core Device Utilization (Speeds up to 3072.0 Mb/s)[1]**

Parameter Values			Device Resources					
Ethernet	R21	Master or Slave	LUTs	FFs	Block RAMs	MMCMs	BUFRs	BUFGs
Yes	No	Slave	1310	1670	5	1	1	1
Yes	Yes	Slave	1280	1810	5	1	1	1
No	No	Slave	810	1070	1	1	1	1
No	Yes	Slave	940	1230	1	1	1	1
No	No	Master	830	1050	2	1	1	1
No	Yes	Master	960	1240	2	1	1	1
Yes	No	Master	1330	1660	6	1	1	1
Yes	Yes	Master	1400	1850	6	1	1	1

1. Additional clocking resources will be required for `eth_ref_clk` (if Ethernet is selected), `hires_clk` (if R21 is selected) and `aux_clk`. These are not included in Table 2 and are external to the core which allows them to be shared.

Virtex-7 Devices (Supporting Speeds of up to 4915.2/6144.0 Mb/s)

Table 3 provides approximate device utilization figures for example configurations of the 4915.2/6144.0 Mb/s core in Virtex-7 devices. The values include GTXE2 control logic and the clock control logic.

Table 3: **Virtex-7 Core Device Utilization (Speeds of up to 4915.2/6144.0 Mb/s)[1]**

Parameter Values			Device Resources					
Ethernet	R21	Master or Slave	LUTs	FFs	Block RAMs	MMCMs	BUFRs	BUFGs
Yes	No	Slave	1950	2460	5	1	1	1
Yes	Yes	Slave	1980	2620	5	1	1	1
No	No	Slave	1480	1850	1	1	1	1
No	Yes	Slave	1560	2010	1	1	1	1
No	No	Master	1500	1840	2	1	1	1
No	Yes	Master	1600	2030	2	1	1	1
Yes	No	Master	1930	2450	6	1	1	1
Yes	Yes	Master	2050	2630	6	1	1	1

1. Additional clocking resources will be required for `eth_ref_clk` (if Ethernet is selected), hires_clk (if R21 is selected) and `aux_clk`. These are not included in Table 3 and are external to the core which allows them to be shared.

Virtex-7 Devices (Supporting Speeds of up to 9830.4 Mb/s)

Table 4 provides approximate device utilization figures for example configurations of the 9830.4 Mb/s core in Virtex-7 devices. The values include GTXE2 control logic and the clock control logic.

Table 4: **Virtex-7 Core Device Utilization[1]**

Parameter Values			Device Resources					
Ethernet	R21	Master or Slave	LUTs	FFs	Block RAMs	MMCMs	BUFRs	BUFGs
Yes	No	Slave	2330	2940	5	1	1	1
Yes	Yes	Slave	2530	3100	5	1	1	1
No	No	Slave	1920	2330	1	1	1	1
No	Yes	Slave	2020	2490	1	1	1	1
No	No	Master	1940	2290	2	1	1	1
No	Yes	Master	2040	2470	2	1	1	1
Yes	No	Master	2370	2900	6	1	1	1
Yes	Yes	Master	2390	3080	6	1	1	1

1. Additional clocking resources will be required for `eth_ref_clk` (if Ethernet is selected), hires_clk (if R21 is selected) and `aux_clk`. These are not included in Table 4 and are external to the core which allows them to be shared.

Kintex-7 Devices (Supporting Speeds of up to 3072.0 Mb/s)

Table 5 provides approximate device utilization figures for example configurations of the 3072.0 Mb/s core in Kintex-7 devices. The values include GTXE2 control logic and the clock control logic.

Table 5: **Kintex-7 Core Device Utilization (Speeds of up to 3072.0 Mb/s)[1]**

Parameter Values				Device Resources				
Ethernet	R21	Master or Slave	LUTs	FFs	Block RAMs	MMCMs	BUFHs	BUFGs
Yes	No	Slave	1250	1730	5	1	1	2
Yes	Yes	Slave	1410	1900	5	1	1	2
No	No	Slave	820	1130	1	1	1	2
No	Yes	Slave	930	1290	1	1	1	2
No	No	Master	840	1120	2	1	1	2
No	Yes	Master	980	1300	2	1	1	2
Yes	No	Master	1300	1720	6	1	1	2
Yes	Yes	Master	1400	1910	6	1	1	2

1. Additional clocking resources will be required for `eth_ref_clk` (if Ethernet is selected), `hires_clk` (if R21 is selected) and `aux_clk`. These are not included in Table 5 and are external to the core which allows them to be shared.

Kintex-7 Devices (Supporting Speeds of up to 4915.2/6144.0 Mb/s)

Table 6 provides approximate device utilization figures for example configurations of the 4915.2/6144.0 Mb/s core in Kintex-7 devices. The values include GTXE2 control logic and the clock control logic.

Table 6: **Kintex-7 Core Device Utilization (Speeds of up to 4915.2/6144.0 Mb/s)[1]**

Parameter Values				Device Resources				
Ethernet	R21	Master or Slave	LUTs	FFs	Block RAMs	MMCMs	BUFHs	BUFGs
Yes	No	Slave	1950	2520	5	1	1	2
Yes	Yes	Slave	2010	2680	5	1	1	2
No	No	Slave	1540	1910	1	1	1	2
No	Yes	Slave	1590	2070	1	1	1	2
No	No	Master	1530	1900	2	1	1	2
No	Yes	Master	1610	2090	2	1	1	2
Yes	No	Master	1920	2510	6	1	1	2
Yes	Yes	Master	2090	2690	6	1	1	2

1. Additional clocking resources will be required for `eth_ref_clk` (if Ethernet is selected), `hires_clk` (if R21 is selected) and `aux_clk`. These are not included in Table 6 and are external to the core which allows them to be shared.

Kintex-7 Devices (Supporting Speeds of up to 9830.4 Mb/s)

Table 7 provides approximate device utilization figures for example configurations of the 9830.4 Mb/s core in Kintex-7 devices. The values include GTXE2 control logic and the clock control logic.

Table 7: **Kintex-7 Core Device Utilization (Speeds of up to 9830.4 Mb/s)[1]**

Parameter Values				Device Resources				
Ethernet	R21	Master or Slave	LUTs	FFs	Block RAMs	MMCMs	BUFHs	BUFGs
Yes	No	Slave	2400	3000	5	1	1	2
Yes	Yes	Slave	2540	1240	5	1	1	2
No	No	Slave	1940	2390	1	1	1	2
No	Yes	Slave	2060	2550	1	1	1	2
No	No	Master	1880	2350	2	1	1	2
No	Yes	Master	2020	2530	2	1	1	2
Yes	No	Master	2390	2960	6	1	1	2
Yes	Yes	Master	2490	3140	6	1	1	2

1. Additional clocking resources will be required for `eth_ref_clk` (if Ethernet is selected), `hires_clk` (if R21 is selected) and `aux_clk`. These are not included in Table 7 and are external to the core which allows them to be shared.

Virtex-6 Devices (Supporting Speeds of up to 3072.0 Mb/s)

Table 8 provides approximate device utilization figures for example configurations of the 3072.0 Mb/s core in Virtex-6 devices. The values include the GTXE1 control logic and the clock control logic.

Table 8: **Virtex-6 Core Device Utilization (Speeds of up to 3072.0 Mb/s)[1]**

Parameter Values			Device Resources					
Ethernet	R21	Master or Slave	LUTs	FFs	Block RAMs	MMCMs	BUFRs	BUFGs
Yes	No	Slave	1280	1720	5	1	1	2
Yes	Yes	Slave	1430	1880	5	1	1	2
No	No	Slave	840	1120	1	1	1	2
No	Yes	Slave	980	1280	1	1	1	2
No	No	Master	880	1100	2	1	1	2
No	Yes	Master	1020	1290	2	1	1	2
Yes	No	Master	1260	1710	6	1	1	2
Yes	Yes	Master	1480	1900	6	1	1	2

1. Additional clocking resources will be required for `eth_ref_clk` (if Ethernet is selected), `hires_clk` (if R21 is selected) and `aux_clk`. These are not included in Table 8 and are external to the core which allows them to be shared.

Virtex-6 Devices (Supporting Speeds of up to 4915.2/6144.0 Mb/s)

Table 9 provides approximate device utilization figures for example configurations of the 4915.2/6144.0 Mb/s core in Virtex-6 devices. The values include the GTXE1 control logic and the clock control logic.

Table 9: **Virtex-6 Core Device Utilization (Speeds of up to 4915.2/6144.0 Mb/s)[1]**

Parameter Values			Device Resources					
Ethernet	R21	Master or Slave	LUTs	FFs	Block RAMs	MMCMs	BUFRs	BUFGs
Yes	No	Slave	1880	2510	5	1	1	2
Yes	Yes	Slave	2040	2670	5	1	1	2
No	No	Slave	1530	1900	1	1	1	2
No	Yes	Slave	1620	2060	1	1	1	2
No	No	Master	1520	1890	2	1	1	2
No	Yes	Master	1640	2070	2	1	1	2
Yes	No	Master	1920	2500	6	1	1	2
Yes	Yes	Master	2090	2680	6	1	1	2

1. Additional clocking resources will be required for `eth_ref_clk` (if Ethernet is selected), `hires_clk` (if R21 is selected) and `aux_clk`. These are not included in Table 9 and are external to the core which allows them to be shared.

Spartan-6 Devices

Table 10 provides approximate device utilization figures for example configurations of the core in Spartan-6 devices. The values include the GTPA1 control logic and the clock control logic.

Table 10: **Spartan-6 Core Device Utilization[1]**

Parameter Values				Device Resources				
Ethernet	R21	Master or Slave	LUTs	FFs	Block RAMs	PLLs	DCMs	BUFGs
Yes	No	Slave	1380	1750	7	1	1	4
Yes	Yes	Slave	1510	1910	7	1	1	4
No	No	Slave	870	1130	1	1	1	4
No	Yes	Slave	1000	1290	1	1	1	4
No	No	Master	860	1100	2	1	1	4
No	Yes	Master	1010	1300	2	1	1	4
Yes	No	Master	1380	1730	8	1	1	4
Yes	Yes	Master	1540	1920	8	1	1	4

1. Additional clocking resources will be required for `eth_ref_clk` (if Ethernet is selected), `hires_clk` (if R21 is selected) and `aux_clk`. These are not included in Table 10 and are external to the core which allows them to be shared.

Virtex-5 Devices

Table 11 provides approximate device utilization figures for example configurations of the core in Virtex-5 devices. The values include the GTP/GTX control logic and the clock control logic

Table 11: **Virtex-5 Core Device Utilization[1]**

Parameter Values				Device Resources					
Device	Ethernet	R21	Master or Slave	LUTs	FFs	Block RAMs	PLLs	BUFRs	BUFGs
LXT/SXT	Yes	No	Slave	1450	1780	5	1	1	3
LXT/SXT	Yes	Yes	Slave	1590	1940	5	1	1	3
LXT/SXT	No	No	Slave	980	1160	1	1	1	3
LXT/SXT	No	Yes	Slave	1090	1330	1	1	1	3
LXT/SXT	No	No	Master	970	1150	2	1	1	3
LXT/SXT	No	Yes	Master	1140	1340	2	1	1	3
LXT/SXT	Yes	No	Master	1460	1760	6	1	1	3
LXT/SXT	Yes	Yes	Master	1630	1950	6	1	1	3
FXT	No	No	Slave	1470	1750	1	1	1	2
FXT	No	Yes	Slave	1580	1910	1	1	1	2
FXT	Yes	No	Slave	980	1140	5	1	1	2
FXT	Yes	Yes	Slave	1090	1300	5	1	1	2
FXT	No	No	Master	990	1120	2	1	1	2
FXT	No	Yes	Master	1140	1310	2	1	1	2
FXT	Yes	No	Master	1490	1740	6	1	1	2
FXT	Yes	Yes	Master	1690	1920	6	1	1	2

1. Additional clocking resources will be required for `eth_ref_clk` (if Ethernet is selected), `hires_clk` (if R21 is selected) and `aux_clk`. These are not included in Table 11 and are external to the core which allows them to be shared.

Speed Grade Support

1. 9830 Mb/s is only supported on -2 and -3 speed grades for Virtex-7 devices.
2. 6144 Mb/s is only supported on -1 speed grades in FFG type packages and -2 and -3 speed grades in all packages for Kintex-7 devices. 9830 Mb/s is only supported on -2 and -3 speed grades in FFG packages.
3. CPRI cores supporting maximum line rates of 3072.0 Mb/s, 4915.2 Mb/s and 6144.0 Mb/s use a 2 byte internal transceiver datapath. This might limit support for -2L, -2G and -2LE Virtex-7 and Kintex-7 devices. See the Virtex-7 and Kintex-7 FPGA data sheets for more information.
4. 6144 Mb/s is only supported on -2 and -3 speed grades for Virtex-6 devices.

References

To search for Xilinx documentation, go to www.xilinx.com/support.

- *CPRI Specification v4.2*, September 29, 2010 (www.cpri.info)
- *IEEE Standard 802.3-2005* (standards.ieee.org/getieee802)
- *Xilinx AXI Reference Guide* (UG761)

Support

Xilinx provides technical support for this LogiCORE IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices not listed in the documentation, or if customized beyond that allowed in the product documentation, or if any changes are made to the sections marked DO NOT MODIFY.

Ordering Information

The CPRI core can be generated using the Xilinx CORE Generator™ system v14.1 or higher with the applicable service pack. The CORE Generator system is shipped with Xilinx ISE® Design Suite Series Development software.

Related Information

Xilinx products are not intended for use in life-support appliances, devices, or systems. Use of a Xilinx product in such application without the written consent of the appropriate Xilinx officer is prohibited.

Revision History

Date	Version	Revision
08/08/07	1.0	Initial Xilinx release.
3/24/08	1.5	Updated supported tools and performance numbers.
9/05/08	2.1	Early access release.
10/31/08	2.2	Early access release 2.
4/24/09	3.0	Updated to support ISE v11.1.
6/24/09	4.0	Updated to support ISE v11.2.
09/16/09	5.0	Updated to support ISE v11.3.
10/15/09	6.0	Early access release.
4/19/10	7.0	Updated to support ISE v12.1.
7/23/10	8.0	Updated to support ISE v12.2.
3/01/11	9.0	Updated to support ISE v13.1. Supports new Virtex-7 and Kintex-7 devices and AXI4-Lite interconnect.
4/24/12	10.0	Summary of Changes • Updated to support ISE v14.1. • Support added for the ORI interface and dynamically switchable operation between master and slave and Virtex-7 GTHE2 transceivers. • Added Speed Grade Support section.

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