LogiCORE IP AXI to APB Bridge (v1.00a)

DS788 June 22, 2011 **Product Specification**

Introduction

The AMBA® (Advanced Microcontroller Bus Architecture) AXI (Advanced eXtensible Interface) to APB (Advanced Peripheral Bus) Bridge translates AXI4-Lite transactions into APB transactions. It functions as a slave on the AXI4-Lite interface and as a master on the APB interface. The AXI to APB Bridge main use model is to connect the APB slaves with AXI masters.

Features

The Xilinx AXI to APB Bridge is a soft IP core with these features:

- AXI interface is based on the AXI4-Lite specification
- APB interface is based on the APB3 specification, supports optional APB4 selection
- Supports 1:1 (AXI:APB) synchronous clock ratio
- Connects as a 32-bit slave on 32-bit AXI4-Lite
- Connects as a 32-bit master on 32-bit APB3/APB4
- Supports optional data phase time out

LogiCORE IP Facts Table					
Core Specifics					
Supported Device Family[1]	Artix™-7[(2)], Virtex®-7, Kintex™-7, Virtex-6, Spartan®-6				
Supported User Interfaces	AXI4-Lite, APB3/APB4				
	Resources[2, 3, 4]				**Frequency**
Configuration	**LUTs**	**FFs**	**DSP Slices**	**Block RAM**	**Max. Freq.**
Config1	Refer to Table 4, Table 5, Table 6, Table 7, and Table 8			0	
Provided with Core					
Documentation	Product Specification				
Design Files	VHDL				
Example Design	Not Provided				
Test Bench	Not Provided				
Constraints File	None				
Simulation Model	None				
Tested Design Tools[5]					
Design Entry Tools	XPS 13.2 or later[(3)]				
Simulation	ModelSim 6.6d or later				
Synthesis Tools	XST 13.2 or later				
Support					
Provided by Xilinx @ www.xilinx.com/support					

Notes:

1. For a complete list of supported derivative devices, see the IDS Embedded Edition Derivative Device Support.
2. For more information, see DS150 Virtex-6 Family Overview.
3. For more information, see DS160 Spartan-6 Family Overview.
4. For more information, see DS180 7 Series FPGAs Overview.
5. For the supported versions of the tools, see the ISE Design Suite 13: Release Notes Guide.

Functional Description

Overview

The AXI to APB Bridge translates AXI4-Lite transactions into APB transactions. The bridge functions as a slave on the AXI4-Lite interface and as a master on the APB interface.

The AXI to APB Bridge block diagram is shown in Figure 1 and described in subsequent sections.

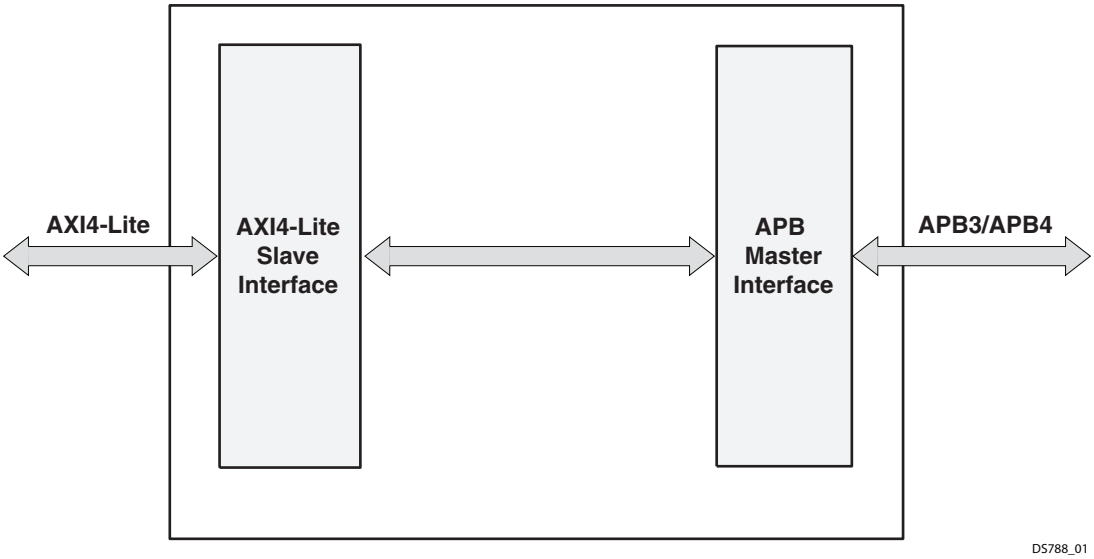

Figure 1: **AXI to APB Bridge Block Diagram**

AXI4-Lite Slave Interface

The AXI4-Lite Slave Interface module provides a bi-directional slave interface to the AXI. The AXI address and data bus widths are always fixed to 32-bits. When both write and read transfers are simultaneously requested on AXI4-Lite, the read request is given more priority than the write request. This module also contains the data phase time out logic for generating OK response on AXI interface when APB slave does not respond.

APB Master Interface

The APB Master module provides the APB master interface on the APB. This interface can be APB3 or APB4, which can be selected by setting the generic C_M_APB_PROTOCOL. When C_M_APB_PROTOCOL=apb4, the M_APB_PSTRB, and M_APB_PPROT signals are driven at the APB Interface. The APB address and data bus widths are fixed to 32-bits.

I/O Signals

Table 1 shows the I/O signals of the AXI to APB Bridge.

Table 1: **I/O Signal Description**

Port	Signal Name	Interface	I/O	Initial State	Description
AXI Interface System Signals					
P1	S_AXI_ACLK	System	I	-	AXI clock
P2	S_AXI_ARESETN	System	I	-	AXI reset, active low
AXI Write Address Channel Signals					
P3	S_AXI_AWADDR[C_S_AXI_ADDR_WIDTH-1:0]	AXI4-Lite	I	-	AXI Write address. The write address bus gives the address of the first transfer in a write burst transaction
P4	S_AXI_AWPROT[2:0](1)	AXI4-Lite	I	-	Protection type. This signal indicates the normal, privileged, or secure protection level of the write transaction and whether the transaction is a data access or an instruction access. The default value is normal non secure data access
P5	S_AXI_AWVALID	AXI4-Lite	I	-	Write address valid. This signal indicates that valid write address and control information are available
P6	S_AXI_AWREADY	AXI4-Lite	O	0	Write address ready. This signal indicates that the slave is ready to accept an address and associated control signals
AXI Write Data Channel Signals					
P7	S_AXI_WDATA[C_S_AXI_DATA_WIDTH-1:0]	AXI4-Lite	I	-	Write data bus
P8	S_AXI_WSTB[C_S_AXI_DATA_WIDTH/8-1:0](1)	AXI4-Lite	I	-	Write strobes. This signal indicates which byte lanes to update in memory
P10	S_AXI_WVALID	AXI4-Lite	I	-	Write valid. This signal indicates that valid write data and strobes are available
P11	S_AXI_WREADY	AXI4-Lite	O	0	Write ready. This signal indicates that the slave can accept the write data
AXI Write Response Channel Signals					
P12	S_AXI_BRESP[1:0]	AXI4-Lite	O	0	Write response. This signal indicates the status of the write transaction
P13	S_AXI_BVALID	AXI4-Lite	O	0	Write response valid. This signal indicates that a valid write response is available
P14	S_AXI_BREADY	AXI4-Lite	I	-	Response ready. This signal indicates that the master can accept the response information
AXI Read Address Channel Signals					
P15	S_AXI_ARADDR[C_S_AXI_ADDR_WIDTH -1:0]	AXI4-Lite	I	-	Read address. The read address bus gives the initial address of a read burst transaction
P16	S_AXI_ARPROT[2:0](1)	AXI4-Lite	I	-	Protection type. This signal provides protection unit information for the read transaction. The default value is normal non secure data access

Table 1: **I/O Signal Description *(Cont'd)***

Port	Signal Name	Interface	I/O	Initial State	Description
P17	S_AXI_ARVALID	AXI4-Lite	I	-	Read address valid. When High, this signal indicates that the read address and control information is valid and remains stable until the address acknowledgement signal, S_AXI_ARREDY, is High.
P18	S_AXI_ARREADY	AXI4-Lite	O	0	Read address ready. This signal indicates that the slave is ready to accept an address and associated control signals.
AXI Read Data Channel Signals					
P19	S_AXI_RDATA[C_S_AXI_DATA_WIDTH -1:0]	AXI4-Lite	O	0	Read data bus
P20	S_AXI_RRESP[1:0]	AXI4-Lite	O	0	Read response. This signal indicates the status of the read transfer.
P21	S_AXI_RVALID	AXI4-Lite	O	0	Read valid. This signal indicates that the required read data is available and the read transfer can complete
P22	S_AXI_RREADY	AXI4-Lite	I	-	Read ready. This signal indicates that the master can accept the read data and response information
APB Signals					
P23	M_APB_PCLK	APB	O	0	APB Clock - S_AXI_ACLK is tied to M_APB_PCLK
P24	M_APB_PRESETN	APB	O	0	APB Reset, active low - S_AXI_ARESETN is tied to M_APB_PRESETN
P25	M_APB_PADDR[C_M_APB_ADDR_WIDTH -1:0]	APB	O	0	Address. This is the APB address bus and is fixed to 32-bit.
P26	M_APB_PPROT[2:0](1)	APB	O	0	Protection type. This signal indicates the normal, privileged, or secure protection level of the transaction and whether the transaction is a data access or an instruction access.
P27	M_APB_PSEL[C_APB_NUM_SLAVES -1:0]	APB	O	0	Select. The AXI to APB bridge generates this signal to each peripheral bus slave. It indicates that the slave device is selected and that a data transfer is required. There is a M_APB_PSEL signal for each slave.
P28	M_APB_PENABLE	APB	O	0	Enable. This signal indicates the second and subsequent cycles of an APB transfer
P29	M_APB_PWRITE	APB	O	0	Direction. This signal indicates an APB write access when High and an APB read access when Low.
P30	M_APB_PWDATA[C_M_APB_DATA_WIDTH -1:0]	APB	O	0	Write data. This bus is driven by the AXI to APB bridge during write cycles when M_APB_PWRITE is High. This bus is fixed to 32 bits wide.
P31	M_APB_PSTRB[C_M_APB_DATA_WIDTH/8-1:0](1)	APB	O	0	Write strobes. This signal indicates which byte lanes to update during a write transfer. Write strobes must not be active during a read transfer.
P32	M_APB_PREADY[C_APB_NUM_SLAVES -1:0]	APB	I	-	Ready. The APB slave uses this signal to extend an APB transfer.

Table 1: **I/O Signal Description *(Cont'd)***

Port	Signal Name	Interface	I/O	Initial State	Description
P33	M_APB_PRDATA[C_M_APB_DATA_WIDTH -1:0]	APB	I	-	Read Data. The selected slave drives this bus during read cycles when M_APB_PWRITE is Low. This bus is fixed to 32-bits wide.
P34	M_APB_PSLVERR[C_APB_NUM_SLAVES -1:0]	APB	I	-	This signal indicates a transfer failure.

Notes:

1. This signal is only used when C_M_APB_PROTOCOL = apb4.

Design Parameters

Table 2 shows the design parameters of the AXI to APB Bridge.

Inferred Parameters

In addition to the parameters listed in Table 2, there are also parameters that are inferred for each AXI interface in the EDK tools. Through the design, these EDK-inferred parameters control the behavior of the AXI Interconnect. For a complete list of the interconnect settings related to the AXI interface, see DS768, *AXI Interconnect IP Data Sheet*.

Table 2: **Design Parameters**

Generic	Feature/Description	Parameter Name	Allowable Values	Default Values	VHDL Type
System Parameter					
G1	Target FPGA family	C_FAMILY	virtex6, spartan6	virtex6	string
AXI Parameters					
G2	AXI address bus width	C_S_AXI_ADDR_WIDTH	32	32	integer
G3	AXI data bus width	C_S_AXI_DATA_WIDTH	32	32	integer
G4	AXI interface type	C_S_AXI_PROTOCOL	axi4lite	axi4lite(1)	string
G5	AXI Base address	C_BASEADDR	Valid Address(2)	0xFFFFFFFF(4)	std_logic_vector
G6	AXI High address	C_HIGHADDR	Valid Address(3)	0x00000000(4)	std_logic_vector
APB Parameters					
G6	APB address bus width	C_M_APB_ADDR_WIDTH	32	32	integer
G7	APB data bus width	C_M_APB_DATA_WIDTH	32	32	integer
G8	Number of APB slaves connected to AXI to APB Bridge	C_APB_NUM_SLAVES	1	1	integer
G9	APB interface type	C_M_APB_PROTOCOL	apb3,apb4	apb3	string
AXI to APB Bridge Parameters					
G10	Data phase time out value in AXI clocks	C_DPHASE_TIMEOUT	0,16,32,64, 128,256	0	integer

Table 2: **Design Parameters *(Cont'd)***

Generic	Feature/Description	Parameter Name	Allowable Values	Default Values	VHDL Type

Notes:

1. This generic is needed by the system. Only AXI4-Lite interface is supported by AXI to APB Bridge.
2. The user must set the values. The C_BASEADDR must be a multiple of the range, where the range is C_HIGHADDR - C_BASEADDR + 1.
3. The range specified by C_HIGHADDR - C_BASEADDR must be a power of 2 and greater than or equal to 0xFFF.
4. An invalid default value is specified to ensure that the actual value is set; that is, if the value is not set, a compiler error is generated.

Parameter - I/O Signal Dependencies

The dependencies between the AXI to APB Bridge core design parameters and I/O signals are described in Table 3. In addition, when certain features are parameterized out of the design, the related logic is no longer a part of the design. The unused input signals and related output signals are set to a specified value.

Table 3: **Parameter-I/O Signal Dependencies**

Generic or Port	Name	Affects	Depends	Relationship Description
Design Parameters				
G5	C_M_APB_PROTOCOL	P4, P16, P26, P31	-	When C_M_APB_PROTOCOL = apb4, the signals C_M_APB_PPROT and C_M_APB_PWSTB are used.
I/O Signals				
P4	S_AXI_AWPROT[2:0]	-	G5	This signal is used when C_M_APB_PROTOCOL = apb4
P16	S_AXI_ARPROT[2:0]	-	G5	This signal is used when C_M_APB_PROTOCOL = apb4
P26	M_APB_PPROT[2:0]	-	G5	This signal is driven when C_M_APB_PROTOCOL = apb4
P31	M_APB_PWSTB[3: 0]	-	G5	This signal is driven when C_M_APB_PROTOCOL = apb4

Design Details

Clocking

The AXI to APB Bridge is a synchronous design and uses the S_AXI_ACLK at both AXI and APB interfaces. M_APB_PCLK is driven by the AXI to APB Bridge (tied to S_AXI_ACLK).

Reset

S_AXI_ARESETN is a synchronous reset input that resets the AXI to APB Bridge upon assertion. The S_AXI_ARESETN is also used to reset the APB interface. M_APB_PRESETN is driven by the AXI to APB Bridge (tied to S_AXI_ARESETN).

Memory Mapping

The AXI memory map and the APB memory map are one single complete 32-bit (4 GB) memory space. The AXI to APB Bridge does not modify the address for APB; hence, the address that is presented on the APB is exactly as received on the AXI.

Read and Write Ordering

When a read and a write requests are issued simultaneously (S_AXI_AWVALID/S_AXI_WVALID and S_AXI_ARVALID are asserted High) from AXI4-Lite, the AXI to APB Bridge gives more priority to the read request than to the write request. When both write and read requests are always valid, the write request is initiated on APB after the read is requested on APB.

AXI Response Signaling

EXOKAY is never used.

Endianness

Both AXI and APB are little-endian.

Address/data translation

No address/data translation/conversion from AXI4-Lite to APB takes place inside AXI to APB Bridge. The write/read address from AXI4-Lite is passed to APB address. AXI4-Lite write data is passed on to APB and APB read data is passed on to AXI4-Lite read data.

APB4 operation

When C_M_APB_PROTOCOL is set to apb4, AXI to APB Bridge drives M_APB_PSTRB and M_APB_PPROT signals. S_AXI_WSTRB is passed to M_APB_PSTRB during write transfers. S_AXI_ARPROT is driven on M_APB_PPROT during a read transfer and S_AXI_AWPROT is driven on M_APB_PPROT during a write transfer.

Bridge Error Conditions

M_APB_PSLVERR on APB results with the response of SLVERR on AXI4-Lite. AXI to APB Bridge never generates DECERR.

Bridge Time out Condition

A data phase time-out is implemented inside the AXI to APB Bridge, when C_DPHASE_TIMEOUT is not equal to 0. When a request is issued from AXI, the AXI to APB Bridge translates this request into corresponding APB transfer. If there is no response to the request by the APB slave (M_APB_PREADY is not asserted), the AXI to APB bridge waits for the number of clock cycles mentioned in C_DPHASE_TIMEOUT, then responds to AXI with OK response (and drives zeroes on S_AXI_RDATA during read transfer).

Register Descriptions

There are no registers in AXI to APB Bridge.

Not Supported Features/Limitations

AXI4-Lite Slave Interface

- 64-bit width is not supported
- When both write and read transfers are requests, read request is accepted and then write request is accepted.

Timing Diagrams

The timing diagram shown in Figure 2 illustrates the AXI to APB Bridge operation for various read and write transfers. This diagram shows that when both write and read requests are active, read is given more priority.

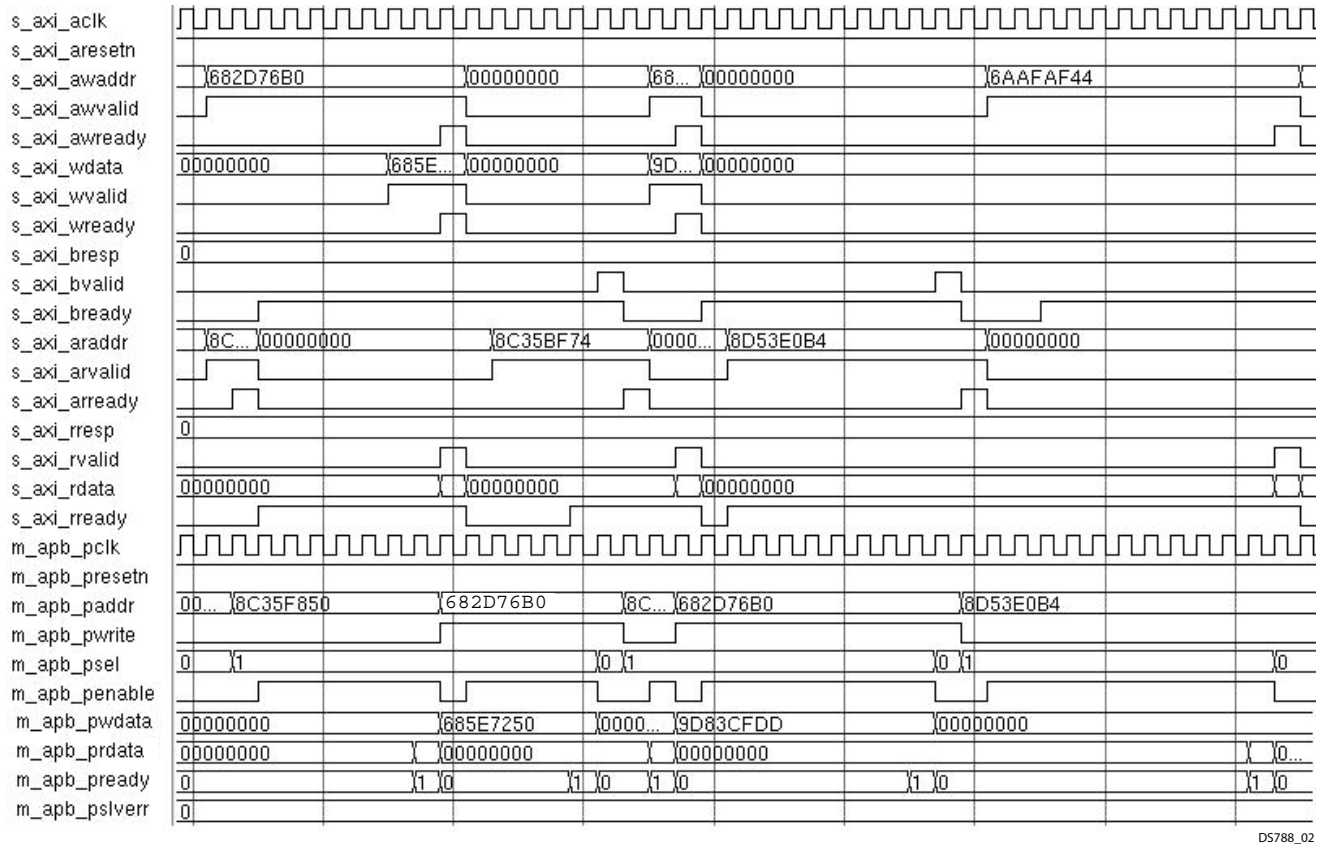

Figure 2: **Read and Write Transfers**

Device Utilization and Performance Benchmarks

Core Performance

Because the AXI to APB Bridge is a module that is used with other design pieces in the FPGA, the resource utilization and timing numbers reported in this section are estimates only. When the AXI to APB Bridge is combined with other pieces of the FPGA design, the utilization of FPGA resources and timing of the design varies from the results reported here.

The AXI to APB Bridge resource utilization benchmarks for a variety of parameter combinations measured with Virtex-6 FPGA as the target device are shown in Table 4.

Table 4: **Performance and Resource Utilization Benchmarks on the Virtex-6 FPGA (xc6vlx130t-ff1156-1)**

Parameter Values (other parameters at default value)			Device Resources			Performance
C_APB_NUM_SLAVES	C_M_APB_PROTOCOL	C_DPHASE_TIMEOUT	Slices	Slice Flip-Flops	LUTs	F_{MAX} (MHz)
1	apb3	0	30	146	120	436
1	apb3	16	39	152	153	389
1	apb4	256	49	167	160	399

The AXI to APB Bridge resource utilization benchmarks for a variety of parameter combinations measured with Spartan-6 FPGA as the target device are shown in Table 5.

Table 5: **Performance and Resource Utilization Benchmarks on the Spartan-6 FPGA (xc6slx100t-fgg900-2)**

Parameter Values (other parameters at default value)			Device Resources			Performance
C_APB_NUM_SLAVES	C_M_APB_PROTOCOL	C_DPHASE_TIMEOUT	Slices	Slice Flip-Flops	LUTs	F_{MAX} (MHz)
1	apb3	0	40	146	138	190
1	apb3	16	47	152	158	179
1	apb4	256	52	168	164	170

The AXI to APB Bridge resource utilization benchmarks for a variety of parameter combinations measured with Virtex-7 FPGA as the target device are shown in Table 6.

Table 6: **Performance and Resource Utilization Benchmarks on the Virtex-7 FPGA (xc7v855tffg1157-3)**

Parameter Values (other parameters at default value)			Device Resources			Performance
C_APB_NUM_SLAVES	C_M_APB_PROTOCOL	C_DPHASE_TIMEOUT	Slices	Slice Flip-Flops	LUTs	F_{MAX} (MHz)
1	apb3	0	35	145	133	659
1	apb3	16	39	151	143	459
1	apb4	256	44	166	169	391

The AXI to APB Bridge resource utilization benchmarks for a variety of parameter combinations measured with Artix-7 FPGA as the target device are shown in Table 7.

Table 7: **Performance and Resource Utilization Benchmarks on the Artix-7 FPGA (xc7a355tdie)**

Parameter Values (other parameters at default value)			Device Resources			Performance
C_APB_NUM_SLAVES	C_M_APB_PROTOCOL	C_DPHASE_TIMEOUT	Slices	Slice Flip-Flops	LUTs	F_{MAX} (MHz)
1	apb3	0	36	145	135	408
1	apb3	16	40	151	153	385
1	apb4	256	41	165	154	400

he AXI to APB Bridge resource utilization benchmarks for a variety of parameter combinations measured with Kintex-7 FPGA as the target device are shown in Table 8.

Table 8: **Performance and Resource Utilization Benchmarks on the Kintex-7 FPGA (xc7k410tffg676-3))**

Parameter Values (other parameters at default value)			Device Resources			Performance
C_APB_NUM_SLAVES	C_M_APB_PROTOCOL	C_DPHASE_TIMEOUT	Slices	Slice Flip-Flops	LUTs	F_{MAX} (MHz)
1	apb3	0	34	145	133	613
1	apb3	16	38	151	143	524
1	apb4	256	43	166	169	410

Read Latency

The core is configured for best possible configuration for calculation of read latency. The read latency from read address valid (S_AXI_ARVALID) to the data beat (S_AXI_RVALID) of AXI to APB Bridge is 3 clock cycles.

Reference Documents

The documents listed contain reference information important to understanding the AXI to APB Bridge design:

1. AXI4 AMBA AXI Protocol Version: 2.0 Specification
2. AMBA APB protocol Version: 2.0 Specification
3. DS160 Spartan-6 Family Overview
4. DS150 Virtex-6 Family Overview
5. DS180 7 Series FPGAs Overview

Support

Xilinx provides technical support for this LogiCORE product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

Ordering Information

This Xilinx LogiCORE IP module is provided at no additional cost with the Xilinx ISE® Design Suite Embedded Edition software under the terms of the Xilinx End User License. The core is generated using the Xilinx ISE Embedded Edition software (EDK).

Information about this and other Xilinx LogiCORE IP modules is available at the Xilinx Intellectual Property page. For information on pricing and availability of other Xilinx LogiCORE modules and software, contact your local Xilinx sales representative.

Revision History

This table shows the revision history for this document:

Date	Version	Description of Revisions
9/21/10	1.0	Initial release
6/22/11	1.1	Updated to ISE 13.2. Updated for Artix-7, Virtex-7, and Kintex-7.

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