IBERT for UltraScale GTY Transceivers v1.1

LogiCORE IP Product Guide

Vivado Design Suite

PG196 April 1, 2015

XILINX
ALL PROGRAMMABLE™

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Introduction

The customizable LogiCORE™ IP Integrated Bit Error Ratio Tester (IBERT) core for UltraScale architecture GTY transceivers is designed for evaluating and monitoring the GTY transceivers. This core includes pattern generators and checkers that are implemented in FPGA logic, and access to ports and the dynamic reconfiguration port attributes of the GTY transceivers. Communication logic is also included to allow the design to be run time accessible through JTAG. This core can be used as a self-contained or open design, based on customer configuration, and as described in this document.

Features

- Provides a communication path between the Vivado® serial I/O analyzer feature and the IBERT for UltraScale GTY Transceivers core
- Provides a user-selectable number of UltraScale architecture GTY transceivers
- Transceivers can be customized for the desired line rate, reference clock rate, and reference clock source
- Requires a system clock that can be sourced from a pin or one of the enabled GTY transceivers

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family(1)	Virtex® UltraScale
Supported User Interfaces	N/A
Resources	See Table 2-1 and Table 2-2.
Provided with Core	
Design Files	RTL
Example Design	Verilog
Test Bench	Not Provided
Constraints File	XDC
Simulation Model	Not Provided
Supported S/W Driver	N/A
Tested Design Flows(2)	
Design Entry	Vivado® Design Suite
Simulation	Not Provided
Synthesis	Vivado Synthesis
Support	
Provided by Xilinx @ www.xilinx.com/support	

Notes:

1. For a complete listing of supported devices, see the Vivado IP catalog.
2. For the supported versions of the tools, see the Xilinx Design Tools: Release Notes Guide.

Overview

Functional Description

The IBERT for UltraScale GTY Transceivers core provides a broad-based Physical Medium Attachment (PMA) evaluation and demonstration platform for UltraScale architecture GTY transceivers. Parameterizable to use different GTY transceivers and clocking topologies, the IBERT for UltraScale GTY Transceivers core can also be customized to use different line rates, reference clock rates, and logic widths. Data pattern generators and checkers are included for each GTY transceiver desired, giving several different Pseudo-random binary sequence (PRBS) and clock patterns to be sent over the channels.

In addition, the configuration and tuning of the GTY transceivers is accessible though logic that communicates to the Dynamic Reconfiguration Port (DRP) of the GTY transceiver, to change attribute settings, as well as registers that control the values on the ports. At run time, the Vivado™ serial I/O analyzer communicates to the IBERT for UltraScale GTY Transceivers core through JTAG, using the Xilinx cables and proprietary logic that is part of the IBERT for UltraScale GTY Transceivers core.

Feature Summary

The IBERT for UltraScale GTY Transceivers is designed for PMA evaluation and demonstration. All the major PMA features of the GTY transceiver are supported and controllable, including:

- TX pre-emphasis and post-emphasis
- TX differential swing
- RX equalization
- Decision Feedback Equalizer (DFE)
- Phase-Locked Loop (PLL) divider settings

Some of the Physical Coding Sublayer (PCS) features offered by the transceiver are outside the scope of IBERT, including:

- Clock Correction
- Channel Bonding
- 8B/10B, 64B/66B, or 64B/67B encoding
- TX or RX Buffer Bypass

PLL Configuration

For each serial transceiver channel, there is a ring PLL called Channel PLL (CPLL). The UltraScale GTY architecture has two additional shared PLLs per quad, QPLL0 and QPLL1. These PLLs are shared to support high speed, high performance, and low power multi-lane applications.

Figure 1-1 shows a Quad in the UltraScale architecture. The GTYE3_CHANNEL component has the serial transceiver and CPLL units and the GTYE3_COMMON has the QPLL unit.

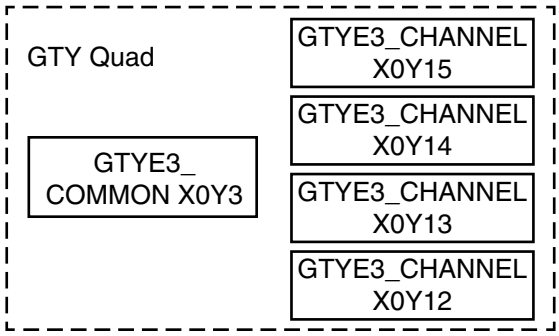

Figure 1-1: **Quad in UltraScale Architecture**

The serial transceiver REFCLK can be sourced from either CPLL or QPLL based on multiplexers as shown in Figure 1-2.

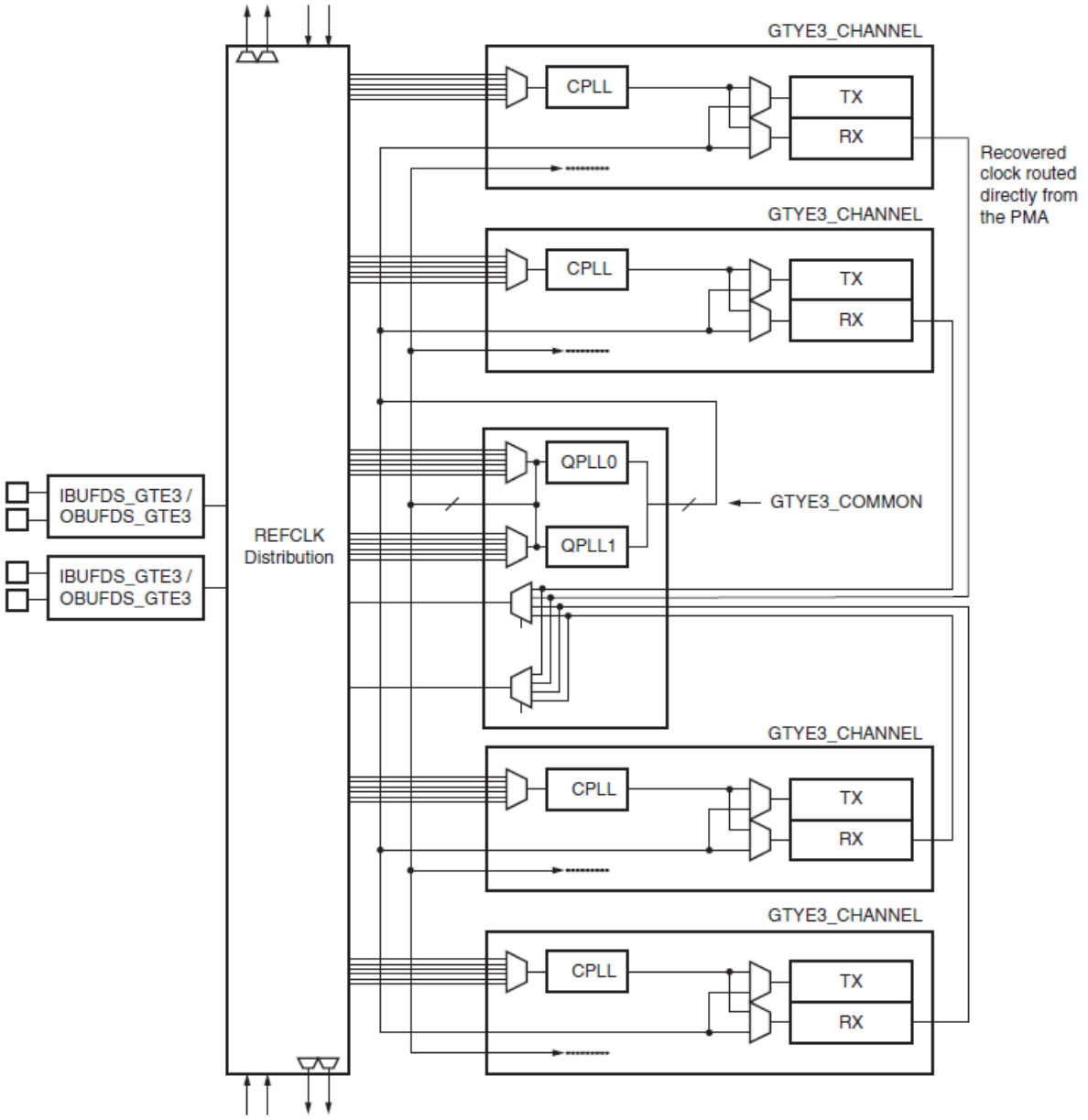

Figure 1-2: **Serial Transceiver REFCLK Sourcing**

Pattern Generation and Checking

Each GTY transceiver enabled in the IBERT design has a pattern generator and a pattern checker. The pattern generator sends data out through the transmitter. The pattern checker accepts data through the receiver and checks it against an internally generated pattern. IBERT offers PRBS 7-bit, PRBS 15-bit, PRBS 23-bit, PRBS 31-bit, Clk 2x (101010...), and Clk 10x (11111111110000000000...) patterns.

These patterns are optimized for the logic width that was selected at run time. The TX and RX patterns are individually selected.

Using the pattern checker logic, the incoming data is compared against a pattern that is internally generated. When the checker receives five consecutive cycles of data with no errors, the `LINK` signal is asserted. If the `LINK` signal is asserted and the checker receives five consecutive cycles with data errors, the `LINK` signal is deasserted. Internal counters accumulate the number of words and errors received.

DRP and Port Access

GTY transceiver ports and attributes can be changed. The DRP interface logic allows the run time software to monitor and change any attribute of the GTY transceivers and the corresponding CPLL/QPLL. When applicable, readable and writable registers are also included that are connected to the various ports of the GTY transceiver. All are accessible at run time using the Vivado serial I/O analyzer.

Applications

The IBERT for UltraScale GTY Transceivers core is designed to be used in any application that requires verification or evaluation of UltraScale architecture GTY transceivers.

Licensing and Ordering Information

This Xilinx LogiCORE IP module is provided at no additional cost with the Xilinx Vivado Design Suite tool under the terms of the Xilinx End User License.

Information about this and other Xilinx LogiCORE IP modules is available at the Xilinx Intellectual Property page. For information on pricing and availability of other Xilinx LogiCORE IP modules and tools, contact your local Xilinx sales representative.

Product Specification

Performance

The IBERT for UltraScale™ GTY Transceivers core can be configured to run any of the allowable line rates for the GTY transceivers.

Maximum Frequencies

The IBERT for UltraScale GTY Transceivers core can operate at the maximum user clock frequencies for the FPGA logic width/speed grade selected. The maximum system clock rate is 100 MHz and the generated design divides any incoming system clock to adhere to this constraint.

Resource Utilization

Resources required for the IBERT for UltraScale GTY Transceivers core have been estimated for the UltraScale architecture (Table 2-1 and Table 2-2). These values were generated using Vivado® IP catalog. They are derived from post-synthesis reports, and might change during place and route.

Table 2-1: **Configuration Details**

Configuration	Device	IBERT Setup
Config1	XCVU095-FFVD1924-3-E-ES1	1 Quad, 1 protocol set to 80b data width at 16.25 Gb/s with QPLL1 enabled.

Table 2-2: **UltraScale Architecture Resource Estimates**

Configuration	Device Resources				Performance
	LUTs	Flip-Flops	DSP Slices	Block RAMs	F_{Max} (MHz)
Config1	15,051	18,432	8	20	126.953125

Port Descriptions

The I/O signals of the IBERT for UltraScale GTY Transceivers core consist only of the GTY transceiver reference clocks, the GTY transceiver transmit and receive pins, and a system clock (optional).

Table 2-3: **IBERT I/O Signals**

Signal Name	I/O	Description
IBERT_SYSCLOCK_I	I	Clock that clocks all communication logic. This port is present only when an external clock is selected in the generator.
X_iY_j_TX_N_OPAD[n - 1:0](1)	O	Transmit differential pairs for each of the n GTY transceivers used.
X_iY_j_TX_P_OPAD[n - 1:0](1)		
X_iY_j_RX_N_IPAD[n - 1:0](1)	I	Receive differential pairs for each of the n GTY transceivers used.
X_iY_j_RX_P_IPAD[n - 1:0](1)		
Q_k_CLK0_MGTREFCLK_I[m - 1:0](2)	I	GTY transceiver reference clocks used. The number of MGTREFCLK ports can be equal to or less than the number of transmit and receive ports because some GTY transceivers can share clock inputs.
Q_k_CLK1_MGTREFCLK_I[m - 1:0](2)		

Notes:

1. The X_iY_j name refers to the GTY transceiver site location.
2. The Q_k name refers to the GTY transceiver quad site location.

Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the core.

General Design Guidelines

GTY Transceiver Naming Style

There are two conventions for naming the GTY transceiver, based on the location in the serial transceiver tile in the device. In the XmYn naming convention, m and n indicate the X and Y coordinates of the serial transceiver location. In serial transceiver m_n naming convention, m and n indicate serial transceiver number and the associated quad.

Line Rate Support

IBERT supports a maximum of three different line rates in a single design. For each of these line rates, you can select a custom value based on your requirements. Specify the number of serial transceivers for each line rate that is programmed with these settings. Because usage of QPLL is recommended for line rates above 8 Gb/s, you can select QPLL/CPLL for each line rate falling in the range 0.5 Gb/s to 30.5 Gb/s.

Serial Transceiver Location

Based on the total number of serial transceivers selected, provide the specific location of each serial transceiver that you intend to use. The region shown in the panel indicates the location of serial transceivers in the tile. This demarcation of region is based on the physical placement of serial transceivers with respect to median of BUFGs available for each device.

Clocking

System Clock

The IBERT for UltraScale GTY Transceivers core requires a free-running system clock for communication and other logic that is included in the core. This clock can be chosen at generation time to originate from an FPGA pin, or from a dedicated `REFCLK` input of one of the GTY transceivers. In order for the core to operate properly, this system clock source must remain operational and stable when the FPGA is configured with the IBERT for UltraScale GTY Transceivers core design.

If the system clock is running faster than 100 MHz, it is divided down internally using an Mixed-Mode Clock Manager (MMCM) to satisfy timing constraints. The clock source selected must be stable and free running after the FPGA is configured with the IBERT design. The system clock is used for core communication and as a reference for system measurements. Therefore, the clock source selected must remain operational and stable when using the IBERT for UltraScale GTY Transceivers core.

Receiver Output Clock

The receiver clock probe enable is provided to pull out a recovered clock from any serial transceiver, if desired. When enabled, a new panel appears just before the summary page where you can fill in the serial transceiver source and probe pin standards.

Reference Clock

The reference clock source should be provided for all the serial transceivers selected. The drop-down list provides you with possible sources based on local clocks in the same quad and shared clocks from north/south quads.

Resets

Run time resets are available for the IBERT counters and all GT resets are available. The reset controller helper block from the UltraScale Transceiver Wizard is used to properly time and sequence resets. See *UltraScale FPGAs Transceivers Wizard Product Guide* (PG182) [Ref 8] for details.

Design Flow Steps

This chapter describes customizing and generating the core, constraining the core, and synthesis and implementation steps that are specific to this IP core. More detailed information about the standard Vivado® design flows in the IP Integrator can be found in the following Vivado Design Suite user guides:

- *Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator* (UG994) [Ref 5]
- *Vivado Design Suite User Guide: Designing with IP* (UG896) [Ref 7]
- *Vivado Design Suite User Guide: Getting Started* (UG910) [Ref 4]

Customizing and Generating the Core

Vivado Integrated Design Environment (IDE)

You can customize the IP for use in your design by specifying values for the various parameters associated with the IP core using the following steps:

1. Select the IP from the Vivado IP catalog.
2. Double-click the selected IP or select the Customize IP command from the toolbar or right-click menu.

For details, see the *Vivado Design Suite User Guide: Designing with IP* (UG896) [Ref 7] and the *Vivado Design Suite User Guide: Getting Started* (UG910) [Ref 4].

Note: Figures in this chapter are illustrations of the Vivado IDE. The layout depicted here might vary from the current version.

The IBERT for UltraScale GTY Transceivers core can be found in `/Debug & Verification/Debug/` in the Vivado IP catalog.

To access the core name, perform the following:

1. Open a project by selecting **File** then **Open Project** or create a new project by selecting **File** then **New Project**.
2. Open the IP catalog and navigate to any of the taxonomies.
3. Double-click **IBERT UltraScale GTY** to bring up the IBERT Customize IP dialog box.

Entering the Component Name

The **Component Name** field can consist of any combination of alpha-numeric characters including the underscore symbol. However, the underscore symbol cannot be the first character in the component name.

Figure 4-1 to Figure 4-4 show the IBERT Customize IP dialog boxes with information about customizing ports.

Protocol Definition

A protocol is a line rate/data width/reference clock rate combination. Up to three protocols can be defined for an IBERT for UltraScale GTY Transceivers core, and any number of available Quads can be designated as any protocol defined.

1. Choose the number of protocols desired.
2. In the Protocol combination box, select either Custom or a Pre-defined protocol. If Custom, type in the line rate (the rate appears in red text if outside the range allowed).
   a. Select the data width.
   b. Choose the `REFCLK` rate and the number of Quads running at this rate.
3. Changing the line rate entered changes the choices in the `REFCLK` combination box.
4. The Quad PLL (QPLL0/QPLL1) is selected by default. To select CPLL instead, select CPLL from the combination box named PLL.

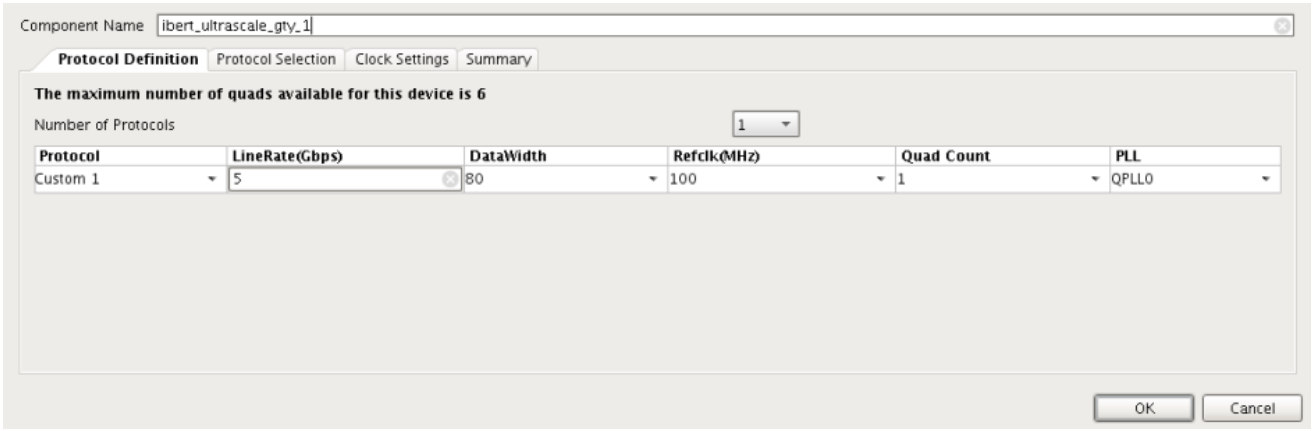

Figure 4-1: **Vivado Customize IP Dialog Box – Protocol Definition**

Protocol Selection

In the **Protocol Selection** tab, the Quads available in the device/package combination are shown. To allocate a Quad to a specific protocol, select it in the **Protocol Selected** combination. The legal choices for the reference clock input are listed in the REFCLK selection combination. Each channel uses its own TXOUTCLK as TXUSRCLK. The TXUSCLK source selection option is removed (as compared to IBERT 7 series GTH transceiver).

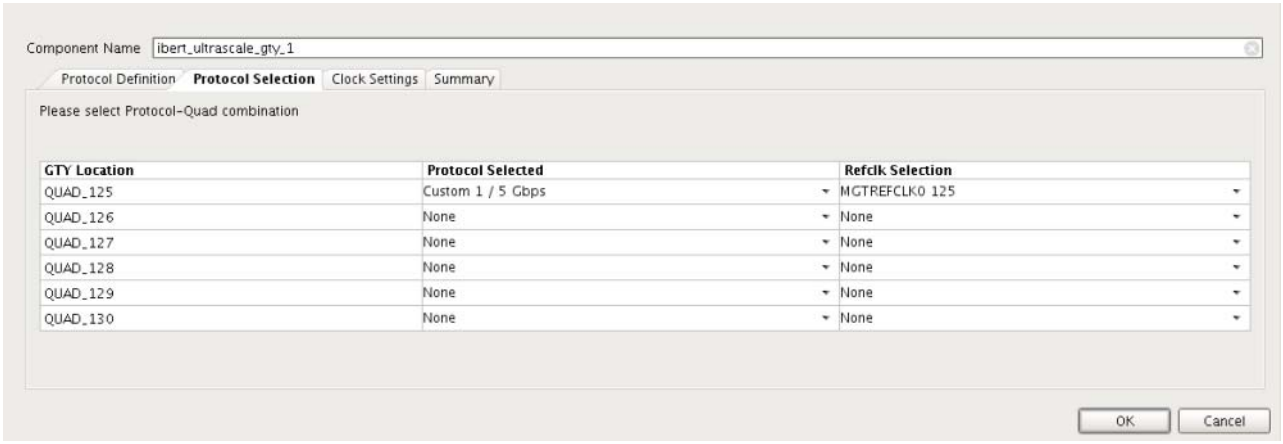

Figure 4-2: **Vivado Customize IP Dialog Box – Protocol Selection**

Clock Settings

In the **Clock Settings** tab, select **Add RXOUTCLK Probes** to drive an output pin or pin pair with the RXOUTCLK of required lane (0 to 3) of the Quad. Select the **I/O Standard** from the list and assign valid pin locations. For System Clock, specify an I/O Standard, valid pin locations, and frequency to complete the system clock settings. Alternatively, any enabled Quad reference clock can be selected instead.

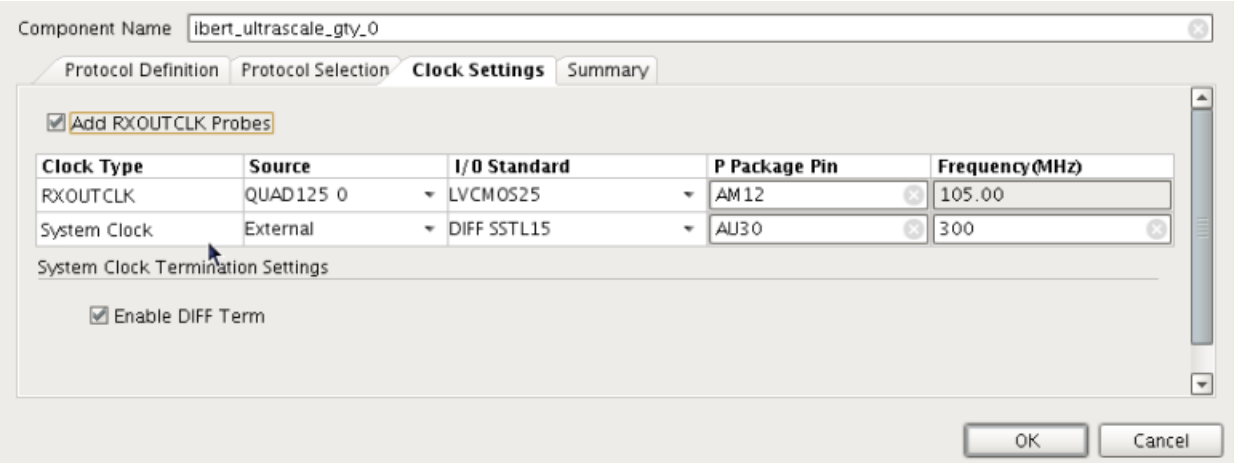

Figure 4-3: **Vivado Customize IP Dialog Box – Clock Settings**

Summary

Review the settings chosen in the summary page and if they are satisfactory, click **OK** to generate the IBERT for UltraScale GTY Transceivers core.

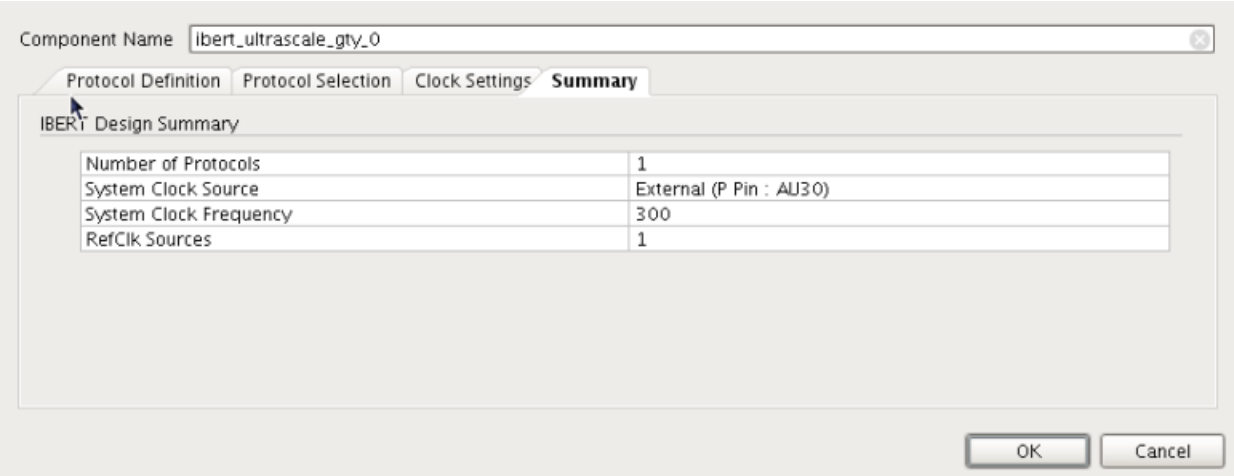

Figure 4-4: **Vivado Customize IP Dialog Box – Summary**

Output Generation

For details, see the *Vivado Design Suite User Guide: Designing with IP* (UG896) [Ref 7].

Constraining the Core

This section contains information about constraining the core in the Vivado Design Suite.

Required Constraints

The IBERT for UltraScale GTY Transceivers core is generated with its own timing and location constraints, based on the choices made when customizing the core. No additional constraints are required.

Device, Package, and Speed Grade Selections

This section is not applicable for this IP core.

Clock Frequencies

This section is not applicable for this IP core.

Clock Management

This section is not applicable for this IP core.

Clock Placement

This section is not applicable for this IP core.

Banking

This section is not applicable for this IP core.

Transceiver Placement

This section is not applicable for this IP core.

I/O Standard and Placement

This section is not applicable for this IP core.

Simulation

The IBERT for UltraScale GTY Transceivers core does not support simulation.

Synthesis and Implementation

This section contains information about synthesis and implementation in the Vivado Design Suite. For details about synthesis and implementation, see the *Vivado Design Suite User Guide: Designing with IP* (UG896) [Ref 7].

Interacting with Tcl Commands

After the design is loaded into the device, a set of `hw_sio` commands interact with the IBERT for UltraScale GTY Transceivers core. See the *Generating an IBERT Core using the Vivado IP Catalog* chapter in the *Vivado Design Suite User Guide: Programming and Debugging* (UG908) [Ref 2] for more details on Tcl commands.

Migrating and Upgrading

This appendix contains information about migrating a design from the ISE® Design Suite to the Vivado® Design Suite, and for upgrading to a more recent version of the IP core. For customers upgrading in the Vivado Design Suite, important details (where applicable) about any port changes and other impact to user logic are included.

Migrating to the Vivado Design Suite

For information about migrating to the Vivado Design Suite, see the *ISE to Vivado Design Suite Migration Guide* (UG911) [Ref 1].

Upgrading in the Vivado Design Suite

This section provides information about any changes to the user logic or port designations that take place when upgrading to a more current version of this IP core in the Vivado Design Suite.

Parameter Changes

No changes.

Port Changes

No changes.

Other Changes

No changes.

Debugging

This appendix includes details about resources available on the Xilinx Support website and debugging tools. In addition, this appendix provides a step-by-step debugging process to guide you through debugging the IBERT for UltraScale GTY Transceivers core.

The following topics are included in this appendix:

Finding Help on Xilinx.com

To help in the design and debug process when using the IBERT for UltraScale GTY Transceivers, the Xilinx Support web page (www.xilinx.com/support) contains key resources such as product documentation, release notes, answer records, information about known issues, and links for opening a Technical Support WebCase.

Documentation

This product guide is the main document associated with the IBERT for UltraScale GTY Transceivers. This guide, along with documentation related to all products that aid in the design process, can be found on the Xilinx Support web page (www.xilinx.com/support) or by using the Xilinx Documentation Navigator.

Download the Xilinx Documentation Navigator from the Design Tools tab on the Downloads page (www.xilinx.com/download). For more information about this tool and the features available, open the online help after installation.

Known Issues

Answer Records include information about commonly encountered problems, helpful information on how to resolve these problems, and any known issues with a Xilinx product. Answer Records are created and maintained daily ensuring that users have access to the most accurate information available.

Answer Records for this core are listed below, and can also be located by using the Search Support box on the main Xilinx support web page. To maximize your search results, use proper keywords such as

- Product name
- Tool message(s)
- Summary of the issue encountered

A filter search is available after results are returned to further target the results.

Master Answer Record for the IBERT for UltraScale GTY Transceivers Core

AR 54607.

Contacting Technical Support

Xilinx provides technical support at www.xilinx.com/support for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled DO NOT MODIFY.

To contact Xilinx Technical Support:

1. Navigate to www.xilinx.com/support.
2. Open a WebCase by selecting the WebCase link located under Support Quick Links.

When opening a WebCase, include:

- Target FPGA including package and speed grade.
- All applicable Xilinx Design Tools and simulator software versions.
- Additional files based on the specific issue might also be required. See the relevant sections in this debug guide for guidelines about which file(s) to include with the WebCase.

Debug Tools

There are many tools available to address IBERT for UltraScale GTY Transceivers design issues. It is important to know which tools are useful for debugging various situations.

Vivado Lab Edition

Vivado® Lab Edition inserts logic analyzer and virtual I/O cores directly into your design. Vivado Lab Edition also allows you to set trigger conditions to capture application and integrated block port signals in hardware. Captured signals can then be analyzed. This feature in the Vivado IDE is used for logic debugging and validation of a design running in Xilinx.

The Vivado logic analyzer is used to interact with the logic to debug LogiCORE IP cores, including:

- ILA 4.0 (and later versions)
- VIO 3.0 (and later versions)

License Checkers

If the IP requires a license key, the key must be verified. The Vivado design tools have several license check points for gating licensed IP through the flow. If the license check succeeds, the IP can continue generation. Otherwise, generation halts with error. License checkpoints are enforced by the following tools:

- Vivado Synthesis
- Vivado Implementation
- Bitstream Generation

IMPORTANT: *IP license level is ignored at checkpoints. The test confirms a valid license exists. It does not check IP license level.*

Appendix C

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

References

These documents provide supplemental material useful with this product guide:

1. *ISE to Vivado Design Suite Migration Guide* (UG911)
2. *Vivado Design Suite User Guide: Programming and Debugging* (UG908)
3. *Vivado Design Suite User Guide: Logic Simulation* (UG900)
4. *Vivado Design Suite User Guide: Getting Started* (UG910)
5. *Vivado Design Suite User Guide: Designing IP Subsystems Using IP Integrator* (UG994)
6. *Vivado Design Suite User Guide: Implementation* (UG904)
7. *Vivado Design Suite User Guide, Designing with IP* (UG896)
8. *UltraScale FPGAs Transceivers Wizard Product Guide* (PG182)

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
04/01/2015	1.1	Updated GUI screens. Updated Line Rate Support.
10/01/2014	1.0	Initial Xilinx release.

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