LogiCORE IP JESD204 (v1.1)

DS814 October 19, 2011 **Product Specification**

Introduction

The Xilinx® LogiCORE™ IP JESD204 core implements a JESD204A or JESD204B interface supporting a line rate of up to 6.25 Gb/s on 1, 2 or 4 lanes using GTX transceivers in Virtex®-6 and Kintex™-7 FPGAs. The JESD204 core can be configured as Transmit or Receive.

Features

- Designed to JEDEC JESD204A [Ref 1] and JESD204B [Ref 3]
- Supports 1, 2 and 4 lane configurations
- Supports Initial Lane Alignment
- Supports Scrambling
- Supports 1-256 Octets per frame
- Supports 1-32 Frames per Multi frame
- Physical and Data Link Layer functions provided
- AXI4-Lite Configuration Interface
- AXI4-Stream Data Interface [Ref 2]
- Delivered by CORE Generator™ software

LogiCORE IP Facts Table					
Core Specifics					
Supported Device Family(1)	Virtex-6 Kintex-7				
Supported User Interfaces	AXI4-Stream, AXI4-Lite Control/Status				
	Resources				
Configuration	**Slices**	**FFs**	**LUT**	**BUFG**	**Block RAM36**
Rx 1 Lane	430	880	1300	4(2)	1
Rx 2 Lane	920	1500	2070	4(2)	2
Rx 4 Lane	1750	2750	3800	4(2)	4
Tx 1 Lane	410	620	950	3	0
Tx 2 Lane	520	810	1230	3	0
Tx 4 Lane	770	1180	1740	3	0
Provided with Core					
Documentation	Product Specification User Guide				
Design Files	NGC Netlist				
Example Design	Verilog				
Test Bench	Verilog				
Constraints File	UCF				
Simulation Model	Verilog				
Tested Design Tools (3)					
Design Entry Tools	ISE software				
Simulation	ModelSim				
Synthesis Tools	XST				
Support					
Provided by Xilinx @ www.xilinx.com/support					

1. For a complete listing of supported devices, see the release notes for this core.
2. Four BUFGs required on Virtex-6 devices, two on Kintex-7 devices.
3. For the supported versions of the tool, see the ISE Design Suite 13: Release Notes Guide.

Overview

JESD204 is a high-speed serial interface designed to connect Analog-to-Digital Converter (ADCs) and Digital-to-Analog Converter (DACs) to logic devices. The JESD204 interface is specified in the JEDEC JESD204A Specification 2008 [Ref 1]and the JEDEC JESD204B Specification 2011 available from www.jedec.com [Ref 3].

Applications

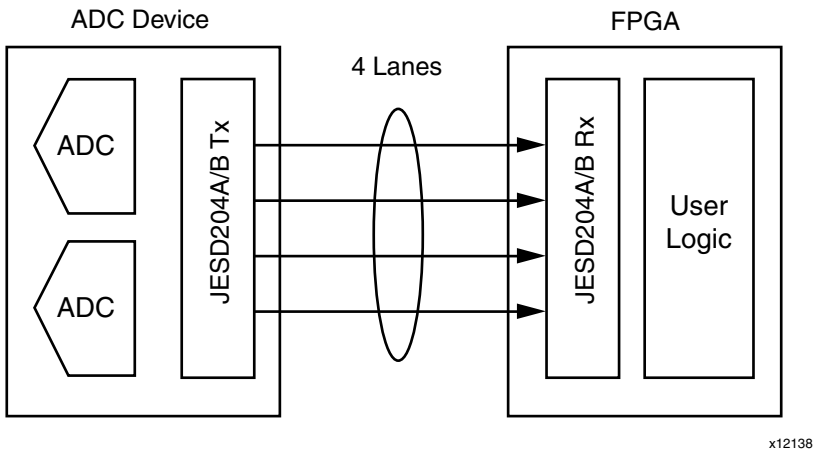

Figure 1: **ADC Application**

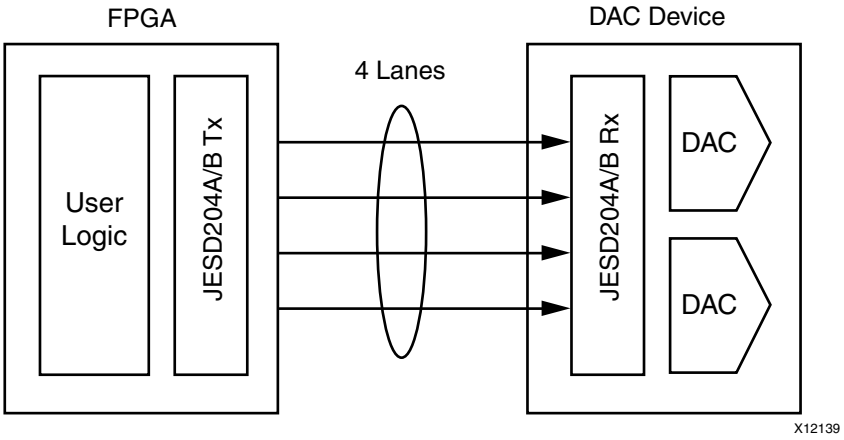

Figure 2: **DAC Application**

Functional Description

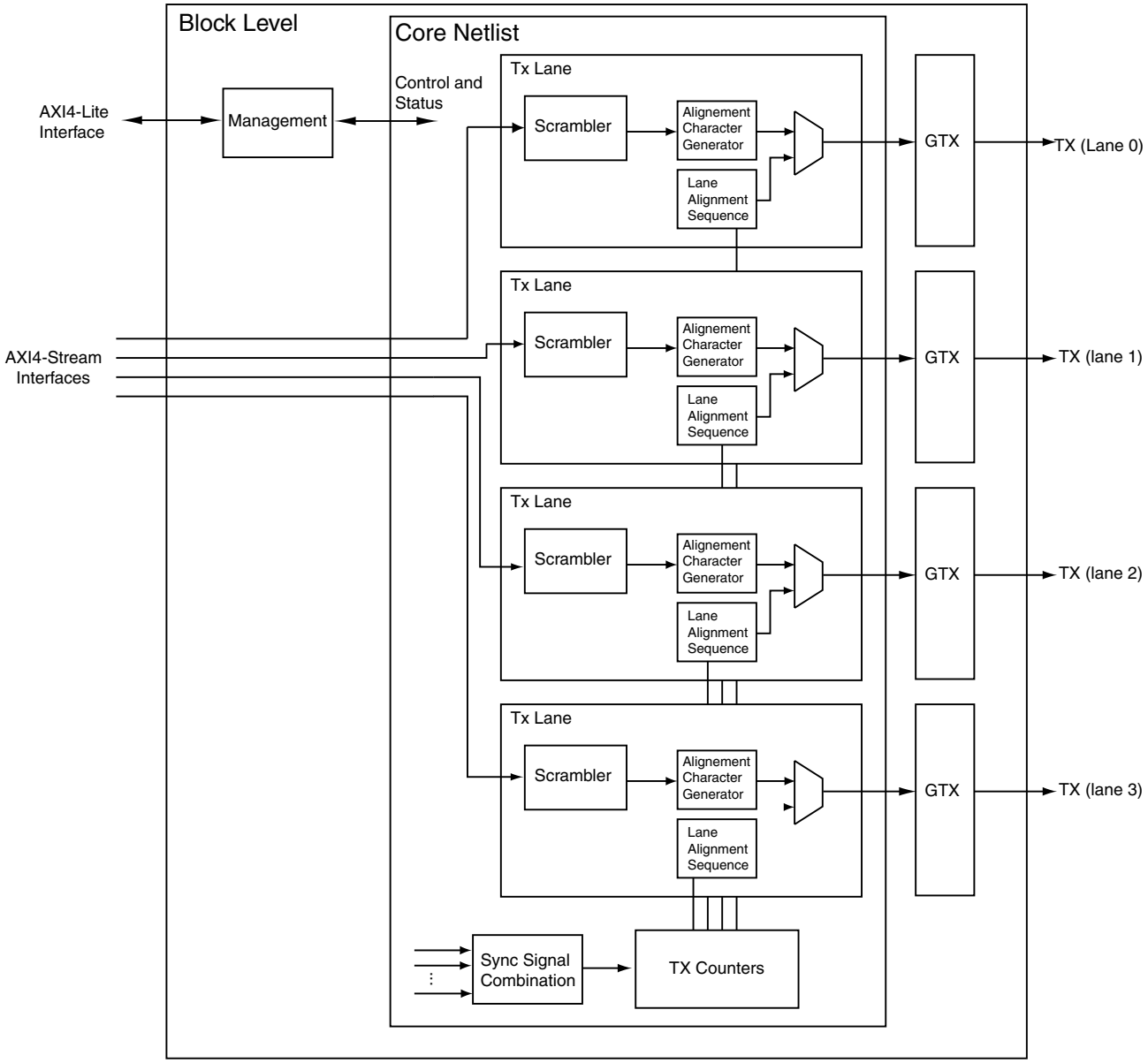

Figure 3: **Transmitter**

Description of Transmitter

- AXI4-Stream Interface for each lane
- Integrated Logic Analyzer (ILA) Generation for each lane
- Scrambling for each lane
- Alignment character insertion logic for each lane
- Control State Machine and Sync interface
- Transceiver Wrapper Logic
- Block Level Wrapper

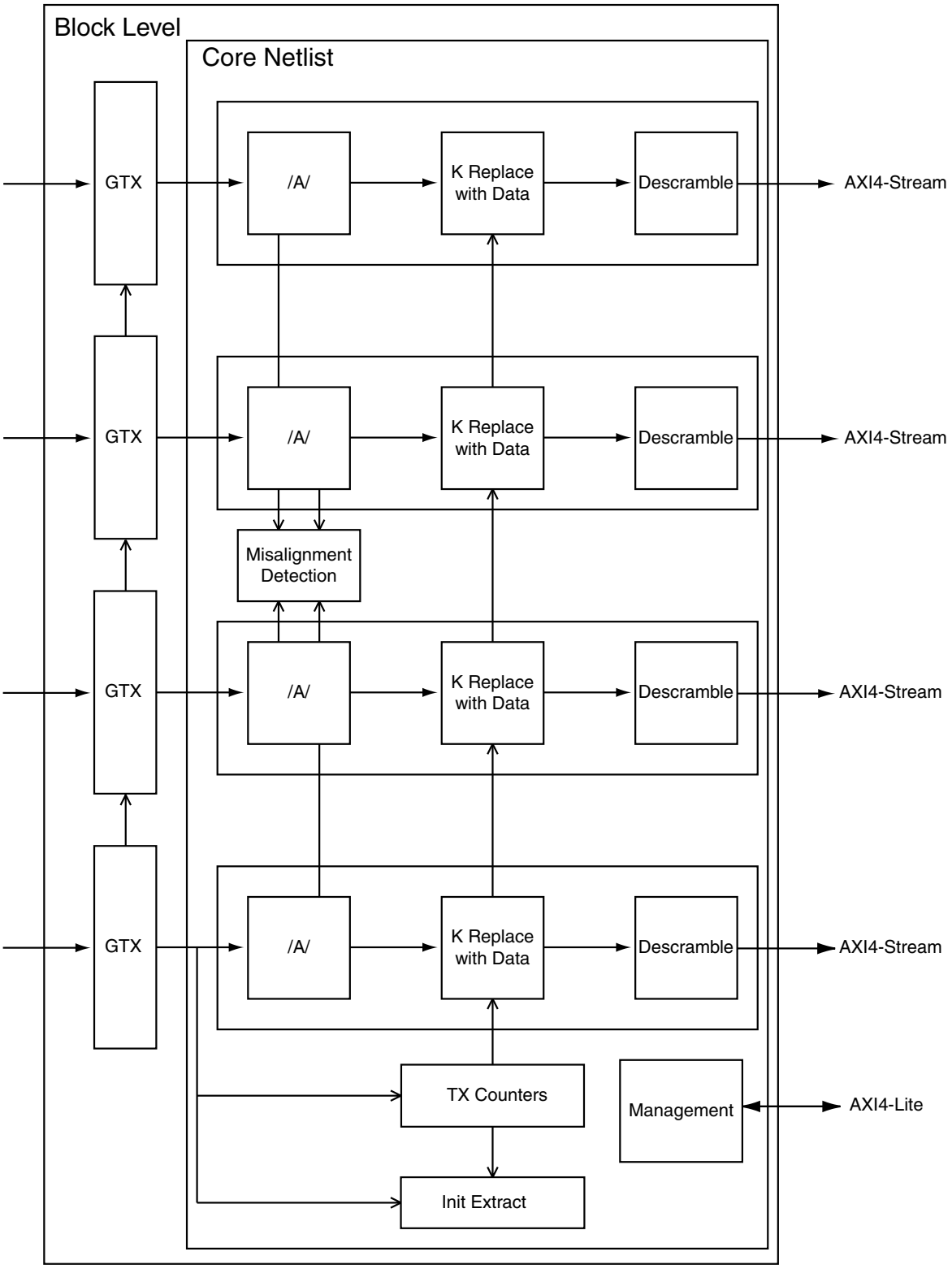

Figure 4: **Receiver**

Description of Receiver

- AXI4-Stream Interface for each lane
- ILA Capture for each lane
- Descrambling for each lane
- Alignment character detection and replacement logic for each lane
- Control State Machine and Sync interface
- Transceiver Wrapper Logic
- Block Level Wrapper
- Sample Mapping logic (optional)

References

To search for Xilinx documentation, go to http://www.xilinx.com/support.

To search for JESD204 documentation, go to http://www.jedec.org

1. JEDEC JESD204A April, 2008
2. Xilinx AXI User Guide
3. JEDEC JESD204B July, 2011

Support

Xilinx provides technical support for this LogiCORE IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

Ordering Information

A free evaluation version of the core is provided with the Xilinx CORE Generator software, which lets you assess the core functionality and demonstrates the various interfaces of the core in simulation. After purchase, the core can be downloaded from the Xilinx IP Center for use with the CORE Generator software v13.3 and higher. The CORE Generator software is bundled with ISE® Design Suite v13.3 software at no additional charge.

Contact your Xilinx sales representative for pricing and availability about the JESD204 core or go to the JESD204 product page for additional information.

List of Acronyms

Table 1: **List of Acronyms**

Acronym	Spelled Out
ADC	Analog-to-Digital Converter
AXI	Advanced eXtensible Interface
DAC	Digital-to-Analog Converter
DSP	Digital Signal Processing
FF	Flip-Flop
FPGA	Field Programmable Gate Array
ILA	Initial Lane Alignment
IP	Intellectual Property
ISE	Integrated Software Environment
JESD	JEDEC Standard
LUT	Lookup Table
NGC	Native Generic Circuit
RAM	Random Access Memory
Rx	Receive or Receiver
Tx	Transmit or Transmitter
XST	Xilinx Synthesis Technology

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
10/19/11	1.0	Initial Xilinx Release

Notice of Disclaimer