

## Introduction

The Xilinx® LogiCORE™ IP JESD204 core implements a JESD204B interface supporting line rates from 1 Gb/s to 12.5 Gb/s. The JESD204 core can be configured as transmit or receive.

## Additional Documentation

A product guide is available for this core. Access to this material may be requested by clicking on this registration link:  
[www.xilinx.com/member/jesd204/index.htm](http://www.xilinx.com/member/jesd204/index.htm).

## Features

- Designed to JEDEC® JESD204B
  - 1 to 12 lane configurations
  - Supports Initial Lane Alignment
  - Supports scrambling
  - 1-256 octets per frame<sup>(1)</sup>
  - 1-32 frames per multi frame<sup>(1)</sup>
  - Subclass 0, 1 and 2
  - Physical and Data Link Layer functions provided
  - AXI4-Lite configuration interface
  - AXI4-Stream data interface
  - Supports transceiver sharing between TX and RX cores
1. The maximum supported multi frame size is 1000 octets and the minimum is 20 octets.

LogiCORE IP Facts Table	
<b>Core Specifics</b>	
Supported Device Family <sup>(1)</sup>	UltraScale™ Architecture, Zynq®-7000 SoC, 7 Series
Supported User Interfaces	AXI4-Stream, AXI4-Lite
<b>Provided with Core</b>	
Design Files	Encrypted RTL
Example Design	Verilog
Test Bench	Verilog
Constraints File	XDC
Simulation Model	Verilog
Supported S/W Driver	N/A
<b>Tested Design Flows<sup>(2)</sup></b>	
Design Entry	Vivado® Design Suite IP Integrator
Simulation	For supported simulators, see the <a href="#">Xilinx Design Tools: Release Notes Guide</a> .
Synthesis	Vivado Synthesis
<b>Support</b>	
Provided by Xilinx @ <a href="http://www.xilinx.com/support">www.xilinx.com/support</a>	

### Notes:

1. For a complete listing of supported devices, see the Vivado IP catalog.
2. For the supported versions of the tools, see the [Xilinx Design Tools: Release Notes Guide](#).

## Overview

JESD204 is a high-speed serial interface designed to connect Analog-to-Digital Converter (ADCs) and Digital-to-Analog Converter (DACs) to logic devices. The JESD204 interface is specified in the *JEDEC JESD204A Specification 2008* and the *JEDEC JESD204B Specification 2011*. [Figure 1](#) and [Figure 2](#) illustrate how the JESD204 core provides the interface between an ADC/DAC and user logic over an example four lane interface.

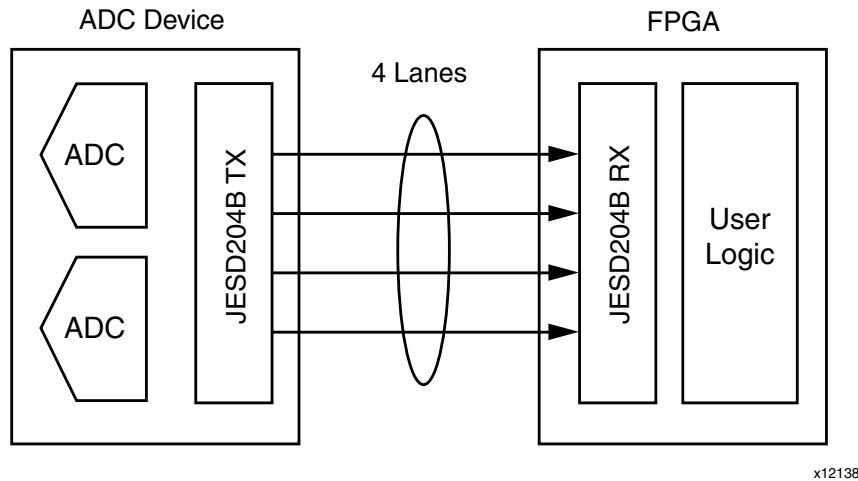


Figure 1: Example ADC Application

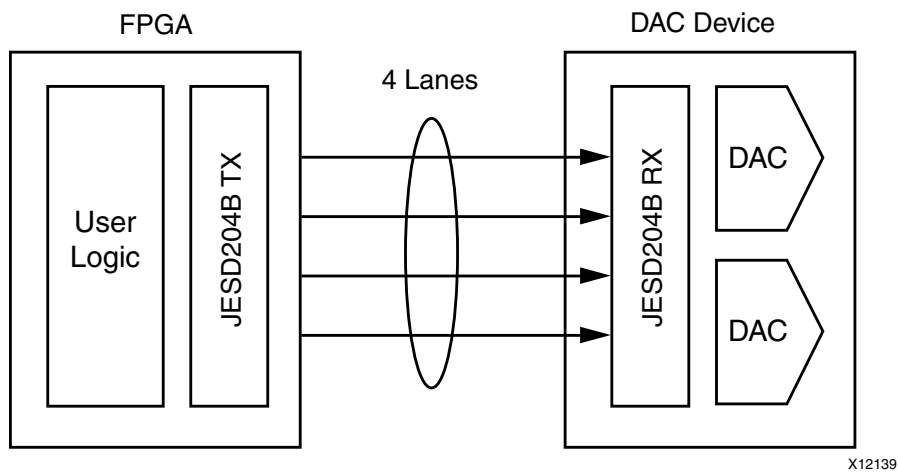


Figure 2: Example DAC Application

## Technical Support

Xilinx provides technical support at [www.xilinx.com/support](http://www.xilinx.com/support) for this LogiCORE IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled DO NOT MODIFY.

## Licensing and Ordering Information

A free evaluation version of the core is provided with the Xilinx Vivado Design Suite, which lets you assess the core functionality and demonstrates the various interfaces of the core in simulation. To access the evaluation version visit the [JESD204 IP Evaluation](#) page.

This Xilinx LogiCORE IP module is provided under the terms of the [Xilinx Core License Agreement](#). The module is shipped as part of the Vivado Design Suite. For full access to all core functionalities in simulation and in hardware, you must purchase a license for the core. Contact your [local Xilinx sales representative](#) for information about pricing and availability.

For more information, visit the JESD204 [product web page](#).

Information about other Xilinx LogiCORE IP modules is available at the [Xilinx Intellectual Property](#) page. For information on pricing and availability of other Xilinx LogiCORE IP modules and tools, contact your [local Xilinx sales representative](#).

## Revision History

The following table shows the revision history for this document:

Date	Version	Revision
06/04/2014	5.2	Associated Product Guide (PG066) updated with parameter table.
04/02/2014	5.2	Added core support for 12 lanes.
12/18/2013	5.1	Added UltraScale architecture support
10/02/2013	5.0	<ul style="list-style-type: none"> <li>Revision number advanced to 5.0 to align with core version number.</li> <li>Replaced option to generate shared core with option to include or exclude shareable logic resources in the core.</li> <li>Added option to include or exclude RPAT and JSPAT modules.</li> <li>Added optional transceiver control and status ports.</li> <li>Removed GUI option for JESD204 subclass selection; subclass is now selected using a register.</li> <li>AXI4-Lite address map has been updated.</li> <li>A single AXI4-Stream bus is used for all txdata and rxdata lanes</li> </ul>

Date	Version	Revision
03/20/2013	3.0	Updated to core version 4.0. <ul style="list-style-type: none"> <li>• Hierarchy updated; block level now the default core top level</li> <li>• AXI4-Lite address map corrections, including addition of byte write support</li> <li>• Added Artix-7 support</li> <li>• Increase rx_buffer_adjust from 256 to 1024</li> <li>• Pipeline stage added to receiver to improve timing</li> <li>• Zynq support added to HW demonstration platform</li> </ul>
12/18/2012	2.0	Updated for 2012.4 <ul style="list-style-type: none"> <li>• The core now supports 1, 2, 3, 4, 5, 6, 7 and 8 lane configurations in 7 series devices</li> <li>• Added 12.5 Gb/s line rate support</li> <li>• Removed JESD204A (new designs should use JESD204B subclass 0)</li> <li>• Removed ISE</li> <li>• Added three new test modes</li> <li>• Added software lane select</li> </ul>
07/25/2012	1.0	Initial Xilinx release.

## Please Read: Important Legal Notices

The information disclosed to you hereunder (the "Materials") is provided solely for the selection and use of Xilinx products. To the maximum extent permitted by applicable law: (1) Materials are made available "AS IS" and with all faults, Xilinx hereby DISCLAIMS ALL WARRANTIES AND CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY, INCLUDING BUT NOT LIMITED TO WARRANTIES OF MERCHANTABILITY, NON-INFRINGEMENT, OR FITNESS FOR ANY PARTICULAR PURPOSE; and (2) Xilinx shall not be liable (whether in contract or tort, including negligence, or under any other theory of liability) for any loss or damage of any kind or nature related to, arising under, or in connection with, the Materials (including your use of the Materials), including for any direct, indirect, special, incidental, or consequential loss or damage (including loss of data, profits, goodwill, or any type of loss or damage suffered as a result of any action brought by a third party) even if such damage or loss was reasonably foreseeable or Xilinx had been advised of the possibility of the same. Xilinx assumes no obligation to correct any errors contained in the Materials or to notify you of updates to the Materials or to product specifications. You may not reproduce, modify, distribute, or publicly display the Materials without prior written consent. Certain products are subject to the terms and conditions of Xilinx's limited warranty, please refer to Xilinx's Terms of Sale which can be viewed at <http://www.xilinx.com/legal.htm#tos>; IP cores may be subject to warranty and support terms contained in a license issued to you by Xilinx. Xilinx products are not designed or intended to be fail-safe or for use in any application requiring fail-safe performance; you assume sole risk and liability for use of Xilinx products in such critical applications, please refer to Xilinx's Terms of Sale which can be viewed at <http://www.xilinx.com/legal.htm#tos>.