LogiCORE IP Virtex-4 FX FPGA RocketIO Multi-Gigabit Transciever Wizard v1.7

DS138 April 19, 2010 **Product Specification**

Introduction

The LogiCORE™ IP Virtex®-4 FX FPGA RocketIO™ Multi-Gigabit Transceiver (MGT) Wizard automates the task of creating HDL wrappers to configure the high-speed serial multi-gigabit transceivers in the Virtex-4 FX family. The menu-driven interface allows one or more transceivers to be configured using pre-defined templates for popular industry standards, or from scratch, to support a wide variety of custom protocols.

The Wizard produces a wrapper, an example design, and a test bench for rapid integration and verification of the serial interface with your custom function.

Features

- Creates customized HDL wrappers to configure Virtex-4 FX FPGA RocketIO MGTs
- Users can configure Virtex-4 FX FPGA MGTs to conform to industry standard protocols using predefined templates, or tailor the templates for custom protocols
- Templates include support for the following specifications: Aurora 8B/10B, Fibre Channel, Gigabit Ethernet, GPON, Infiniband, OC12, PCI Express®, SATA 1.5 Gbps and SATA 3 Gbps, Serial RapidIO, and XAUI
- Automatically configures analog settings
- Each custom wrapper includes example design, test bench; and both implementation and simulation scripts

Note: See the *Virtex-4 FX FPGA RocketIO Multi-Gigabit Transceiver Wizard Getting Started Guide* [Ref 2] for a general overview of the wrapper creation procedure.

LogiCORE IP Facts	
Core Specifics	
Supported Device Family(1)	Virtex-4 FX
Provided with Core	
Documentation	Product Specification Getting Started Guide
Design File Formats	Verilog and VHDL
Constraints File	.ucf (user constraints file)
Verification	Example Design and Test Bench
Instantiation Template	Verilog or VHDL Wrapper
Design Tool Requirements	
Xilinx Implementation Tools	ISE® 12.1 (2)
Verification	Mentor Graphics ModelSim 6.5c and above
Simulation	Mentor Graphics ModelSim 6.5c and above
Synthesis	XST 12.1 Synopsys Synplify Pro D-2009.12
Support	
Provided by Xilinx, Inc. at http://www.xilinx.com/support	

1. For more information on the Virtex-4 devices, see *Virtex-4 Family Overview* [Ref 1]
2. ISE Service Packs can be downloaded from http://www.xilinx.com/support/download.htm

Functional Overview

Figure 1 outlines the steps required to configure multi-gigabit transceivers using the Wizard. Start the CORE Generator™ tool and select the Virtex-4 FX FPGA RocketIO Multi-Gigabit Transceiver Wizard, then follow the steps outlined in the chart to configure the transceivers and generate a wrapper that includes an accompanying example design. If an existing template is being used with no changes, click Generate. If modifying a standard template or starting from scratch, proceed through the Wizard and adjust the settings as needed.

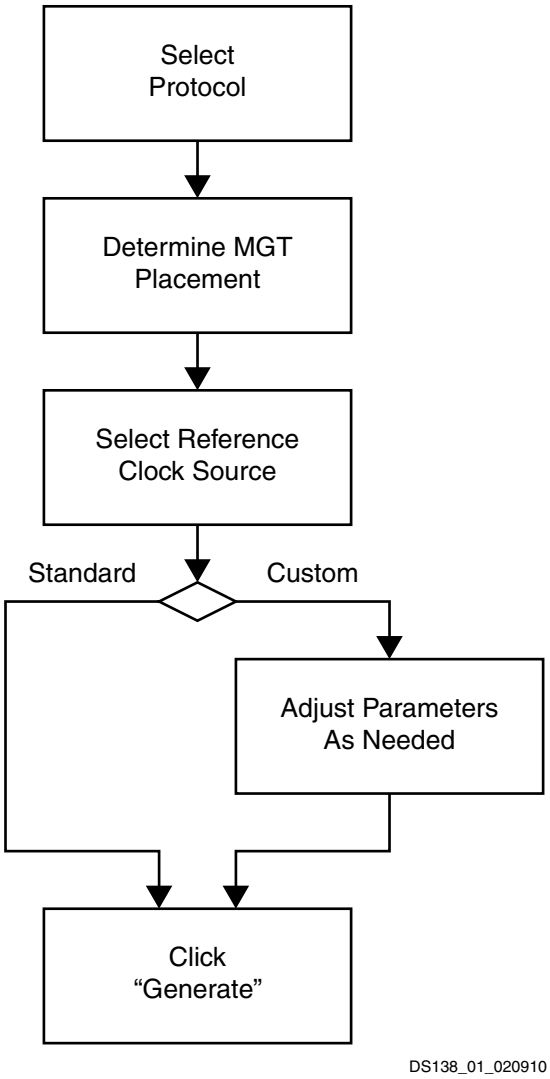

Figure 1: **RocketIO MGT Configuration Steps**

See *Virtex-4 RocketIO Multi-Gigabit Transceiver User Guide* [Ref 3] for details on the various features and parameters available.

Wrapper Overview

Figure 2 shows the block diagram of the wrapper, example design, and test bench produced by the Wizard.

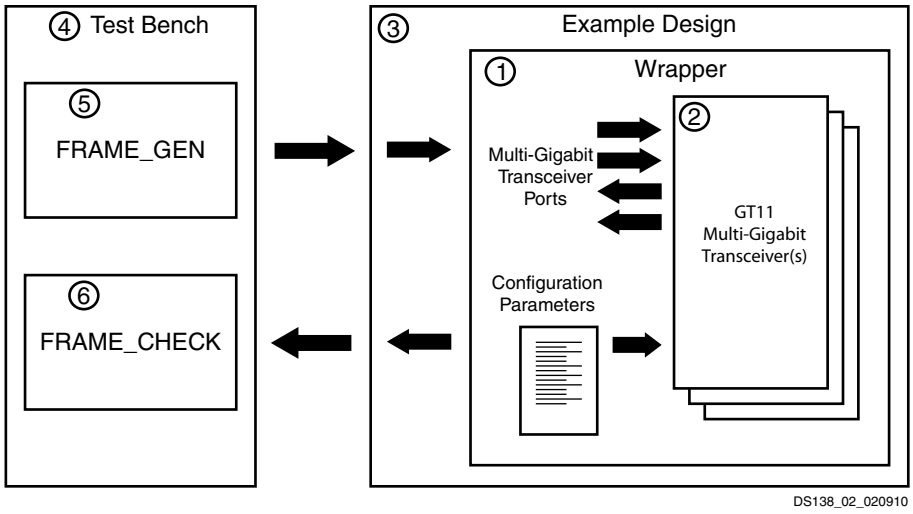

Figure 2: **Wrapper Block Diagram**

The wrapper comprises six components:

1. Wrapper: The specific transceiver configuration parameters set with the Wizard.
2. GT11 Multi-Gigabit Transceivers: Instantiated transceivers selected with the Wizard.
3. Example Design: Temporary top-level design that will be replaced with the actual application.
4. Test Bench: Top-level test bench to aid in simulation of the design.
5. FRAME_GEN Module: Generates a user-definable data stream for simulation analysis.
6. FRAME_CHECK Module: Tests for correct transmission of data stream for simulation analysis.

Support

Xilinx provides technical support for this LogiCORE IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled DO NOT MODIFY.

Ordering Information

The Virtex-4 FX FPGA RocketIO Multi-Gigabit Transceiver Wizard LogiCORE IP core is provided free of charge under the terms of the Xilinx End User License Agreement. The core can be generated by the Xilinx ISE CORE Generator software, which is a standard component of the Xilinx ISE Design Suite. This version of the core can be generated using the ISE CORE Generator system v12.1 or higher. For more information, please visit the Architecture Wizards web page. Information about additional Xilinx LogiCORE modules is available at the Xilinx IP Center. For pricing and availability of other Xilinx LogiCORE modules and software, please contact your local Xilinx sales representative.

References

1. DS112: *Virtex-4 Family Overview*
2. UG246: *Virtex-4 FX FPGA RocketIO Multi-Gigabit Transceiver Wizard Getting Started Guide*
3. UG076: *Virtex-4 RocketIO Multi-Gigabit Transceiver User Guide*

Revision History

Date	Version	Revision
03/01/07	1.4	Initial Xilinx release of data sheet for Virtex-4 RocketIO MGT Wizard.
03/24/08	1.6	Wizard v1.6 release.
03/24/08	1.6.1	Change “test bench” to two words. Add “IP” after “LogiCORE”. Add support link. Move ISE trademark from footnote to table. Add line above copyright statement.
05/16/08	1.6.2	Correct URL link to UG246.
04/19/10	1.7	Wizard 1.7 release. Replaced “GT11 Transceiver” with “Multi-Gigabit Transceiver” in the Wizard’s name. Added “LogiCORE IP” to the document’s title. Added "Support" and "Ordering Information."

Notice of Disclaimer