LogiCORE IP 10-Gigabit Ethernet PCS/PMA v2.1

DS739 March 1, 2011 **Product Specification**

Introduction

The LogiCORE™ IP 10-Gigabit Ethernet PCS/PMA core forms a seamless interface between the Xilinx® 10-Gigabit Ethernet Media Access Controller (MAC) and a 10 Gb/s-capable PHY, enabling the design of high-speed Ethernet systems and subsystems.

The core supports 10GBASE-R on Virtex®-7, Kintex™-7 and Virtex-6 HXT

Features

- Designed to 10-Gigabit Ethernet specification *IEEE 802.3-2008 clause 49*
- Optional Management Data Interface (MDIO) interface to manage PCS/PMA registers according to specification *IEEE 802.3-2008 clause 45*
- No-Cost core available under End User License Agreement
- Delivered through the Xilinx CORE Generator™ software
- Supports 10GBASE-SR, -LR and -ER optical links in Virtex-7, Kintex-7 and Virtex-6 devices (LAN mode only)
- SDR XGMII interface connects seamlessly to the Xilinx 10G Ethernet MAC

LogiCORE IP Facts			
Core Specifics			
Supported Device Family (1)	Virtex-7/Kintex-7 Virtex-6 HXT		
Supported User Interfaces	XGMII		
Resources Used			
Device	**LUTs**	**FFs**	**Block RAMs**
Virtex-7/Kintex-7	2100-2650	1910-2210	3
Virtex-6	590-876	710-960	0
Provided with Core			
Documentation	Product Specification User Guide		
Design Files	NGC netlist		
Example Design	VHDL, Verilog		
Test Bench	VHDL, Verilog		
Constraints File	.ucf (user constraints file)		
Verification	VHDL, Verilog Test Bench		
Instantiation Template	VHDL, Verilog Wrapper		
Tested Design Tools			
Design Entry Tools	ISE software v13.1		
Simulation	Mentor Graphics ModelSim version 6.6d Cadence Incisive Enterprise Simulator IES) v10.2 Synopsys VCS and VCS MX 2010.06		
Synthesis Tools	XST v13.1		
Support			
Provided by Xilinx, Inc.			

1. 10GBASE-R is pre-production status for all families. This IP was verified in software using pre-production speed files. For the complete list of supported devices, see the 13.1 release notes for this core.

Applications

Figure 1 shows a typical Ethernet system architecture and the 10-Gigabit Ethernet PCS/PMA core within it. The MAC and all the blocks to the right are defined in Ethernet IEEE specifications [Ref 1][Ref 2].

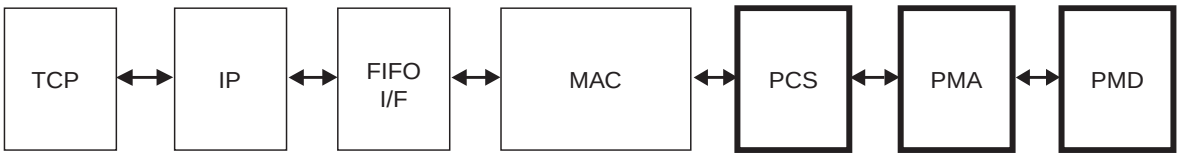

Figure 1: **Typical Ethernet System Architecture**

Figure 2 shows the 10-Gigabit Ethernet PCS/PMA core connected on one side to a 10-Gigabit MAC and on the other to an optical module (BASE-R) using a serial interface. The optional WIS part of the 10GBASE-R standard is not implemented in this core.

The 10-Gigabit Ethernet PCS/PMA core is designed to be attached to the Xilinx IP 10-Gigabit Ethernet MAC core over XGMII.

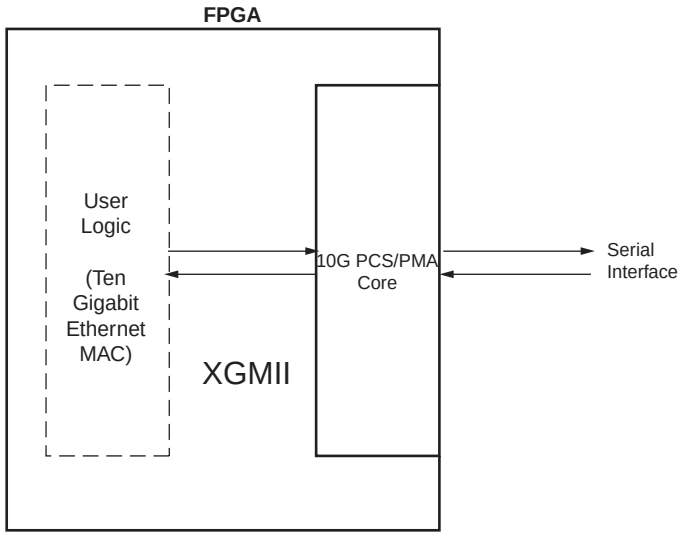

Figure 2: **10-Gigabit Ethernet PCS/PMA Core Connected to MAC Core Using XGMII Interface**

Functional Overview

10GBASE-R

Figure 3 illustrates a block diagram of the 10-Gigabit Ethernet PCS/PMA (BASE-R) core implementation on Virtex-6 devices. As you can see, in Virtex-6 devices, most of the functionality is contained within the GTH transceiver.

For Virtex-7/Kintex-7, all of the PCS and Management blocks illustrated, except the Gearbox and SERDES, are implemented in logic.

The major functional blocks of the core include the following:

- XGMII interface, designed for simple attachment of 10-Gigabit Ethernet MAC
- Transmit path, including Scrambler, 64B/66b Encoder and Gearbox
- Receive path, including Block Synchronization, Descrambler, Decoder and BER (Bit Error Rate) monitor
- Test Pattern Generation and Checking
- Serial interface to optics
- Management registers (PCS/PMA) with optional MDIO interface

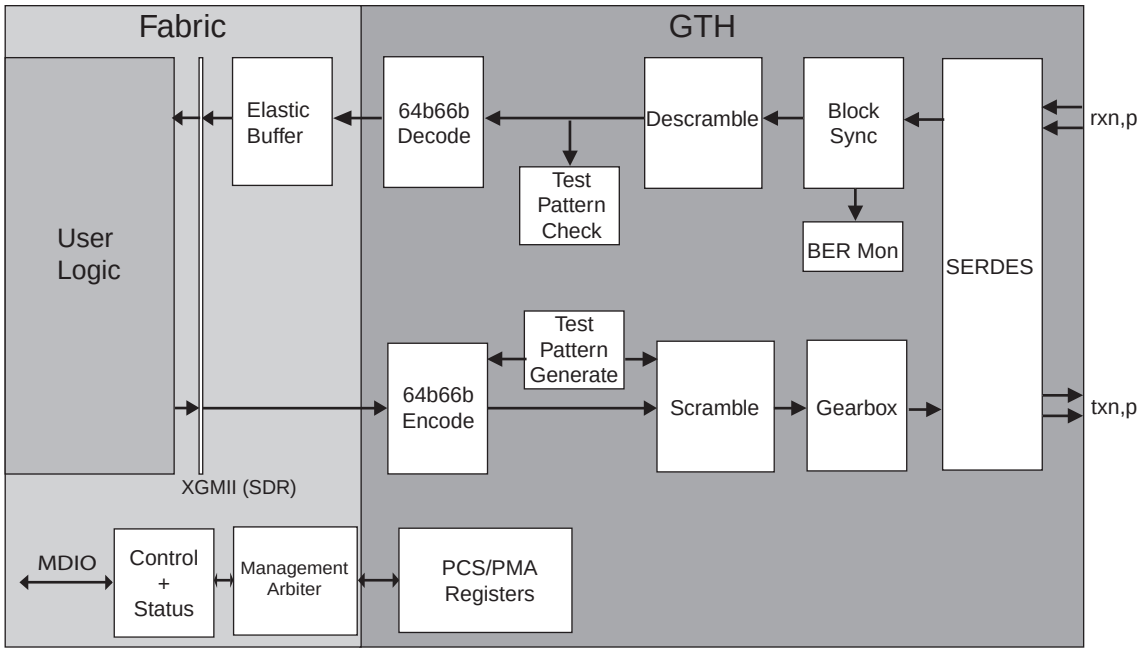

Figure 3: **Virtex-6 Implementation of the 10-Gigabit Ethernet PCS/PMA (BASE-R) Core**

Core Interfaces

MAC-Side Interface: XGMII

The MAC (or client) side of the core has a 64-bit datapath plus 8 control bits implementing an XGMII interface. Table 1 defines the signals, which are all synchronous to the 156.25 MHz core clock. It is designed to be easily connected to either user logic within the FPGA or, by using SelectIO™ technology DDR registers in the user's own design top-level, to provide an external 32-bit 312 Mb/s DDR XGMII defined in clause 46 of *IEEE 802.3-2008*.

Table 1: **MAC-Side Interface Port Description**

Signal Name	Direction	Description
xgmii_txd[63:0]	In	64-bit transmit data word
xgmii_txc[7:0]	In	8-bit transmit control word
xgmii_rxd[63:0]	Out	64-bit receive data word
xgmii_rxc[7:0]	Out	8-bit receive control word

Figure 4 illustrates transmitting a frame through the client-side interface.

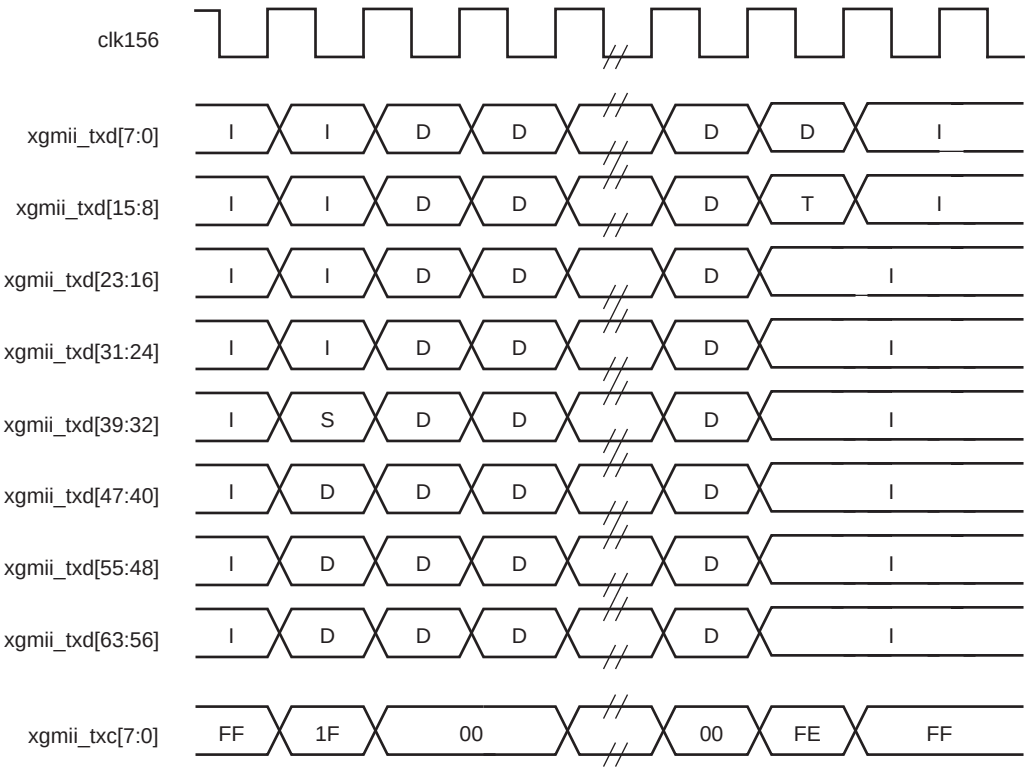

Figure 4: **Transmitting a Frame Through the Client-Side Interface**

Figure 5 illustrates receiving a frame through the client-side interface.

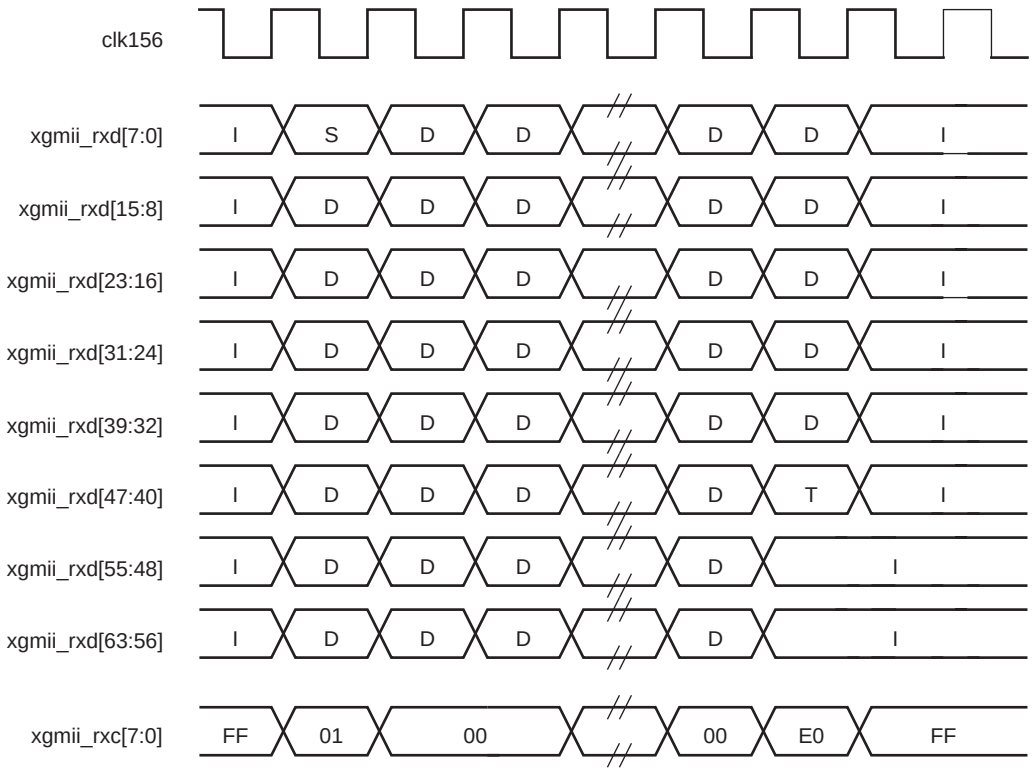

Figure 5: **Receiving a Frame Through the Client-Side Interface**

Transceiver Interface

The following tables describe the signals which connect the core to the transceiver. For Virtex-7/Kintex-7 FPGAs, the mapping of transceiver signals is not one-to-one.

Table 2: **Transceiver-Side Interface Port Description - Virtex-6 10GBASE-R**

Signal Name	Direction	Description
gt_txd[63:0]	Out	64-bit transmit data word
gt_txc[7:0]	Out	8-bit transmit control word
gt_rxd[63:0]	In	64-bit receive data word
gt_rxc[7:0]	In	8-bit receive control word

Table 3: **Transceiver-Side Interface Port Description - Virtex-7/Kintex-7**

Signal Name	Direction	Description
gt_txd[63:0]	Out	64-bit transmit data word
gt_txc[1:0]	Out	2-bit transmit sync header
gt_txc[7:2]	Out	6-bit txsequence count (0..32)
gt_rxd[63:0]	In	64-bit receive data word
gt_rxc[1:0]	In	2-bit receive sync header
gt_rxc[2]	In	RXDATAVALID (high for 32 in 33 rxusrclk2 cycles)
gt_rxc[7:3]	In	Not Used

Management Interface (MDIO)

The optional MDIO interface is a simple low-speed two-wire interface for management of the 10-Gigabit Ethernet PCS/PMA core, consisting of a clock signal and a bidirectional data signal. The interface is defined in clause 45 of the *IEEE 802.3-2008* standard.

In this core, the MDIO interface is an optional block. If implemented, the bidirectional data signal MDIO is implemented as three unidirectional signals. These can be used to drive a 3-state buffer either in the FPGA IOB or in a separate device.

For the BASE-R core in Virtex-6 FPGAs, the registers in the GTHE1 is pre-read as soon as the address phase of the MDIO transfer is complete and this data is provided back to the MDIO interface on completion of the READ phase of the MDIO transfer.

Table 4: **MDIO Management Interface Ports**

Signal Name	Direction	Description
mdc	In	Management clock
mdio_in	In	MDIO Input
mdio_out	Out	MDIO Output
mdio_tri	Out	MDIO 3-state control. "1" disconnects the output driver from the MDIO bus.
prtad[4:0]	In	MDIO port address. When multiple MDIO-managed ports appear on the same bus, this address can be used to address each port individually.

Configuration and Status Signals

As an alternative to the MDIO interface, vector-based interfaces can be provided to allow control and status to flow to and from the core. Table 5 describes these two vectors. Neither vector is completely populated so the actual number of pins required is much lower than the maximum widths of the vectors. For the status vector, correct default values are provided for all bits in the associated IEEE registers.

Table 5: **Configuration and Status Vectors**

Signal Name	Direction	Description
configuration_vector[535:0]	In	Configures the PCS/PMA registers
status_vector[447:0]	Out	Reflects *recent* status of PCS/PMA registers

Clock, Reset and Miscellaneous Signals

The various clocks, resets and other ports on the core are described in Table 6.

Table 6: **Clock, Reset and Miscellaneous Signals**

Signal Name	Direction	Description
dclk_reset	In	Sync reset in dclk domain
reset	In	Synchronous reset signal in clk156 domain
rxreset	In	Sync reset in rxclk156 domain (1)
txreset161	In	Sync reset in txusrclk2 domain (1)
rxreset161	In	Sync reset in rxusrclk2 domain (1)
dclk	In	Management clock
clk156	In	Core clock - User should use this in their own logic
rxclk156	In	Receive path clock - Derived from recovered clock
rxusrclk2	In	Receive path clock - Derived from recovered clock (1)
txusrclk2	In	Transmit path clock - Derived from TXCLKOUT (1)
signal_detect	In	Signal Detect indication from Optics (2)
tx_fault	In	Tx Fault indication from Optics (2)
tx_disable	Out	Disable the laser in Optics
core_status[7:0]	Out	PCS Block lock in bit 0 (1). Other bits are reserved

1. Not connected in Virtex-6 devices
2. These signals are not connected inside the core; the user should employ these signals where applicable, to reset the core. An example is given in the core example design.

Verification

The 10-Gigabit Ethernet PCS/PMA core has been verified using simulation. Check the core product page for more information.

Simulation

A highly parameterizable transaction-based simulation test suite was used to verify the core. Verification tests include:

- Register access over MDIO
- Loss and regain of synchronization
- Frame transmission
- Frame reception
- Clock compensation
- Recovery from error conditions

Device Utilization

Virtex-7/Kintex-7 FPGAs

Table 7 provides approximate slice counts for the BASE-R options on Virtex-7/Kintex-7 FPGAs.

Table 7: **Device Utilization - BASE-R on Virtex-7/Kintex-7 FPGAs**

Parameter Values	Device Resources		
MDIO Interface	Slices	LUTs	FFs
No	900	2096	1907
Yes	981	2633	2209

Virtex-6 HXT FPGAs

Table 8 provides approximate slice counts for the two BASE-R core options on Virtex-6 HXT FPGAs.

Table 8: **Device Utilization - Virtex-6 HXT FPGAs**

Parameter Values	Device Resources		
MDIO Interface	Slices	LUTs	FFs
No	355	876	961
Yes	236	590	706

References

1. *IEEE Std. 802.3-2008*, Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications
2. *IEEE Std. 802.3-2008*, Media Access Control (MAC) Parameters, Physical Layers, and Management Parameters for 10-Gb/s Operation

Support

Visit www.xilinx.com/support for technical support. Xilinx provides technical support for this LogiCORE IP product when used as described in the product documentation.

Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not listed in the documentation or if customized beyond that allowed in the product documentation, or if any changes are made in sections of the design marked *DO NOT MODIFY*.

Ordering Information

The core is provided under the Xilinx End User License Agreement and can be generated using CORE Generator software v13.1 and higher. The CORE Generator software is shipped with Xilinx ISE® Design Suite software.

In ISE v13.1 software and later, a license key is not required to access the IP. To access the IP in previous versions, a no cost full license must be obtained from Xilinx. See the 10GBASE-R product page. Contact your local Xilinx sales representative for pricing and availability of Xilinx LogiCORE IP modules and software. Information on additional LogiCORE IP modules is available on the Xilinx IP Center.

List of Acronyms

Acronym	Spelled Out
CSMA/CD	Carrier Sense Multiple Access with Collision Detection
DDR	Double Data Rate
FF	flip-flop
FIFO	First In First Out
FPGA	Field Programmable Gate Array.
Gb/s	Gigabits per second
IES	Incisive Enterprise Simulator
IO	Input/Output
IP	Intellectual Property
ISE	Integrated Software Environment
LUT	Lookup Table
MAC	Media Access Controller
Mb/s	Megabits per second
MDIO	Management Data Input/Output
MHz	Mega Hertz
NGC	Native Generic Circuit
PCS	Physical Coding Sublayer
PMA	Physical Medium Attachment
PMD	Physical Medium Dependent
UCF	User Constraints File
VHDL	VHSIC Hardware Description Language (VHSIC an acronym for Very High-Speed Integrated Circuits)
WIS	WAN Interface Sublayer
XGMII	10-Gigabit Ethernet Media Independent Interface

Revision History

Date	Version	Revision
12/02/09	1.1	Initial Xilinx release.
04/19/10	1.2	Updated to core version 1.2; updated to Xilinx tools 12.1.
03/01/11	2.1	Updated to core version 2.1; updated to Xilinx tools 13.1.

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