

LogiCORE IP Gamma Correction v6.01.a

Product Guide

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SECTION I: SUMMARY

IP Facts

Overview

Product Specification

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Introduction

The Xilinx LogiCORE™ IP Gamma Correction core provides customers with an optimized hardware block for manipulating image data to match the response of display devices. This core is implemented using a look-up table structure that is programmed to implement a gamma correction curve transform on the input image data. Programmable number of Gamma tables enable having separate gamma tables for all color channels, separate tables for luminance and chrominance channels, or one gamma table to be shared by all color channels.

Features

- Programmable gamma table supports gamma correction or any user defined function
- One, two or three channel independent or shared look-up table structure allow potential resource reduction
- AXI4-Stream data interfaces
- Supports 8, 10 and 12-bits per color component input and output
- Supports Spatial resolutions from 32x32 up to 7680x7680
 - Supports 1080P60 in all supported device families ⁽¹⁾
 - Supports 4kx2k @24Hz in supported high performance devices
- Optional features:
 - Interpolated output values for 12-bit data to reduce resource requirements
 - AXI4-Lite Control interface allowing real-time re-programming of gamma tables
 - Double buffering of control interface to prevent image tearing
 - Built-in throughput monitors to assist with system optimization
 - Bypass and test pattern generator mode to assist with system bring up and debug

1. Performance on low power devices may be lower.

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family ⁽¹⁾	Zynq-7000 ⁽²⁾ , Artix-7, Virtex®-7, Kintex®-7, Virtex-6, Spartan®-6
Supported User Interfaces	AXI4-Lite, AXI4-Stream ⁽³⁾
Resources	See Table 2-1 through Table 2-8 .
Provided with Core	
Documentation	Product Guide
Design Files	ISE: NGC netlist, Encrypted HDL Vivado: Encrypted RTL
Example Design	Not Provided
Test Bench	Verilog ⁽⁴⁾
Constraints File	Not Provided
Simulation Models	VHDL or Verilog Structural, C Model ⁽⁴⁾
Supported Software Drivers	Not Applicable
Tested Design Flows ⁽⁶⁾	
Design Entry Tools	ISE™ v14.3 tool, Vivado™ v2012.3 Design Suite ⁽⁷⁾ , Platform Studio (XPS)
Simulation ⁽⁵⁾	Mentor Graphics ModelSim, Xilinx® ISim
Synthesis Tools	Xilinx Synthesis Technology (XST) Vivado Synthesis
Support	
Provided by Xilinx, Inc.	

1. For a complete listing of supported devices, see the [release notes](#) for this core.
2. Supported in ISE Design Suite implementations only.
3. Video protocol as defined in the *Video IP: AXI Feature Adoption* section of [UG761 AXI Reference Guide](#).
4. HDL test bench and C Model available on the product page on Xilinx.com at <http://www.xilinx.com/products/ipcenter/EF-DI-GAMMA.htm>
5. For the supported versions of the tools, see the [ISE Design Suite 14: Release Notes Guide](#).
6. For the supported versions of the tools, see the [Xilinx Design Tools: Release Notes Guide](#).
7. Supports only 7 series devices.

Overview

Gamma correction, also known as gamma compression or encoding, is used to encode linear luminance or RGB values to match the non-linear characteristics of display devices. Gamma correction helps to map data into a more perceptually uniform domain, so as to optimize perceptual performance of a limited signal range, such as a limited number of bits in each RGB component.

Gamma correction is, in the simplest cases, defined by

$$V_{out} = V_{in}^{\gamma}$$

where the input and output values are between 0 and 1 (Figure 1-1). The case $\gamma < 1$ is often called gamma compression and $\gamma > 1$ is called gamma expansion.

When used in conjunction with an embedded or external processor, the Gamma Correction core supports frame-by-frame dynamic reprogramming of the gamma tables. The gamma tables can be reprogrammed with arbitrary functions, supporting a wide range of applications, such as intensity correction, feature enhancement, lin-log, log-lin conversion and thresholding.

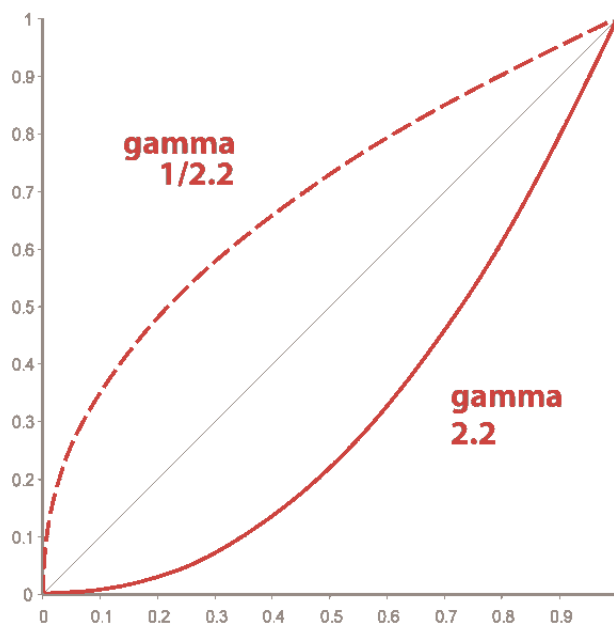


Figure 1-1: Gamma Correction

The Gamma Correction core also offers various configuration options for a designer to optimize the block RAM footprint required by the core.

The Gamma Correction core is implemented as a set of Look-Up-Tables that are used to perform the data transformation. The width of the input data determines the number of entries in the Look-Up-Table. For example, 8-bit input data would require 2^8 (256) entries in the Look-Up-Table. The width of the output data determines the width of each entry in the Look-Up-Table. For example, 12-bit output data would require that each entry in the table be 12-bits wide.

Feature Summary

The Gamma Correction core provides programmable look-up tables for gamma correction. A programmable number of Gamma tables allows for separate gamma tables for all color channels, separate tables for luminance and chrominance channels, or one gamma table to be shared by all color channels. Higher resolutions and frame rates can be supported in Xilinx high-performance device families.

Applications

- Pre-processing block for image sensors
- Post-processing block for image data adjustment
- Intensity correction
- Video surveillance
- Consumer displays
- Video conferencing
- Machine vision

Licensing and Ordering Information

This Xilinx LogiCORE IP module is provided under the terms of the [Xilinx Core License Agreement](#). The module is shipped as part of the Vivado Design Suite/ISE Design Suite. For full access to all core functionalities in simulation and in hardware, you must purchase a license for the core. Contact your [local Xilinx sales representative](#) for information about pricing and availability.

For more information, visit the Gamma Correction product web page.

Information about other Xilinx LogiCORE IP modules is available at the [Xilinx Intellectual Property](#) page. For information on pricing and availability of other Xilinx LogiCORE IP modules and tools, contact your [local Xilinx sales representative](#).

Product Specification

Standards

The Gamma Correction core is compliant with the AXI4-Stream Video Protocol and AXI4-Lite interconnect standards. Refer to the *Video IP: AXI Feature Adoption* section of the *AXI Reference Guide* (UG761) [Ref 1] for additional information.

Performance

The following sections detail the performance characteristics of the Gamma Correction core.

Maximum Frequencies

This section contains typical clock frequencies for the target devices. The maximum achievable clock frequency can vary. The maximum achievable clock frequency and all resource counts can be affected by other tool options, additional logic in the FPGA device, using a different version of Xilinx tools and other factors. Refer to in [Table 2-1](#) through [Table 2-8](#) for device-specific information.

Latency

The propagation delay of the Gamma Correction core is always five clock cycles.

Throughput

The Gamma Correction core outputs one sample per clock cycle.

Resource Utilization

For an accurate measure of the usage of primitives, slices, and CLBs for a particular instance, check the **Display Core Viewer after Generation**.

Resource Utilization using ISE Tools

The information presented in [Table 2-1](#) through [Table 2-5](#) is a guide to the resource utilization and maximum clock frequency of the Gamma Correction core for all input/output width combinations for Virtex-7, Kintex-7, Artix-7, Zynq-7000, Virtex-6, and Spartan-6 FPGA families. This core does not use any DSP48s, dedicated I/O, or CLK resources. The design was tested using ISE[®] v14.3 tools with default tool options for characterization data. For resource utilization using Vivado Design Suite, see [Resource Utilization using Vivado Tools](#).

When the AXI4-Lite Register Interface is enabled, add the following values to the values in the tables: LUT-FF Pairs: 500, LUTs: 300 and FFs: 470. Enabling the Double-Buffered Interface typically doubles the RAM resources that are used.

Table 2-1: Spartan-6

Input Data Width	Output Data Width	Interpolation	LUT-FF Pairs	LUTs	FFs	RAM 16 / 8	DSP48S	Fmax (MHz)
8	8	0	280	261	159	0 / 0	0	180
	10	0	292	261	172	0 / 0	0	180
	12	0	306	269	184	0 / 0	0	180
10	8	0	293	267	171	0 / 0	0	188
	10	0	298	271	184	0 / 0	0	188
	12	0	307	282	196	0 / 0	0	180
12	8	0	327	277	207	0 / 0	0	172
	10	0	337	284	226	0 / 0	0	172
	12	0	356	291	244	0 / 0	0	180
	12	1	444	432	220	0 / 0	0	148

Table 2-2: Virtex-7

Input Data Width	Output Data Width	Interpolation	LUT-FF Pairs	LUTs	FFs	RAM 36/ 18	DSP48S	Fmax (MHz)
8	8	0	257	231	155	0 / 2	0	312
	10	0	267	235	167	0 / 2	0	304
	12	0	274	251	179	0 / 2	0	312
10	8	0	267	241	167	0 / 2	0	304
	10	0	275	247	179	0 / 2	0	312
	12	0	290	254	191	0 / 2	0	312

Table 2-2: Virtex-7 (Cont'd)

Input Data Width	Output Data Width	Interpolation	LUT-FF Pairs	LUTs	FFs	RAM 36/18	DSP48S	Fmax (MHz)
12	8	0	274	251	179	2 / 0	0	304
	10	0	286	256	191	2 / 2	0	304
	12	0	296	267	203	2 / 2	0	288
	12	1	438	421	221	0 / 3	0	258

Table 2-3: Virtex-6

Input Data Width	Output Data Width	Interpolation	LUT-FF Pairs	LUTs	FFs	RAM 36/18	DSP48S	Fmax (MHz)
8	8	0	251	225	155	0 / 2	0	274
	10	0	258	232	167	0 / 2	0	266
	12	0	272	241	179	0 / 2	0	274
10	8	0	259	234	167	0 / 2	0	281
	10	0	266	242	179	0 / 2	0	274
	12	0	284	246	191	0 / 2	0	274
12	8	0	268	244	179	2 / 0	0	281
	10	0	279	248	191	2 / 2	0	258
	12	0	292	258	203	2 / 2	0	258
	12	1	416	401	215	0 / 3	0	212

Table 2-4: Kintex-7 (and Zynq-7000 Devices with Kintex Based Fabric)

Input Data Width	Output Data Width	Interpolation	LUT-FF Pairs	LUTs	FFs	RAM 36/18	DSP48S	Fmax (MHz)
8	8	0	257	231	155	0 / 2	0	312
	10	0	267	235	167	0 / 2	0	312
	12	0	278	247	179	0 / 2	0	328
10	8	0	267	241	167	0 / 2	0	304
	10	0	265	249	179	0 / 2	0	304
	12	0	288	256	191	0 / 2	0	304
12	8	0	276	252	179	2 / 0	0	304
	10	0	285	257	191	2 / 2	0	312
	12	0	301	263	203	2 / 2	0	304
	12	1	436	420	221	0 / 3	0	258

Table 2-5: Artix-7(and Zynq-7000 Devices with Artix Based Fabric)

Input Data Width	Output Data Width	Interpolation	LUT-FF Pairs	LUTs	FFs	RAM 36/18	DSP48S	Fmax (MHz)
8	8	0	263	245	155	0 / 2	0	196
	10	0	276	245	167	0 / 2	0	212
	12	0	272	261	179	0 / 2	0	212
10	8	0	272	254	167	0 / 2	0	219
	10	0	284	256	179	0 / 2	0	204
	12	0	292	265	191	0 / 2	0	212
12	8	0	285	261	179	2 / 0	0	212
	10	0	292	268	191	2 / 2	0	219
	12	0	308	274	203	2 / 2	0	212
	12	1	480	463	221	0 / 3	0	188

For an accurate measure of the usage of primitives, slices, and CLBs for a particular instance, check the **Display Core Viewer after Generation**.

Resource Utilization using Vivado Tools

Table 2-6 through Table 2-8 were generated using Vivado Design Suite 2012.3 with default tool options for characterization data.

Table 2-6: Virtex-7

Input Data Width	Output Data Width	Interpolation	LUT-FF Pairs	LUTs	FFs	Slices	RAM 36/18	DSP48S	Fmax (MHz)
8	8	0	287	181	265	89	0 / 2	0	266
	10	0	302	184	283	92	0 / 2	0	258
	12	0	292	192	301	95	0 / 2	0	274
10	8	0	308	187	295	98	0 / 2	0	258
	10	0	324	190	313	99	0 / 2	0	242
	12	0	324	195	331	100	0 / 2	0	274
12	8	0	322	189	325	96	2 / 0	0	242
	10	0	347	193	343	111	2 / 2	0	274
	12	0	344	199	361	102	2 / 2	0	296
	12	1	455	309	409	136	0 / 3	0	304

Table 2-7: Kintex-7

Input Data Width	Output Data Width	Interpolation	LUT-FF Pairs	LUTs	FFs	Slices	RAM 36/18	DSP48S	Fmax (MHz)
8	8	0	285	182	265	86	0 / 2	0	266
	10	0	313	187	283	100	0 / 2	0	250
	12	0	305	190	301	97	0 / 2	0	266
10	8	0	302	186	295	91	0 / 2	0	266
	10	0	333	188	313	105	0 / 2	0	274
	12	0	347	194	331	117	0 / 2	0	258
12	8	0	322	191	325	101	2 / 0	0	281
	10	0	350	194	343	113	2 / 2	0	281
	12	0	363	194	361	119	2 / 2	0	274
	12	1	485	310	409	164	0 / 3	0	296

Table 2-8: Artix-7

Input Data Width	Output Data Width	Interpolation	LUT-FF Pairs	LUTs	FFs	Slices	RAM 36/18	DSP48S	Fmax (MHz)
8	8	0	283	181	265	86	0 / 2	0	188
	10	0	308	187	283	101	0 / 2	0	196
	12	0	308	190	301	99	0 / 2	0	180
10	8	0	293	187	295	89	0 / 2	0	188
	10	0	334	190	313	106	0 / 2	0	180
	12	0	320	196	331	105	0 / 2	0	188
12	8	0	312	191	325	97	2 / 0	0	196
	10	0	356	196	343	121	2 / 2	0	180
	12	0	360	194	361	119	2 / 2	0	180
	12	1	471	307	409	152	0 / 3	0	204

Core Interfaces and Register Space

Port Descriptions

The Gamma Correction core uses industry standard control and data interfaces to connect to other system components. The following sections describe the various interfaces available with the core. [Figure 2-1](#) illustrates an I/O diagram of the Gamma Correction core. Some signals are optional and not present for all configurations of the core. The AXI4-Lite interface and the `IRQ` pin are present only when the core is configured via the GUI with an AXI4-Lite control interface. The `INTC_IF` interface is present only when the core is configured via the GUI with the INTC interface enabled.

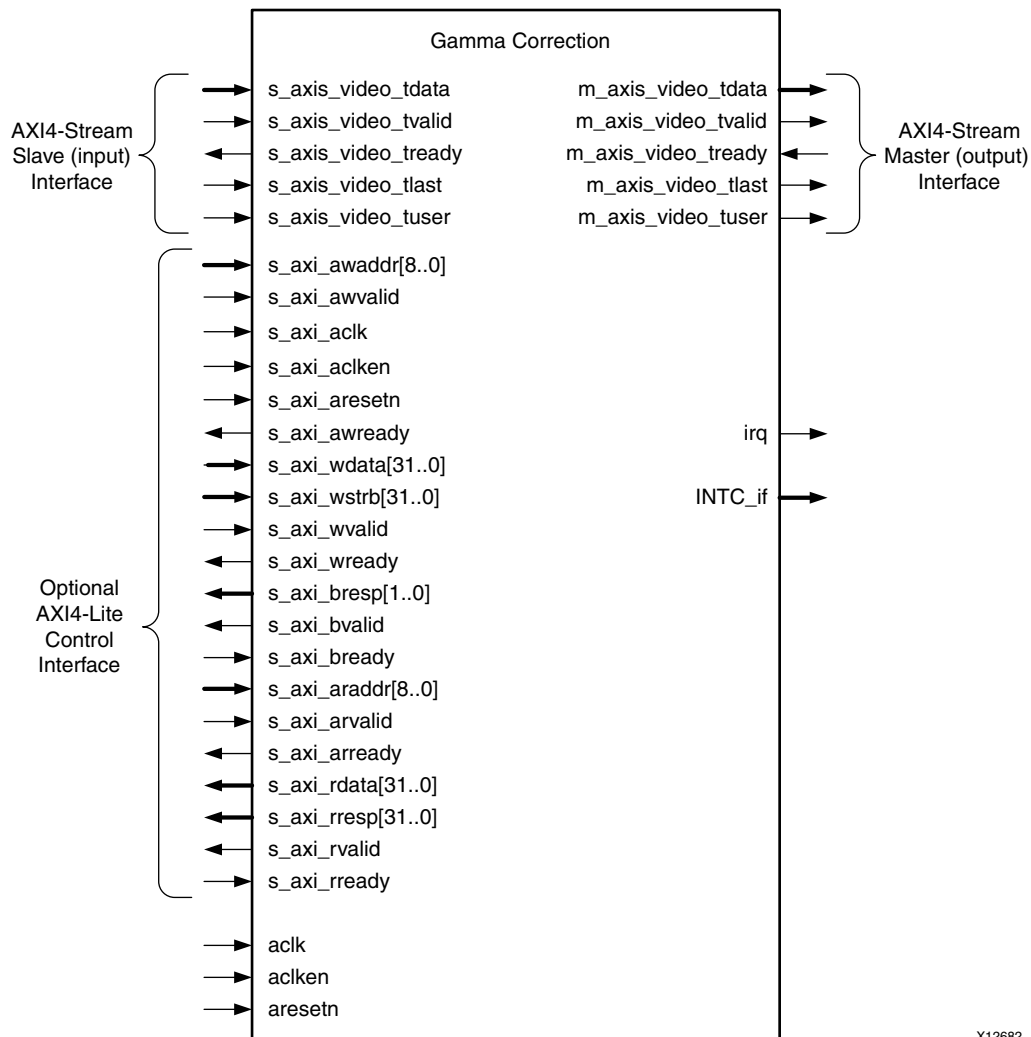


Figure 2-1: Gamma Correction Core Top-Level Signaling Interface

X12682

Common Interface Signals

Table 2-9 summarizes the signals which are either shared by, or not part of the dedicated AXI4-Stream data or AXI4-Lite control interfaces.

Table 2-9: Common Interface Signals

Signal Name	Direction	Width	Description
ACLK	In	1	Video Core Clock
ACLKEN	In	1	Video Core Active High Clock Enable
ARESETn	In	1	Video Core Active Low Synchronous Reset
INTC_IF	Out	9	Optional External Interrupt Controller Interface. Available only when INTC_IF is selected on GUI.
IRQ	Out	1	Optional Interrupt Request Pin. Available only when AXI4-Lite interface is selected on GUI.

The ACLK, ACLKEN and ARESETn signals are shared between the core and the AXI4-Stream data interfaces. The AXI4-Lite control interface has its own set of clock, clock enable and reset pins: S_AXI_ACLK, S_AXI_ACLKEN and S_AXI_ARESETn. Refer to [The Interrupt Subsystem](#) for a description of the INTC_IF and IRQ pins.

ACLK

The AXI4-Stream interface must be synchronous to the core clock signal ACLK. All AXI4-Stream interface input signals are sampled on the rising edge of ACLK. All AXI4-Stream output signal changes occur after the rising edge of ACLK. The AXI4-Lite interface is unaffected by the ACLK signal.

ACLKEN

The ACLKEN pin is an active-high, synchronous clock-enable input pertaining to AXI4-Stream interfaces. Setting ACLKEN low (de-asserted) halts the operation of the core despite rising edges on the ACLK pin. Internal states are maintained, and output signal levels are held until ACLKEN is asserted again. When ACLKEN is de-asserted, core inputs are not sampled, except ARESETn, which supersedes ACLKEN. The AXI4-Lite interface is unaffected by the ACLKEN signal.

ARESETn

The ARESETn pin is an active-low, synchronous reset input pertaining to only AXI4-Stream interfaces. ARESETn supersedes ACLKEN, and when set to 0, the core resets at the next rising edge of ACLK even if ACLKEN is de-asserted. The ARESETn signal must be synchronous to the ACLK and must be held low for a minimum of 32 clock cycles of the slowest clock. The AXI4-Lite interface is unaffected by the ARESETn signal.

Data Interface

The Gamma Correction core receives and transmits data using AXI4-Stream interfaces that implement a video protocol as defined in the *Video IP: AXI Feature Adoption* section of the *AXI Reference Guide* (UG761) [Ref 1].

AXI4-Stream Signal Names and Descriptions

Table 2-10 describes the AXI4-Stream signal names and descriptions.

Table 2-10: AXI4-Stream Data Interface Signal Descriptions

Signal Name	Direction	Width	Description
s_axis_video_tdata	In	8,16,24,32,40	Input Video Data
s_axis_video_tvalid	In	1	Input Video Valid Signal
s_axis_video_tready	Out	1	Input Ready
s_axis_video_tuser	In	1	Input Video Start Of Frame
s_axis_video_tlast	In	1	Input Video End Of Line
m_axis_video_tdata	Out	8,16,24,32,40	Output Video Data
m_axis_video_tvalid	Out	1	Output Valid
m_axis_video_tready	In	1	Output Ready
m_axis_video_tuser	Out	1	Output Video Start Of Frame
m_axis_video_tlast	Out	1	Output Video End Of Line

Video Data

The AXI4-Stream interface specification restricts TDATA widths to integer multiples of 8 bits. Therefore, 10 and 12 bit data must be padded with zeros on the MSB to form N*8-bit wide vector before connecting to s_axis_video_tdata. Padding does not affect the size of the core.

Similarly, RGB data on the Gamma Correction core output m_axis_video_tdata is packed and padded to multiples of 8 bits as necessary, as seen in Figure 2-2. Zero padding the most significant bits is only necessary for 10 and 12 bit wide data.

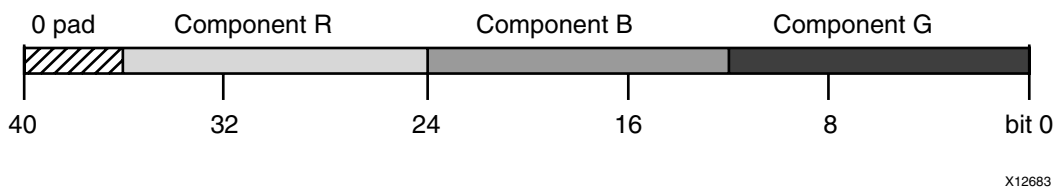


Figure 2-2: RGB Data Encoding on m_axis_video_tdata

READY/VALID Handshake

A valid transfer occurs whenever READY, VALID, ACLKEN, and ARESETn are high at the rising edge of ACLK, as seen in Figure 2-3. During valid transfers, DATA only carries active video data. Blank periods and ancillary data packets are not transferred via the AXI4-Stream video protocol.

Guidelines on Driving s_axis_video_tvalid

Once `s_axis_video_tvalid` is asserted, no interface signals (except the Gamma Correction core driving `s_axis_video_tready`) may change value until the transaction completes (`s_axis_video_tready`, `s_axis_video_tvalid` `ACLKEN` high on the rising edge of `ACLK`). Once asserted, `s_axis_video_tvalid` may only be de-asserted after a transaction has completed. Transactions may not be retracted or aborted. In any cycle following a transaction, `s_axis_video_tvalid` can either be de-asserted or remain asserted to initiate a new transfer.

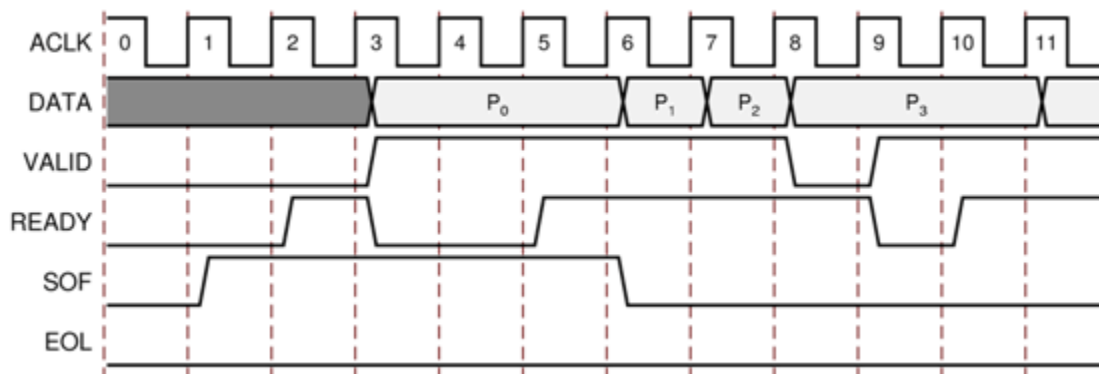


Figure 2-3: Example of READY/VALID Handshake, Start of a New Frame

Guidelines on Driving m_axis_video_tready

The `m_axis_video_tready` signal may be asserted before, during or after the cycle in which the Gamma Correction core asserted `m_axis_video_tvalid`. The assertion of `m_axis_video_tready` may be dependent on the value of `m_axis_video_tvalid`. A slave that can immediately accept data qualified by `m_axis_video_tvalid`, should pre-assert its `m_axis_video_tready` signal until data is received. Alternatively, `m_axis_video_tready` can be registered and driven the cycle following `VALID` assertion.



RECOMMENDED: To minimize latency, the AXI4-Stream slave should drive `READY` independently, or pre-assert `READY`.

Start of Frame Signals - m_axis_video_tuser0, s_axis_video_tuser0

The Start-Of-Frame (SOF) signal, physically transmitted over the AXI4-Stream `TUSER0` signal, marks the first pixel of a video frame. The SOF pulse is 1 valid transaction wide, and must coincide with the first pixel of the frame, as seen in Figure 2-3. SOF serves as a frame synchronization signal, which allows downstream cores to re-initialize, and detect the first pixel of a frame. The SOF signal may be asserted an arbitrary number of `ACLK` cycles before the first pixel value is presented on `DATA`, as long as a `VALID` is not asserted.

End of Line Signals - `m_axis_video_tlast`, `s_axis_video_tlast`

The End-Of-Line signal, physically transmitted over the AXI4-Stream TLAST signal, marks the last pixel of a line. The EOL pulse is 1 valid transaction wide, and must coincide with the last pixel of a scan-line, as seen in Figure 2-4.

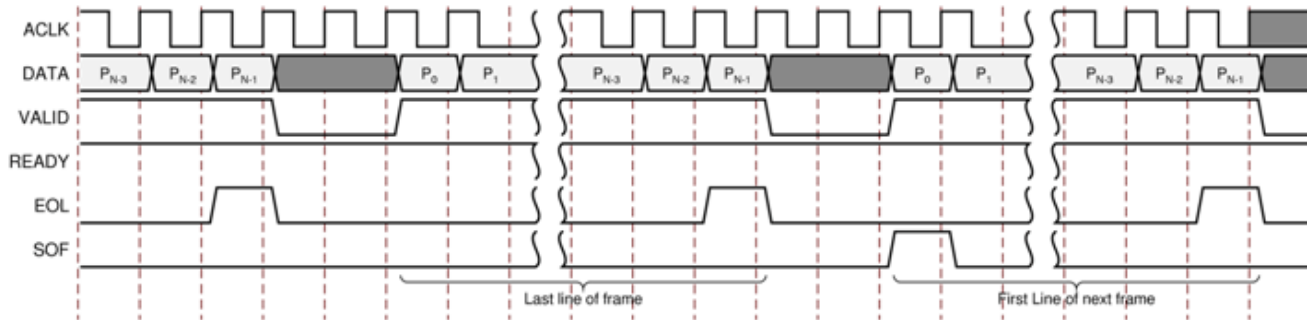


Figure 2-4: Use of EOL and SOF Signals

Control Interface

When configuring the core, you can add an AXI4-Lite register interface to dynamically control the behavior of the core. The AXI4-Lite slave interface facilitates integrating the core into a processor system, or along with other video or AXI4-Lite compliant IP, connected via AXI4-Lite interface to an AXI4-Lite master. In a static configuration with a fixed set of parameters (constant configuration), the core is instantiated without the AXI4-Lite control interface, which reduces the core Slice footprint.

Constant Configuration

The constant configuration caters to designs that use the core in one setup that will not need to change over time. In constant configuration the image resolution (number of active pixels per scan line and the number of active scan lines per frame) and the Gamma Correction Look-Up-Tables (LUTs) are hard coded into the core via the Gamma Correction core GUI. Since there is no AXI4-Lite interface, the core is not programmable, but can be reset, enabled, or disabled using the `ARESETn` and `ACLKEN` ports.

AXI4-Lite Interface

The AXI4-Lite interface allows you to dynamically control parameters within the core. Core configuration can be accomplished using an AXI4-Stream master state machine, or an embedded ARM or soft system processor such as MicroBlaze.

The Gamma Correction core can be controlled via the AXI4-Lite interface using read and write transactions to the Gamma register space.

Table 2-11: AXI4-Lite Interface Signals

Signal Name	Direction	Width	Description
s_axi_aclk	In	1	AXI4-Lite clock
s_axi_aclken	In	1	AXI4-Lite clock enable
s_axi_aresetn	In	1	AXI4-Lite synchronous Active Low reset
s_axi_awvalid	In	1	AXI4-Lite Write Address Channel Write Address Valid.
s_axi_awread	Out	1	AXI4-Lite Write Address Channel Write Address Ready. Indicates DMA ready to accept the write address.
s_axi_awaddr	In	32	AXI4-Lite Write Address Bus
s_axi_wvalid	In	1	AXI4-Lite Write Data Channel Write Data Valid.
s_axi_wready	Out	1	AXI4-Lite Write Data Channel Write Data Ready. Indicates DMA is ready to accept the write data.
s_axi_wdata	In	32	AXI4-Lite Write Data Bus
s_axi_bresp	Out	2	AXI4-Lite Write Response Channel. Indicates results of the write transfer.
s_axi_bvalid	Out	1	AXI4-Lite Write Response Channel Response Valid. Indicates response is valid.
s_axi_bready	In	1	AXI4-Lite Write Response Channel Ready. Indicates target is ready to receive response.
s_axi_arvalid	In	1	AXI4-Lite Read Address Channel Read Address Valid
s_axi_arready	Out	1	Ready. Indicates DMA is ready to accept the read address.
s_axi_araddr	In	32	AXI4-Lite Read Address Bus
s_axi_rvalid	Out	1	AXI4-Lite Read Data Channel Read Data Valid
s_axi_rready	In	1	AXI4-Lite Read Data Channel Read Data Ready. Indicates target is ready to accept the read data.
s_axi_rdata	Out	32	AXI4-Lite Read Data Bus
s_axi_rresp	Out	2	AXI4-Lite Read Response Channel Response. Indicates results of the read transfer.

S_AXI_ACLK

The AXI4-Lite interface must be synchronous to the S_AXI_ACLK clock signal. The AXI4-Lite interface input signals are sampled on the rising edge of ACLK. The AXI4-Lite output signal changes occur after the rising edge of ACLK. The AXI4-Stream interfaces signals are not affected by the S_AXI_ACLK.

S_AXI_ACLKEN

The S_AXI_ACLKEN pin is an active-high, synchronous clock-enable input for the AXI4-Lite interface. Setting S_AXI_ACLKEN low (de-asserted) halts the operation of the AXI4-Lite interface despite rising edges on the S_AXI_ACLK pin. AXI4-Lite interface states are

maintained, and AXI4-Lite interface output signal levels are held until `S_AXI_ACLKEN` is asserted again. When `S_AXI_ACLKEN` is de-asserted, AXI4-Lite interface inputs are not sampled, except `S_AXI_ARESETn`, which supersedes `S_AXI_ACLKEN`. The AXI4-Stream interfaces signals are not affected by the `S_AXI_ACLKEN`.

S_AXI_ARESETn

The `S_AXI_ARESETn` pin is an active-low, synchronous reset input for the AXI4-Lite interface. `S_AXI_ARESETn` supersedes `S_AXI_ACLKEN`, and when set to 0, the core resets at the next rising edge of `S_AXI_ACLK` even if `S_AXI_ACLKEN` is de-asserted. The `S_AXI_ARESETn` signal must be synchronous to the `S_AXI_ACLK` and must be held low for a minimum of 32 clock cycles of the slowest clock. The `S_AXI_ARESETn` input is resynchronized to the `ACLK` clock domain. The AXI4-Stream interfaces and core signals are also reset by `S_AXI_ARESETn`.

Register Space

The standardized Xilinx Video IP register space is partitioned to control-, timing-, and core specific registers. The Gamma Correction core uses only one timing related register, `ACTIVE_SIZE` (0x0020), which allows specifying the input frame dimensions. The core has two core specific registers, the `Gamma_Addr_Data` (0x0104) which is used to reprogram the Gamma Look-Up-Tables and the `Gamma_Table_Update` (0x0100) which is used to tell the Gamma Correction core when to move to a new LUT.

Table 2-12: Register Names and Descriptions

Address (hex) BASEADDR +	Register Name	Access Type	Double Buffered	Default Value	Register Description
0x0000	CONTROL	R/W	N	Power-on-Reset : 0x0	Bit 0: SW_ENABLE Bit 1: REG_UPDATE Bit 4: BYPASS ⁽¹⁾ Bit 5: TEST_PATTERN ⁽¹⁾ Bit 30: FRAME_SYNC_RESET (1: reset) Bit 31: SW_RESET (1: reset)
0x0004	STATUS	R/W	No	0	Bit 0: PROC_STARTED Bit 1: EOF Bit 16: SLAVE_ERROR
0x0008	ERROR	R/W	No	0	Bit 0: SLAVE_EOL_EARLY Bit 1: SLAVE_EOL_LATE Bit 2: SLAVE_SOF_EARLY Bit 3: SLAVE_SOF_LATE
0x000C	IRQ_ENABLE	R/W	No	0	16-0: Interrupt enable bits corresponding to STATUS bits

Table 2-12: Register Names and Descriptions

Address (hex) BASEADDR +	Register Name	Access Type	Double Buffered	Default Value	Register Description
0x0010	VERSION	R	N/A	0x0601a000	7-0: REVISION_NUMBER 11-8: PATCH_ID 15-12: VERSION_REVISION 23-16: VERSION_MINOR 31-24: VERSION_MAJOR
0x0014	SYSDEBUG0	R	N/A	0	0-31: Frame Throughput monitor ⁽¹⁾
0x0018	SYSDEBUG1	R	N/A	0	0-31: Line Throughput monitor ⁽¹⁾
0x001C	SYSDEBUG2	R	N/A	0	0-31: Pixel Throughput monitor ⁽¹⁾
0x0020	ACTIVE_SIZE	R/W	Yes	Specified via GUI	12-0: Number of Active Pixels per Scanline 28-16: Number of Active Lines per Frame
0x0100	Gamma_Table_Update	R/W	Yes	0	Denotes when the core should swap to the inactive LUT.
0x0104	Gamma_Addr_Data	R/W	No	0	[31-16]: Target address in gamma LUT [15-0]: Value to write to gamma LUT

1. Only available when the debugging features option is enabled in the GUI at the time the core is instantiated.

CONTROL (0x0000) Register

Bit 0 of the CONTROL register, SW_ENABLE, facilitates enabling and disabling the core from software. Writing '0' to this bit effectively disables the core halting further operations, which blocks the propagation of all video signals. After Power up, or Global Reset, the SW_ENABLE defaults to 0 for the AXI4-Lite interface. Similar to the ACLKEN pin, the SW_ENABLE flag is not synchronized with the AXI4-Stream interfaces: Enabling or Disabling the core takes effect immediately, irrespective of the core processing status. Disabling the core for extended periods may lead to image tearing.

Bit 1 of the CONTROL register, REG_UPDATE is a write done semaphore for the host processor, which facilitates committing all user and timing register updates simultaneously. The Gamma Correction core ACTIVE_SIZE and BAYER_PHASE registers are double buffered. One set of registers (the processor registers) is directly accessed by the processor interface, while the other set (the active set) is actively used by the core. New values written to the processor registers will get copied over to the active set at the end of the AXI4-Stream frame, if and only if REG_UPDATE is set. Setting REG_UPDATE to 0 before updating multiple register values, then setting REG_UPDATE to 1 when updates are completed ensures all registers are updated simultaneously at the frame boundary without causing image tearing.

Bit 4 of the `CONTROL` register, `BYPASS`, switches the core to bypass mode if debug features are enabled. In bypass mode the Gamma Correction core processing function is bypassed, and the core repeats AXI4-Stream input samples on its output. Refer to [Debugging Features in Appendix C](#) for more information. If debug features were not included at instantiation, this flag has no effect on the operation of the core. Switching bypass mode on or off is not synchronized to frame processing, therefore can lead to image tearing.

Bit 5 of the `CONTROL` register, `TEST_PATTERN`, switches the core to test-pattern generator mode if debug features are enabled. Refer to [Debugging Features in Appendix C](#) for more information. If debug features were not included at instantiation, this flag has no effect on the operation of the core. Switching test-pattern generator mode on or off is not synchronized to frame processing, therefore can lead to image tearing.

Bits 30 and 31 of the `CONTROL` register, `FRAME_SYNC_RESET` and `SW_RESET` facilitate software reset. Setting `SW_RESET` reinitializes the core to GUI default values, all internal registers and outputs are cleared and held at initial values until `SW_RESET` is set to 0. The `SW_RESET` flag is not synchronized with the AXI4-Stream interfaces. Resetting the core while frame processing is in progress will cause image tearing. For applications where the soft-ware reset functionality is desirable, but image tearing has to be avoided a frame synchronized software reset (`FRAME_SYNC_RESET`) is available. Setting `FRAME_SYNC_RESET` to 1 will reset the core at the end of the frame being processed, or immediately if the core is between frames when the `FRAME_SYNC_RESET` was asserted. After reset, the `FRAME_SYNC_RESET` bit is automatically cleared, so the core can get ready to process the next frame of video as soon as possible. The default value of both `RESET` bits is 0. Core instances with no AXI4-Lite control interface can only be reset via the `ARESETn` pin.

STATUS (0x0004) Register

All bits of the `STATUS` register can be used to request an interrupt from the host processor. To facilitate identification of the interrupt source, bits of the `STATUS` register remain set after an event associated with the particular `STATUS` register bit, even if the event condition is not present at the time the interrupt is serviced.

Bits of the `STATUS` register can be cleared individually by writing '1' to the bit position.

Bit 0 of the `STATUS` register, `PROC_STARTED`, indicates that processing of a frame has commenced via the AXI4-Stream interface.

Bit 1 of the `STATUS` register, End-of-frame (EOF), indicates that the processing of a frame has completed.

Bit 16 of the `STATUS` register, `SLAVE_ERROR`, indicates that one of the conditions monitored by the `ERROR` register has occurred.

ERROR (0x0008) Register

Bit 16 of the `STATUS` register, `SLAVE_ERROR`, indicates that one of the conditions monitored by the `ERROR` register has occurred. This bit can be used to request an interrupt from the host processor. To facilitate identification of the interrupt source, bits of the `STATUS` and `ERROR` registers remain set after an event associated with the particular `ERROR` register bit, even if the event condition is not present at the time the interrupt is serviced.

Bits of the `ERROR` register can be cleared individually by writing '1' to the bit position to be cleared.

Bit 0 of the `ERROR` register, `EOL_EARLY`, indicates an error during processing a video frame via the AXI4-Stream slave port. The number of pixels received between the latest and the preceding End-Of-Line (`EOL`) signal was less than the value programmed into the `ACTIVE_SIZE` register.

Bit 1 of the `ERROR` register, `EOL_LATE`, indicates an error during processing a video frame via the AXI4-Stream slave port. The number of pixels received between the last `EOL` signal surpassed the value programmed into the `ACTIVE_SIZE` register.

Bit 2 of the `ERROR` register, `SOF_EARLY`, indicates an error during processing a video frame via the AXI4-Stream slave port. The number of pixels received between the latest and the preceding Start-Of-Frame (`SOF`) signal was less than the value programmed into the `ACTIVE_SIZE` register.

Bit 3 of the `ERROR` register, `SOF_LATE`, indicates an error during processing a video frame via the AXI4-Stream slave port. The number of pixels received between the last `SOF` signal surpassed the value programmed into the `ACTIVE_SIZE` register.

IRQ_ENABLE (0x000C) Register

Any bits of the `STATUS` register can generate a host-processor interrupt request via the `IRQ` pin. The Interrupt Enable register facilitates selecting which bits of `STATUS` register will assert `IRQ`. Bits of the `STATUS` registers are masked by (AND) corresponding bits of the `IRQ_ENABLE` register and the resulting terms are combined (OR) together to generate `IRQ`.

Version (0x0010) Register

Bit fields of the Version Register facilitate software identification of the exact version of the hardware peripheral incorporated into a system. The core driver can take advantage of this Read-Only value to verify that the software is matched to the correct version of the hardware. See [Table 2-12](#) for details.

SYSDEBUG0 (0x0014) Register

The `SYSDEBUG0`, or Frame Throughput Monitor, register indicates the number of frames processed since power-up or the last time the core was reset. The `SYSDEBUG` registers can

be useful to identify external memory / Frame buffer / or throughput bottlenecks in a video system. Refer to [Debugging Features in Appendix C](#) for more information.

SYSDEBUG1 (0x0018) Register

The `SYSDEBUG1`, or Line Throughput Monitor, register indicates the number of lines processed since power-up or the last time the core was reset. The `SYSDEBUG` registers can be useful to identify external memory / Frame buffer / or throughput bottlenecks in a video system. Refer to [Debugging Features in Appendix C](#) for more information.

SYSDEBUG2 (0x001C) Register

The `SYSDEBUG2`, or Pixel Throughput Monitor, register indicates the number of pixels processed since power-up or the last time the core was reset. The `SYSDEBUG` registers can be useful to identify external memory / Frame buffer / or throughput bottlenecks in a video system. Refer to [Debugging Features in Appendix C](#) for more information.

ACTIVE_SIZE (0x0020) Register

The `ACTIVE_SIZE` register encodes the number of active pixels per scan line and the number of active scan lines per frame. The lower half-word (bits 12:0) encodes the number of active pixels per scan line. Supported values are between 32 and the value provided in the **Maximum number of pixels per scan line** field in the GUI. The upper half-word (bits 28:16) encodes the number of active lines per frame. Supported values are 32 to 7680. To avoid processing errors, the user should restrict values written to `ACTIVE_SIZE` to the range supported by the core instance.

Gamma_Table_Update (0x0100)

The `Gamma_Table_Update` register is used when the Gamma Correction core is configured to use Double Buffered Look-Up-Tables. When configured to use double buffered Look-Up-Tables, the Gamma Correction core uses two banks of memory for Look-Up-Table. One bank is active and process valid data. The other bank is inactive and can be programmed with new values by way of the AXI4-Lite interface. Once the inactive bank has been fully programmed, the Gamma Correction core can be signaled to swap banks by setting bit 0 of the `Gamma_Table Update` register to 1.

Gamma_Addr_Data (0x0104)

The Gamma Look-Up-Tables can be reprogrammed dynamically through the AXI4-Lite interface. A new value is written to the Look-Up-Table by writing the address of the Look-Up-Table location and the new data value to the `Gamma_Addr_Data` register.

Updating the Gamma Tables Using the AXI4-Lite Interface

The double- and single-buffered interfaces require that each write operation contain a valid address and data. Bits [31-16] of the Gamma_Addr_Data register are designated as the look-up table address, while bits [15-0] represent the value of word to be written into the gamma look-up table(s). The valid address range for the data depends on the input width, number of shared look-up tables, and whether interpolation is used, as shown in [Table 2-13](#) and [Table 2-14](#).

Table 2-13: Valid Address Ranges for Look-up Tables for RGB Data

Input Width	Look-up Tables ⁽¹⁾	Interpolation	Red Baseaddr, Range	Green Baseaddr, Range	Blue Baseaddr, Range
8	3	0	0x0000, 0x00FF	0x0100, 0x01FF	0x0200, 0x02FF
8	2	0	0x0000, 0x00FF	0x0100, 0x01FF	N/A
8	1	0	0x0000, 0x00FF	N/A	N/A
10	3	0	0x0000, 0x03FF	0x0400, 0x07FF	0x0800, 0x0BFF
10	2	0	0x0000, 0x03FF	0x0400, 0x07FF	N/A
10	1	0	0x0000, 0x03FF	N/A	N/A
12	3	0	0x0000, 0x0FFF	0x1000, 0x1FFF	0x2000, 0x2FFF
12	2	0	0x0000, 0x0FFF	0x1000, 0x1FFF	N/A
12	1	0	0x0000, 0x0FFF	N/A	N/A
12	3	1	0x0000, 0x03FF	0x0400	0x0800, 0x0BFF
12	2	1	0x0000, 0x03FF	0x0400	N/A
12	1	1	0x0000, 0x03FF	N/A	N/A

- The number of lookup tables used is as follows:
 - 3: when Independent look-up tables for each Color Channel is selected
 - 2: when Identical look-up tables for Chrominance Channels Only is selected
 - 1: when Identical look-up tables for all Color Channels is selected

Table 2-14: Valid Address Ranges for Look-up Tables for YCrCb 4:4:4/4:2:2/4:2:0 or Mono Data

Input Width	Look-up Tables ⁽¹⁾	Interpolation	Y/Mono Baseaddr, Range	Cb or (Cb/Cr) Baseaddr, Range	Cr Baseaddr, Range
8	3	0	0x0000, 0x00FF	0x0100, 0x01FF	0x0200, 0x02FF
8	2	0	0x0000, 0x00FF	0x0100, 0x01FF	N/A
8	1	0	0x0000, 0x00FF	N/A	N/A
10	3	0	0x0000, 0x03FF	0x0400, 0x07FF	0x0800, 0x0BFF
10	2	0	0x0000, 0x03FF	0x0400, 0x07FF	N/A
10	1	0	0x0000, 0x03FF	N/A	N/A
12	3	0	0x0000, 0x0FFF	0x1000, 0x1FFF	0x2000, 0x2FFF
12	2	0	0x0000, 0x0FFF	0x1000, 0x1FFF	N/A
12	1	0	0x0000, 0x0FFF	N/A	N/A

Table 2-14: Valid Address Ranges for Look-up Tables for YCrCb 4:4:4/4:2:2/4:2:0 or Mono Data (Cont'd)

Input Width	Look-up Tables ⁽¹⁾	Interpolation	Y/Mono Baseaddr, Range	Cb or (Cb/Cr) Baseaddr, Range	Cr Baseaddr, Range
12	3	1	0x0000, 0x03FF	0x0400	0x0800, 0x0BFF
12	2	1	0x0000, 0x03FF	0x0400	N/A
12	1	1	0x0000, 0x03FF	N/A	N/A

1. The number of lookup tables used is as follows:
 - 3: when Independent look-up tables for each Color Channel is selected
 - 2: when Identical look-up tables for Chrominance Channels Only is selected
 - 1: when Identical look-up tables for all Color Channels is selected

The Interrupt Subsystem

STATUS register bits can trigger interrupts so embedded application developers can quickly identify faulty interfaces or incorrectly parameterized cores in a video system. Irrespective of whether the AXI4-Lite control interface is present or not, the Gamma Correction core detects AXI4-Stream framing errors, as well as the beginning and the end of frame processing.

When the core is instantiated with an AXI4-Lite Control interface, the optional interrupt request pin (IRQ) is present. Events associated with bits of the STATUS register can generate a (level triggered) interrupt, if the corresponding bits of the interrupt enable register (IRQ_ENABLE) are set. Once set by the corresponding event, bits of the STATUS register stay set until the user application clears them by writing '1' to the desired bit positions. Using this mechanism the system processor can identify and clear the interrupt source.

Without the AXI4-Lite interface the user can still benefit from the core signaling error and status events. By selecting the **Enable INTC Port** check-box on the GUI, the core generates the optional INTC_IF port. This vector of signals gives parallel access to the individual interrupt sources, as seen in Table 2-15.

Unlike STATUS and ERROR flags, INTC_IF signals are not held, rather stay asserted only while the corresponding event persists.

Table 2-15: INTC_IF Signal Functions

INTC_IF signal	Function
0	Frame processing start
1	Frame processing complete
2	Reserved
3	Reserved
4	Slave_Error
5	EOL Early
6	EOL Late

Table 2-15: INTC_IF Signal Functions (Cont'd)

INTC_IF signal	Function
7	SOF Early
8	SOF Late

In a system integration tool, such as EDK, the interrupt controller INTC IP can be used to register the selected `INTC_IF` signals as edge triggered interrupt sources. The INTC IP provides functionality to mask (enable or disable), as well as identify individual interrupt sources from software. Alternatively, for an external processor or MCU the user can custom build a priority interrupt controller to aggregate interrupt requests and identify interrupt sources.

Designing with the Core

General Design Guidelines

The Gamma Correction core uses a Look-up Table (LUT) programmed with a Gamma Correction Curve or user-defined function to convert input data to output data. The core processes samples provided via an AXI4-Stream slave interface, outputs pixels via an AXI4-Stream master interface, and can be controlled via an optional AXI4-Lite interface. The Gamma block cannot change the input/output image sizes, the input and output pixel clock rates, or the frame rate. It is recommended that the Gamma Correction core is used in conjunction with the Video In to AXI4-Stream and Video Timing Controller cores. The Video Timing Controller core measures the timing parameters, such as number of active scan lines, number of active pixels per scan line of the image sensor. The Video In to AXI4-Stream core converts a clocked parallel video interface with sync and or blank signals to AXI4-Stream.

Typically, the Gamma Correction core is part of a larger video processing system such as the Image Sensor Pipeline (ISP) System shown in [Figure 3-1](#).

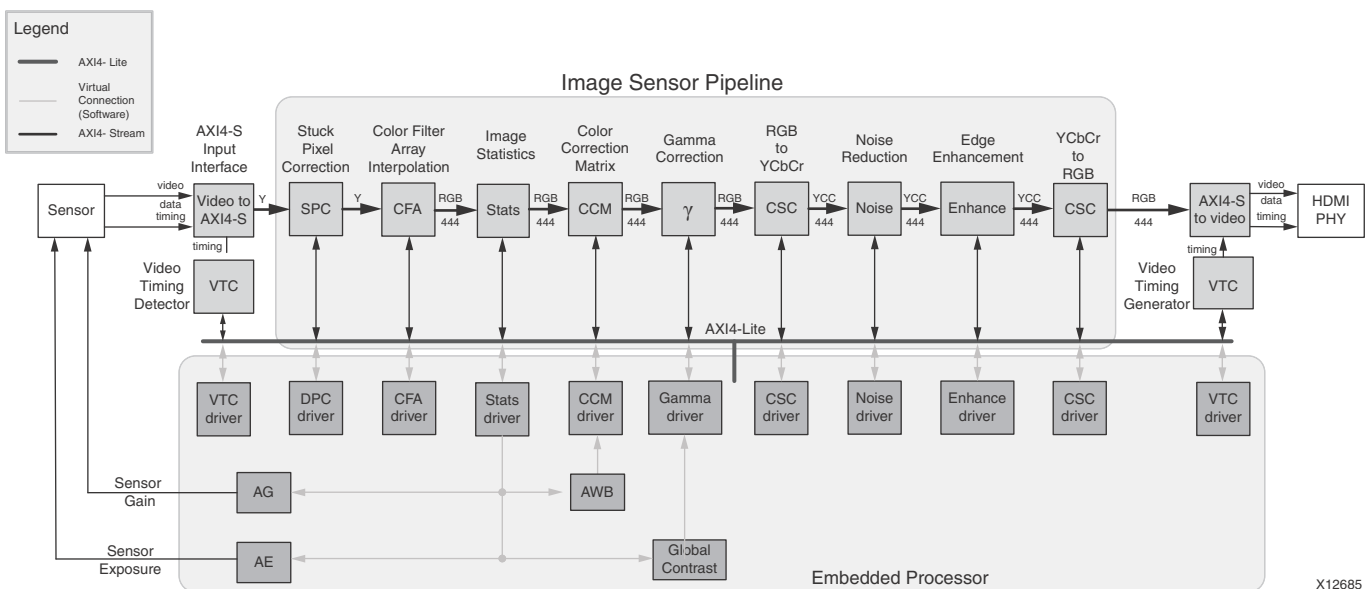


Figure 3-1: Image Sensor Pipeline System with Gamma Correction Core

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The Gamma Correction core allows you to select an input data width that is different than the output data width. The core is implemented as a set of Look-Up-Tables that are used to perform the data transformation. The width of the input data determines the number of entries in the Look-Up-Table. For example, 8-bit input data would require 2^8 (256) entries in the Look-Up-Table. The width of the output data determines the width of each entry in the Look-Up-Table. For example, 12-bit output data would require that each entry in the table be 12-bits wide. When the **Calculate Gamma Value** option is used when generating the core, the tables are properly sized and scaled to match the selected input and output data widths. When the **Load Initialization File** option is used, the tables are properly sized to match the input data width, but the user is responsible for properly scaling the data. The user is also responsible for properly scaling the data when new values are loaded into the core using the AXI4-Lite processor interface.

Clock, Enable, and Reset Considerations

ACLK

The master and slave AXI4-Stream video interfaces use the `ACLK` clock signal as their shared clock reference, as shown in Figure 3-2.

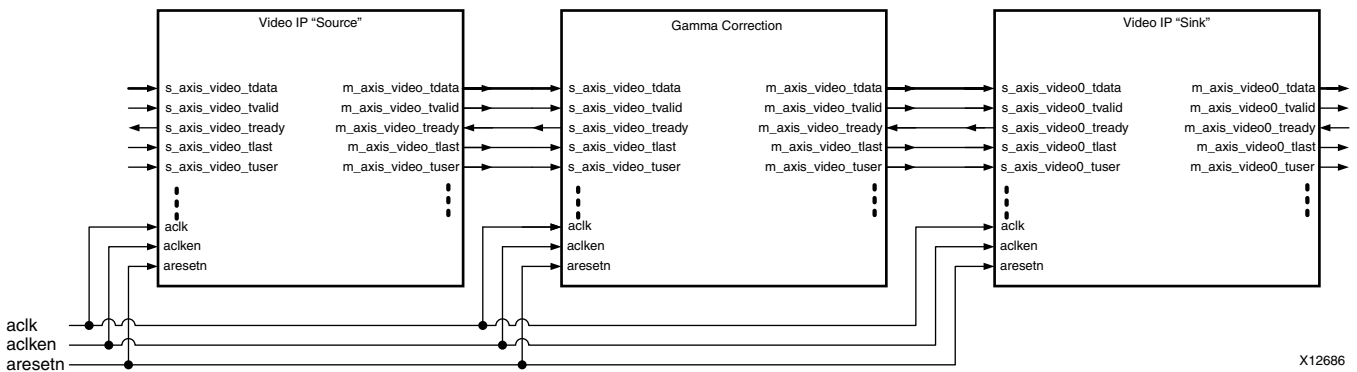


Figure 3-2: Example of ACLK Routing in an ISP Processing Pipeline

S_AXI_ACLK

The AXI4-Lite interface uses the `A_AXI_ACLK` pin as its clock source. The `ACLK` pin is not shared between the AXI4-Lite and AXI4-Stream interfaces. The Gamma core contains clock-domain crossing logic between the `ACLK` (AXI4-Stream and Video Processing) and `S_AXI_ACLK` (AXI4-Lite) clock domains. The core automatically ensures that the AXI4-Lite transactions will complete even if the video processing is stalled with `ARESETn`, `ACLKEN` or with the video clock not running.

ACLKEN

The Gamma Correction core has two enable options: the `ACLKEN` pin (hardware clock enable), and the software reset option provided via the AXI4-Lite control interface (when present).

`ACLKEN` is by no means synchronized internally to AXI4-Stream frame processing therefore de-asserting `ACLKEN` for extended periods of time may lead to image tearing.

The `ACLKEN` pin facilitates:

- Multi-cycle path designs (high speed clock division without clock gating),
- Standby operation of subsystems to save on power
- Hardware controlled bring-up of system components



IMPORTANT: When `ACLKEN` (clock enable) pins are used (toggled) in conjunction with a common clock source driving the master and slave sides of an AXI4-Stream interface, the `ACLKEN` pins associated with the master and slave component interfaces must also be driven by the same signal to prevent transaction errors (Figure 2-2).



IMPORTANT: When two cores connected via AXI4-Stream interfaces, where only the master or the slave interface has an `ACLKEN` port, which is not permanently tied high, the two interfaces should be connected via the AXI4-Stream Interconnect or AXI-FIFO cores to avoid data corruption (Figure 2-3).

S_AXI_ACLKEN

The `S_AXI_ACLKEN` is the clock enable signal for the AXI4-Lite interface only. Driving this signal low will only affect the AXI4-Lite interface and will not halt the video processing in the `ACLK` clock domain.

ARESETn

The Gamma Correction core has two reset source: the `ARESETn` pin (hardware reset), and the software reset option provided via the AXI4-Lite control interface (when present).



IMPORTANT: `ARESETn` is not synchronized internally to AXI4-Stream frame processing, therefore de-asserting `ARESETn` while a frame is being process will lead to image tearing.

The external reset pulse needs to be held for 32 `ACLK` cycles to reset the core. The `ARESETn` signal will only reset the AXI4-Stream interfaces. The AXI4-Lite interface is unaffected by the `ARESETn` signal to allow the video processing core to be reset without halting the AXI4-Lite interface.



IMPORTANT: *When resetting a system with multiple clocks and corresponding reset signals, the reset generator must ensure that all reset signals are asserted or de-asserted have enough time that all interfaces and clock-domains in all IP cores are correctly reinitialized.*

S_AXI_ARESETn

The S_AXI_ARESETn signal is synchronous to the S_AXI_ACLK clock domain, but is internally synchronized to the ACLK clock domain. The S_AXI_ARESETn signal will reset the entire core including the AXI4-Lite and AXI4-Stream interfaces.

System Considerations

When using the Gamma Correction core, it needs to be configured for the actual image sensor frame-size to operate properly. To gather the frame size information from the input video, it can be connected to the Video In to AXI4-Stream input and the Video Timing Controller cores. The timing detector logic in the Video Timing Controller will gather the video timing signals. The AXI4-Lite control interface on the Video Timing Controller allows the system processor to read out the measured frame dimensions, and program all downstream cores, such as the Gamma, with the appropriate image dimensions.

If the target system uses only one unchanging setup of the Gamma registers, the user may choose to create a constant configuration by removing the AXI4-Lite interface. This option allows reducing the core Slice footprint.

Clock Domain Interaction

The ARESETn and ACLKEN input signals will not reset or halt the AXI4-Lite interface. This allows the video processing to be reset or halted separately from the AXI4-Lite interface without disrupting AXI4-Lite transactions.

The AXI4-Lite interface will respond with an error if the core registers cannot be read or written within 128 S_AXI_ACLK clock cycles. The core registers cannot be read or written if the ARESETn signal is held low, if the ACLKEN signal is held low or if the ACLK signal is not connected or not running. If core register read does not complete, the AXI4-Lite read transaction will respond with **10** on the S_AXI_RRESP bus. Similarly, if a core register write does not complete, the AXI4-Lite write transaction will respond with **10** on the S_AXI_BRESP bus. The S_AXI_ARESETn input signal resets the entire core.

Programming Sequence

If processing parameters such as the image size needs to be changed on the fly, or the system needs to be reinitialized, it is recommended that pipelined Xilinx IP video cores are disabled/reset from system output towards the system input, and programmed/enabled

from system input to system output. *STATUS* register bits allow system processors to identify the processing states of individual constituent cores, and successively disable a pipeline as one core after another is finished processing the last frame of data.

Error Propagation and Recovery

Parameterization and/or configuration registers define the dimensions of video frames video IP should process. Starting from a known state, based on these configuration settings the IP can predict when the beginning of the next frame is expected. Similarly, the IP can predict when the last pixel of each scan line is expected. SOF detected before it was expected (early), or SOF not present when it is expected (late), EOL detected before expected (early), or EOL not present when expected (late), signals error conditions indicative of either upstream communication errors or incorrect core configuration.

When SOF is detected early, the output SOF signal is generated early, terminating the previous frame immediately. When SOF is detected late, the output SOF signal is generated according to the programmed values. Extra lines / pixels from the previous frame are dropped until the input SOF is captured.

Similarly, when EOL is detected early, the output EOL signal is generated early, terminating the previous line immediately. When EOL is detected late, the output EOL signal is generated according to the programmed values. Extra pixels from the previous line are dropped until the input EOL is captured.

Shared Look-Up Tables

When multiple channels require the same correction curve, a single look-up table may be shared between two or more channels. Sharing look-up tables between multiple channels reduces the number of write operations required to update the look-up tables when using the AXI4-Lite interface. It also can reduce the number of Block RAM resources used.

Interpolation of Look-up Table Contents

When the gamma function is configured for 12-bit input data, an optional look-up table interpolation is provided to reduce the size of look-up tables and thereby the number of block RAMs. This interpolation stores every 4th sample in the look-up table (Figure 3-3), which can reduce the number of block RAMs used by 75%. The Gamma Correction core supports linear interpolation, which trades off block RAM(s) for adders to implement the 1-to-4 interpolation. When used to interpolate sufficiently smooth functions, such as the power functions used for gamma correction, the interpolation error is orders of magnitude smaller than the output quantization error.

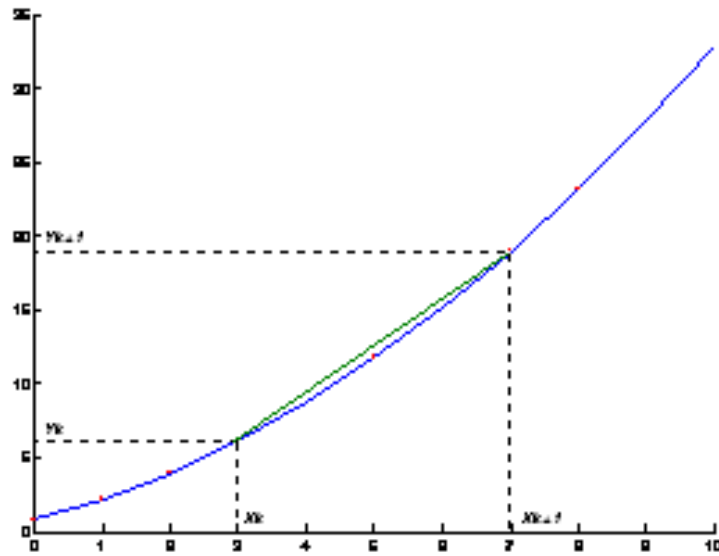


Figure 3-3: Interpolation of Look-up Table Contents

C Model Reference

Installation and Directory Structure

This chapter contains information for installing the Gamma Correction C Model, and describes the file contents and directory structure.

Software Requirements

The Gamma Correction v6.01.a C models were compiled and tested with the following software versions.

Table 4-1: Supported Systems and Software Requirements

Platform	C Compiler
Linux 32-bit and 64-bit	GCC 4.1.1
Windows 32-bit and 64-bit	Microsoft Visual Studio 2005, Visual Studio 2008 (Visual C++ 8.0)

Installation

The installation of the C Model requires updates to the PATH variable, as described below.

Linux

Ensure that the directory in which the `libIp_v_gamma_v6_01_a_bitacc_cmodel.so` and `libstlport.so.5.1` files are located is in your `$LD_LIBRARY_PATH` environment variable.

C Model File Contents

Unzipping the `v_gamma_v6_01_a_bitacc_model.zip` file creates the following directory structures and files which are described in [Table 4-2](#).

Table 4-2: C Model Files

File	Description
/lin	Pre-compiled bit accurate ANSI C reference model for simulation on 32-bit Linux Platforms
libIp_v_gamma_v6_01_a_bitacc_cmodel.lib	Gamma Correction v6.01.a model shared object library (Linux platforms only)
libstlport.so.5.1	STL library, referenced by the Gamma Correction library (Linux platforms only)
run_bitacc_cmodel	Pre-compiled bit accurate executable for simulation on 32-bit Linux Platforms
/lin64	Pre-compiled bit accurate ANSI C reference model for simulation on 64-bit Linux Platforms
libIp_v_gamma_v6_01_a_bitacc_cmodel.lib	Gamma Correction v6.01.a model shared object library (Linux platforms only)
libstlport.so.5.1	STL library, referenced by the Gamma Correction library (Linux platforms only)
run_bitacc_cmodel	Pre-compiled bit accurate executable for simulation on 32-bit Linux Platforms
/nt	Pre-compiled bit accurate ANSI C reference model for simulation on 32-bit Windows Platforms
libIp_v_gamma_v6_01_a_bitacc_cmodel.lib	Pre-compiled library file for win32 compilation
run_bitacc_cmodel.exe	Pre-compiled bit accurate executable for simulation on 32-bit Windows Platforms
/nt64	Pre-compiled bit accurate ANSI C reference model for simulation on 64-bit Windows Platforms
libIp_v_gamma_v6_01_a_bitacc_cmodel.lib	Pre-compiled library file for win32 compilation
run_bitacc_cmodel.exe	Pre-compiled bit accurate executable for simulation on 64-bit Windows Platforms
README.txt	Release notes
pg004_v_gamma.pdf	<i>Gamma Correction Core Product Guide</i>
v_gamma_v6_01_a_bitacc_cmodel.h	Model header file
rgb_utils.h	Header file declaring the RGB image / video container type and support functions
bmp_utils.h	Header file declaring the bitmap (.bmp) image file I/O functions

Table 4-2: C Model Files (Cont'd)

File	Description
video_utils.h	Header file declaring the generalized image / video container type, I/O and support functions.
Kodim19_128x192.bmp	128x192 sample test image of the Lighthouse image from the True-color Kodak test images
run_bittacc_cmodel.c	Example code calling the C Model

Using the C Model

The bit accurate C model is accessed through a set of functions and data structures that are declared in the `v_gamma_v6_01_a_bitacc_cmodel.h` file.

Before using the model, the structures holding the inputs, generics and output of the Gamma Correction instance must be defined:

```

struct xilinx_ip_v_gamma_v6_01_a_generics gamma_generics;
struct xilinx_ip_v_gamma_v6_01_a_inputs gamma_inputs;
struct xilinx_ip_v_gamma_v6_01_a_outputs gamma_outputs;
    
```

The declaration of these structures is in the `v_gamma_v6_01_a_bitacc_cmodel.h` file.

Table 4-3 lists the generic parameters taken by the Gamma Correction v6.01.a IP core bit accurate model, as well as the default values. For an actual instance of the core, these parameters can only be set in generation time through the Xilinx software GUI.

Table 4-3: Model Generic Parameters and Default Values

Generic variable	Type	Default Value	Range	Description
IWIDTH	int	8	8,10,12	Input data width.
OWIDTH	int	8	8,10,12	Output data width.
VIDEO_FORMAT	int	2	0,1,2,3,1 2	Video Format 0=YUV 4:2:2 1=YUV 4:4:4 2=RGB 3=YUV 4:2:0 4=Mono
INTPOL	int	0	0,1	Interpolation 0=No Interpolation 1=Use Interpolation Interpolation is only valid for IWIDTH=12
NUM_CHANNELS	int	3	1,2,3	Number of valid channels to be processed
LUTS	int	3	1,2,3	Specifies how the Look-Up-Tables are initialized: 3=Each channel has an independent LUT 2=Channel 1 has an independent LUT, channels 2&3 use the same LUT 1=All channels use the same LUT
default_gamma1	double	0.45	0.1 - 10.0	Double precision value used to initialize the default contents of the gamma correction table for channel 1

Table 4-3: Model Generic Parameters and Default Values (Cont'd)

default_gamma2	double	0.45	0.1 - 10.0	Double precision value used to initialize the default contents of the gamma correction table for channel 2. Only valid when LUTS > 1.
default_gamma3	double	0.45	0.1 - 10.0	Double precision value used to initialize the default contents of the gamma correction table for channel 3. Only valid when LUTS = 3.

Calling `xilinx_ip_v_gamma_v6_01_a_get_default_generics (&gamma_generics)` initializes the generics structure with the Gamma GUI defaults, listed in Table 4-3.

Table 4-4: Core Generic Parameters and Default Values

Input Variable	Type	Default Value	Range	Description
video_in	video_struct	Null	N/A	Container to hold input image or video data. ¹
TABLE1	uint16[4096]	$round\left(255 \frac{k^{0.45}}{255^{0.45}}\right)$	0 to $2^{OWIDTH-1} - 1$	Correction Tables for Channels 1,2 and 3. For RGB, R=1, G=2, B=3. For YUV 4:4:4, Y=1, U=2, V=3, For YUV 4:2:2/0, Y=1, U/V=2. For Mono, Y=1.
TABLE2	uint16[4096]			
TABLE3	uint16[4096]			

¹ For the description of the input structure, see [Initializing the Gamma Correction Input Video Structure](#).

The structure `gamma_inputs` defines the values of run time parameters and the actual input image. The TABLES 1-3 can be set dynamically through the AXI4-Lite interface. Consequently, these values are passed as inputs to the core, along with the actual test image, or video sequence (see Table 4-4).

Calling `xilinx_ip_v_gamma_v6_01_a_get_default_inputs (&gamma_generics, &gamma_inputs)` initializes members of the input structure default values (see Table 4-4).



IMPORTANT: The `video_in` variable is not initialized because the initialization depends on the actual test image to be simulated. [Chapter 4, Example Code](#) describes the initialization of the `video_in` structure.

After the inputs are defined, the model can be simulated by calling this function:

```
int xilinx_ip_v_gamma_v6_01_a_bitacc_simulate(
struct xilinx_ip_v_gamma_v6_01_a_generics* generics,
struct xilinx_ip_v_gamma_v6_01_a_inputs* inputs,
struct xilinx_ip_v_gamma_v6_01_a_outputs* outputs).
```

Results are included in the outputs structure, which contains only one member, type `video_struct`. After the outputs are evaluated and saved, dynamically allocated memory for input and output video structures must be released by calling this function:

```
void xilinx_ip_v_gamma_v6_01_a_destroy(
```

```

struct xilinx_ip_v_gamma_v6_01_a_inputs *input,
struct xilinx_ip_v_gamma_v6_01_a_outputs *output).
    
```

Successful execution of all provided functions, except for the destroy function, return value 0. A non-zero error code indicates that problems occurred during function calls.

Gamma Correction Input and Output Video Structure

Input images or video streams can be provided to the Gamma Correction v6.01.a reference model using the `video_struct` structure, defined in `video_utils.h`:

```

struct video_struct{
    int      frames, rows, cols, bits_per_component, mode;
    uint16*** data[5]; };
    
```

Table 4-5: Member Variables

Member Variable	Designation
frames	Number of video/image frames in the data structure.
rows	Number of rows per frame. Pertaining to the image plane with the most rows and columns, such as the luminance channel for YUV data. Frame dimensions are assumed constant through all frames of the video stream. However different planes, such as y, u and v can have different dimensions.
cols	Number of columns per frame. Pertaining to the image plane with the most rows and columns, such as the luminance channel for YUV data. Frame dimensions are assumed constant through all frames of the video stream. However different planes, such as y, u and v can have different dimensions.
bits_per_component	Number of bits per color channel/component. All image planes are assumed to have the same color/component representation. Maximum number of bits per component is 16.
mode	Contains information about the designation of data planes. Named constants to be assigned to mode are listed in Table 4-6.
data	Set of five pointers to three dimensional arrays containing data for image planes. Data is in 16-bit unsigned integer format accessed as <code>data[plane][frame][row][col]</code> .

Table 4-6: Named Constants with Planes and Representations ⁽¹⁾

Mode	Planes	Video Representation
FORMAT_MONO	1	Monochrome – Luminance only

Table 4-6: Named Constants with Planes and Representations ⁽¹⁾ (Cont'd)

FORMAT_RGB	3	RGB image/video data
FORMAT_C444	3	444 YUV, or YCrCb image/video data
FORMAT_C422	3	422 format YUV video, (u, v chrominance channels horizontally sub-sampled)
FORMAT_C420	3	420 format YUV video, (u, v sub-sampled both horizontally and vertically)
FORMAT_MONO_M	3	Monochrome (Luminance) video with Motion
FORMAT_RGBA	4	RGB image/video data with alpha (transparency) channel
FORMAT_C420_M	5	420 YUV video with Motion
FORMAT_C422_M	5	422 YUV video with Motion
FORMAT_C444_M	5	444 YUV video with Motion
FORMAT_RGBM	5	RGB video with Motion

1. The Gamma Correction core supports the FORMAT_RGB, FORMAT_C444, FORMAT_C422, FORMAT_C420, and FORMAT_MONO modes.

Initializing the Gamma Correction Input Video Structure

The easiest way to assign stimuli values to the input video structure is to initialize it with an image or video. The `bmp_util.h` and `video_util.h` header files packaged with the bit accurate C models contain functions to facilitate file I/O.

Bitmap Image Files

The header `bmp_utils.h` declares functions that help access files in Windows Bitmap format (http://en.wikipedia.org/wiki/BMP_file_format). However, this format limits color depth to a maximum of 8-bits per pixel, and operates on images with three planes (R,G,B). Consequently, the following functions operate on arguments type `rgb8_video_struct`, which is defined in `rgb_utils.h`. Also, both functions support only true-color, non-indexed formats with 24-bits per pixel.

```
int write_bmp(FILE *outfile, struct rgb8_video_struct *rgb8_video);
int read_bmp(FILE *infile, struct rgb8_video_struct *rgb8_video);
```

Exchanging data between `rgb8_video_struct` and general `video_struct` type frames/videos is facilitated by these functions:

```
int copy_rgb8_to_video(struct rgb8_video_struct* rgb8_in,
                     struct video_struct* video_out );
int copy_video_to_rgb8(struct video_struct* video_in,
```

```
struct rgb8_video_struct* rgb8_out );
```

Note: All image/video manipulation utility functions expect both input and output structures initialized; for example, pointing to a structure that has been allocated in memory, either as static or dynamic variables. Moreover, the input structure must have the dynamically allocated container (data or r, g, b) structures already allocated and initialized with the input frame(s). If the output container structure is pre-allocated at the time of the function call, the utility functions verify and issue an error if the output container size does not match the size of the expected output. If the output container structure is not pre-allocated, the utility functions create the appropriate container to hold results.

Binary Image/Video Files

The `video_utils.h` header file declares functions that help load and save generalized video files in raw, uncompressed format.

```
int read_video( FILE* infile, struct video_struct* in_video);
int write_video(FILE* outfile, struct video_struct* out_video);
```

These functions serialize the `video_struct` structure. The corresponding file contains a small, plain text header defining, "Mode", "Frames", "Rows", "Columns", and "Bits per Pixel". The plain text header is followed by binary data, 16-bits per component in scan line continuous format. Subsequent frames contain as many component planes as defined by the video mode value selected. Also, the size (rows, columns) of component planes can differ within each frame as defined by the actual video mode selected.

Working with Video_struct Containers

The `video_utils.h` header file defines functions to simplify access to video data in `video_struct`.

```
int video_planes_per_mode(int mode);
int video_rows_per_plane(struct video_struct* video, int plane);
int video_cols_per_plane(struct video_struct* video, int plane);
```

The `video_planes_per_mode` function returns the number of component planes defined by the mode variable, as described in [Table 4-6](#). The `video_rows_per_plane` and `video_cols_per_plane` functions return the number of rows and columns in a given plane of the selected video structure. The following example demonstrates using these functions in conjunction to process all pixels within a video stream stored in the `in_video` variable:

```
for (int frame = 0; frame < in_video->frames; frame++) {
    for (int plane = 0; plane < video_planes_per_mode(in_video->mode); plane++) {
        for (int row = 0; row < rows_per_plane(in_video,plane); row++) {
            for (int col = 0; col < cols_per_plane(in_video,plane); col++) {
                // User defined pixel operations on
                // in_video->data[plane][frame][row][col]
            }
        }
    }
}
```

}

Example Code

An example C file, `run_bitacc_cmodel.c`, is provided to demonstrate the steps required to run the model. After following the compilation instructions, run the example executable. The executable takes the path/name of the input file and the path/name of the output file as parameters. If invoked with insufficient parameters, this help message is issued:

```
Usage: run_bitacc_cmodel in_file out_path
in_file      : path/name of the input BMP file
out_path     : path to the output files
```

During successful execution, two directories will be created at the location specified by the `out_path` command line parameter. The first directory is the "expected" directory. This directory will contain a BMP file that corresponds to the output of the first frame that was processed. This directory will also contain a txt file called `golden_1.txt`. This txt file contains the output of the model in a format that can be directly used with the demonstration test bench. The second directory that is created is the "stimuli" directory. This directory will contain a txt file called `stimuli_1.txt`. This txt file contains the input of the model in a format that can be directly used with the demonstration test bench.

Compiling with the Gamma C Model

Linux (32- and 64-bit)

To compile the example code, first ensure that the directory in which the files `libIp_v_gamma_v6_01_a_bitacc_cmodel.so` and `libstlport.so.5.1` are located is present in your `$LD_LIBRARY_PATH` environment variable. These shared libraries are referenced during the compilation and linking process. Then `cd` into the directory where the header files, library files and `run_bitacc_cmodel.c` were unpacked. The libraries and header files are referenced during the compilation and linking process.

Place the header file and C source file in a single directory. Then in that directory, compile using the GNU C Compiler:

```
gcc -m32 -x c++ ../run_bitacc_cmodel.c ../gen_stim.c -o run_bitacc_cmodel -L.  
-lIp_v_gamma_v6_01_a_bitacc_cmodel -Wl,-rpath,.  
  
gcc -m64 -x c++ ../run_bitacc_cmodel.c ../gen_stim.c -o run_bitacc_cmodel -L.  
-lIp_v_gamma_v6_01_a_bitacc_cmodel -Wl,-rpath,.
```

Windows (32- and 64-bit)

Precompiled library `v_gamma_v6_01_a_bitacc_cmodel.dll`, and top level demonstration code `run_bitacc_cmodel.c` should be compiled with an ANSI C compliant compiler under Windows. Here an example is presented using Microsoft Visual Studio.

In Visual Studio create a new, empty Windows Console Application project. As existing items, add:

- The `llibIpv_gamma_v6_01_a_bitacc_cmodel.dll` file to the "Resource Files" folder of the project
- The `run_bitacc_cmodel.c` and `gen_stim.c` files to the "Source Files" folder of the project
- The `v_gamma_v6_01_a_bitacc_cmodel.h` header files to "Header Files" folder of the project (optional)

After the project has been created and populated, it needs to be compiled and linked (built) to create a win32 executable. To perform the build step, choose **Build Solution** from the Build menu. An executable matching the project name has been created either in the Debug or Release subdirectories under the project location based on whether **Debug** or **Release** has been selected in the **Configuration Manager** under the Build menu.

SECTION II: VIVADO DESIGN SUITE

Customizing and Generating the Core

Constraining the Core

Detailed Example Design

Customizing and Generating the Core

This chapter includes information about using Xilinx tools to customize and generate the core in the Vivado™ Design Suite environment.

Graphical User Interface

The Gamma Correction core is easily configured to meet the user's specific needs through the Vivado Design Suite GUI. This section provides a quick reference to parameters that can be configured at generation time. [Figure 5-1](#) shows the main Vivado Gamma Correction screen.

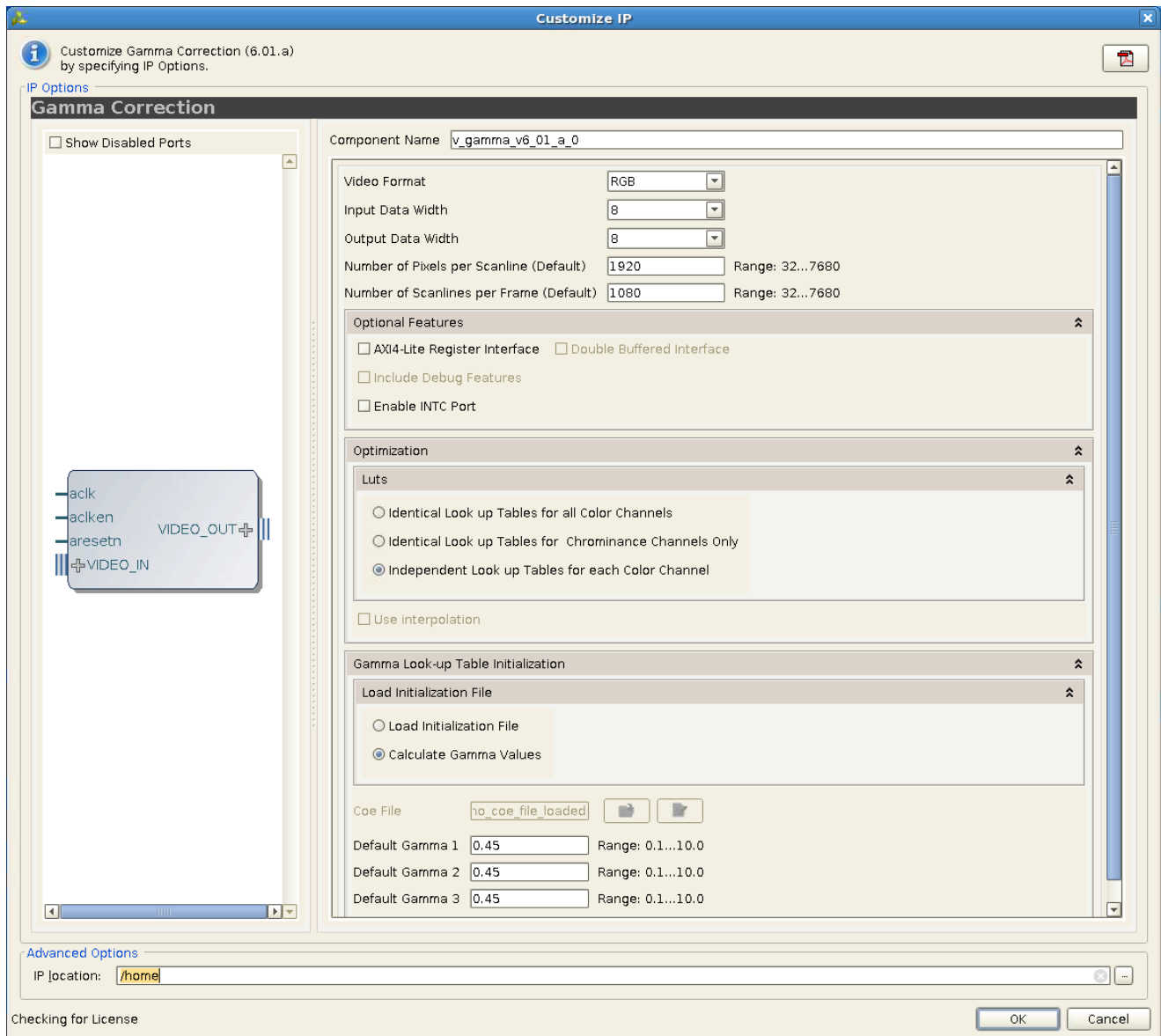


Figure 5-1: Gamma Correction Vivado IP Catalog GUI

The main screen displays a representation of the IP symbol on the left side, and the parameter assignments on the right side, which are described as follows:

- **Component Name:** The component name is used as the base name of output files generated for the module. Names must begin with a letter and must be composed from characters: a to z, 0 to 9 and "_". **The name v_gamma_v6_01_a is not allowed.**
- **Video Format:** Specifies the format of the video to be processed. Permitted values are RGB and YUV 4:4:4, YUV 4:2:2, YUV 4:2:0 and Mono.
- **Input Data Width:** Specifies the bit width of the input color channel for each component. Permitted values are 8, 10 and 12 bits.

- **Output Data Width:** Specifies the bit width of the output color channel for each component. Permitted values are 8, 10 and 12 bits.
- **Number of Active Pixels per Scan line:** When the AXI4-Lite control interface is enabled, the generated core will use the value specified in the Vivado GUI as the default value for the lower half-word of the `ACTIVE_SIZE` register. When an AXI4-Lite interface is not present, the GUI selection permanently defines the horizontal size of the frames the generated core instance is to process.
- **Number of Active Lines per Frame:** When the AXI4-Lite control interface is enabled, the generated core will use the value specified in the Vivado GUI as the default value for the upper half-word of the `ACTIVE_SIZE` register. When an AXI4-Lite interface is not present, the GUI selection permanently defines the vertical size (number of lines) of the frames the generated core instance is to process.
- **Optional Features:**
 - **AXI4-Lite Register Interface:** When selected, the core will be generated with an AXI4-Lite interface, which gives access to dynamically program and change processing parameters. For more information, refer to [Control Interface in Chapter 2](#).
 - **Include Debugging Features:** When selected, the core will be generated with debugging features, which simplify system design, testing and debugging. For more information, refer to [Debugging Features in Appendix C](#).



IMPORTANT: *Debugging features are only available when the AXI4-Lite Register Interface is selected.*

- **INTC Interface:** When selected, the core will generate the optional `INTC_IF` port, which gives parallel access to signals indicating frame processing status and error conditions. For more information, refer to [The Interrupt Subsystem in Chapter 2](#).
- **Double-Buffered Interface:** Double-buffering is used to eliminate tearing of the output images by writing to an inactive look-up table, then providing the ability to swap inactive and active look-up tables. This feature is only available for the AXI4-Lite Interface. However, using this feature may increase the memory footprint of the core.
- **Optimization:** Specifies options to reduce memory usage.
 - **Independent Look-up Tables for each Color Channel:** When selected, each color channel uses a separate look-up table, permitting each channel to implement a distinct function. This option requires the most Block RAM resources.
 - **Identical Look-up Tables for Chrominance Channels Only:** When selected, the chrominance channels (Cr, Cb) will share the same look-up table contents. (This also applies to the U and V channels for YUV or the Green and Blue channels of RGB). When two channels can use the same look-up table, the required number of write operations to modify the function stored in the look-up tables is reduced, and in some cases the number of Block RAM resources required is reduced.

- **Identical Look-up Tables for all Color Channels:** When selected, the red, green, and blue (or luminance and chrominance channels) all share the same look-up table contents. When all channels can use the same look-up tables, the required number of write operations to modify the function stored in the look-up tables is reduced, and in some cases the number of Block RAM resources required is reduced.
- **Use Interpolation:** Interpolation is used to reduce block RAM counts when using 12-bit input from 4k entries per look-up table to only 1k per look-up table.
- **Gamma Look-Up Table Initialization**
 - **Load Initialization File:** When selected, the Load Initialization File feature allows a custom COE file to be loaded which specifies the contents of the gamma look-up tables. This permits the Gamma Correction core to be used to implement any function for a variety of tasks.
 - **Calculate Gamma Values:** When selected, specifies the gamma value for initializing the look-up tables. Permitted values are floating-point values from 0.1 to 10. If the Input Data Width is different from the Output Data Width, the generated tables are sized and scaled appropriately.

Output Generation

Vivado generates the files necessary to build the core and places those files in the <project>/<project>.srcs/sources_1/ip/<core> directory.

File Details

The Vivado output consists of some or all the files in [Table 5-1](#).

Table 5-1: Vivado Tools Output Files

Name	Description
v_gamma_v6_01_a	Library directory for the v_gamma_v6_01_a core which contains the encrypted source files.
v_tc_v5_01_a	Library directory for the helper core which contain the encrypted source files used with the v_gamma_v6_01_a.
<component_name>.veo	The HDL template for instantiating the core.
<component_name>.vho	
<component_name>.xci	IP-XACT XML file describing which options were used to generate the core. An XCI file can also be used as a source file for Vivado.
<component_name>.xml	IP-XACT XML file describing how the core is constructed so Vivado can properly build the core.

Constraining the Core

Required Constraints

The `ACLK` pin should be constrained at the desired pixel clock rate for your video stream.

The `S_AXI_ACLK` pin should be constrained at the frequency of the AXI4-Lite subsystem.

In addition to clock frequency, the following constraints should be applied to cover all clock domain crossing data paths.

UCF

```
INST "*U_VIDEO_CTRL*/*SYNC2PROCCLK_I*/data_sync_reg[0]*" TNM =
"async_clock_conv_FFDEST";
TIMESPEC "TS_async_clock_conv" = FROM FFS TO "async_clock_conv_FFDEST" 2 NS
DATAPATHONLY;
INST "*U_VIDEO_CTRLk*/*SYNC2VIDCLK_I*/data_sync_reg[0]*" TNM =
"vid_async_clock_conv_FFDEST";
TIMESPEC "TS_vid_async_clock_conv" = FROM FFS TO "vid_async_clock_conv_FFDEST" 2 NS
DATAPATHONLY;
```

XDC

```
set_max_delay -to [get_cells -hierarchical -match_style ucf "*U_VIDEO_CTRL*/
*SYNC2PROCCLK_I*/data_sync_reg[0]*"] -datapath_only 2
set_max_delay -to [get_cells -hierarchical -match_style ucf "*U_VIDEO_CTRL*/
*SYNC2VIDCLK_I*/data_sync_reg[0]*"] -datapath_only 2
```

Device, Package, and Speed Grade Selections

There are no device, package, or speed grade requirements for this core. For a complete listing of supported devices, see the [release notes](#) for this core.

Clock Frequencies

The pixel clock (`ACLK`) frequency is the required frequency for the Gamma Correction core. See [Maximum Frequencies in Chapter 2](#). The `S_AXI_ACLK` maximum frequency is the same as the `ACLK` maximum.

Clock Management

The core automatically handles clock domain crossing between the `ACLK` (video pixel clock and AXI4-Stream) and the `S_AXI_ACLK` (AXI4-Lite) clock domains. The `S_AXI_ACLK` clock can be slower or faster than the `ACLK` clock signal, but must not be more than 128x faster than `ACLK`.

Clock Placement

There are no specific Clock placement requirements for this core.

Banking

There are no specific Banking rules for this core.

Transceiver Placement

There are no Transceiver Placement requirements for this core.

I/O Standard and Placement

There are no specific I/O standards and placement requirements for this core.

Detailed Example Design

No example design is available at the time for the LogiCORE IP Gamma Correction v6.01.a core.

Demonstration Test Bench

A demonstration test bench is provided with the core which enables you to observe core behavior in a typical scenario. This test bench is generated together with the core in Vivado design tools. You are encouraged to make simple modifications to the configurations and observe the changes in the waveform.

Generating the Test Bench

1. After customizing the IP, right-click on the core instance in **Sources** pane and select **Generate Output Products** ([Figure 7-1](#)).

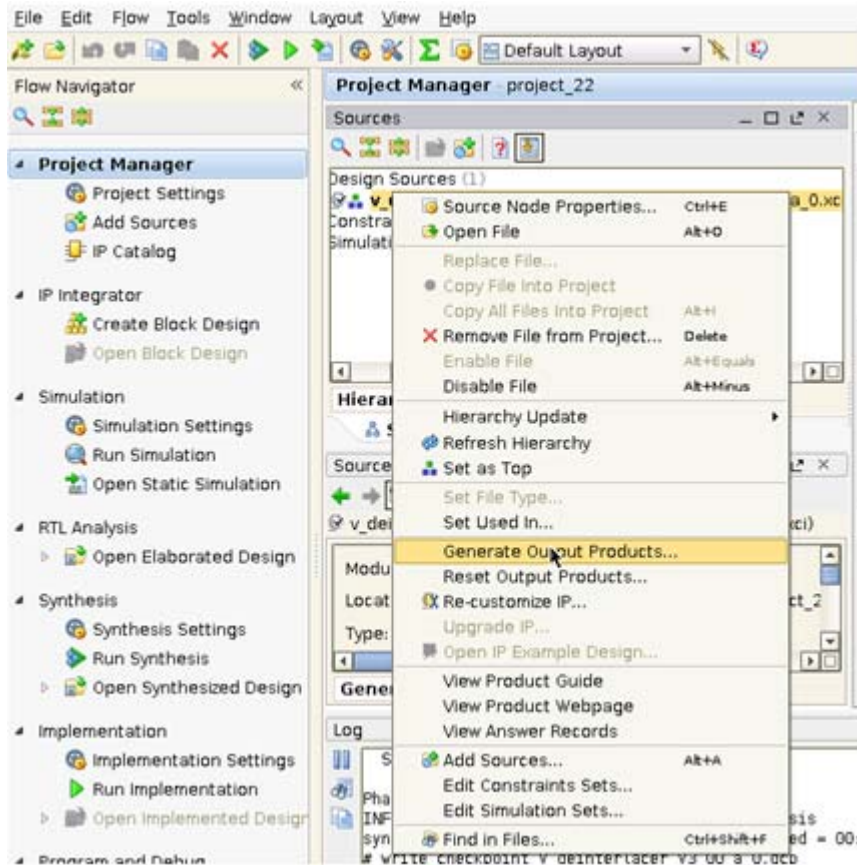


Figure 7-1:

A pop-up window prompts you to select items to generate.

2. Click on **Test Bench** and make sure **Action: Generate** is selected.

The demo test bench package will be generated in the following directory (Figure 7-2):

```
<PROJ_DIR>/<PROJ_NAME>.srcs/sources_1/ip/<IP_INSTANCE_NAME>/<IP_INSTANCE_NAME>/demo_tb/
```

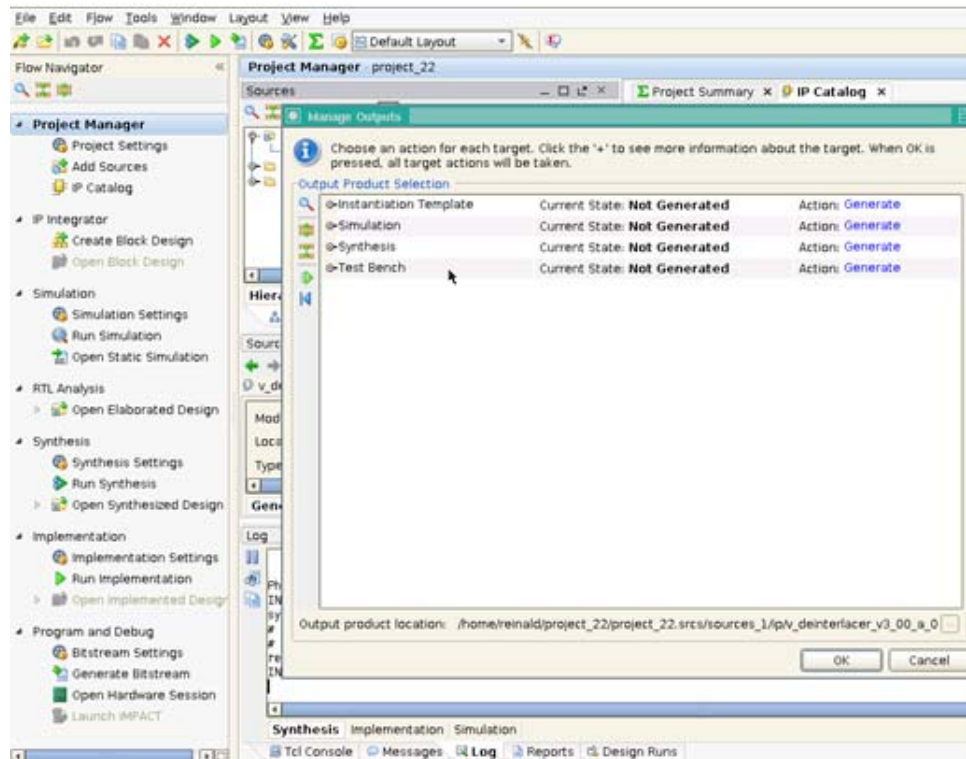


Figure 7-2:

Directory and File Contents

The following files are expected to be generated in the in the demo test bench output directory:

- axi4lite_mst.v
- axi4s_video_mst.v
- axi4s_video_slv.v
- ce_generator.v
- tb_<IP_instance_name>.v

Test Bench Structure

The top-level entity is **tb_<IP_instance_name>**.

It instantiates the following modules:

- DUT
 - The <IP> core instance under test.
- axi4lite_mst

The AXI4-Lite master module, which initiates AXI4-Lite transactions to program core registers.

- `axi4s_video_mst`

The AXI4-Stream master module, which generates ramp data and initiates AXI4-Stream transactions to provide video stimuli for the core and can also be used to open stimuli files generated from the reference C models and convert them into corresponding AXI4-Stream transactions.

To do this, edit `tb_<IP_instance_name>.v`:

- a. Add define macro for the stimuli file name and directory path
`define STIMULI_FILE_NAME<path><filename>.`
- b. Comment-out/remove the following line:
`MST.is_ramp_gen(`C_ACTIVE_ROWS, `C_ACTIVE_COLS, 2);`
and replace with the following line:
`MST.use_file(`STIMULI_FILE_NAME);`

For information about generating stimuli files, refer to [C Model Reference](#).

- `axi4s_video_slv`

The AXI4-Stream slave module, which acts as a passive slave to provide handshake signals for the AXI4-Stream transactions from the core's output, can be used to open the data files generated from the reference C model and verify the output from the core.

To do this, edit `tb_<IP_instance_name>.v`:

- a. Add define macro for the golden file name and directory path
`define GOLDEN_FILE_NAME "<path><filename>".`
- b. Comment-out the following line:
`SLV.is_passive;`
and replace with the following line:
`SLV.use_file(`GOLDEN_FILE_NAME);`

For information about generating golden files, refer to [C Model Reference](#).

- `ce_gen`

Programmable Clock Enable (ACLKEN) generator.

Running the Simulation

There are two ways to run the demonstration test bench.

Option 1: Launch Simulation from the Vivado GUI

This runs the test bench with the AXI4-Stream Master producing ramp data as stimuli, and AXI4-Stream Slave set to passive mode.

- Click **Simulation Settings** in the Flow Navigation window, change Simulation top module name to **tb_<IP_instance_name>**.
- Click **Run Simulation**. XSIM launches and you should be able to see the signals.
- You can also choose Modelsim for simulation by going to **Project Settings** and selecting Modelsim as the Target Simulator ([Figure 7-3](#)).

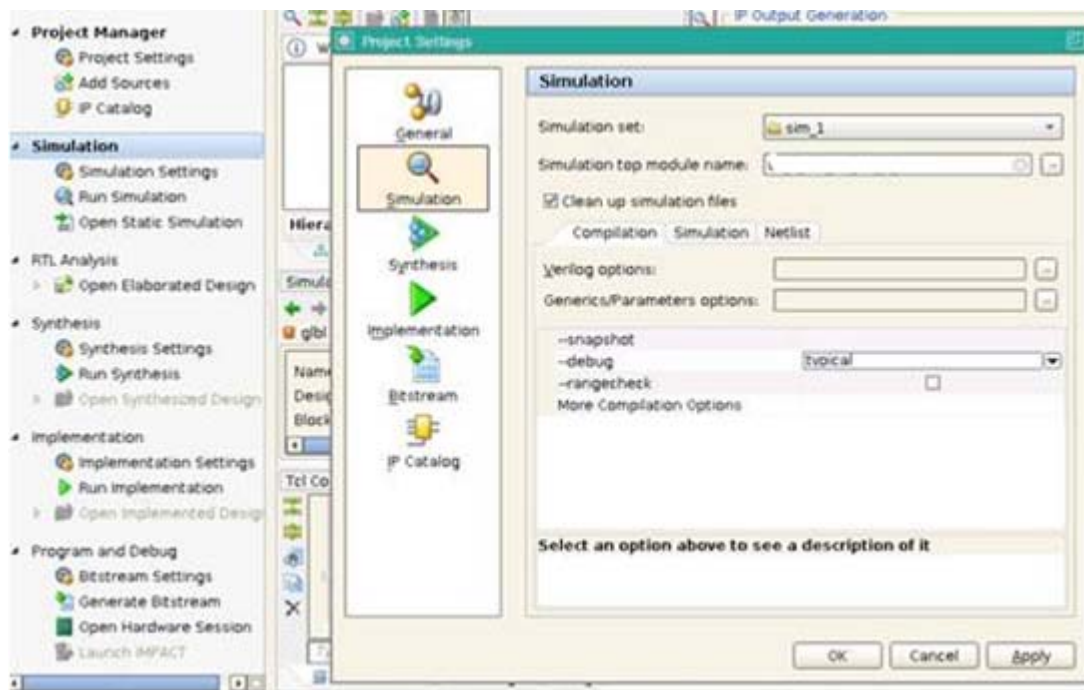


Figure 7-3: Simulation GUI

Option 2: Manually Compile and Run the Simulation from Your Environment

- Add the generated test bench files to a new simulation set, along with the customized IP. For information on the location of generated test bench files, refer to [Generating the Test Bench](#).
- Setup the environment variables for Xilinx libraries
- Compile the generated IP
- Compile the test bench files

- Run the simulation



RECOMMENDED: *To change the default simulation time from **1000 ns** to **all** to be able observe a full frame transaction.*

SECTION III: ISE DESIGN SUITE

Customizing and Generating the Core

Constraining the Core

Detailed Example Design

Customizing and Generating the Core

This chapter includes information about using Xilinx tools to customize and generate the core in the ISE® Design Suite environment.

Graphical User Interface

The Gamma Correction core is easily configured to meet the user's specific needs through the CORE Generator or EDK GUI. This section provides a quick reference to parameters that can be configured at generation time. [Figure 8-1](#) shows the main CORE Generator Gamma Correction screen. [Figure 8-2](#) shows the main EDK Gamma Correction screen.

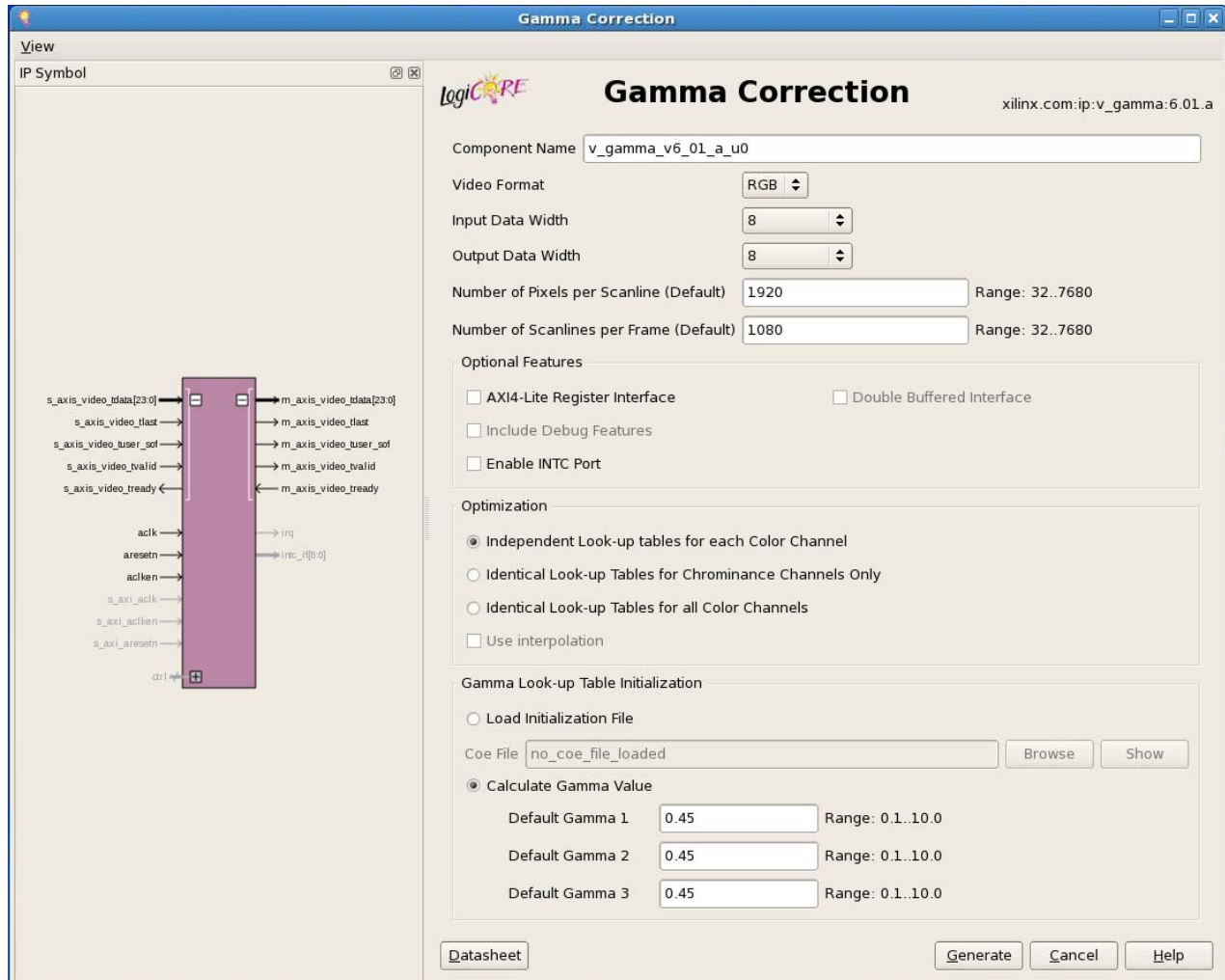


Figure 8-1: Gamma Correction Main Screen

The main screen displays a representation of the IP symbol on the left side, and the parameter assignments on the right side, which are described as follows:

- **Component Name:** The component name is used as the base name of output files generated for the module. Names must begin with a letter and must be composed from characters: a to z, 0 to 9 and "_". **The name v_gamma_v6_01_a is not allowed.**
- **Video Format:** Specifies the format of the video to be processed. Permitted values are RGB and YUV 4:4:4, YUV 4:2:2, YUV 4:2:0 and Mono.
- **Input Data Width:** Specifies the bit width of the input color channel for each component. Permitted values are 8, 10 and 12 bits.
- **Output Data Width:** Specifies the bit width of the output color channel for each component. Permitted values are 8, 10 and 12 bits.
- **Number of Active Pixels per Scan line:** When the AXI4-Lite control interface is enabled, the generated core will use the value specified in the CORE Generator GUI as

the default value for the lower half-word of the `ACTIVE_SIZE` register. When an AXI4-Lite interface is not present, the GUI selection permanently defines the horizontal size of the frames the generated core instance is to process.

- **Number of Active Lines per Frame:** When the AXI4-Lite control interface is enabled, the generated core will use the value specified in the CORE Generator GUI as the default value for the upper half-word of the `ACTIVE_SIZE` register. When an AXI4-Lite interface is not present, the GUI selection permanently defines the vertical size (number of lines) of the frames the generated core instance is to process.
- **Optional Features:**
 - **AXI4-Lite Register Interface:** When selected, the core will be generated with an AXI4-Lite interface, which gives access to dynamically program and change processing parameters. For more information, refer to [Control Interface in Chapter 2](#).
 - **Include Debugging Features:** When selected, the core will be generated with debugging features, which simplify system design, testing and debugging. For more information, refer to [Debugging Features in Appendix C](#).



IMPORTANT: *Debugging features are only available when the AXI4-Lite Register Interface is selected.*

- **INTC Interface:** When selected, the core will generate the optional `INTC_IF` port, which gives parallel access to signals indicating frame processing status and error conditions. For more information, refer to [The Interrupt Subsystem in Chapter 2](#).
- **Double-Buffered Interface:** Double-buffering is used to eliminate tearing of the output images by writing to an inactive look-up table, then providing the ability to swap inactive and active look-up tables. This feature is only available for the AXI4-Lite Interface. However, using this feature may increase the memory footprint of the core.
- **Optimization:** Specifies options to reduce memory usage.
 - **Independent Look-up Tables for each Color Channel:** When selected, each color channel uses a separate look-up table, permitting each channel to implement a distinct function. This option requires the most Block RAM resources. In the EDK GUI, the equivalent selection is `LUTS = 3`.
 - **Identical Look-up Tables for Chrominance Channels Only:** When selected, the chrominance channels (Cr, Cb) will share the same look-up table contents. (This also applies to the U and V channels for YUV or the Green and Blue channels of RGB). When two channels can use the same look-up table, the required number of write operations to modify the function stored in the look-up tables is reduced, and in some cases the number of Block RAM resources required is reduced. In the EDK GUI, the equivalent selection is `LUTS = 2`.
 - **Identical Look-up Tables for all Color Channels:** When selected, the red, green, and blue (or luminance and chrominance channels) all share the same look-up table

contents. When all channels can use the same look-up tables, the required number of write operations to modify the function stored in the look-up tables is reduced, and in some cases the number of Block RAM resources required is reduced. In the EDK GUI, the equivalent selection is LUTS = 1.

- **Use Interpolation:** Interpolation is used to reduce block RAM counts when using 12-bit input from 4k entries per look-up table to only 1k per look-up table.
- **Gamma Look-Up Table Initialization**
 - **Load Initialization File:** When selected, the Load Initialization File feature allows a custom COE file to be loaded which specifies the contents of the gamma look-up tables. This permits the Gamma Correction core to be used to implement any function for a variety of tasks.
 - **Calculate Gamma Value:** When selected, specifies the gamma value for initializing the look-up tables. Permitted values are floating-point values from 0.1 to 10. If the Input Data Width is different from the Output Data Width, the generated tables are sized and scaled appropriately.

Figure 8-2 shows the main Gamma Correction EDK screen. Definitions of the EDK GUI controls are identical to the corresponding CORE Generator GUI functions.

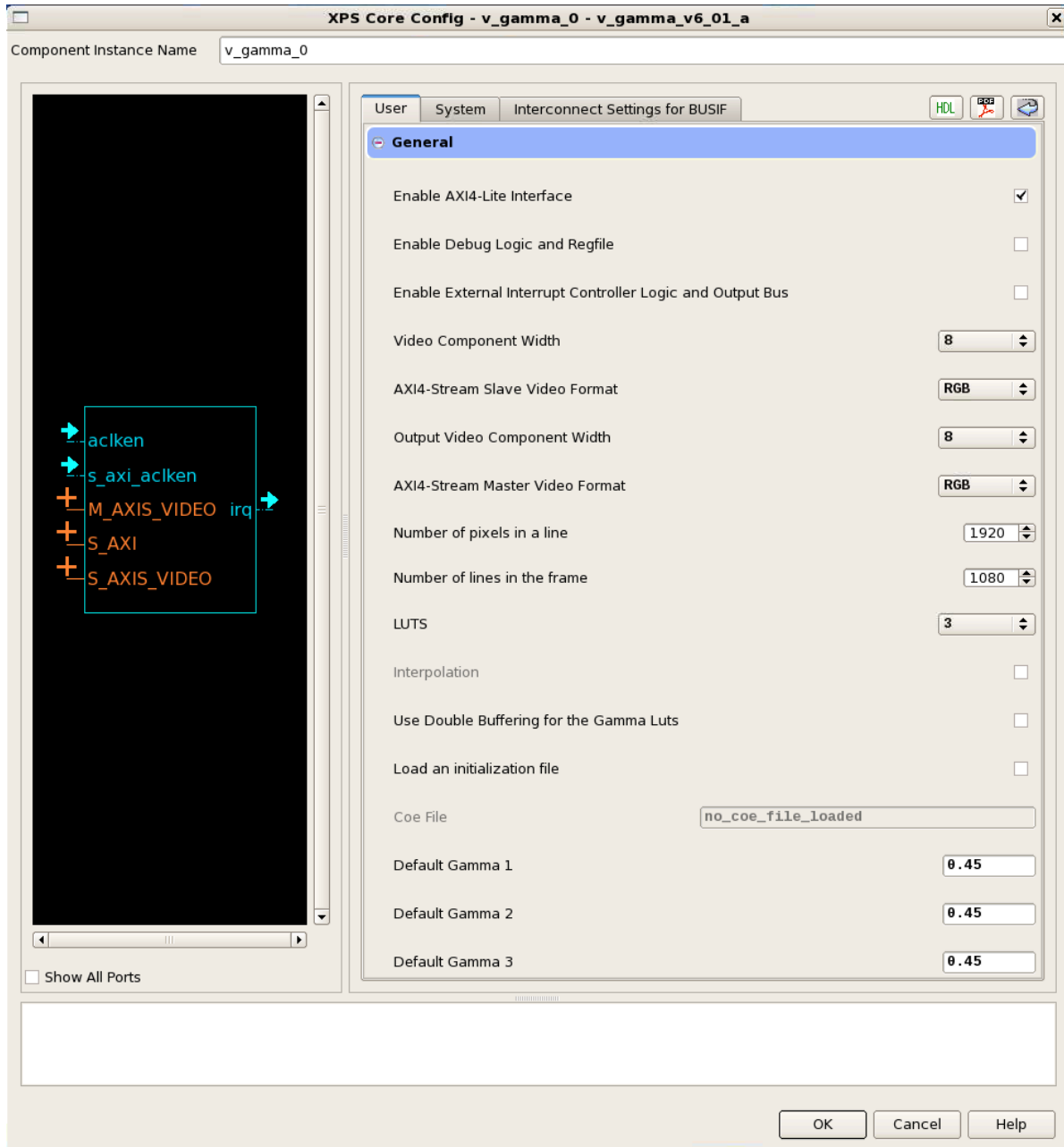


Figure 8-2: Gamma Correction EDK Screen

Parameter Values in the XCO File

Table 8-1 defines valid entries for the XCO parameters. Xilinx strongly suggests that XCO parameters are not manually edited in the XCO file; instead, use the CORE Generator software GUI to configure the core and perform range and parameter value checking. The XCO parameters are helpful in defining the interface to other Xilinx tools.

Table 8-1: XCO Parameters

XCO Parameter	Default Value
component_name	v_gamma_v6_01_a_u0
s_axis_video_data_width	8
m_axis_video_data_width	8
s_axis_video_format	RGB
m_axis_video_format	RGB
intpol	false
luts	1
dbl_buf	false
load_init_file	0
default_gamma1	0.45
default_gamma2	0.45
default_gamma3	0.45
coe_file	no_coe_file_loaded
active_cols	1920
active_rows	1080
has_axi4_lite	false
has_debug	false
has_intc_if	false

Output Generation

CORE Generator will output the core as a netlist that can be inserted into a processor interface wrapper or instantiated directly in an HDL design. The output is placed in the <project director>.

File Details

The CORE Generator output consists of some or all the following files.

Table 8-2: Output Files

Name	Description
<component_name>_readme.txt	Readme file for the core.
<component_name>.ngc	The netlist for the core.
<component_name>.veo	The HDL template for instantiating the core.
<component_name>.vho	

Table 8-2: Output Files (Cont'd)

Name	Description
<component_name>.v	The structural simulation model for the core. It is used for functionally simulating the core.
<component_name>.vhd	
<component_name>.xco	Log file from CORE Generator software describing which options were used to generate the core. An XCO file can also be used as an input to the CORE Generator software.

Constraining the Core

Required Constraints

The `ACLK` pin should be constrained at the desired pixel clock rate for your video stream. The `S_AXI_ACLK` pin should be constrained at the frequency of the AXI4-Lite subsystem. In addition to clock frequency, the following constraints should be applied to cover all clock domain crossing data paths.

UCF

```
INST "*U_VIDEO_CTRL*/*SYNC2PROCCLK_I*/data_sync_reg[0]*" TNM =
"async_clock_conv_FFDEST";
TIMESPEC "TS_async_clock_conv" = FROM FFS TO "async_clock_conv_FFDEST" 2 NS
DATAPATHONLY;
INST "*U_VIDEO_CTRLk*/*SYNC2VIDCLK_I*/data_sync_reg[0]*" TNM =
"vid_async_clock_conv_FFDEST";
TIMESPEC "TS_vid_async_clock_conv" = FROM FFS TO "vid_async_clock_conv_FFDEST" 2 NS
DATAPATHONLY;
```

XDC

```
set_max_delay -to [get_cells -hierarchical -match_style ucf "*U_VIDEO_CTRL*/
*SYNC2PROCCLK_I*/data_sync_reg[0]*"] -datapath_only 2
set_max_delay -to [get_cells -hierarchical -match_style ucf "*U_VIDEO_CTRL*/
*SYNC2VIDCLK_I*/data_sync_reg[0]*"] -datapath_only 2
```

Device, Package, and Speed Grade Selections

There are no device, package, or speed grade requirements for this core. For a complete listing of supported devices, see the release notes for this core.

Clock Frequencies

The pixel clock (`ACLK`) frequency is the required frequency for the Gamma Correction core. See [Maximum Frequencies in Chapter 2](#). The `S_AXI_ACLK` maximum frequency is the same as the `ACLK` maximum.

Clock Management

The core automatically handles clock domain crossing between the `ACLK` (video pixel clock and AXI4-Stream) and the `S_AXI_ACLK` (AXI4-Lite) clock domains. The `S_AXI_ACLK` clock can be slower or faster than the `ACLK` clock signal, but must not be more than 128x faster than `ACLK`.

Clock Placement

There are no specific Clock placement requirements for this core.

Banking

There are no specific Banking rules for this core.

Transceiver Placement

There are no Transceiver Placement requirements for this core.

I/O Standard and Placement

There are no specific I/O standards and placement requirements for this core.

Detailed Example Design

No example design is currently available for the LogiCORE IP Gamma Correction v6.01.a core.

Demonstration Test Bench

A demonstration test bench is provided which enables core users to observe core behavior in a typical use scenario. The user is encouraged to make simple modifications to the test conditions and observe the changes in the waveform.

Test Bench Structure

The top-level entity, `tb_main.v`, instantiates the following modules:

- DUT
The Gamma core instance under test.
- `axi4lite_mst`
The AXI4-Lite master module, which initiates AXI4-Lite transactions to program core registers.
- `axi4s_video_mst`
The AXI4-Stream master module, which opens the stimuli txt file and initiates AXI4-Stream transactions to provide stimuli data for the core
- `axi4s_video_slv`
The AXI4-Stream slave module, which opens the result txt file and verifies AXI4-Stream transactions from the core
- `ce_gen`
Programmable Clock Enable (`ACLKEN`) generator

Running the Simulation

- Simulation using ModelSim for Linux:
From the console, Type "source run_mti.sh".
 - Simulation using iSim for Linux:
From the console, Type "source run_isim.sh".
 - Simulation using ModelSim for Windows:
Double-click on "run_mti.bat" file.
 - Simulation using iSim:
Double-click on "run_isim.bat" file.
-

Directory and File Contents

The directory structure underneath the top-level folder is:

- **Expected:**
Contains the pre-generated expected/golden data used by the test bench to compare actual output data.
- **Stimuli:**
Contains the pre-generated input data used by the test bench to stimulate the core (including register programming values).
- **Results:**
Actual output data will be written to a file in this folder.
- **Src:**
Contains the .vhd simulation files and the .xco CORE Generator parameterization file of the core instance. The .vhd file is a netlist generated using CORE Generator. The .xco file can be used to regenerate a new netlist using CORE Generator.

The available core C model can be used to generate stimuli and expected results for any user bmp image. For more information, refer to [Chapter 4, C Model Reference](#).

The top-level directory contains packages and Verilog modules used by the test bench, as well as:

- isim_wave.wcfg:
Waveform configuration for ISIM
- mti_wave.do:
Waveform configuration for ModelSim

- run_isim.bat:
Runscript for iSim in Windows
- run_isim.sh:
Runscript for iSim in Linux
- run_mti.bat:
Runscript for ModelSim in Windows
- run_mti.sh:
Runscript for ModelSim in Linux

SECTION IV: APPENDICES

Verification, Compliance, and Interoperability

Migrating

Debugging

Application Software Development

Additional Resources

Verification, Compliance, and Interoperability

Simulation

A highly parameterizable test bench was used to test the Gamma Correction core. Testing included the following:

- Register accesses
 - Processing multiple frames of data
 - AXI4-Stream bidirectional data-throttling tests
 - Testing detection, and recovery from various AXI4-Stream framing error scenarios
 - Testing different `ACLKEN` and `ARESETn` assertion scenarios
 - Testing of various frame sizes
 - Varying parameter settings
-

Hardware Testing

The Gamma Correction core has been validated in hardware at Xilinx to represent a variety of parameterizations, including the following:

- A test design was developed for the core that incorporated a MicroBlaze™ processor, AXI4-Lite interconnect and various other peripherals. The software for the test system included pre-generated input and output data along with live video stream. The MicroBlaze processor was responsible for:
 - Initializing the appropriate input and output buffers
 - Initializing the Gamma Correction core
 - Launching the test
 - Comparing the output of the core against the expected results

- Reporting the Pass/Fail status of the test and any errors that were found

Interoperability

The core slave (input) AXI4-Stream interface can work directly with any Xilinx Video core that can produce the video format for which the Gamma Correction core is configured. The core master (output) AXI4-Stream interface can work directly with any Xilinx Video core which can consume the video format for which the Gamma Correction core is configured.

Migrating

For information about migration from ISE Design Suite to Vivado Design Suite, see *Vivado Design Suite Migration Methodology Guide* (UG911).

For a complete list of Vivado User and Methodology Guides, see the [Vivado Design Suite - 2012.3 User Guides web page](#).

From version v4.0 to v5.00.a of the Gamma Correction core the following significant changes took place:

- AXI4-Stream interfaces replaced XSVI interfaces.
- Since AXI4-Stream does not carry video timing data, the timing detector and timing generator modules were trimmed.
- The pCore, General Purpose Processor and Transparent modes became obsolete and were removed.
- Added native support for EDK; the Gamma Correction core appears in the EDK IP Catalog
- Added Debugging features.
- The AXI4-Lite control interface register map is standardized between Xilinx video cores.

From v5.00.a to v6.01.a of the Gamma core, the following changes took place:

- The core originally had `aclk`, `aclken`, and `aresetn` to control both the Video over AXI4-Stream and AXI4-Lite interfaces. Separate clock, clock enable and reset pins now control the Video over AXI4-Stream and the AXI4-Lite interfaces with clock domain crossing logic added to the core to handle the dissimilar clock domains between the AXI4-Lite and Video over AXI4-Stream domains.

Because of the complex nature of these changes, replacing a v4.0 version of the core in a customer design is not trivial. An existing EDK pCore, Transparent, or Constant Gamma instance can be converted from XSVI to AXI4-Stream, using the Video In to AXI4-Stream core or components from XAPP521 (v1.0), *Bridging Xilinx Streaming Video Interface with the AXI4-Stream Protocol* located at:

http://www.xilinx.com/support/documentation/application_notes/xapp521_XSVI_AXI4.pdf.

A v4.0 pCore instance in EDK can be replaced from v6.01.a directly from the EDK IP Catalog. However, the application software needs to be updated for the changed functionality and

addresses of the `IRQ_ENABLE`, `STATUS`, `ERROR`, and core-specific registers. Consider replacing a legacy Gamma pCore from EDK with a v6.01.a instance without AXI4-Lite interface to save resources.

If the user design explicitly used the timing detector or generator functionality of the Gamma Correction core, consider adding the Video Timing Controller core to migrate the functionality.

An ISE design using the General Purpose Processor interface, all of the above steps might be necessary:

- Timing detection, generation using the Video Timing Controller Core
- Replacing XSVI interfaces with conversion modules described in XAPP521 or try using the Video In to AXI4-Stream core
- Updating the Gamma Correction core instance to v6.01.a with or without AXI4-Lite interface

The INTC interface and debug functionality are new features for v6.01.a. When migrating an existing design, these functions may be disabled.

Debugging



RECOMMENDED: *It is recommended to prototype the system with the AXI4-Stream interface enabled, so status and error detection, reset, and dynamic size programming can be used during debugging.*

The following steps are recommended to bring-up/debug the core in a video/imaging system:

1. Bring up the AXI4-Lite interface
2. Bring up the AXI4-Stream interfaces
 - (Optional) Balancing throughput

Once the core is working as expected, the user may consider 'hardening' the configuration by replacing the Gamma Correction core with an instance where GUI default values are set to the established register values, but the AXI4-Lite interface is disabled. This configuration reduces the core slice footprint.

Bringing up the AXI4-Lite Interface

Table C-1 describes how to troubleshoot the AXI4-Lite interface.

Table C-1: Troubleshooting the AXI4-Lite Interface

Symptom	Solution
Readback from the Version Register via the AXI4-Lite interface times out, or a core instance without an AXI4-Lite interface seems non-responsive.	Are the <code>S_AXI_ACLK</code> and <code>ACLK</code> pins connected? In EDK, verify that the <code>S_AXI_ACLK</code> and <code>ACLK</code> pin connections in the system.mhs file. The <code>VERSION_REGISTER</code> readout issue may be indicative of the core not receiving the AXI4-Lite interface.
Readback from the Version Register via the AXI4-Lite interface times out, or a core instance without an AXI4-Lite interface seems non-responsive.	Is the core enabled? Is <code>s_axi_aclken</code> connected to <code>vcc</code> ? In EDK, verify that signal <code>ACLKEN</code> is connected in the system.mhs to either <code>net_vcc</code> or to a designated clock enable signal.

Table C-1: Troubleshooting the AXI4-Lite Interface (Cont'd)

Symptom	Solution
Readback from the Version Register via the AXI4-Lite interface times out, or a core instance without an AXI4-Lite interface seems non-responsive.	Is the core in reset? S_AXI_ARESETn and ARESETn should be connected to vcc for the core not to be in reset. In EDK, verify that the S_AXI_ARESETn and ARESETn signals are connected in the system.mhs to either net_vcc or to a designated reset signal.
Readback value for the VERSION_REGISTER is different from expected default values	The core and/or the driver in a legacy EDK/SDK project has not been updated. Ensure that old core versions, implementation files, and implementation caches have been cleared.

Assuming the AXI4-Lite interface works, the second step is to bring up the AXI4-Stream interfaces.

Bringing up the AXI4-Stream Interfaces

Table C-2 describes how to troubleshoot the AXI4-Stream interface.

Table C-2: Troubleshooting AXI4-Stream Interface

Symptom	Solution
Bit 0 of the ERROR register reads back set.	Bit 0 of the ERROR register, EOL_EARLY, indicates the number of pixels received between the latest and the preceding End-Of-Line (EOL) signal was less than the value programmed into the ACTIVE_SIZE register. If the value was provided by the Video Timing Controller core, read out ACTIVE_SIZE register value from the VTC core again, and make sure that the TIMING_LOCKED flag is set in the VTC core. Otherwise, using Chipscope, measure the number of active AXI4-Stream transactions between EOL pulses.
Bit 1 of the ERROR register reads back set.	Bit 1 of the ERROR register, EOL_LATE, indicates the number of pixels received between the last End-Of-Line (EOL) signal surpassed the value programmed into the ACTIVE_SIZE register. If the value was provided by the Video Timing Controller core, read out ACTIVE_SIZE register value from the VTC core again, and make sure that the TIMING_LOCKED flag is set in the VTC core. Otherwise, using Chipscope, measure the number of active AXI4-Stream transactions between EOL pulses.
Bit 2 or Bit 3 of the ERROR register reads back set.	Bit 2 of the ERROR register, SOF_EARLY, and bit 3 of the ERROR register SOF_LATE indicate the number of pixels received between the latest and the preceding Start-Of-Frame (SOF) differ from the value programmed into the ACTIVE_SIZE register. If the value was provided by the Video Timing Controller core, read out ACTIVE_SIZE register value from the VTC core again, and make sure that the TIMING_LOCKED flag is set in the VTC core. Otherwise, using Chipscope, measure the number EOL pulses between subsequent SOF pulses.

Table C-2: Troubleshooting AXI4-Stream Interface

Symptom	Solution
s_axis_video_tready stuck low, the upstream core cannot send data.	During initialization, line-, and frame-flushing, the Gamma Correction core keeps its s_axis_video_tready input low. Afterwards, the core should assert s_axis_video_tready automatically. Is m_axis_video_tready low? If so, the Gamma Correction core cannot send data downstream, and the internal FIFOs are full.
m_axis_video_tvalid stuck low, the downstream core is not receiving data	<ol style="list-style-type: none"> No data is generated during the first two lines of processing. If the programmed active number of pixels per line is radically smaller than the actual line length, the core drops most of the pixels waiting for the (s_axis_video_tlast) End-of-line signal. Check the ERROR register.
Generated SOF signal (m_axis_video_tuser0) signal misplaced.	Check the ERROR register.
Generated EOL signal (m_axis_video_tlast) signal misplaced.	Check the ERROR register.
Data samples lost between Upstream core and the Gamma Correction core. Inconsistent EOL and/or SOF periods received.	<ol style="list-style-type: none"> Are the Master and Slave AXI4-Stream interfaces in the same clock domain? Is proper clock-domain crossing logic instantiated between the upstream core and the Gamma Correction core (Asynchronous FIFO)? Did the design meet timing? Is the frequency of the clock source driving the Gamma ACLK pin lower than the reported Fmax reached?
Data samples lost between Downstream core and the Gamma Correction core. Inconsistent EOL and/or SOF periods received.	<ol style="list-style-type: none"> Are the Master and Slave AXI4-Stream interfaces in the same clock domain? Is proper clock-domain crossing logic instantiated between the upstream core and the Gamma Correction core (Asynchronous FIFO)? Did the design meet timing? Is the frequency of the clock source driving the Gamma ACLK pin lower than the reported Fmax reached?

If the AXI4-Stream communication is healthy, but the data seems corrupted, the next step is to find the correct configuration for the Gamma Correction core.

Debugging Features

The Gamma Correction core is equipped with optional debugging features which aim to accelerate system bring-up, optimize memory and data-path architecture and reduce time to market. The optional debug features can be turned on/off via the **Include Debug Features** checkbox on the GUI when an AXI4-Lite interface is present. Turning off debug features reduces the core Slice footprint.

Core Bypass Option

The bypass option facilitates establishing a straight through connection between input (AXI4-Stream slave) and output (AXI4-Stream master) interfaces bypassing any processing functionality.

Flag `BYPASS` (bit 4 of the `CONTROL` register) can turn bypass on (1) or off, when the core instance Debugging Features were enabled at generation. Within the IP this switch controls multiplexers in the AXI4-Stream path.

In bypass mode the Gamma Correction core processing function is bypassed, and the core repeats AXI4-Stream input samples on its output. In bypass mode sensor samples are presented via the Green component output, while Red and Blue component outputs are set to zero.

Starting a system with all processing cores set to bypass, then by turning bypass off from the system input towards the system output allows verification of subsequent cores with known good stimuli.

Built in Test-Pattern Generator

The optional built-in test-pattern generator facilitates to temporarily feed the output AXI4-Stream master interface with a predefined pattern.

Flag `TEST_PATTERN` (bit 5 of the `CONTROL` register) can turn test-pattern generation on (1) or off, when the core instance Debugging Features were enabled at generation. Within the IP this switch controls multiplexers in the AXI4-Stream path, switching between the regular core processing output and the test-pattern generator. When enabled, a set of counters generate 256 scan-lines of color-bars, each color bar 64 pixels wide, repetitively cycling through Black, Red, Green, Yellow, Blue, Magenta, Cyan, and White colors till the end of each scan-line. After the Color-Bars segment, the rest of the frame is filled with a monochrome horizontal and vertical ramp.

Starting a system with all processing cores set to test-pattern mode, then by turning test-pattern generation off from the system output towards the system input allows successive bring-up and parameterization of subsequent cores.

Throughput Monitors

Throughput monitors enable the user to monitor processing performance within the core. This information can be used to help debug frame-buffer bandwidth limitation issues, and if possible, allow video application software to balance memory pathways.

Often times video systems, with multiport access to a shared external memory, have different processing islands. For example a pre-processing sub-system working in the input video clock domain may clean up, transform, and write a video stream, or multiple video

streams, to memory. The processing sub-system may read the frames out, process, scale, encode, then write frames back to the frame buffer, in a separate processing clock domain. Finally, the output sub-system may format the data and read out frames locked to an external clock.

Typically, access to external memory using a multiport memory controller involves arbitration between competing streams. However, to maximize the throughput of the system, different memory ports may need different specific priorities. To fine tune the arbitration and dynamically balance frame rates, it is beneficial to have access to throughput information measured in different video data paths.

The SYSDEBUG0 (0x0014), or Frame Throughput Monitor, register indicates the number of frames processed since power-up or the last time the core was reset. The SYSDEBUG1 (0x0018), or Line Throughput Monitor, register indicates the number of lines processed since power-up or the last time the core was reset. The SYSDEBUG2 (0x001C), or Pixel Throughput Monitor, register indicates the number of pixels processed since power-up or the last time the core was reset.

Priorities of memory access points can be modified by the application software dynamically to equalize frame, or partial frame rates.

Interfacing to Third-Party IP

[Table C-3](#) describes how to troubleshoot third-party interfaces.

Table C-3: Troubleshooting Third-Party Interfaces

Symptom	Solution
Severe color distortion or color-swap when interfacing to third-party video IP.	<p>Verify that the color component logical addressing on the AXI4-Stream TDATA signal is in according to Data Interface in Chapter 2. If misaligned:</p> <p>In HDL, break up the TDATA vector to constituent components and manually connect the slave and master interface sides.</p> <p>In EDK, create a new vector for the slave side TDATA connection. In the MPD file, manually assign components of the master-side TDATA vector to sections of the new vector.</p>
Severe color distortion or color-swap when processing video written to external memory using the AXI-VDMA core.	<p>Unless the particular software driver was developed with the AXI4-Stream TDATA signal color component assignments described in Data Interface in Chapter 2 in mind, there are no guarantees that the software will correctly identify bits corresponding to color components.</p> <p>Verify that the color component logical addressing TDATA is in alignment with the data format expected by the software drivers reading/writing external memory. If misaligned:</p> <p>In HDL, break up the TDATA vector to constituent components, and manually connect the slave and master interface sides.</p> <p>In EDK, create a new vector for the slave side TDATA connection. In the MPD file, manually assign components of the master-side TDATA vector to sections of the new vector.</p>

Application Software Development

Programmer Guide

The software API is provided to allow easy access to the Gamma AXI4-Lite registers defined in [Table 2-12](#). To utilize the API functions, the following two header files must be included in the user C code:

```
#include "gamma.h"
#include "xparameters.h"
```

The hardware settings of your system, including the base address of your Gamma Correction core, are defined in the `xparameters.h` file. The `gamma.h` file contains the macro function definitions for controlling the Gamma pCore.

For examples on API function calls and integration into a user application, the `drivers` subdirectory of the pCore contains a file, `example.c`, in the `gamma_v5_00_a/example` subfolder. This file is a sample C program that demonstrates how to use the Gamma pCore API.

Table D-1: Gamma Driver Function Definitions

Function Name and Parameterization	Description
GAMMA_Enable (uint32 BaseAddress)	Enables a Gamma instance.
GAMMA_Disable (uint32 BaseAddress)	Disables a Gamma instance.
GAMMA_Reset (uint32 BaseAddress)	Immediately resets a Gamma instance. The core stays in reset until the RESET flag is cleared.
GAMMA_ClearReset (uint32 BaseAddress)	Clears the reset flag of the core, which allows it to re-sync with the input video stream and return to normal operation.
GAMMA_AutoSynchReset (uint32 BaseAddress)	Resets a Gamma instance at the end of the current frame being processed, or immediately if the core is not currently processing a frame.
GAMMA_ReadReg (uint32 BaseAddress, uint32 RegOffset)	Returns the 32-bit unsigned integer value of the register. Read the register selected by RegOffset (defined in Table 2-12).

Table D-1: Gamma Driver Function Definitions

Function Name and Parameterization	Description
GAMMA_WriteReg (uint32 BaseAddress, uint32 RegOffset, uint32 Data)	Write the register selected by RegOffset (defined in Table 2-12). Data is the 32-bit value to write to the register.
GAMMA_RegUpdateEnable (uint32 BaseAddress)	Enables copying double buffered registers at the beginning of the next frame. Refer to Double Buffering for more information.
GAMMA_RegUpdateDisable (uint32 BaseAddress)	Disables copying double buffered registers at the beginning of the next frame. Refer to Double Buffering for more information.

Software Reset

Software reset reinitializes registers of the AXI4-Lite control interface to their initial value, resets FIFOs, forces `m_axis_video_tvalid` and `s_axis_video_tready` to 0.

`GAMMA_Reset()` and `GAMMA_AutoSyncReset()` reset the core immediately if the core is not currently processing a frame. If the core is currently processing a frame calling `GAMMA_Reset()`, or setting bit 30 of the `CONTROL` register to 1 will cause image tearing. After calling `GAMMA_Reset()`, the core remains in reset until `GAMMA_ClearReset()` is called.

Calling `GAMMA_AutoSyncReset()` automates this reset process by waiting until the core finishes processing the current frame, then asserting the reset signal internally, keeping the core in reset only for 32 `ACLK` cycles, then deasserting the signal automatically. After calling `GAMMA_AutoSyncReset()`, it is not necessary to call `GAMMA_ClearReset()` for the core to return to normal operating mode.



IMPORTANT: *Calling `GAMMA_AutoSyncReset()` does not guarantee prompt, or real-time resetting of the core. If the AXI4-Stream communication is halted mid frame, the core will not reset until the upstream core finishes sending the current frame or starts a new frame.*

Double Buffering

Registers `TABLE_UPDATE` and `ACTIVE_SIZE` are double-buffered to ensure no image tearing happens if values are modified during frame processing. Values from the AXI4-Lite interface are latched into processor registers immediately after writing, and processor register values are copied into the active register set at the Start Of Frame (SOF) signal. Double-buffering decouples AXI4-Lite register updates from the AXI4-Stream processing, allowing software a large window of opportunity to update processing parameter values without image tearing.

If multiple register values are changed during frame processing, simple double buffering would not guarantee that all register updates would take effect at the beginning of the same frame. Using a semaphore mechanism, the `RegUpdateEnable()` and

RegUpdateDisable() functions allows synchronous commitment of register changes. The Gamma Correction core will start using the updated ACTIVE_SIZE and TABLE_UPDATE values only if the REGUPDATE flag of the CONTROL register is set (1), after the next Start-Of-Frame signal (s_axis_video_tuser0) is received. Therefore, it is recommended to disable the register update before writing multiple double-buffered registers, then enable register update when register writes are completed.

Reading and Writing Registers

Each software register that is defined in Table 2-12 has a constant that is defined in gamma.h which is set to the offset for that register listed in Table D-2. It is recommended that the application software uses the predefined register names instead of register values when accessing core registers, so future updates to the Gamma drivers which may change register locations will not affect the application dependent on the Gamma driver.



RECOMMENDED: *It is recommended that the application software uses the predefined register names instead of register values when accessing core registers, so future updates to the Gamma drivers which may change register locations will not affect the application dependent on the Gamma driver.*

Table D-2: Predefined Constants Defined in gamma.h

Constant Name Definition	Value	Target Register
GAMMA_CONTROL	0x0000	CONTROL
GAMMA_STATUS	0x0004	STATUS
GAMMA_ERROR	0x0008	ERROR
GAMMA_IRQ_ENABLE	0x000C	IRQ_ENABLE
GAMMA_VERSION	0x0010	VERSION
GAMMA_SYSDEBUG0	0x0014	SYSDEBUG0
GAMMA_SYSDEBUG1	0x0018	SYSDEBUG1
GAMMA_SYSDEBUG2	0x001C	SYSDEBUG2
GAMMA_ACTIVE_SIZE	0x0020	ACTIVE_SIZE
GAMMA_TABLE_UPDATE	0x0100	TABLE_UPDATE
GAMMA_ADDR_DATA	0x0104	ADDR_DATA

Additional Resources

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see the Xilinx Support website at:

<http://www.xilinx.com/support>.

For a glossary of technical terms used in Xilinx documentation, see:

http://www.xilinx.com/support/documentation/sw_manuals/glossary.pdf.

For a comprehensive listing of Video and Imaging application notes, white papers, reference designs and related IP cores, see the Video and Imaging Resources page at:

http://www.xilinx.com/esp/video/refdes_listing.htm#ref_des.

Solution Centers

See the [Xilinx Solution Centers](#) for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

References

These documents provide supplemental material useful with this user guide:

1. [UG761 AXI Reference Guide](#)
2. Vivado™ Design Suite user documentation (www.xilinx.com/cgi-bin/docs/rdoc?v=2012.3;t=vivado+docs)

Technical Support

Xilinx provides technical support at www.xilinx.com/support for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled DO NOT MODIFY.

See the IP Release Notes Guide ([XTP025](#)) for more information on this core. For each core, there is a master Answer Record that contains the Release Notes and Known Issues list for the core being used. The following information is listed for each version of the core:

- New Features
- Resolved Issues
- Known Issues

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
10/19/2011	1.0	Initial Xilinx release of Product Guide, replacing DS719 and UG829.
4/24/2012	2.0	Updated for core version. Added Zynq-7000 devices, added AXI4-Stream interfaces, deprecated GPP interface.
07/25/2012	3.0	Updated for core version. Added Vivado information.
10/16/2012	3.1	Updated for core version. Added Vivado test bench.

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