Motion Adaptive Noise Reduction v5.01a

Product Guide

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Introduction

The Xilinx® LogiCORE™ IP Motion Adaptive Noise Reduction (MANR) is a module for both motion detection and motion adaptive noise reduction in video systems. The core allows the motion detection function to be used independently of the noise reduction function for applications where noise reduction is not needed. The noise reduction algorithm is implemented as a recursive temporal filter with a user programmable transfer function allowing the user to control both the shape of the motion transfer and the strength of the noise reduction applied.

The motion transfer function is initialized according to the settings in the CORE Generator™ tool, Vivado IP catalog, or Xilinx Platform Studio, but is also programmable at runtime via the register interface.

Features

- Programmable register control.
- Optional AXI4-Lite Dynamic Control interface or fixed-mode operation.
- Selectable and programmable motion transfer function (MTF).
  - Five pre-loaded MTF curves: none, weak, medium, strong, and aggressive.
  - Supports user-defined MTF functions.
- Full support for interrupts and status registers for easy system control.
- Supports YUV 4:2:2, 4:2:0 at 8 bits per pixel.
- Gives calculated Y/C motion data output for optional use by downstream IP.
- Supports spatial resolutions from 32x32 to 4096x4096.
  - Supports 1080P60 in all supported device families (1)

1. Performance on low power devices may be lower.

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family(1)	Zynq™-7000 (2), Artix™-7, Virtex®-7, Kintex®-7, Virtex-6, Spartan®-6
Supported User Interfaces	AXI4-Lite, AXI4-Stream
Resources	See Table 2-1 through Table 2-10.
Provided with Core	
Documentation	Product Guide
Design Files	ISE: NGC netlist, Encrypted HDL Vivado: Encrypted RTL
Example Design	Not Provided
Test Bench	Verilog (4)
Constraints File	Not Provided
Simulation Models	VHDL or Verilog Structural, C-Model (4)
Tested Design Tools	
Design Entry Tools	CORE Generator™ tool, Vivado™ Design Suite (6), Xilinx® Platform Studio (XPS)
Simulation(5)	Mentor Graphics ModelSim, Xilinx ISim
Synthesis Tools	Xilinx Synthesis Technology (XST) Vivado Synthesis
Support	
Provided by Xilinx, Inc.	

1. For a complete listing of supported devices, see the release notes for this core.
2. Supported in ISE® Design Suite implementations only.
3. Video Protocol as defined in UG761, *Xilinx AXI Reference Guide* [Ref 3].
4. HDL test bench and C-Model available on the product page on Xilinx.com at www.xilinx.com/products/intellectual-property/EF-DI-IMG-MA-NOISE.htm.
5. For the supported versions of the tools, see the Xilinx Design Tools: Release Notes Guide.
6. Supports only 7 series devices.

Overview

Noise reduction is a common function in video systems and can be used to clean up sensor artifacts or other types of noise present in most video systems. In addition, many surveillance systems and other analytical video processing systems need real-time motion information to provide intelligent processing such as object detection and tracking or camera tampering detection. The MANR core provides both of these capabilities in a single, efficient implementation.

Noise reduction is achieved by recursively combining the current pixel values and a percentage of the previous pixel values. Large changes in pixel values between successive frames likely indicate motion, and should be preserved in the output frame. Smaller changes are more likely caused by noise in the current frame, therefore averaging with pixel values from the previous can be applied to suppress noise. This recursive action effectively reduces noise while preserving the output image content by masking small changes but preserving larger pixel changes.

The core uses pixel values from the current and previous frames as inputs from which temporal differences are established on a pixel-by-pixel basis. The absolute value of the inter-frame difference is used as an argument to a grading function, the motion-transfer-function (MTF). The function value corresponding to the absolute difference is used as a blending factor between the current pixel value and the previous pixel value. This temporal IIR structure allows core to generate optimal output values where temporal noise is reduced, but motion is conserved.

The grading, or MTF is programmable in the MANR core. Typically, the function maps the smaller pixel-differences, likely to be noise, to large blending factor values. Conversely, larger pixel-differences, likely to be motion, are mapped to small blending factor values. The blending factor controls what portion of an output pixel comes from the previous frame, and what is carried forward from the current frame.

Feature Summary

The MANR core supports resolutions of up to 4096x4096 using 8-bit YC4:2:0 or YC4:2:2 chroma formats. The core GUI provides five preset MANR strengths which correspond to preset MTFs. Also, the software driver provided with the EDK version of this core includes the five MTF strengths and allows the user to load them using the software. The core also supports loading a user-defined MTF into the core using the processor interface.

The MANR core uses two AXI4-Stream input (slave) interfaces in parallel: one for the current frame and one for the previous frame. Typically, the current frame will be provided from a live source or an AXI VDMA. The previous frame typically originates from a frame buffer, usually connected to the AXI-VDMA core. The core processes 8 bit video data in YCC 422 format only.

To dynamically change the noise reduction strength on a frame-by-frame basis, a processor interface is required. When generating the MANR core, the user has the option of including a processor interface that is instantiated in the core.

Applications

- Video Surveillance
- Industrial Imaging
- Video Conferencing
- Machine Vision

Licensing and Ordering Information

This Xilinx® LogiCORE™ IP module is provided under the terms of the Xilinx Core License Agreement. The module is shipped as part of the Vivado Design Suite/ISE Design Suite. For full access to all core functionalities in simulation and in hardware, you must purchase a license for the core. Contact your local Xilinx sales representative for information about pricing and availability.

For more information, please visit the LogiCORE IP Motion Adaptive Noise Reduction product page.

Information about other Xilinx LogiCORE IP modules is available at the Xilinx Intellectual Property page. For information on pricing and availability of other Xilinx LogiCORE IP modules and tools, contact your local Xilinx sales representative.

Product Specification

The Motion Adaptive Noise Reduction LogiCORE™ IP can be used as either a stand-alone core or as peripheral to a processor system. An optional AXI4-Lite interface with user registers, interrupts and device driver make the Motion Adaptive Noise Reduction module highly programmable and easy to control in real-time with a processor.

Standards Compliance

The MANR core is compliant with the AXI4-Stream Video Protocol and AXI4-Lite interconnect standards. See *Video IP: AXI Feature Adoption* section of the *AXI Reference Guide (UG761)*[Ref 3] for additional information.

Performance

For the MANR to process a complete 720p60 or 1080p30 frame within one frame period, the internal clock must be run at least at the pixel rate, or 74.25 MHz. For the MANR to process a complete 1080p60 frame within one frame period, the internal clock must be run at least at the pixel rate, or 148.5 MHz.

Maximum Frequency

This section contains typical clock frequencies for the target devices. These figures are typical, and have been used as target clock frequencies for the MANR in the slowest speed-grade for each device family. The figures apply to the main operation clock signal `aclk`.

The maximum achievable clock frequency can vary depending on configuration.

Latency

The latency through the MANR core is fixed at 26 clock cycles. This measures the number of cycles between a value being clocked into the core and its equivalent data being delivered on the core output.

This latency does not take back-pressure exerted on the MANR core into account.

Throughput

The MANR core produces as much data as it consumes. If timing constraints are met, the throughput is equal to the rate at which video data is written into the core. In numeric terms, 1080P/60 YC4:2:2 represents an average data rate of 124.4 Mpixels/sec, or a burst data rate of 148.5 Mpixels/sec.

Resource Utilization

For an accurate measure of the usage of primitives, slices, and CLBs for a particular instance, check the **Display Core Viewer after Generation** check box in the CORE Generator™ interface. To help guide the user making system-level and board-level decisions, Table 2-1 through Table 2-10 show the resource usage observed for the MANR for all supported devices in either Vivado™ Design Suite 2012.4 or ISE® Design Suite 14.4, as noted. This post-PAR characterization data has been collated through automated implementation of each configuration. Results will vary between implementations, and is intended as a guideline. Resource count and Fmax values are independent of the actual and supported maximum video resolution, as well as the Noise Reduction value selected in the GUI.

Note: Performance (FMax) on Zynq™-7020, Zynq-7010 and low-power (-L) devices may be lower than quoted in Table 2-1 through Table 2-10.

Table 2-1: **Resources and Performance for Zynq-7000 Devices, Vivado Design Suite**

AXI4-Lite	LUTs	FFs	BRAM36	BRAM18	DSP48	FMax (MHz) Per Speed Grade		
						-1	-2	-3
No	885	878	0	1	3	258	296	336
Yes	1158	1440	0	1	3	258	296	336

Notes:

1. Speedfile: XC7Z045 FFG676 (ADVANCED 1.04a 2012-11-02)

Table 2-2: **Resources and Performance for Zynq-7000 Devices, ISE Design Suite**

AXI4-Lite	LUTs	FFs	BRAM36	BRAM18	DSP48	FMax (MHz) Per Speed Grade		
						-1	-2	-3
No	1005	797	0	1	3	172	212	234
Yes	1376	1350	0	1	3	172	212	234

Notes:

1. Speedfile: XC7Z045 FFG676 (ADVANCED 1.04b 2012-11-19)

Table 2-3: **Resources and Performance for Virtex®-7 Devices, Vivado Design Suite**

AXI4-Lite	LUTs	FFs	BRAM36s	BRAM18s	DSP48s	FMax (MHz) Per Speed Grade		
						-1	-2	-3
No	885	878	0	1	2	250	296	344
Yes	1158	1440	0	1	2	250	296	344

Notes:

1. Speedfile: XC7V585T FFG1157 (PRODUCTION 1.08b 2012-11-02)

Table 2-4: **Resources and Performance for Virtex-7 Devices, ISE Design Suite**

AXI4-Lite	LUTs	FFs	BRAM36s	BRAM18s	DSP48s	FMax (MHz) Per Speed Grade		
						-1	-2	-3
No	1004	791	0	1	3	172	226	226
Yes	1370	1344	0	1	3	172	226	226

Notes:

1. Speedfile: XC7V585T FFG1157 (PRODUCTION 1.08c 2012-11-19)

Table 2-5: **Resources and Performance for Kintex™-7 Devices, Vivado Design Suite**

AXI4-Lite	LUTs	FFs	BRAM36s	BRAM18s	DSP48s	FMax (MHz) Per Speed Grade		
						-1	-2	-3
No	886	878	0	1	2	250	N/A	344
Yes	1155	1440	0	1	2	250	N/A	344

Notes:

1. Speedfile: XC7K70T FBG484 (ADVANCED 1.08a 2012-10-21)

Table 2-6: **Resources and Performance for Kintex-7 Devices, ISE Design Suite**

AXI4-Lite	LUTs	FFs	BRAM36s	BRAM18s	DSP48s	FMax (MHz) Per Speed Grade		
						-1	-2	-3
No	997	791	0	1	3	172	219	234
Yes	1372	1344	0	1	3	172	219	234

Notes:

1. Speedfile: XC7K70T FBG484 (ADVANCED 1.08b 2012-11-19)

Table 2-7: **Resources and Performance for Artix™-7 Devices, Vivado Design Suite**

AXI4-Lite	LUTs	FFs	BRAM36s	BRAM18s	DSP48s	FMax (MHz) Per Speed Grade		
						-1	-2	-3
No	884	878	0	1	2	204	234	266
Yes	1156	1440	0	1	2	204	234	266

Notes:

1. Speedfile: XC7A100T FFG484 (ADVANCED 1.06c 2012-11-02)

Table 2-8: **Resources and Performance for Artix-7 Devices, ISE Design Suite**

AXI4-Lite	LUTs	FFs	BRAM36s	BRAM18s	DSP48s	FMax (MHz) Per Speed Grade		
						-1	-2	-3
No	1004	786	0	1	3	110	148	156
Yes	1256	1344	0	1	3	110	148	156

Notes:

1. Speedfile: XC7A100T FFG484 (ADVANCED 1.06e 2012-11-19)

Table 2-9: **Resources and Performance for Virtex-6 Devices, ISE Design Suite**

AXI4-Lite	LUTs	FFs	BRAM36s	BRAM18s	DSP48s	FMax (MHz) Per Speed Grade		
						-1	-2	-3
No	991	797	0	1	3	156	180	196
Yes	1293	1350	0	1	3	156	180	196

Notes:

1. Speedfile: XC6VLX75T FF484 (PRODUCTION 1.17 2012-11-19)

Table 2-10: **Resources and Performance for Spartan®-6 Devices, ISE Design Suite**

AXI4-Lite	LUTs	FFs	BRAM36s	BRAM18s	DSP48s	FMax (MHz) Per Speed Grade		
						-1	-2	-3
No	984	795	0	1	3	N/A	110	125
Yes	1316	1347	0	1	3	N/A	110	125

Notes:

1. Speedfile: XC6SLX25 FGG484 (PRODUCTION 1.23 2012-11-19)

Port Descriptions

The MANR core uses industry standard control and data interfaces to connect to other system components. The following sections describe the various interfaces available with the core. Figure 2-1 illustrates an I/O diagram of the MANR core. Some signals are optional and not present for all configurations of the core. The AXI4-Lite interface and the IRQ pin are present only when the core is configured through the GUI with an AXI4-Lite control interface. The INTC_IF interface is present only when the core is configured through the GUI with the INTC interface enabled.

Core Interfaces

The MANR core includes control interfaces and data interfaces, as described in this section. These interfaces and signals are shown in Figure 2-1.

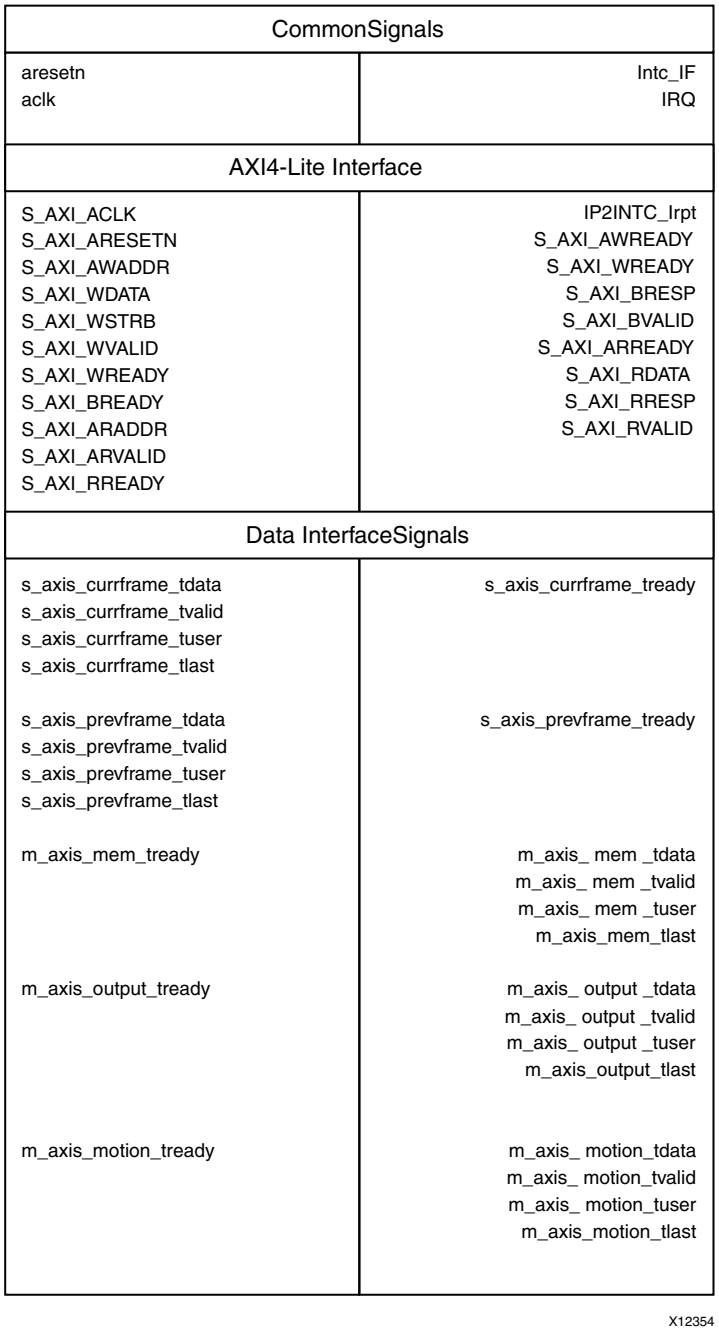

Figure 2-1: **MANR Interfaces and Signals**

Common Interface Signals

Table 2-11 summarizes the signals which are either shared by, or not part of the dedicated AXI4-Stream data or AXI4-Lite control interfaces.

Table 2-11: **Common Interface Signals**

Signal Name	Direction	Width	Description
ACLK	In	1	Video Core Clock
ARESETn	In	1	Video Core Active Low Synchronous Reset
INTC_IF	Out	31	Optional external interrupt controller interface. Available only when INTC_IF is selected in the GUI.
IRQ	Out	1	Optional interrupt request pin. Available only when INTC_IF is selected in the GUI.

The ACLK and ARESETn signals are shared between the core and the AXI4-Stream data interfaces. The AXI4-Lite control interface has its own set of clock, clock enable and reset pins: S_AXI_ACLK and S_AXI_ARESETn. See Interrupt Subsystem for a description of the INTC_IF and IRQ pins.

ACLK

The AXI4-Stream interface must be synchronous to the core clock signal ACLK. All AXI4-Stream interface input signals are sampled on the rising edge of ACLK. All AXI4-Stream output signal changes occur after the rising edge of ACLK. The AXI4-Lite interface is unaffected by the ACLK signal.

ARESETn

The ARESETn pin is an active-low, synchronous reset input pertaining to only AXI4-Stream interfaces. The core resets on the next rising ACLK edge after ARESETN is asserted low. The ARESETn signal must be synchronous to the ACLK and must be held low for a minimum of 32 clock cycles of the slowest clock. The AXI4-Lite interface is unaffected by the ARESETn signal.

Data Interface

The core receives and transmits data using AXI4-Stream interfaces that implement a video protocol as defined in *Xilinx AXI Reference Guide (UG761)*[Ref 3], Video IP: "AXI Feature Adoption."

AXI4-Stream Signal Names and Descriptions

Table 2-12 describes the AXI4-Stream signal names and descriptions

Table 2-12: **AXI4-Stream Data Interface Signal Descriptions**

Signal Name	Direction	Width	Description
s_axis_currframe_tdata	In	16	Current frame input video data
s_axis_currframe_tvalid	In	1	Current frame input video valid signal
s_axis_currframe_tready	Out	1	Current frame input ready

Table 2-12: **AXI4-Stream Data Interface Signal Descriptions *(Cont'd)***

Signal Name	Direction	Width	Description
s_axis_currframe_tuser	In	1	Current frame input video Start-of-Frame signal
s_axis_currframe_tlast	In	1	Current frame input video End-of-Line signal
s_axis_prevframe_tdata	In	16	Previous frame input video data
s_axis_prevframe_tvalid	In	1	Previous frame input video valid signal
s_axis_prevframe_tready	Out	1	Previous frame input ready
s_axis_prevframe_tuser	In	1	Previous frame input video Start-of-Frame signal
s_axis_prevframe_tlast	In	1	Previous frame input video End-of-Line signal
m_axis_output_tdata	Out	16	Downstream video output data
m_axis_output_tvalid	Out	1	Downstream video output valid signal
m_axis_output_tready	In	1	Downstream video output ready
m_axis_output_tuser	Out	1	Downstream video output Start-of-Frame signal
m_axis_output_tlast	Out	1	Downstream video output End-of-Line signal
m_axis_mem_tdata	Out	16	Memory (temporal feedback) video output data
m_axis_mem_tvalid	Out	1	Memory (temporal feedback) video output valid signal
m_axis_mem_tready	In	1	Memory (temporal feedback) video output ready
m_axis_mem_tuser	Out	1	Memory (temporal feedback) video output Start-of-Frame signal
m_axis_mem_tlast	Out	1	Memory (temporal feedback) video output End-of-Line signal
m_axis_motion_tdata	Out	16	Motion output data
m_axis_motion_tvalid	Out	1	Motion output valid signal
m_axis_motion_tready	In	1	Motion output ready
m_axis_motion_tuser	Out	1	Motion output Start-of-Frame signal
m_axis_motion_tlast	Out	1	Motion output End-of-Line signal

Video Data

The MANR core processes 8-bit YCC 422 data only. The corresponding AXI4-Stream TDATA width is fixed at 16 bits to accommodate 8 Luma and 8 bits Chroma.

READY/VALID Handshake

A valid transfer occurs whenever READY, VALID, and ARESETn are high at the rising edge of ACLK, as seen in Figure 2-2. During valid transfers, DATA only carries active video data. Blank periods and ancillary data packets are not transferred via the AXI4-Stream video protocol.

Note: When interfacing to an AXI4-Stream master interface using an ACLKEN input, which is not permanently tied high, the two interfaces must be connected using the AXI4 FIFO core to avoid data corruption. See the *LogiCORE IP FIFO Generator Product Guide (PG057)*[Ref 2].

Guidelines on Driving VALID into Slave (Data Input) Interfaces

Once VALID is asserted, no interface signals except the core's driving READY output may change value until the transaction completes (READY, VALID high on the rising edge of ACLK). Once asserted, VALID may only be de-asserted after a transaction has completed. Transactions may not be retracted or aborted. In any cycle following a transaction, VALID can either be de-asserted or remain asserted to initiate a new transfer.

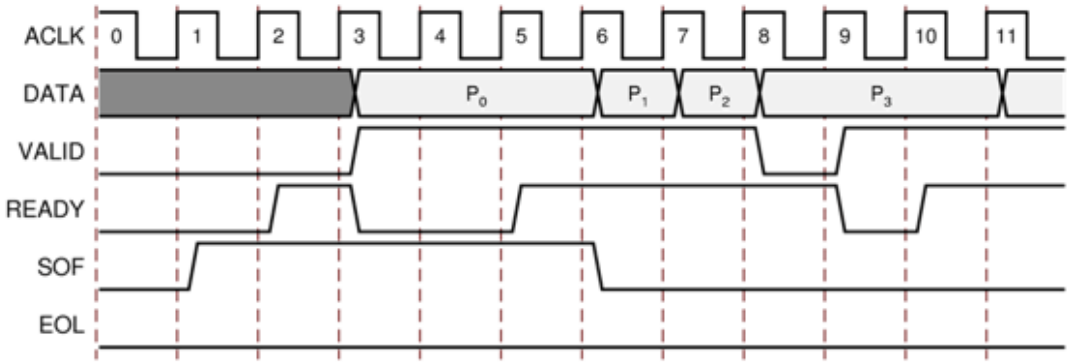

Figure 2-2: **Example of READY/VALID Handshake, Start of a New Frame**

Guidelines on Driving READY into Master (Data Output) Interfaces.

The READY signal may be asserted before, during or after the cycle in which the core asserted VALID. The assertion of READY may be dependent on the value of VALID. A slave that can immediately accept data qualified by this VALID signal should pre-assert its slave TREADY signal until data is received.

Alternatively, READY can be registered and driven the cycle following VALID assertion. It is recommended that the AXI4-Stream slave should drive READY independently, or pre-assert READY to minimize latency.

Start of Frame Signals: m_axis_video_tuser0, s_axis_video_tuser0

The Start-Of-Frame (SOF) signal, physically transmitted over the AXI4-Stream TUSER0 signal, marks the first pixel of a video frame. The SOF pulse is one valid transaction wide,

and must coincide with the first pixel of the frame, as seen in Figure 2-2. SOF serves as a frame synchronization signal, which allows downstream cores to re-initialize, and detect the first pixel of a frame. The SOF signal can be asserted an arbitrary number of ACLK cycles before the first pixel value is presented on TDATA, as long as a VALID is not asserted.

End of Line Signals: m_axis_video_tlast, s_axis_video_tlast

The End-Of-Line (EOL) signal, physically transmitted over the AXI4-Stream TLAST signal, marks the last pixel of a line. The EOL pulse is one valid transaction wide, and must coincide with the last pixel of a scan-line, as seen in Figure 2-3.

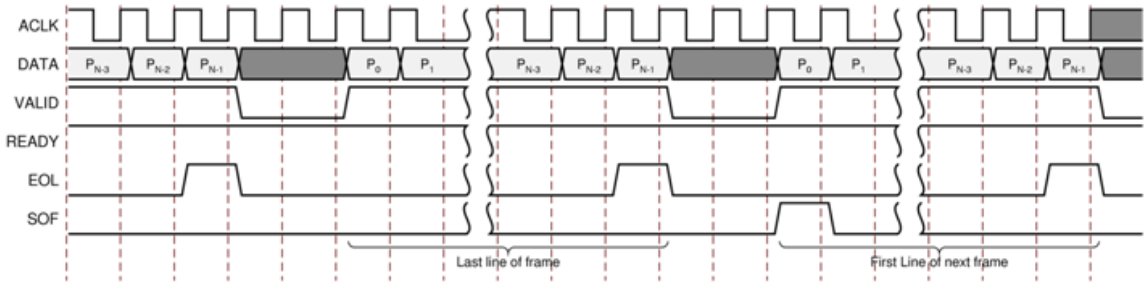

Figure 2-3: **Use of EOL and SOF Signals**

Control Interface

When configuring the core, there is an option to add an AXI4-Lite register interface to dynamically control the behavior of the core. The AXI4-Lite slave interface facilitates integrating the core into the processor system along with other AXI4-Lite compliant IP.

In a static configuration with a fixed set of parameters (constant (fixed-mode) configuration), the core can be instantiated without the AXI4-Lite control interface, which reduces the core footprint.

Constant Configuration

The constant configuration caters to users who will interface the core to a fixed input video source. In constant configuration, parameters such as the image resolution (number of active pixels per scan line and the number of active scan lines per frame) and the Noise-Reduction strength are hard coded into the core through the CORE GeneratorGUI. Because there is no AXI4-Lite interface, the core is not programmable, but can be reset using the ARESETn port.

AXI4-Lite Interface

The AXI4-Lite interface enables dynamic control of parameters within the core. Core configuration can be accomplished using an AXI4-Stream master state machine, or an embedded ARM or soft system processor such as a MicroBlaze processor. The core can be

controlled through the AXI4-Lite interface using read and write transactions to the register space. The AXI4-Lite interface signals are listed in Table 2-13.

Table 2-13: **AXI4-Lite Control Bus Signals**

Name	Direction	Description
S_AXI_AWADDR	In	AXI4-Lite Write Address Bus. The write address bus gives the address of the write transaction.
S_AXI_AWVALID	In	AXI4-Lite Write Address Channel Write Address Valid. This signal indicates that valid write address is available. 1 = Write address is valid. 0 = Write address is not valid.
S_AXI_AWREADY	Out	AXI4-Lite Write Address Channel Write Address Ready. Indicates core is ready to accept the write address. 1 = Ready to accept address. 0 = Not ready to accept address.
S_AXI_WDATA	In	AXI4-Lite Write Data Bus
S_AXI_WSTRB	In	AXI4-Lite Write Strobes. This signal indicates which byte lanes to update in memory.
S_AXI_WVALID	In	AXI4-Lite Write Data Channel Write Data Valid. This signal indicates that valid write data and strobes are available. 1 = Write data/strobes are valid. 0 = Write data/strobes are not valid.
S_AXI_WREADY	Out	AXI4-Lite Write Data Channel Write Data Ready. Indicates core is ready to accept the write data. 1 = Ready to accept data. 0 = Not ready to accept data.
S_AXI_BRESP(2)	Out	AXI4-Lite Write Response Channel. Indicates results of the write transfer. 00b = OKAY - Normal access has been successful. 01b = EXOKAY - Not supported. 10b = SLVERR - Error. 11b = DECERR - Not supported.
S_AXI_BVALID	Out	AXI4-Lite Write Response Channel Response Valid. Indicates response is valid. 1 = Response is valid. 0 = Response is not valid.
S_AXI_BREADY	In	AXI4-Lite Write Response Channel Ready. Indicates Master is ready to receive response. 1 = Ready to receive response. 0 = Not ready to receive response.
S_AXI_ARADDR	In	AXI4-Lite Read Address Bus. The read address bus gives the address of a read transaction.
S_AXI_ARVALID	In	AXI4-Lite Read Address Channel Read Address Valid. 1 = Read address is valid. 0 = Read address is not valid.

Table 2-13: **AXI4-Lite Control Bus Signals *(Cont'd)***

Name	Direction	Description
S_AXI_ARREADY	Out	AXI4-Lite Read Address Channel Read Address Ready. Indicates core is ready to accept the read address. 1 = Ready to accept address. 0 = Not ready to accept address.
S_AXI_RDATA	Out	AXI4-Lite Read Data Bus
S_AXI_RRESP[(2)]	Out	AXI4-Lite Read Response Channel Response. Indicates results of the read transfer. 00b = OKAY - Normal access has been successful. 01b = EXOKAY - Not supported. 10b = SLVERR - Error. 11b = DECERR - Not supported.
S_AXI_RVALID	Out	AXI4-Lite Read Data Channel Read Data Valid. This signal indicates that the required read data is available and the read transfer can complete. 1 = Read data is valid. 0 = Read data is not valid.
S_AXI_RREADY	In	AXI4-Lite Read Data Channel Read Data Ready. Indicates master is ready to accept the read data. 1 = Ready to accept data. 0 = Not ready to accept data.

Register Space

The standardized Xilinx® Video IP register space is partitioned into control-, timing-, and core-specific registers, as described in Table 2-14.

Table 2-14: **MANR Registers**

Address (hex) BASEADDR +	Register Name	Access Type	Double Buffered	Default Value	Register description
0x0000	CONTROL	R/W	No	Pwr-on-Rst: 0x0	b0: SW_ENABLE b1: REG_UPDATE b2: MTF_BYPASS b30: FRAME_SYNC_RESET (1: reset) b31: SW_RESET (1: reset)
0x0004	STATUS	R/W	No	0	b0: MTF_LOAD_DONE b1: FRAME_STARTED b2: AXI4_SLAVE_ERROR
0x0008	ERROR	R/W	No	0	b0: curr_eol_error b2: curr_sof_error b4: prev_eol_error b6: prev_sof_error

Table 2-14: **MANR Registers *(Cont'd)***

Address (hex) BASEADDR +	Register Name	Access Type	Double Buffered	Default Value	Register description
0x000C	IRQ_ENABLE	R/W	No	0	b0: MTF_LOAD_DONE_IRQEN b1: FRAME_STARTED_IRQ_EN b2: AXI4_SLAVE_ERROR_IRQ_EN
0x0010	Version	R	No	0x0501a000	7-0: REVISION_NUMBER 11-8: PATCH_ID 15-12: VERSION_REVISION 23-16: VERSION_MINOR 31-24: VERSION_MAJOR
0x0014	(Reserved)	-	-	-	-
0x0018	(Reserved)	-	-	-	-
0x001C	(Reserved)	-	-	-	-
0x0020	(Reserved)	-	-	-	-
0x0100	FRAME_SIZE	R/W	Yes	Specified in GUI	12-0: Number of active pixels per line 28-16: Number of active lines per frame
0x0104	MTF_DIn	W	Yes (internal multiple -MTF memory)	0	7-0: MTF Input Data.
0x0108	MTF_Active	R/W	Yes	Specified in GUI	2-0: Internal MTF Bank currently in use by MANR core
0x010C	MTF_Write	R/W	Yes	0	2-0: Internal MTF Bank to which MTF_Din data will be written.

Control (0x0000) Register

- Bit 0 of the CONTROL register, SW_ENABLE, facilitates enabling and disabling the core from software. Writing '0' to this bit effectively disables the core halting further operations, which blocks the propagation of all video signals.

  For the AXI4-Lite interface, after Power up, or Global Reset, the SW_ENABLE defaults to 0. The SW_ENABLE flag is not synchronized with the AXI4-Stream interfaces: Enabling or Disabling the core takes effect immediately, irrespective of the core processing status.

- Bit 1 of the CONTROL register, REG_UPDATE is a semaphore for the host processor, which facilitates committing all updates to double-buffered user and timing registers simultaneously. One set of registers (the processor registers) is directly accessed by the processor interface, while the other set (the active set) is actively used by the core. New values written to the processor registers will get copied over to the active set at the end of the AXI4-Stream frame, if and only if REG_UPDATE is set at the start of a new frame,

indicated by the SOF signal. Setting REG_UPDATE to 0 before updating multiple register values, then setting REG_UPDATE to 1 when updates are completed ensures all registers are updated simultaneously at the frame boundary without causing image tearing.

- Bit 2 of the CONTROL register is the MTF_BYPASS control bit. When this bit is set, noise-reduction is turned off.
- Bit 31 of the CONTROL register, SW_RESET facilitates software reset. Setting SW_RESET reinitializes the core to GUI default values, all internal registers and outputs are cleared and held at initial values until SW_RESET is set to 0. The SW_RESET flag is not synchronized with the AXI4-Stream interfaces. Resetting the core while frame processing is in progress is likely to cause image tearing.
- Bits 30 and 31 of the CONTROL register, FRAME_SYNC_RESET and SW_RESET facilitate reset.
    - Setting SW_RESET reinitializes the core to GUI default values; all internal registers and outputs are cleared and held at initial values until SW_RESET is set to 0. The SW_RESET flag is not synchronized with the AXI4-Stream interfaces. Resetting the core while frame processing is in progress causes image tearing. For applications where the reset functionality is desirable, but image tearing has to be avoided, a frame synchronized reset (FRAME_SYNC_RESET) is available.
    - Setting FRAME_SYNC_RESET to 1 resets the core at the end of the frame being processed, or immediately if the core is between frames when the FRAME_SYNC_RESET was asserted. After reset, the FRAME_SYNC_RESET bit is automatically cleared, so the core can get ready to process the next frame of video as soon as possible.
    - The default value of both RESET bits is 0. Core instances with no AXI4-Lite control interface can only be reset through the ARESETn pin.

STATUS (0x0004) Register

Bit 0 of the STATUS register can be used to request an interrupt from the host processor. In order to facilitate identification of the interrupt source, bits of the STATUS register remain set after an event associated with the particular STATUS register bit, even if the event condition is not present at the time the interrupt is serviced. Bits of the STATUS register can be cleared individually by writing '1' to the bit position to be cleared.

- Bit 0 of the STATUS register, MTF_LOAD_DONE, should be used when loading MTF values into the core. Following a successful transfer of 128 MTF values, the core asserts the MTF_LOAD_DONE status bit. For more information, see MTF_DIn (0x0104) Register, MTF_Active (0x0108) Register and MTF_Write (0x010C) Register.
- Bit 1 of the STATUS register, FRAME_STARTED signals the processor that the core started using the set of register updates recently committed by REG_UPDATE (Bit 1 of the CONTROL register)

- Bit 2 of the STATUS register, AXI4_SLAVE_ERROR indicates that one of the bits of the ERROR registers were set by an AXI4-Stream error either on the previous or current frame inputs.

ERROR (0x0008) Register

Table 2-15 describes the ERROR register bit.

Table 2-15: **Error Register Bit Functions**

ERROR Register Bit	Name	Function
0	curr_eol_error	Indicates that s_axis_currframe_tlast was asserted when the core did not expect it. The expected position of this pulse is defined according to the source video resolution settings.
1	Not Used	
2	curr_sof_error	Indicates that s_axis_currframe_tuser was asserted when the core did not expect it. The expected position of this pulse is defined according to the source video resolution settings.
3	Not Used	
4	prev_eol_error	Indicates that s_axis_prevframe_tlast was asserted when the core did not expect it. The expected position of this pulse is defined according to the source video resolution settings.
5	Not Used	
6	prev_sof_error	Indicates that s_axis_prevframe_tuser was asserted when the core did not expect it. The expected position of this pulse is defined according to the source video resolution settings.
7	Not Used	

Bits 2, 4, 6, and 8 of the ERROR register can be used to request an interrupt from the host processor.

To facilitate identification of the interrupt source, bits of the ERROR register remain set after an event associated with the particular STATUS register bit, even if the event condition is not present at the time the interrupt is serviced. Bits of the ERROR register can be cleared individually by writing '1' to the bit position to be cleared.

IRQ_ENABLE (0x000C) Register

Bits 0-2 of the STATUS register can generate a host-processor interrupt request via the IRQ pin. The Interrupt Enable register facilitates selecting which bits of STATUS register will assert IRQ. Bits of the STATUS register are masked by (AND) corresponding bits of the IRQ_ENABLE register. The resulting terms are combined (OR) together to generate IRQ.

Version (0x0010) Register

Bit fields of the Version Register facilitate software identification of the exact version of the hardware peripheral incorporated into a system. The core driver can take advantage of this Read-Only value to verify that the software is matched to the correct version of the hardware.

FRAME_SIZE (0x0100) Register

The `FRAME_SIZE` register encodes the number of active pixels per line and the number of active lines per frame. The lower half-word (bits 12:0) encodes the number of active pixels per line. The upper half-word (bits 28:16) encodes the number of active lines per frame.

Supported values for both are between 32 and the values provided by the user in the GUI. In order to avoid processing errors, the user should restrict values written to `FRAME_SIZE` the range supported by the core instance.

MTF_DIn (0x0104) Register, MTF_Active (0x0108) Register and MTF_Write (0x010C) Register

Here are some Motion Transfer Function (MTF) loading guidelines:

- The user loads the desired motion transfer function into the Motion Transfer LUT through the MTF_DIn port. Loading the MTF involves writing 128 8-bit unsigned values within the range 0 through 255.
- Of the 128 MTF values to be loaded, the first 64 values must be the Luma MTF values.
- The MSB is bit 7.
- There are eight banks available for the MTF.
- It is not necessary to have MTFs loaded into all banks. However, it is important to make sure that the correct bank is selected active use and for writing.
- Active bank selection is handled by setting the MTF_Active register accordingly. Switching will occur after completion of an output frame.
- MTF bank writing and selection is handled by setting the MTF_Write register accordingly.
- Writing any value to this register resets the internal MTF loading process.
- The 128 values must be loaded sequentially, starting at element 0.
- Following a successful transfer of 128 MTF values, the MTF_LOAD_DONE status bit is set High. If this does not occur, the load process should be re-attempted from element 0, starting with re-writing the MTF_Write register as described above.

Interrupt Subsystem

STATUS register bits can trigger interrupts so embedded application developers can quickly identify faulty interfaces or incorrectly parameterized cores in a video system.

When the core is instantiated with an AXI4-Lite Control interface, the optional interrupt request pin (IRQ) is present. Events associated with bits of the STATUS register can generate a (level triggered) interrupt, if the corresponding bits of the interrupt enable register (IRQ_ENABLE) are set. Once set by the corresponding event, bits of the STATUS register stay set until the user application clears them by writing '1' to the desired bit positions. Using this mechanism the system processor can identify and clear the interrupt source.

Without the AXI4-Lite interface the user can still benefit from the core signaling error and status events. By selecting the **Enable INTC Port** check-box on the GUI, the core generates the optional INTC_IF port. This vector of signals gives parallel access to the individual interrupt sources, as shown in Table 2-16. Unlike STATUS and ERROR flags, INTC_IF signals are not held. They stay asserted only while the corresponding event persists.

Table 2-16: **INTC_IF Signal Functions**

INTC_IF Signal	Name	Function
0	mtf_load_done	Following a successful transfer of 128 MTF values, the core asserts the MTF_LOAD_DONE status bit.
1	frame_started	Indicates that the core has started processing a new frame.
2	curr_eol_error	Indicates that s_axis_currframe_tlast was asserted when the core did not expect it. The expected position of this pulse is defined according to the source video resolution settings.
4	curr_sof_error	Indicates that s_axis_currframe_tuser was asserted when the core did not expect it. The expected position of this pulse is defined according to the source video resolution settings.
6	prev_eol_error	Indicates that s_axis_prevframe_tlast was asserted when the core did not expect it. The expected position of this pulse is defined according to the source video resolution settings.
8	prev_sof_error	Indicates that s_axis_prevframe_tuser was asserted when the core did not expect it. The expected position of this pulse is defined according to the source video resolution settings.

In a system integration tool, such as EDK, the interrupt controller INTC IP can be used to register the selected INTC_IF signals as edge triggered interrupt sources. The INTC IP provides functionality to mask (enable or disable), as well as identify individual interrupt sources from software. Alternatively, for an external processor or MCU, the user can custom

build a priority interrupt controller to aggregate interrupt requests and identify interrupt sources.

Designing with the Core

This chapter includes guidelines and additional information to make designing with the core easier.

Theory of Operation

The noise reduction algorithm is implemented with a recursive temporal filter that uses a programmable motion transfer function (MTF) to control both the shape of the noise reduction curve, as well as the “strength” of the noise reduction.

First, the motion value for the current pixel is calculated by taking the absolute value of the difference between the current and previous pixels. This value is then filtered through a fixed coefficient FIR filter to form a scalar value representing the motion value present in the pixel for the current video frame. This motion value is used as an index to the MTF look-up table.

Second, the value corresponding to the calculated motion value from the MTF is used as a multiplier to scale the difference value. The resulting value is summed with the current frame pixel value, resulting in an output pixel that contains a percentage of the previous frame and the current frame. This same output is then written to memory and becomes the previous frame for the next cycle, thus forming a recursive filter. Consequently, the entire input frame is filtered in a recursive fashion as shown in Figure 3-1.

For the MANR core, the above operation is carried out independently for luma and chroma channels. Separate engines are included for each channel. The sub-sampled Cr and Cb channels use this second engine. Switching between Cr and Cb is handled internally.

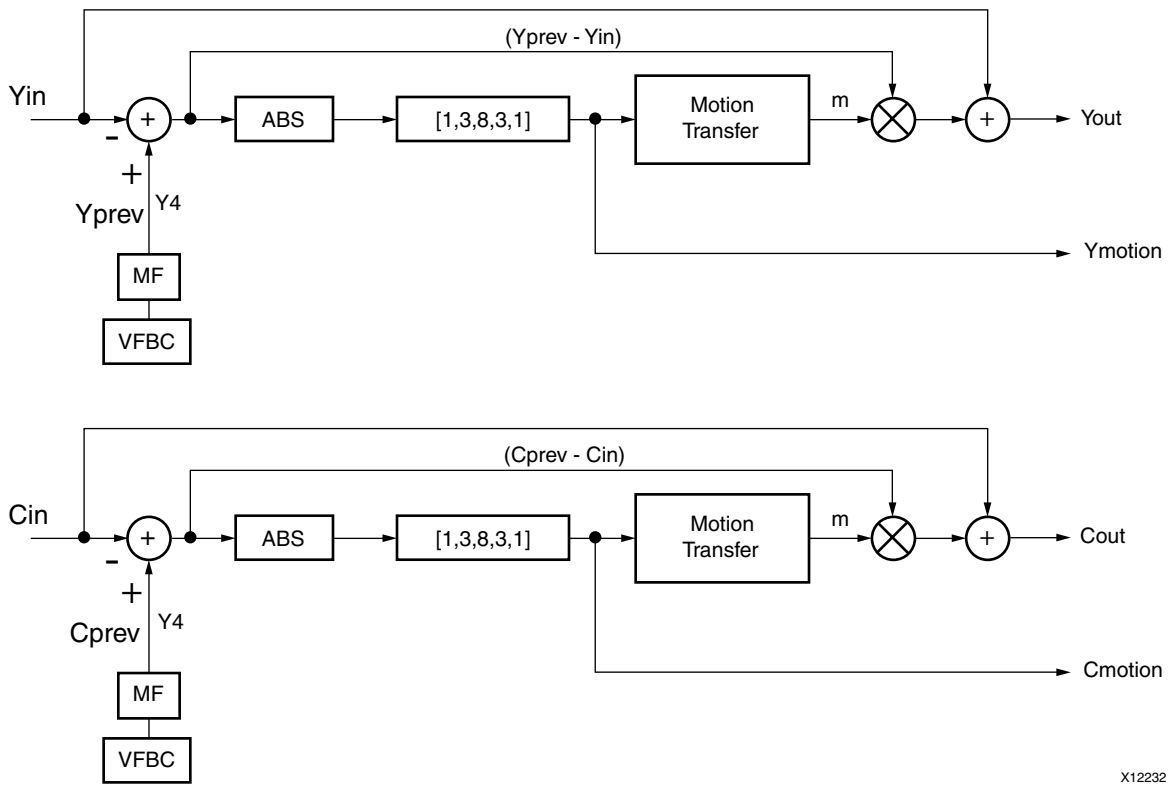

Figure 3-1: **Motion Adaptive Noise Reduction**

When the MANR core is used with an AXI4-Lite interface, the MTF function can be reprogrammed on a frame-by-frame basis using an arbitrary function. Best results have been demonstrated by using the monotonically decreasing portion of Gaussian or exponential functions. The MANR LogiCORE™ IP is initialized from the CORE Generator™ tool using an "exponential" shape for the MTF. This shape is then attenuated to provide the different possible noise reduction strengths available. The exponential shape provided has been shown to be effective at reducing noise while minimizing "smearing" or "ghosting" caused by the recursive nature of the filter.

The exponential transfer function is shown in Figure 3-2. The Y-axis denotes the amount of recursion, and the X-axis denotes the amount of motion.

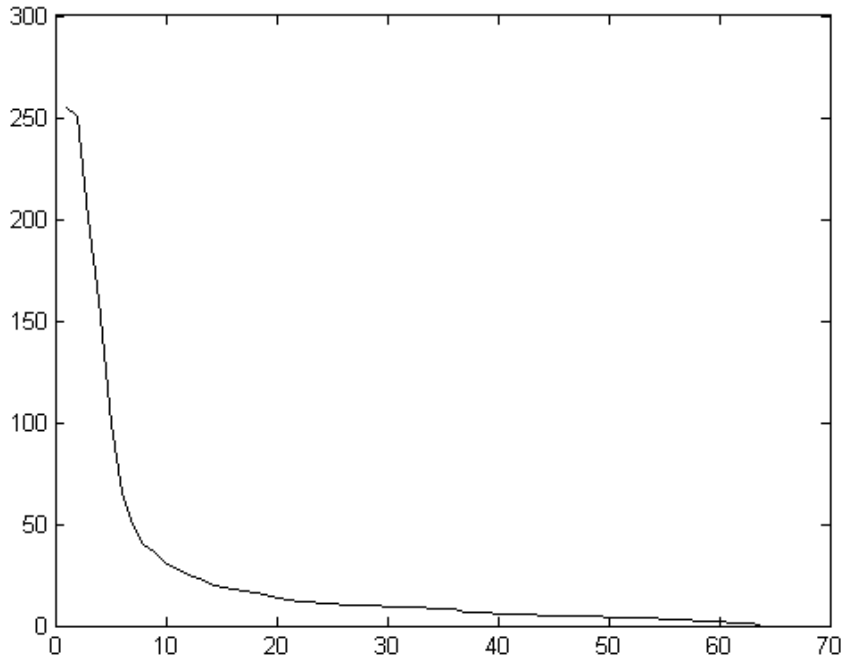

Figure 3-2: **Exponential MTF**

The function shown is monotonically decreasing. This implies that the amount of recursion is inversely proportional to the amount of motion detected. For example, a large motion value of 63 would result in an output of 0 from the MTF. This would result in none of the previous pixel data being applied to the output data. A large motion value indicates that the pixel changes are most likely not due to noise; therefore the output image should consist of mostly or all of the current input image. Conversely, a small motion value results in a large output value from the MTF, hence incurs more recursion which results in more calculations between the previous and current frames. Small changes in the pixel values from frame to frame are more likely due to noise than motion, and hence more of the previous image should be used to form the output image. The function also has a "knee" or "shelf" at the beginning of the curve. This maximizes recursion in the area of the curve where noise is most likely to occur, but the function rolls off quickly as the magnitude of the luma changes increase (indicating that actual motion is present).

Using this same shape, several "strengths" of noise reduction can be realized by applying an attenuation factor to the curve in Figure 3-2. This results in the same shape response, but varying degrees of recursion for the same shape. Shown in Figure 3-3 are the exponential MTFs with an attenuation of 0.75, 0.5, 0.25 and zero applied. The zero case is also called "none" or "bypass" because regardless of the motion scalar value per pixel, the output of the filter is always the current pixel, that is, the motion transfer function of zero results in no recursion. To ease selection of a noise reduction strength setting, each curve has been assigned a qualitative value of aggressive, strong, medium, weak, and none. Each curve is

shown in Figure 3-3. These settings map directly to the selections available in the Core Generator GUI. Selecting a particular strength initializes the MTF on power-up with that setting. The power-up MTF can always be overwritten at run time.

In Figure 3-3, the curves are shown relative to the aggressive setting to illustrate how the attenuation factor is applied. For reference:

- The aggressive curve is shown as a solid line
- The strong setting is shown as a dotted line
- The medium setting is shown as a dashed line
- The weak setting is shown as a "dash-dot" line

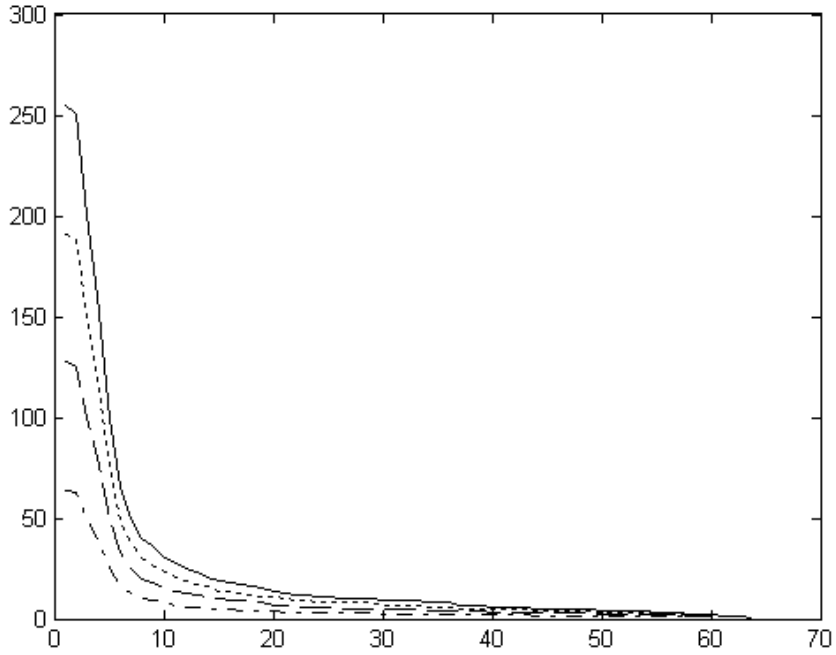

Figure 3-3: **MTF Settings**

The MANR core can store up to eight MTF tables in memory. Only one table can be active in a given frame period. See MTF Storage and Switching in Chapter 3 for details.

General Design Guidelines

MTF Storage and Switching

The MTF values are stored in block RAM internal to the MANR core. The block RAM can store up to eight separate MTF curves. Separate MTF curves are stored for Y and C channels.

Storing different MTFs can be useful in situations where the content being filtered differs in motion content. For example, a source might switch between a camera showing a fixed scene with little movement, to a more complex scene with many moving objects. One MTF can be optimized for noise reduction, while another can balance noise reduction and motion artifact from recursion. The "aggressive" exponential curve shown in Figure 3-3 could be made active when the scene has little motion (because this curve will have more recursion, and hence more smearing artifacts) while the "medium" curve could be used when the material has a large motion content. Using the AXI4-Lite interface enables switching between these curves dynamically.

Xilinx provides five pre-loaded MTF curves by default in the core. In addition, MTF values can be updated on a frame-by-frame basis, allowing a microprocessor to easily control and optimize the MTF based on the expected source material and other conditions.

The MANR core enables you to use custom MTF curves. You can load custom MTF curves into the remaining spaces in the block RAM, or overwrite the existing ones. By overwriting a default MTF, the default MTF is not available again unless the FPGA is reprogrammed.

The MTF for each Y and C components consists of 64 discrete values that form a piecewise linear definition of the MTF curve. For example, using the "aggressive" exponential curve included with the core, the Luma (Y) MTF data would appear as shown in Table 3-1, where "Address" is the offset into the MTF memory from the base address and "Value" is the 8-bit value.

The MTF must be monotonically *decreasing*. This means that for large motion values, the MTF should output a small value; for small motion values, the MTF should output a large value. In addition, for the register bypass mode to work, MTF value at address 63 must be zero.

Table 3-1: **MTF Address Values**

Address	Value	Address	Value	Address	Value	Address	Value
0	255	8	36	16	17	24	11
1	250	9	30	17	16	25	10
2	200	10	28	18	15	26	10
3	160	11	25	19	14	27	10
4	100	12	23	20	13	28	10
5	65	13	21	21	12	29	9
6	50	14	19	22	12	30	9
8	40	15	18	23	11	31	9
32	9	40	6	48	5	56	3
33	8	41	6	49	4	57	2
34	8	42	6	50	4	58	2
35	8	43	5	51	4	59	2
36	7	44	5	52	4	60	1
37	7	45	5	53	4	61	1
38	7	46	5	54	3	62	1
39	6	47	5	55	3	63	0

Input Interfaces

All video data is passed into the MANR core through two AXI4-Stream Video protocol interfaces. The intended use of the MANR core is to simultaneously access two frames that differ temporally by one frame period. These frames are referred to as the “current” and “previous” frames.

The current frame is accessed through the S_AXIS_CURRFRAME AXI4-Stream interface. The previous frame is accessed through the S_AXIS_PREVFRAME AXI4-Stream interface. Typically, the data source for this interface is a frame buffer. The MANR output frame must be fed back through external frame-buffer memory in order to become the previous frame during the next frame period.

Both of these interfaces handle 8-bit YC data, transmitted as the lowest 16 bits of the tData element of the input AXI4-Stream bus. Luma occupies bits 7:0; and chroma occupies bits 15:8.

The MANR uses internal FIFOs and the AXI4-Stream flow-control in order to synchronize incoming data from these two interfaces.

Output Interfaces

Video data is passed from the MANR core through three AXI4-Stream Video protocol interfaces. Because the MANR operates as a recursive temporal filter, the output frame must be written into memory, where it must become available as the previous frame during the next frame period. The M_AXIS_MEM AXI4-Stream interface should be used for writing the frame to the frame buffer. This interface handles 8-bit YC data, transmitted as the lowest 16-bits of the tData element of the output AXI4-Stream bus. Luma occupies bits 7:0, and chroma occupies bits 15:8.

In addition to writing the data back to memory, the same processed output video data is made available on the m_axis_output AXI4-Stream interface, for optional use by downstream processing blocks. The interface handles 8-bit YC data, transmitted as the lowest 16-bits of the tData element of the output AXI4-Stream bus. Luma occupies bits 7:0, and chroma occupies bits 15:8.

A third AXI4-Stream output interface provides the motion data for optional use by downstream processing blocks. It is available on the m_axis_motion AXI4-Stream interface. Similar to video data, the interface handles 8-bit YC data, transmitted as the lowest 16-bits of the tData element of the output AXI4-Stream bus. Luma motion occupies bits 7:0, and chroma motion occupies bits 15:8.

Figure 3-4 shows a typical use-case including the use of the AXI-VDMA block for external memory access.

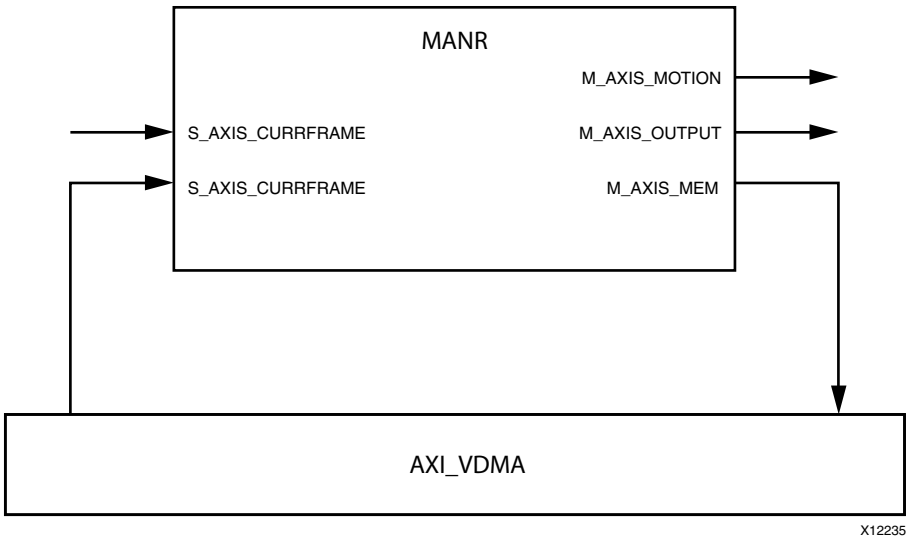

Figure 3-4: **Typical MANR Connectivity**

Interrupts

The MANR core provides an internal interrupt controller with masking and enable to make interrupt handling easier.

The MANR generates a "frame done" interrupt, indicating that it has finished processing the current frame. This signal can be useful for software to manage the core in the context of a larger pipeline.

Use Models

Two examples are provided that show the core usage for noise reduction only, and as the noise-reduction engine and motion-detection engine for a larger system.

Regardless of the application, the MANR core must have access to external memory using the AXI VDMA core. The recursive nature of the filter requires that the current output frame of the core be written to memory to be stored and used as the previous frame for the next set of calculations.

In Figure 3-5 and Figure 3-6, thick lines are used to indicate video data flow in the system.

Use Model 1: Noise Reduction Application

Figure 3-5 shows an example where the MANR is used to reduce noise. In this case, streaming video data (current frames) is propagated to the MANR core directly, while previous frames are provided by the AXI-VDMA block.

Video data originates at a video source (for example, an HDMI™ technology source or a camera), with periodic timing signals, such as sync and blanking signals. The data might need to be pre-processed with Xilinx color-space-converter or chroma re-sampler cores to YCC422 format. Further processing can be undertaken before or after the MANR core.

The AXI-VDMA in Figure 3-5 handles the temporal feedback path. It takes the MANR output for storage as the previous frame input. Also, the bidirectional AXI-VDMA feeds the previous frame back into the core.

The timing controller shown in Figure 3-5 detect the video resolution, and make the detection results available for the system processor. The system processor distributes the resolution to the system components and programs, and initializes the frame-buffer mechanism in the AXI-VDMA.

The AXI4-Stream to Video Out module, after being configured, waits for the streaming video, then enables the Video Timing Controller (VTC) generator side to generate periodic video output timing signals.

When a system processor is not available, it is also possible to create a MANR sub-system to process video with pre-defined resolution. By configuring the constituent cores for no AXI4-Lite interface, the GUI allows you to specify one supported video resolution.

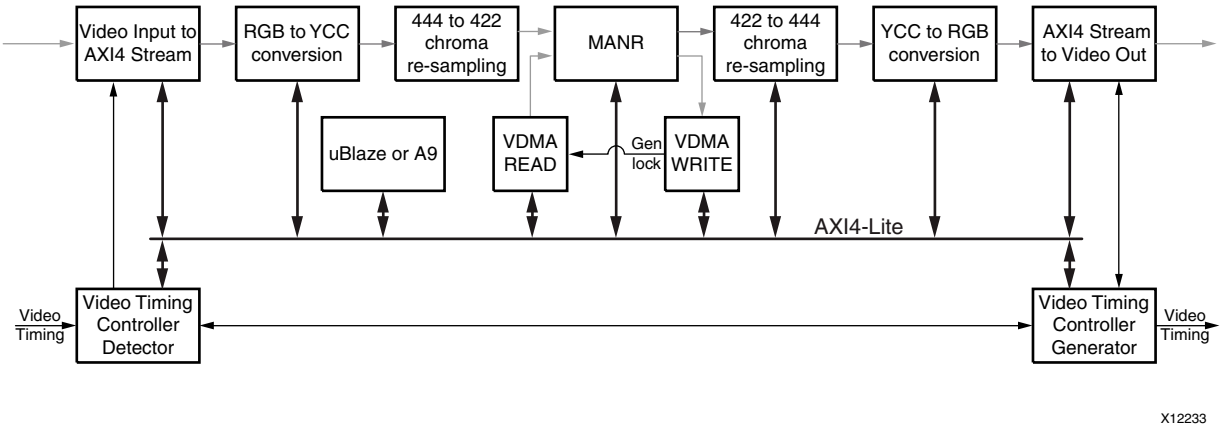

Figure 3-5: **Simple Noise Reduction**

Use Model 2: Noise Reduction and Motion Detection

In Figure 3-6, the MANR is used to calculate and provide motion (change) data and noise reduction in a simple video processing system. The implicit link from the MANR to the (generic) Image Processing block includes video data and pixel motion information which can be used by this target block.

In this example, as in Figure 3-5, the MANR core noise-reduces the incoming video from a camera, or other period video source.

However, in Figure 3-6, the MANR core also provides the video and motion data to a processing module through the AXI4-Stream output ports m_axis_output and m_axis_motion for additional processing of the motion and image data. Typical examples include an Image Characterization block (which makes use of the video data and the motion data outputs) or a Video Scaler block (which only uses the video data).

The MANR output streams can be passed to the Motion and Video Processing module(s) either directly, or indirectly through VDMA interfaces. When the VDMA output is written to memory, the a_axis_output stream may remain unused, because frame data has already been written to memory through the mom_out stream. Another pair of VDMA read ports can be used to read out motion and frame data from the frame buffer, isolating the input frame rate from the output frame rate.

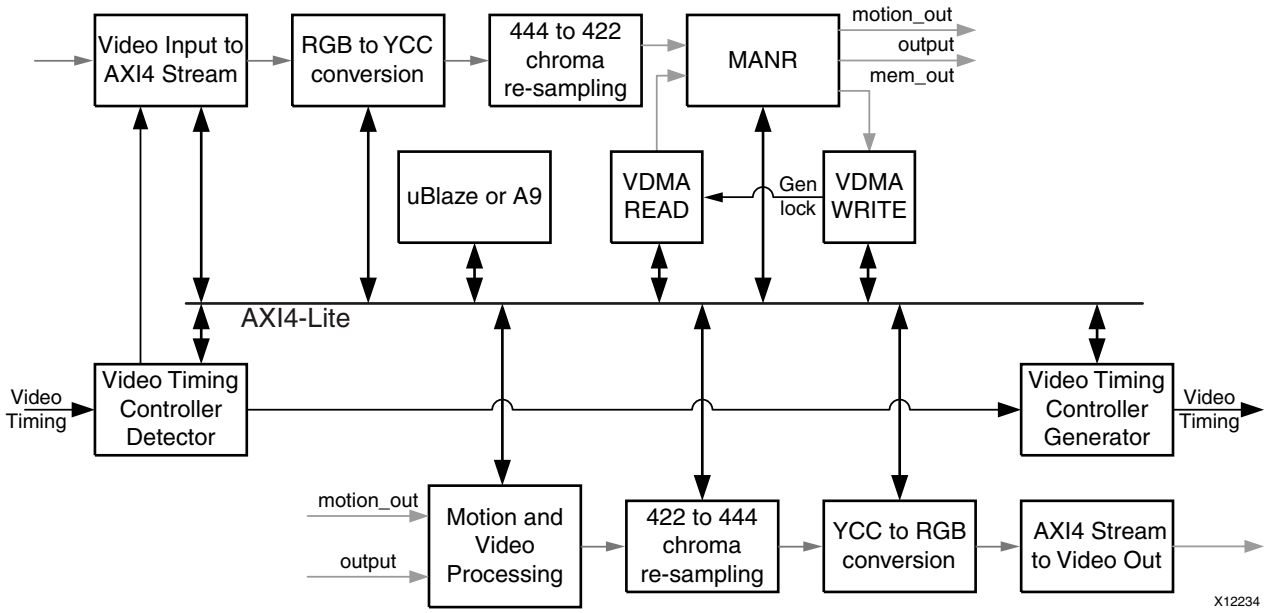

Figure 3-6: **Noise Reduction and Motion Processing**

Clocking

The MANR core has one clock (`aclk`) that is used to clock the datapath of the entire core, and one optional clock, s_axis_aclk, which is used as the clock source for the optional AXI4-Lite interface.

MANR Control and Timing

After reset, when using the AX4-Lite Control interface, you should initialize the registers to set up the frame size. Next, optional loading of an MTF can be done if the defaults chosen during core generation are not sufficient. Prior to enabling the MANR, ensure that the current and previous frame buffer locations are initialized with valid video data. This can be accomplished by enabling core and enabling bypass mode in the control register. After a full frame has been committed to memory, as indicated by STATUS register bit 0, the bypass mode can be disabled and normal operation can begin. Figure 3-7 illustrates MANR initialization.

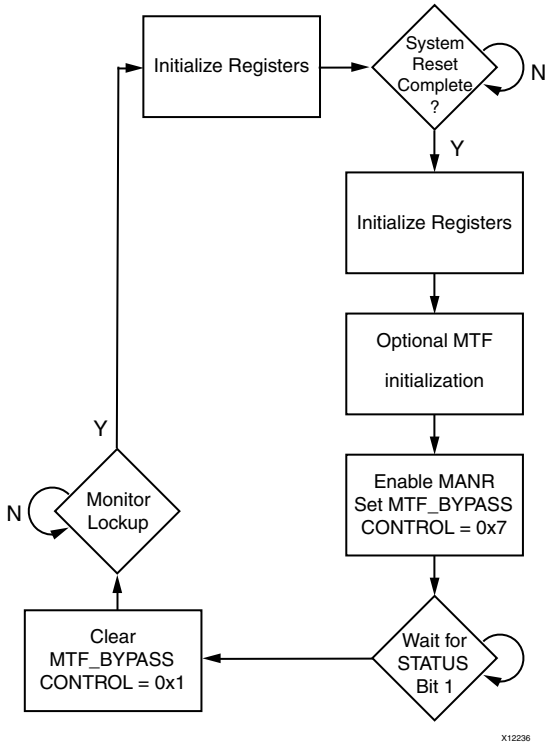

Figure 3-7: **MANR Initialization**

Resets

The MANR core has one active-Low reset (`ARESETn`) that resets the entire core. When using AXI4-Lite, an internal active-High software reset is combined with this signal.

Protocol Description

The register interface is compliant with the AXI4-Lite interface. The video and motion input and output interfaces are compliant with AXI4-Stream Video protocol.

C Model Reference

This chapter introduces the bit accurate C model for the Motion Adaptive Noise Reduction core, which has been developed primarily for system-level modeling. Features of this C model include:

- Bit accurate with v_manr_v5_01_a core
- Library module for the MANR core function
- Available for 32 and 64-bit Windows and 32 and 64-bit Linux platforms
- Supports all features of the HW core that affect numerical results
- Designed for rapid integration into a larger system model
- Example application C code is provided to show how to use the function

Overview

The bit accurate C model for the LogiCORE™ IP MANR can be used on 32/64-bit Windows and 32/64-bit Linux platforms. The model comprises a set of C functions, which reside in a statically linked library (shared library). Full details of the interface to these functions are provided in Interface, page 40.

The main features of the C model package are:

- **Bit Accurate C Model** - produces the same output data as the MANR core on a frame-by-frame basis. However, the model is not cycle accurate, as it does not model the core's latency or its interface signals.
- **Application Source Code** - uses the model library function. This can be used as example code showing how to use the library function. However, it also serves these purposes:
  - **Input .yuv file** is processed by the application; 8-bit YUV422 format accepted.
  - **Output .yuv file** is generated by the application; 8-bit YUV422 format generated.
  - **Report.txt file** is generated for run time status and error messages.

The latest version of the model is available for download on the LogiCORE IP MANR product page at: http://www.xilinx.com/products/ipcenter/EF-DI-IMG-MA-NOISE.htm

Unpacking and Model Contents

Unzip the `v_manr_v5_0_bitacc_model` file, containing the bit accurate models for the MANR IP Core. This creates the directory structure and files in Table 4-1.

Table 4-1: **Directory Structure and Files of MANR C Model**

File Name	Contents
./doc	Documentation directory
README.txt	Release notes
<product Guide>.pdf	This document.
Makefile	Makefile for running gcc via make for 32-bit and 64-bit Linux platforms
v_manr_v5_01_a_bitacc_cmodel.h	Model header file
yuv_utils.h	Header file declaring the YUV image / video container type and support functions including .yuv file I/O
rgb_utils.h	Header file declaring the RGB image / video container type and support functions
bmp_utils.h	Header file declaring the bitmap (.bmp) image file I/O functions.
video_utils.h	Header file declaring the generalized image / video container type, I/O and support functions
video_fio.h	Header file declaring support functions for test bench stimulus file I/O
run_bitacc_cmodel.c	Example code calling the C model
run_bitacc_cmodel_config.c	Example code calling the C model – uses command line and config file arguments
run_bitacc_cmodel.sh	Bash shell script that compiles and runs the model.
./lin64	Directory containing Precompiled bit accurate ANSI C reference model for simulation on 64-bit Linux platforms.
libIp_v_manr_v5_01_a_bitacc_cmodel.so	Model shared object library
libstlport.so.5.1	STL library, referenced by libIp_v_manr_v5_01_a_bitacc_cmodel.so
run_bitacc_cmodel	64-bit Windows fixed configuration executable
./lin	Directory containing Precompiled bit accurate ANSI C reference model for simulation on 32-bit Linux platforms.
libIp_v_manr_v5_01_a_bitacc_cmodel.so	Model shared object library

Table 4-1: **Directory Structure and Files of MANR C Model *(Cont'd)***

File Name	Contents
libstlport.so.5.1	STL library, referenced by libIp_v_manr_v5_01_a_bitacc_cmodel.so
run_bitacc_cmodel	32-bit Windows fixed configuration executable
./nt64	Directory containing Precompiled bit accurate ANSI C reference model for simulation on 64-bit Windows platforms.
libIp_v_manr_v5_01_a_bitacc_cmodel.dll	Precompiled library file for 64-bit Windows platforms compilation
libIp_v_manr_v5_01_a_bitacc_cmodel.lib	Precompiled library file for 64-bit Windows platforms compilation
stlport.5.1.dll	STL library
run_bitacc_cmodel.exe	64-bit Windows fixed configuration executable
./nt	Precompiled bit accurate ANSI C reference model for simulation on 32-bit Windows platforms.
libIp_v_manr_v5_01_a_bitacc_cmodel.dll	Precompiled library file for 32-bit Windows platforms compilation
libIp_v_manr_v5_01_a_bitacc_cmodel.lib	Precompiled library file for 32-bit Windows platforms compilation
stlport.5.1.dll	STL library
run_bitacc_cmodel.exe	32-bit Windows fixed configuration executable
./examples	
video_in.yuv	Example YUV input file, resolution 1280Hx720V
video_in.hdr	Header file for video_in.yuv
video_in_128x128.yuv	Example YUV input file, resolution 128Hx128V
video_in_128x128.hdr	Header file for video_in_128x128.yuv

Software Requirements

The MANR C models were compiled and tested with the software listed in Table 4-2.

Table 4-2: **Compilation Tools for the Bit Accurate C Models**

Platform	C Compiler
32/64-bit Linux	GCC 4.1.1
32/64-bit Windows	Microsoft Visual Studio 2008

Interface

The MANR core function is a statically linked library. A higher level software project can make function calls to this function:

```
int xilinx_ip_v_manr_v3_v3_0_bitacc_simulate(
      struct xilinx_ip_v_manr_v5_00_a_generics generics,
      struct xilinx_ip_v_manr_v5_00_a_inputs inputs,
      struct xilinx_ip_v_manr_v5_00_a_outputs*  outputs).
```

Before using the model, the structures holding the inputs, generics and output of the MANR instance must be defined:

```
struct  xilinx_ip_v_manr_v5_00_a_generics manr_generics;
struct  xilinx_ip_v_manr_v5_00_a_inputs  manr_inputs;
struct xilinx_ip_v_manr_v5_00_a_outputs* manr_outputs
```

The declaration of these structures are in the `v_manr_v5_00_a_bitacc_cmodel.h` file.

Before making the function call, complete these steps:

1. Populate the *generics* structure:

   nr_strength - Between 0 and 4. Describes the strength of the initial noise reduction filter: 0= None; 1=Weak; 2=Med; 3=Strong; 4=Aggressive.

2. Populate the *inputs* structure to define the values of run time parameters:

   Note: This function processes *one frame at a time*.

   - **video_in** - Video structure that comprises these elements:
     - **bits_per_component** - Must be set to 8.
     - **cols** - Horizontal image size: 32 to 1920.
     - **rows** - Vertical image size: 32 to 1080.
     - **frames** - Set to 1; this function processes *one frame at a time*.
     - **mode** - Defines the chroma format (RGB, YUV422, and so on); see Table 4-4. This core can only process YC422 or YC420.
     - **data** - This is the frame of video data to be processed, arranged in raster form.
   - **mtf** - MTF Look-up table. This is a 1D array of 64 integers in the range 0 to 255, which represents the Motion Transfer Function.

3. Populate the *outputs* structure.

   - **video_out** - Video structure that comprises the same elements as the video_in structure element described previously.

Note: The `video_in` variable is not initialized because the initialization depends on the actual test image to be simulated. The next section describes the initialization of the `video_in` structure.

Results are provided in the outputs structure, which contains the output video data in the form of type `video_struct`. After the outputs have been evaluated or saved, dynamically allocated memory for input and output video structures must be released. See Delete the Video Structure, page 42 for more information. Successful execution of all provided functions return a value of 0. Otherwise, a non-zero error code indicates that problems were encountered during function calls.

Input and Output Video Structure

Input images or video streams can be provided to the MANR reference model using the general purpose `video_struct` structure, defined in `video_utils.h`:

```
struct video_struct{
  int       frames, rows, cols, bits_per_component, mode;
  uint16*** data[5]; };
```

Table 4-3: **Member Variables of the Video Structure**

Member Variable	Designation
Frames	Number of video/image frames in the data structure
Rows	Number of rows per frame(1)
Cols	Number of columns per line(1)
Bit_per_component	Number of bits per color channel/component. All image planes are assumed to have the same color/component representation. Maximum number of bits per component is 16.
Mode	Contains information about the designation of data planes. Named constants to be assigned to mode are listed in Table 4-4.
Data	Set of five pointers to three dimensional arrays containing data for image planes. Data is in 16-bit unsigned integer format accessed as data[plane][frame][row][col]. In the MANR C model case, only one frame is processed at any one time. Consequently, the '[frame]' index is always set to 0.

1. Pertaining to the image plane with the most rows and columns, such as the luminance channel for YUV data. Frame dimensions are assumed constant through all frames of the video stream, however, different planes, such as Y,U and V can have different dimensions.

Table 4-4: **Named Constants for Video Modes With Corresponding Planes and Representations**

Mode	Planes	Video Representation
FORMAT_MONO	1	Monochrome – luminance only
FORMAT_RGB	3	RGB image/video data
FORMAT_C444	3	444 YUV, or YCrCb image/video data

Table 4-4: **Named Constants for Video Modes With Corresponding Planes and Representations**

FORMAT_C422[1]	3	422 format YUV video, (U,V chrominance channels horizontally sub-sampled)
FORMAT_C420[1]	3	420 format YUV video, (U,V sub-sampled both horizontally and vertically)
FORMAT_MONO_M	3	Monochrome (luminance) video with motion
FORMAT_RGBA	4	RGB image/video data with alpha (transparency) channel
FORMAT_C420_M	5	420 YUV video with motion
FORMAT_C422_M	5	422 YUV video with motion
FORMAT_C444_M	5	444 YUV video with motion
FORMAT_RGBM	5	RGB video with motion

1. Supported by the MANR core.

Working With Video_struct Containers

The header file `video_utils.h` defines functions to simplify access to video data in `video_struct`.

```
int video_planes_per_mode(int mode);
int video_rows_per_plane(struct video_struct* video, int plane);
int video_cols_per_plane(struct video_struct* video, int plane);
```

The function `video_planes_per_mode` returns the number of component planes defined by the mode variable, as described in Table 4-4. The functions `video_rows_per_plane` and `video_cols_per_plane` return the number of rows and columns in a given plane of the selected video structure. The following example demonstrates using these functions in conjunction to process all pixels within a video stream stored in variable `in_video`:

```
for (int frame = 0; frame < in_video->frames; frame++) {
  for (int plane = 0; plane < video_planes_per_mode(in_video->mode); plane++) {
    for (int row = 0; row < rows_per_plane(in_video,plane); row++) {
      for (int col = 0; col < cols_per_plane(in_video,plane); col++) {
   // User defined pixel operations on
// in_video->data[plane][frame][row][col]
      }
    }
  }
}
```

Delete the Video Structure

Large arrays such as the `video_in` element in the video structure must be deleted to free up memory.

The following example function is defined as part of the `video_utils` package.

```
void free_video_buff(struct video_struct* video )
{
```

```
    int plane, frame, row;

    if (video->data[0] != NULL) {
      for (plane = 0; plane <video_planes_per_mode(video->mode); plane++) {
        for (frame = 0; frame < video->frames; frame++) {
          for (row = 0; row<video_rows_per_plane(video,plane); row++) {
            free(video->data[plane][frame][row]);
          }
          free(video->data[plane][frame]);
        }
        free(video->data[plane]);
      }
    }
}
```

This function can be called as follows:

```
free_video_buff ((struct video_struct*) &manr_outputs.video_out);
```

Example Code

An example C file, `run_bitacc_cmodel.c`, is provided along with the lin32, lin64, NT32 and NT64 executables for this example. This C file has these characteristics:

- Contains an example of how to write an application that makes a function call to the MANR C model core function.
- Contains an example of how to populate the video structures at the input and output, including allocation of memory to these structures.
- Uses a YUV file reading function to extract video information for use by the model.
- Uses a YUV file writing function to provide an optional output YUV file, which allows the user to visualize the result of the MANR operation.

The delivered model extracts a number of frames from the specified .yuv input file, removes noise from this video stream, and outputs the noise reduced stream in the specified .yuv output file.

The MANR algorithm is temporally recursive. Motion is determined by comparing the current frame with the previous frame. For the first input frame, there is no previous frame, so the first output frame always shows zero motion.

The MTF (motion transfer function) determines the level to which each of the two frames contributes to the output frame. The nr_strength parameter selects between five different MTF characteristics. These functions are coded into the wrapper function `run_bitacc_cmodel.c`.

Initializing the MANR Input Video Structure

In the example code wrapper, data is assigned to a video structure by reading from a .yuv video file. This file is described in C Model Example I/O Files, page 44. The `yuv_utils.h` and `video_utils.h` header files packaged with the bit accurate C models contain functions to facilitate file I/O. The `run_bitacc_cmodel` example code uses these functions to read from the YUV file.

YUV Image Files

The header `yuv_utils.h` file declares functions that help access files in standard YUV format. It operates on images with three planes (Y, U and V). The following functions operate on arguments of type yuv8_video_struct, which is defined in `yuv_utils.h`.

```
int write_yuv8(FILE *outfile, struct yuv8_video_struct *yuv8_video);
int read_yuv8(FILE *infile, struct yuv8_video_struct *yuv8_video);
```

Exchanging data between `yuv8_video_struct` and general `video_struct` type frames/videos is facilitated by functions:

```
int copy_yuv8_to_video(struct yuv8_video_struct* yuv8_in,
                       struct video_struct* video_out );
int copy_video_to_yuv8( struct video_struct* video_in,
                        struct yuv8_video_struct* yuv8_out );
```

Note: All image/video manipulation utility functions expect both input and output structures to be initialized. For example, pointing to a structure to which memory has been allocated, either as static or dynamic variables. Moreover, the input structure must have the dynamically allocated container (data or y ,u, v) structures already allocated and initialized with the input frame(s). If the output container structure is pre-allocated at the time of the function call, the utility functions verify and generate an error if the output container size does not match the size of the expected output. If the output container structure is not pre-allocated, the utility functions create the appropriate container to hold results.

C Model Example I/O Files

Input Files

- **<input_filename>.yuv** (Optional; for example, `video_in.yuv`, `video_in_128x128.yuv`).
  - Standard 8-bit YUV file format. Entire Y plane followed by entire Cb plane, followed by the entire Cr plane.
  - Can be viewed in a YUV player.
  - No header.

Output Files

- **<output_filename>.yuv** (Optional; for example, `video_out.yuv`).
  - Standard 8-bit 4:2:2 yuv file format. Entire Y plane followed by entire Cb plane, followed by the entire Cr plane.
  - Can be viewed in a YUV player.

Compiling the MANR C Model With Example Wrapper

Linux (32/64 bits)

For 64-bit Linux, cd into the /lin64 directory. From there, run the command:

```
gcc -m64 -x c++ ../run_bitacc_cmodel.c -o run_bitacc_cmodel -L.
-lIp_v_manr_v5_00_a_bitacc_cmodel -Wl,-rpath,.
```

When using 32-bit Linux, cd into the /lin directory, and run with the '-m32' switch:

```
gcc -m32 -x c++ ../run_bitacc_cmodel.c -o run_bitacc_cmodel -L.
-lIp_v_manr_v5_00_a_bitacc_cmodel -Wl,-rpath,.
```

To run either 32- or 64-bit executables:

1. Set your LD_LIBRARY_PATH environment variable to the location of the two .so libraries.
2. Execute as follows:

```
./run_bitacc_cmodel video_in.yuv video_out.yuv 10 1280 720 2 1
```

Windows (32/64-bits)

The `v_manr_v5_00_a_bitacc_cmodel.zip` file includes all the4 necessary files required to compile the top-level demonstration code `run_bitacc_cmodel.c` with an ANSI C compliant compiler under Windows.

This section includes an example using Microsoft Visual Studio.

In Visual Studio, create a new, empty Win32 Console Application project. In the appropriate project folders, add the following files:

- `v_manr_v5_00_a_bitacc_cmodel.h`
- `libIp_v_manr_v5_00_a_bitacc_cmodel.lib`
- `run_bitacc_cmodel.c`

To run either 32- or 64-bit executables:

1. Cd to a location that includes all the following files
   - `run_bitacc_cmodel.exe` (or the executable file generated by your compiler)
   - `libIp_v_manr_v5_00_a_bitacc_cmodel.dll`
2. Execute as follows:

```
Usage: c_model  -y <YUV filename>
                            -h <H Size (pixels)>
                            -v <V Size (lines)>
                            -f <number of frames to be processed>
                            -n <Noise-reduction strength (0 - 4)>
```

For example:

```
run_bitacc_cmodel video_in.yuv video_out.yuv 10 1280 720 2 2
```

Compile/Run Shell Script

To compile the example code, use the cd command to go to the directory where the header files, the library files and `run_bitacc_cmodel.c` were unpacked. The libraries and header files are referenced during the compilation and linking process. They are in the `/lin64` directory. Use the cd command to go into the `lin/lin64` directory and execute the bash shell script that compiles the project using the GNU C Compiler and runs it:

```
bash run_bitacc_cmodel.sh
```

The bash script text is provided here:

```
#!/bin/bash
################################################
# Compile model and libraries
################################################
gcc -x c++ ../run_bitacc_cmodel.c -o run_bitacc_cmodel -L.
-lIp_v_manr_v5_00_a_bitacc_cmodel -Wl,-rpath,.

################################################
# Run model.
# Usage:
# ./run_bitacc_model -y <input_file>.yuv -h <hsize> -v <vsize> -f <#frames> -n <NR_strength>

# NR_strength:
# 0 = None
# 1 = Weak
# 2 = Medium
# 3 = Strong
# 4 = Aggressive
```

```
# Example:
# ./run_bitacc_cmodel -y ../video_in.yuv -h 1280 -v 720 -f 10 -n 2
################################################
./run_bitacc_cmodel -y ../video_in.yuv -h 1280 -v 720 -f 10 -n 2
```

You can customize this shell script.

SECTION II: VIVADO DESIGN SUITE

Customizing and Generating the Core

Constraining the Core

Detailed Example Design

Customizing and Generating the Core

This chapter includes information on the Vivado™ Design Suite to customize and generate the core.

Graphical User Interface

The Xilinx® Motion Adaptive Noise Reduction (MANR) LogiCORE™ IP is easily configured to meet the developer's specific needs through the Vivado Design Suite Graphical User Interface (GUI). This section provides a quick reference to parameters that can be configured at generation time. Figure 5-1 shows the parameters for the MANR core in the Customize IP dialog box.

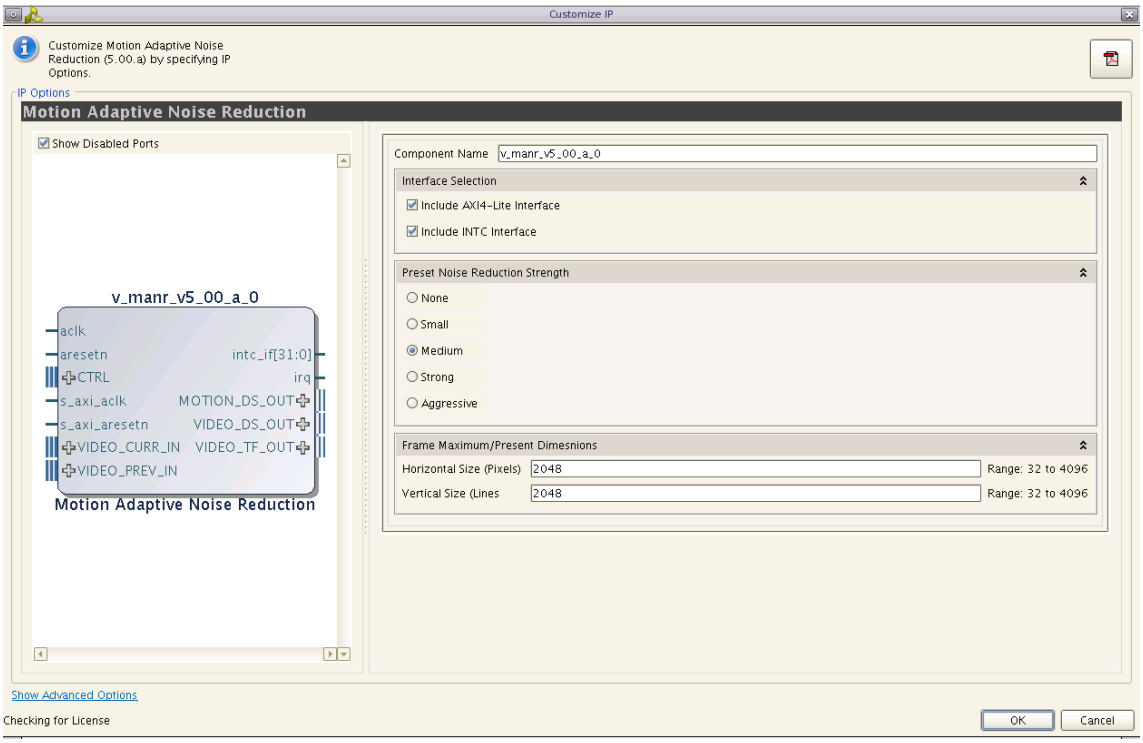

Figure 5-1: **Customize IP Dialog Box**

The Customize IP dialog box displays a representation of the IP symbol on the left side, and the parameter assignments on the right side, which are described as follows:

- **Component Name:** The component name is used as the base name of output files generated for the module. Names must begin with a letter and must be composed from characters: a to z, A to Z, 0 to 9 and "_".

  Note: The name "v_manr_v5_01_a" is not allowed.

- **Noise Reduction Strength:** This parameter selects the default MTF. The MTF is initialized according to one of the following settings. The MTF is fully programmable, and the initial values specified during core generation can easily be overridden by programming the desired MTF at run time.
  - None: Specifies all zeroes for MTF; bypasses noise reduction such that the output pixel always equals the input pixel.
  - Small: Specifies ¼ gain exponential curve for MTF
  - Medium: Specifies ½ gain exponential curve for MTF
  - Strong: Specifies ¾ gain exponential curve for MTF
  - Aggressive: Specifies full gain exponential curve for MTF
- **Frame Maximum/Preset Dimensions:** These fields represent the maximum anticipated rectangle size on the input and output of the MANR core. The rectangle can vary from 32x32 through 4096x4096. When the core is being used in Fixed mode (AXI4_LITE is disabled), these figures represent the fixed frame dimensions.
- Optional Features:
  - **AXI4-Lite Register Interface:** When selected, the core is generated with an AXI4-Lite interface, which gives access to dynamically program and change processing parameters. For more information, see Control Interface in Chapter 2.
  - **INT_IF interface:** When selected, interrupts are generated on this bus. See Interrupt Subsystem in Chapter 2 for more details.

Output Generation

Vivado design tools generate the files necessary to build the core and place those files in the `<project>/<project>.srcs/sources_1/ip/<core>` directory.

File Details

The Vivado design tools output consists of some or all the following files:

Table 5-1: **Vivado Design Tools Output**

Name	Description
v_manr_v5_01_a	Library directory for the v_manr_v5_01_a Core.
v_tc_v5_01_a	Library directory for the helper core used with the v_manr_v5_01_a.
v_manr_v5_01_a.veo	Verilog instantiation template.
v_manr_v5_01_a.vho	VHDL instantiation template.
v_manr_v5_01_a.xci	IP-XACT XML file describing which options were used to generate the core. An XCI file can also be used as a source file for Vivado.
v_manr_v5_01_a.xml	IP-XACT XML file describing how the core is constructed so Vivado can properly build the core

Constraining the Core

This chapter contains applicable constraints for the MANR core.

Required Constraints

The ACLK pin should be constrained at the pixel clock rate desired for the video stream. Additionally, when the optional AXI4-Lite interface is selected, the signal driving the s_axis_aclk pin should be constrained.

Device, Package, and Speed Grade Selections

There are no device, package or speed grade requirements for this core. For a complete list of supported devices, see the release notes for this core.

Clock Frequencies

The required pixel clock (ACLK) frequency is at least 105% of the average nominal video data rate. For example, for 1080p60 video, the video clock frequency is 148.5 MHz, with an average data rate of 124.416 MSPS. The ACLK frequency required for the MANR core to keep up with the 1080p60 data stream without applying backpressure is $1.05 \times 124.416 = 131$ MHz. For more information, see Maximum Frequency in Chapter 2. The S_AXI_ACLK pin should be constrained to the AXI4-Lite interconnect clock rate to ensure that the core can communicate the AXI interconnect.

Clock Management

The core automatically handles clock domain crossing between the ACLK (video pixel clock for AXI4-Stream) and the S_AXI_ACLK (AXI4-Lite) clock domains. The S_AXI_ACLK clock

can be slower or faster than the ACLK clock signal, but must not be more than 128x faster than ACLK.

Clock Placement

There are no specific Clock placement requirements for this core.

Banking

There are no specific Banking requirements for this core.

Transceiver Placement

There are no transceiver placement requirements for this core.

I/O Standard and Placement

There are no specific I/O standards and placement requirements for this core.

Detailed Example Design

No example design is available for the Motion Adaptive Noise Reduction core at the time.

For a comprehensive listing of the latest Video and Imaging application notes, white papers, reference designs and related IP cores, see the Video and Imaging Resources page:

www.xilinx.com/esp/video/refdes_listing.htm

Demonstration Test Bench

A demonstration test bench is provided to enable you to observe core behavior in a typical use scenario. You can download the functional test bench from the Motion Adaptive Noise Reduction page:

www.xilinx.com/products/intellectual-property/EF-DI-IMG-MA-NOISE.htm

SECTION III: ISE DESIGN SUITE

Customizing and Generating the Core

Constraining the Core

Detailed Example Design

Customizing and Generating the Core

This chapter includes information on using Xilinx tools to customize and generate the core in the ISE® Design Suite.

Graphical User Interface

The Xilinx® Motion Adaptive Noise Reduction (MANR) LogiCORE IP is easily configured to meet the developer's specific needs through the CORE Generator™ or Embedded Development Kit (EDK) Graphical User Interface (GUI). This section provides a quick reference to parameters that can be configured at generation time. Figure 8-1 shows the CORE Generator GUI main screen. The EDK GUI is shown in Figure 8-2.

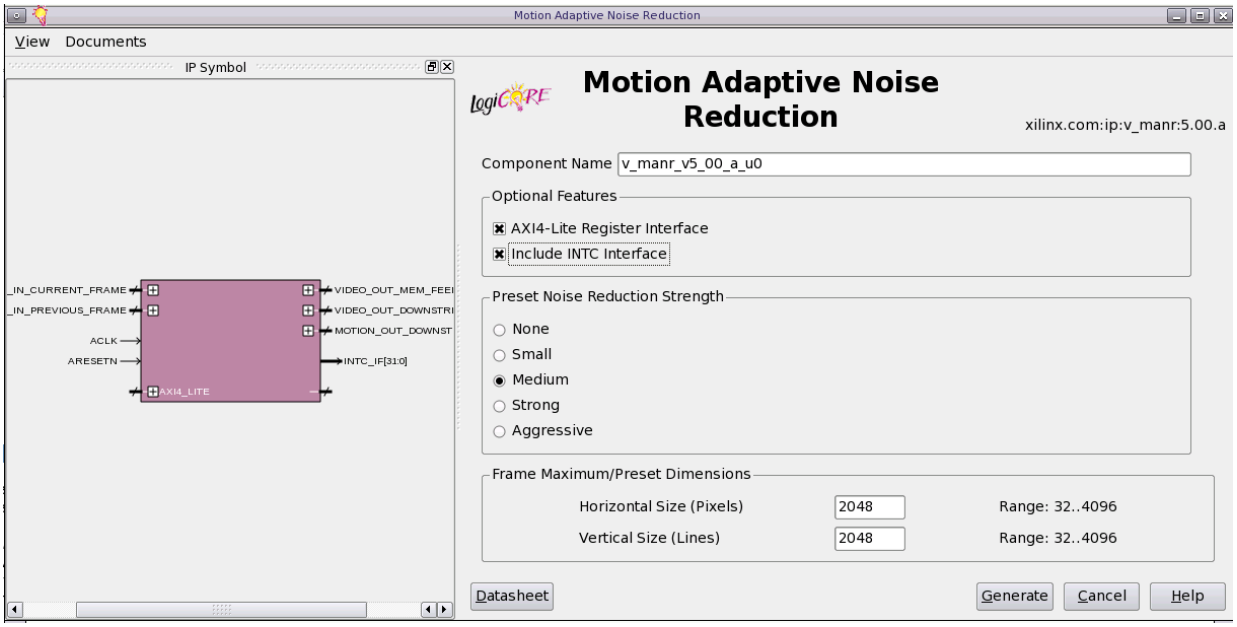

Figure 8-1: **CORE Generator MANR Main Screen**

The main screen displays a representation of the IP symbol on the left side, and the parameter assignments on the right side, which are described as follows:

- **Component Name:** The component name is used as the base name of output files generated for the module. Names must begin with a letter and must be composed from characters: a to z, A to Z, 0 to 9 and "_".

Note: The name "v_manr_v5_01_a" is not allowed.

- **Noise Reduction Strength:** This parameter selects the default MTF. The MTF is initialized according to one of the following settings. The MTF is fully programmable, and the initial values specified during core generation can easily be overridden by programming the desired MTF at run time.
  - None: Specifies all zeroes for MTF; bypasses noise reduction such that the output pixel always equals the input pixel.
  - Small: Specifies ¼ gain exponential curve for MTF
  - Medium: Specifies ½ gain exponential curve for MTF
  - Strong: Specifies ¾ gain exponential curve for MTF
  - Aggressive: Specifies full gain exponential curve for MTF
- **Frame Maximum/Preset Dimensions:** These fields represent the maximum anticipated rectangle size on the input and output of the MANR core. The rectangle can vary from 32x32 through 4096x4096. When the core is being used in Fixed mode (AXI4_LITE is disabled), these figures represent the fixed frame dimensions.
- Optional Features:
  - **AXI4-Lite Register Interface:** When selected, the core is generated with an AXI4-Lite interface, which gives access to dynamically program and change processing parameters. For more information, see Control Interface in Chapter 2.
  - **INT_IF interface:** When selected, interrupts are generated on this bus. See Interrupt Subsystem in Chapter 2 for more details.

EDK GUI

Definitions of the EDK GUI controls, shown in Figure 8-2, are identical to the corresponding CORE Generator GUI functions.

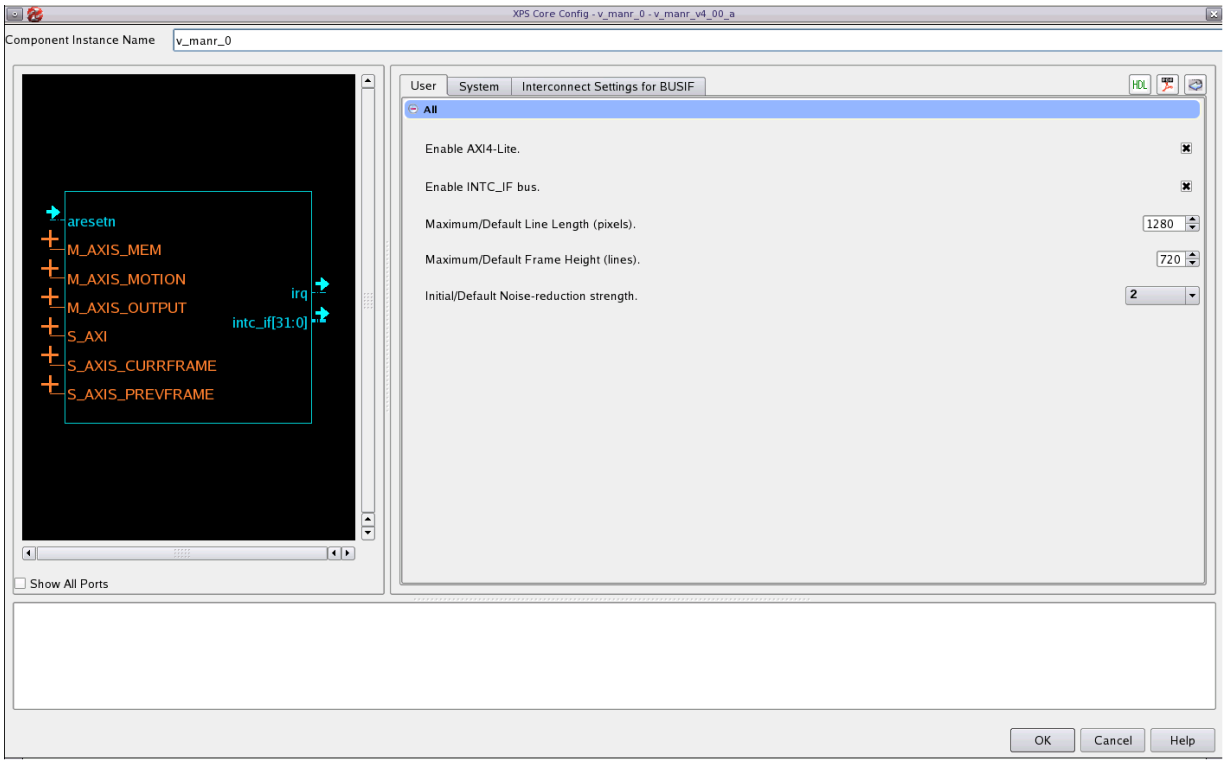

Figure 8-2: **MANR EDK Main Screen**

Constraining the Core

This chapter contains applicable constraints for the MANR core.

Required Constraints

The ACLK pin should be constrained at the pixel clock rate desired for the video stream. Additionally, when the optional AXI4-Lite interface is selected, the signal driving the s_axis_aclk pin should be constrained.

Device, Package, and Speed Grade Selections

There are no device, package or speed grade requirements for this core. For a complete list of supported devices, see the release notes for this core.

Clock Frequencies

The pixel clock (ACLK) frequency is the required frequency for this core. See Maximum Frequency in Chapter 2. The S_AXI_ACLK maximum frequency is the same as the ACLK maximum.

Clock Management

The core automatically handles clock domain crossing between the ACLK (video pixel clock and AXI4-Stream) and the S_AXI_ACLK (AXI4-Lite) clock domains. The S_AXI_ACLK clock can be slower or faster than the ACLK clock signal, but must not be more than 128x faster than ACLK.

Clock Placement

There are no specific Clock placement requirements for this core.

Banking

There are no specific Banking requirements for this core.

Transceiver Placement

There are no transceiver placement requirements for this core.

I/O Standard and Placement

There are no specific I/O standards and placement requirements for this core.

Detailed Example Design

No example design is available for the Motion Adaptive Noise Reduction core at the time.

For a comprehensive listing of the latest Video and Imaging application notes, white papers, reference designs and related IP cores, see the Video and Imaging Resources page:

www.xilinx.com/esp/video/refdes_listing.htm

Demonstration Test Bench

A demonstration test bench is provided to enable you to observe core behavior in a typical use scenario. You can download the functional test bench from the Motion Adaptive Noise Reduction page:

www.xilinx.com/products/intellectual-property/EF-DI-IMG-MA-NOISE.htm

SECTION IV: APPENDICES

Verification, Compliance, and Interoperability

Migrating

Debugging

Application Software Development

Additional Resources

XILINX®

Appendix A

Verification, Compliance, and Interoperability

This appendix includes details on simulation and testing.

Simulation

A parameterizable test bench was used to test the MANR core. Testing included the following:

- Register accessing
- Processing of multiple frames of data
- Various frame sizes
- Various MANR strengths
- Various AXI4-Stream data bus widths.

Hardware Testing

The MANR core has been tested in a variety of hardware platforms at Xilinx for various parameterizations, including the following:

- A test design was developed for the core that incorporated a MicroBlaze™ processor, AXI4 interface and various other peripherals, as described in Chapter 10, Detailed Example Design.
- The software for the test system included input frames embedded in the source-code. The checksums of the processed images were also pre-calculated and included in the software. The frames, resident in external memory, are read by the AXI_VDMA, processed by the MANR and the result is passed back to memory. Software then accesses the processed frame in memory and calculates its checksum. This matches the pre-calculated checksum.

- Various configurations were implemented in this way. The C model was used to create the expected checksums and generate the stimulus C code frame data that is compiled into the software.
- Pass/fail status is reported by the software.

In addition, the MANR core has been more regularly tested using an automated validation flow. Primarily, this instantiates the core in order to read registers back, validating the core Version register and proving that it has been implemented in the design. This has been run regularly in order to validate new core versions during development, and also to guard against EDK tools regressions.

Appendix B

Migrating

This appendix describes migrating from older versions of the IP to the current IP release.

From v5.00.a to v5.01.a of the MANR core, the following changes took place:

- Support for 1080p60 video has been added for all Zynq™, Virtex®-7, Kintex™-7, and Artix™-7 devices.
- A new version of the Embedded Development Kit (EDK) driver was created.

From v4.00.a to v5.00.a of the MANR core, the following significant changes took place:

- AXI4-Stream Interface usage was updated. It no longer supports the AXI4-Stream tKeep usage. It now uses the AXI4-Stream tUser pin as a Start-of-Frame indicator.
- The GPP control option has been removed. The core can now only be controlled dynamically by using the AXI4-Lite interface.
- The core now supports a Constant (Fixed-mode) option whereby parameters such as image size and noise-reduction level are specified in the configuration GUI. You can select from one of the pre-loaded MTF curves ("None", "Weak", "Medium", "Strong" or "Aggressive").
- Core Feature Changes:
  - The MANR v3.0 provided the motion data output as part of the m_axis_output bus. In v5.00.a, the core now supports an independent AXI4-Stream output for the motion data. The v5.00.a core uses two input AXI4-Stream interfaces (current and previous frames) plus three output AXI4-Stream interfaces (downstream video, temporal feedback video, and downstream motion).
  - In v3.0, the MTF table was common for Y and C processing. The core now supports independent Y and C MTF curve storage.
  - As with v3.0, the v5.00.a core includes five pre-loaded MTF curves. However, the v5.00.a core provides dynamic access to all the pre-loaded MTF curves using the AXI4-Lite control interface.

Debugging

This appendix includes details about resources available on the Xilinx® Support website and debugging tools. In addition, this appendix provides a step-by-step debugging process and a flow diagram to guide you through debugging the MANR core.

The following topics are included in this appendix:

Finding Help on Xilinx.com

To help in the design and debug process when using the MANR core, the Xilinx Support web page (www.xilinx.com/support) contains key resources such as product documentation, release notes, answer records, information about known issues, and links for opening a Technical Support WebCase.

Documentation

This product guide is the main document associated with the MANR core. For the Video over AXI4-Stream specification, see *AXI4-Stream Video IP and System Design Guide (UG934)* [Ref 5]. These guides, along with documentation related to all products that aid in the design process, can be found on the Xilinx Support web page (www.xilinx.com/support) or by using the Xilinx Documentation Navigator.

Download the Xilinx Documentation Navigator from the Design Tools tab on the Downloads page (www.xilinx.com/download). For more information about this tool and the features available, open the online help after installation.

Release Notes

Known issues for all cores, including the MANR core are described in the IP Release Notes Guide (XTP025).

Solution Centers

See the Xilinx Solution Centers for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

Known Issues

Answer Records include information about commonly encountered problems, helpful information on how to resolve these problems, and any known issues with a Xilinx product. Answer Records are created and maintained daily ensuring that users have access to the most accurate information available.

Answer Records for this core are listed below, and can also be located by using the Search Support box on the main Xilinx support web page. To maximize your search results, use proper keywords such as

- Product name
- Tool message(s)
- Summary of the issue encountered

A filter search is available after results are returned to further target the results.

Answer Records for the MANR

Known issues for all cores, including the MANR core are described in the IP Release Notes Guide (XTP025).

Contacting Technical Support

Xilinx provides premier technical support for customers encountering issues that require additional assistance.

To contact Xilinx Technical Support:

1. Navigate to www.xilinx.com/support.
2. Open a WebCase by selecting the WebCase link located under Support Quick Links.

When opening a WebCase, include:

- Target FPGA including package and speed grade.
- All applicable Xilinx Design Tools and simulator software versions.
- A block diagram of the video system that explains the video source, destination and IP (custom and Xilinx) used.
- Additional files based on the specific issue might also be required. See the relevant sections in this debug guide for guidelines about which file(s) to include with the WebCase.

Debug Tools

There are many tools available to address MANR core design issues.

Example Design

No example design is delivered with the MANR; however, you can generate a functional test bench for an instantiation of the video core. For more information, see *Demonstration Test Bench*.

ChipScope Pro Tool

The ChipScope™ Pro debugging tool inserts logic analyzer, bus analyzer, and virtual I/O cores directly into your design. The ChipScope Pro debugging tool allows you to set trigger conditions to capture application and integrated block port signals in hardware. Captured signals can then be analyzed through the ChipScope Pro logic analyzer tool. For detailed information for using the ChipScope Pro debugging tool, see www.xilinx.com/tools/cspro.htm.

Vivado Lab Tools

Vivado Lab Tools inserts logic analyzer, bus analyzer, and virtual I/O cores directly into your design. Vivado Lab Tools allows you to set trigger conditions to capture application and integrated block port signals in hardware. Captured signals can then be analyzed.

Reference Boards

Various Xilinx development boards support MANR. These boards can be used to prototype designs and establish that the core can communicate with the system.

- 7 series FPGA evaluation boards
  - KC705
  - ZC702

C-Model Reference

Please see *Chapter 4, C Model Reference* for tips and instructions for using the provided C-Model files to debug your design.

License Checkers

If the IP requires a license key, the key must be verified. The ISE® Design Suite and Vivado™ Design Suite have several license check points for gating licensed IP through the flow. If the license check succeeds, the IP can continue generation. Otherwise, generation halts with error. License checkpoints are enforced by the following design tools.

- **ISE flow**: XST, NgdBuild, Bitgen
- **Vivado flow**: Vivado Synthesis, Vivado Implementation, `write_bitstream` (Tcl command)

IMPORTANT: *IP license level is ignored at checkpoints. The test confirms a valid license exists. It does not check IP license level.*

Hardware Debug

This section provides debug steps for bring-up, lock-up and synchronization issues. The ChipScope debugging tool is a valuable resource to use in hardware debug. The signal names mentioned in the following individual sections can be probed using the ChipScope debugging tool for debugging the specific problems. Many of these common issues can also be applied to debugging design simulations.

General Checks

Ensure that all the timing constraints for the core were properly incorporated from the example design and that all constraints were met during implementation.

- Does it work in post-place and route timing simulation? If problems are seen in hardware but not in timing simulation, this could indicate a PCB issue. Ensure that all clock sources are active and clean.
- If using MMCMs in the design, ensure that all MMCMs have obtained lock by monitoring the `LOCKED` port.
- The evaluation version of the core will time out after running for 8 hours at 75 MHz. If the design works initially, but eventually outputs go to 0, check that all licensed cores in the design have bought licenses.

Interface Debug

AXI4-Lite Interfaces

Table C-1: **Troubleshooting the AXI4-Lite Interfaces**

Symptom	Solution
Readback from the Version Register through the AXI4-Lite interface times out, or a core instance without an AXI4-Lite interface seems non-responsive.	Are the `S_AXI_ACLK` and `ACLK` pins connected? In EDK, verify that the S_AXI_ACLK and ACLK pin connections in the `system.mhs` file. The `VERSION_REGISTER` readout issue can be indicative of the core not receiving the AXI4-Lite interface.
	Is the core enabled? Is `s_axi_aclken` connected to `vcc`? In EDK, verify that the `ACLKEN` signal is connected in the `system.mhs` file to either `net_vcc` or to a designated clock enable signal.
	Is the core in reset? `S_AXI_ARESETn` and `ARESETn` should be connected to `vcc` for the core not to be in reset. In EDK, verify that the `S_AXI_ARESETn` and `ARESETn` signals are connected in the `system.mhs` file to either `net_vcc` or to a designated reset signal.

Table C-1: **Troubleshooting the AXI4-Lite Interfaces *(Cont'd)***

Symptom	Solution
Readback value for the VERSION_REGISTER is different from expected default value.	The core and/or the driver in a legacy EDK/SDK project has not been updated. Ensure that old core versions, implementation files, and implementation caches have been cleared.
	The address maps between software and hardware could get out of sync. Regenerate addresses in EDK, and make sure the MHS file in EDK and the `xparameters.h` file in the SDK project are up to date.
Readback values from registers are stuck, and cannot be overwritten.	Is the target address writable?

Assuming the AXI4-Lite interface works, the second step is to bring up the AXI4-Stream interfaces.

AXI4-Stream Interfaces

Table C-2: **Troubleshooting AXI4-Stream Interface**

Symptom	Solution
Bit 0 of the ERROR register reads back set.	Bit 0 of the `ERROR` register, `CURR_EOL_ERROR`, indicates the number of pixels received between the latest and the preceding End-Of-Line (EOL) signal on the `s_axis_currframe` interface was not equal to the value programmed into the lower word of the `FRAME_SIZE` register. If the value was provided by the Video Timing Controller core, read out the `ACTIVE_SIZE` register value from the VTC core again, and make sure that the `TIMING_LOCKED` flag is set in the VTC core. Otherwise, using ChipScope, measure the number of active AXI4-Stream transactions between EOL pulses.
Bit 2 of the ERROR register reads back set.	Bit 2 of the `ERROR` register, `CURR_SOF_ERROR`, indicates the number of lines received between the latest and the preceding Start-Of-Frame (SOF) signal on the `s_axis_currframe` interface was not equal to the value programmed into the upper word of the `FRAME_SIZE` register. If the value was provided by the Video Timing Controller core, read out the `ACTIVE_SIZE` register value from the VTC core again, and make sure that the `TIMING_LOCKED` flag is set in the VTC core. Otherwise, use ChipScope to measure the number of valid EOL pulse transactions between SOF pulses. Using ChipScope, verify that for the first valid transaction on the `s_axis_currframe` interface `TUSER0` (SOF) is high, and SOF is low for subsequent transactions until the beginning of the next frame.
Bit 4 of the ERROR register reads back set.	Bit 4 of the `ERROR` register, `PREV_EOL_ERROR`, indicates the number of pixels received between the latest and the preceding End-Of-Line (EOL) signal on the `s_axis_prevframe` interface was not equal to the value programmed into the lower word of the `FRAME_SIZE` register. If the value was provided by the Video Timing Controller core, read out the `ACTIVE_SIZE` register value from the VTC core again, and make sure that the `TIMING_LOCKED` flag is set in the VTC core. Otherwise, use ChipScope to measure the number of active AXI4-Stream transactions between EOL pulses.

Table C-2: **Troubleshooting AXI4-Stream Interface *(Cont'd)***

Symptom	Solution
Bit 6 of the ERROR register reads back set.	Bit 6 of the ERROR register, PREV_SOF_ERROR, indicates the number of lines received between the latest and the preceding Start-Of-Frame (SOF) signal on the s_axis_prevframe interface was not equal to the value programmed into the upper word of the FRAME_SIZE register. If the value was provided by the Video Timing Controller core, read out the ACTIVE_SIZE register value from the VTC core again, and make sure that the TIMING_LOCKED flag is set in the VTC core. Otherwise, use ChipScope to measure the number of valid EOL pulse transactions between SOF pulses. Using ChipScope, verify that for the first valid transaction on the s_axis_prevframe interface TUSER0 (SOF) is high, and SOF is low for subsequent transactions until the beginning of the next frame.
No output video on s_axis_output.	Use ChipScope or system simulation to identify which components of the video processing system are stalled. Probe the TVALID and TREADY signals on AXI4-Stream interfaces, and find a slave interface with TVALID high, TREADY low. Likely this is the component that locked up.
s_axis_video_tready stuck low, the upstream core cannot send data.	During initialization, line-, and frame-flushing, the MANR core keeps its s_axis_currframe_tready and s_axis_prevframe_tready inputs low. Afterwards, the core should assert the tready signals automatically. Also, the MANR core can only process data if *all* output (master) AXI4-Stream interface TREADY inputs are high, and data is available on both prev and curr inputs (TVALID high). The core has internal FIFOs on all inputs and outputs, which help even out periodic back-pressures on the different interfaces. However, average data rates are identical on all AXI4-Stream interfaces. If one of the output interfaces encounter periodic back-pressure, this back-pressure will be propagated to upstream components.
m_axis_video_tvalid stuck low, the downstream core is not receiving data.	No data is generated during the first 26 ACLK cycles of processing. If the programmed active number of pixels per line is radically smaller than the actual line length, the core drops most of the pixels waiting for the (s_axis_video_tlast) End-of-line signal. Check the ERROR register.
Generated SOF signal (m_axis_video_tuser0) signal is misplaced.	Check the ERROR register.
Generated EOL signal (m_axis_video_tlast) signal is misplaced.	Check the ERROR register.
Data samples are lost between Upstream core and the MANR core. Inconsistent EOL and/or SOF periods are received.	Are the Master and Slave AXI4-Stream interfaces in the same clock domain? If not, is proper clock-domain crossing logic instantiated between the upstream core and the MANR core (Asynchronous FIFO)? Did the design meet timing? Is the frequency of the clock source driving the MANR ACLK pin lower than the reported Fmax reached?

Table C-2: **Troubleshooting AXI4-Stream Interface *(Cont'd)***

Symptom	Solution
Data samples lost between Downstream core and the MANR core. Inconsistent EOL and/or SOF periods received.	Are the Master and Slave AXI4-Stream interfaces in the same clock domain? Is proper clock-domain crossing logic instantiated between the upstream core and the MANR core (Asynchronous FIFO)? Did the design meet timing? Is the frequency of the clock source driving the MANR `ACLK` pin lower than the reported Fmax reached?
Excessive ghosting between image regions tens / hundreds of pixels apart.	The `s_axis_currframe` and `s_axis_prevframe` channels got out of sync. A likely scenario that can cause this failure is a partial frame fed to the MANR. The application software should monitor both the VDMA and the MANR error registers, and should reset or reinitialize the system after errors were indicated.

Third-Party IP Interfaces

Table C-3 describes how to troubleshoot third-party interfaces.

Table C-3: **Troubleshooting Third-Party Interfaces**

Symptom	Solution
Severe color distortion or color-swap when interfacing to third-party video IP.	Verify that the color component logical addressing on the AXI4-Stream `TDATA` signal is set according to Data Interface in Chapter 2. If misaligned: • In HDL, break up the `TDATA` vector to constituent components and manually connect the slave and master interface sides. • In EDK, create a new vector for the slave side `TDATA` connection. In the MPD file, manually assign components of the master-side `TDATA` vector to sections of the new vector.
Severe color distortion or color-swap when processing video written to external memory using the AXI-VDMA core.	Unless the particular software driver was developed with the AXI4-Stream `TDATA` signal color component assignments described in Data Interface in Chapter 2, there are no guarantees that the software correctly identifies bits corresponding to color components. Verify that the color component logical addressing `TDATA` is in alignment with the data format expected by the software drivers reading/writing external memory. If misaligned: • In HDL, break up the `TDATA` vector to constituent components, and manually connect the slave and master interface sides. • In EDK, create a new vector for the slave side `TDATA` connection. In the MPD file, manually assign components of the master-side `TDATA` vector to sections of the new vector.

Application Software Development

This appendix details the use of the software drivers that are included with the EDK pCore version of the MANR core.

Device Drivers

EDK pCore Driver Files

The MANR Embedded Development Kit (EDK) pCore includes a software driver written in the C programming language that the user can use to control the core. A high-level API provides application developers easy access to the features of the MANR core. A low-level API is also provided for developers to access the core directly through the system registers.

EDK pCore API Functions

This section describes the functions included for the EDK pCore driver generated for the MANR pCore. To use the API functions provided, the following header files must be included in your C code:

```
#include "xparameters.h"
#include "xmanr.h"
```

The system hardware settings, including the base address of the MANR core, are defined in the `xparameters.h` file. The `xmanr.h` file provides the API access to all of the features of the MANR device driver.

More detailed documentation of the API functions can be found by opening `index.html` in the pCore directory `manr_v1_01_a/doc/html/api`.

Functions in xmanr.c

- `int XMANR_CfgInitialize (XMANR *InstancePtr, XMANR_Config *CfgPtr, u32 EffectiveAddr)`

  This function initializes a MANR core.

- `void XMANR_SetFrameSize (XMANR *InstancePtr, u32 Height, u32 Width, u32 Stride)`

  This function sets up the frame size information used by a MANR device. Note that 'stride' parameter is now obsolete and set to 0.

- `void XMANR_GetFrameSize (XMANR *InstancePtr, u32 *HeightPtr, u32 *WidthPtr, u32 *StridePtr)`

  This function sets up the frame size information used by a MANR device. Note that 'StridePtr' is now obsolete.

- `void XMANR_LoadMtfBank(XMANR *InstancePtr, u8 BankIndex, u32 *MTFData)`

  This function loads the Motion Transfer LUT configuration to be used by a MANR device.

- `void XMANR_GetVersion(XMANR *InstancePtr, u16 *Major, u16 *Minor, u16 *Revision)`

  This function returns the version of a MANR device.

Functions in xmanr_sinit.c

- `XMANR_Config * XMANR_LookupConfig (u16 DeviceId)`

  XMANR_LookupConfig returns a reference to a XMANR_Config structure based on the unique device ID, DeviceId.

Functions in xmanr_intr.c

- `void XMANR_IntrHandler (void *InstancePtr)`

  This function is the interrupt handler for the MANR driver.

- `int XMANR_SetCallBack (XMANR *InstancePtr, u32 HandlerType, void *CallBackFunc, void *CallBackRef)`

  This routine installs an asynchronous callback function for the given HandlerType.

Additional Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see the Xilinx Support website at:

http://www.xilinx.com/support.

For a glossary of technical terms used in Xilinx documentation, see:

http://www.xilinx.com/support/documentation/sw_manuals/glossary.pdf.

For a comprehensive listing of Video and Imaging application notes, white papers, reference designs and related IP cores, see the Video and Imaging Resources page:

www.xilinx.com/esp/video/refdes_listing.htm

References

These documents provide supplemental material useful with this user guide:

1. AMBA® AXI4-Stream Protocol Specification
2. *LogiCORE IP FIFO Generator Product Guide* (PG057)
3. *Xilinx AXI Reference Guide* (UG761)
4. *LogiCORE IP AXI Interconnect Product Guide (PG059)*
5. *AXI4-Stream Video IP and System Design Guide* (UG934)

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
10/19/2011	1.0	Initial Xilinx release.
04/24/2012	2.0	Updated core to v4.00a and ISE Design Suite to v14.1.

Date	Version	Revision
07/25/2012	3.0	Updated core to v5.00.a. Added support for Vivado Design Suite implementations.
12/18/2012	3.1	• Updated for core v5.01.a, ISE Design Suite v14.4 and Vivado Design Suite v2012.4. • Updated resource and performance data. • Updated register interface documentation. • Added Appendix C, Debugging.

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