LogiCORE IP XAUI v10.3

DS266 April 24, 2012 **Product Specification**

Introduction

The eXtended Attachment Unit Interface (XAUI) core is a high-performance, low-pin count 10-Gb/s interface intended to allow physical separation between the data link layer and physical layer devices in a 10-Gigabit Ethernet system.

The XAUI core implements a single-speed full-duplex 10-Gb/s Ethernet eXtended Attachment Unit Interface (XAUI) solution for the Virtex®-7, Kintex™-7, Virtex-6, Virtex-5, Virtex-4, and Spartan®-6 Field Programmable Gate Array (FPGA) devices.

Features

- Designed to 10-Gigabit Ethernet *IEEE 802.3-2008* specification
- Supports 20G double-rate XAUI (Double XAUI) using four transceivers at 6.25 Gb/s. For devices and speed grades, see Speed Grades.
- Supports 10-Gigabit Fibre Channel (10-GFC) XAUI data rates and traffic
- Uses four transceivers at 3.125 Gb/s line rate to achieve 10-Gb/s data rate
- Implements Data Terminal Equipment (DTE) XGMII Extender Sublayer (XGXS), PHY XGXS, and 10GBASE-X Physical Coding Sublayer (PCS) in a single netlist
- *IEEE 802.3-2008* clause 45 Management Data Input/Output (MDIO) interface (optional)
- *IEEE 802.3-2008* clause 48 State Machines (optional for Virtex-6, Virtex-5 and Spartan-6 FPGAs)
- Available under the Xilinx End User License Agreement

LogiCORE IP Facts					
Core Specifics					
Supported Device Family [1]	Virtex-7, Kintex-7, Virtex-6, Spartan-6, Virtex-5, Virtex-4				
Supported User Interfaces	64-bit XGMII Interface				
Resources [2, 3]					
Configuration	**LUTs**	**FFs**	**Slices**	**Block RAMs**	**Max Freq**
	676-1361	644-1225	301-575	0	156.25 MHz
Provided with Core					
Documentation	Product Specification User Guide				
Design Files	Native Generic Circuit (NGC) netlist				
Example Design	VHSIC Hardware Description Language (VHDL) and Verilog				
Test Bench	VHDL Test Bench Verilog Test Fixture				
Constraints File	Xilinx Specific User Constraints File (UCF)				
Simulation Model	VHDL/Verilog				
Supported S/W Drivers	NA				
Tested Design Tools					
Design Entry Tools	CORE Generator tool Integrated Software Environment (ISE) v14.1 Design Suite				
Simulation [4]	Mentor Graphics ModelSim Cadence Incisive Enterprise Simulator (IES) Synopsys VCS and VCS MX				
Synthesis Tools	Xilinx Synthesis Technology (XST) 14.1				
Support					
Provided by Xilinx, Inc.@ www.xilinx.com/support					

1. For the complete list of supported devices, see the release notes for this core. See Speed Grades for supported speed grades.
2. Resource utilizations for 20G are the same as those for 10 G. For detailed utilization numbers based upon configuration, see Table 11 through Table 17. For more complete device utilization numbers, see Table 13 through Table 17.
3. Resource utilization depends on target device and configuration. See Table 11 through Table 17 for detailed information.
4. For the supported versions of the tools, see the ISE Design Suite 14: Release Notes Guide.

Overview

XAUI is a four-lane, 3.125 Gb/s-per-lane serial interface. Each lane is a differential pair carrying current mode logic (CML) signaling, and the data on each lane is 8B/10B encoded before transmission. Special code groups are used to allow each lane to synchronize at a word boundary and to deskew all four lanes into alignment at the receiving end. The XAUI standard is fully specified in clauses 47 and 48 of the 10-Gigabit Ethernet *IEEE 802.3-2008* specification.

The XAUI standard was initially developed as a means to extend the physical separation possible between Media Access Controller (MAC) and PHY components in a 10-Gigabit Ethernet system distributed across a circuit board and to reduce the number of interface signals in comparison with the XGMII (10-Gigabit Ethernet Media Independent Interface).

Applications

Figure 1 shows the XAUI core connecting a 10-Gigabit Ethernet MAC to a 10-Gigabit XPAK optical module.

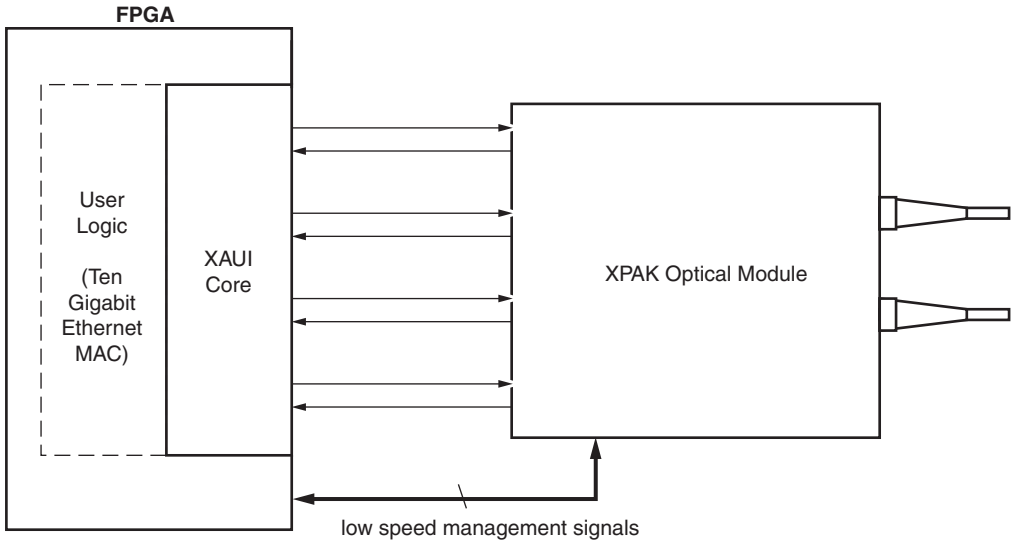

Figure 1: **XAUI Connecting a 10-Gigabit Ethernet MAC to an Optical Module**

After its publication, the applications of XAUI have extended beyond 10-Gigabit Ethernet to the backplane and other general high-speed interconnect applications. Figure 2 shows a typical backplane application.

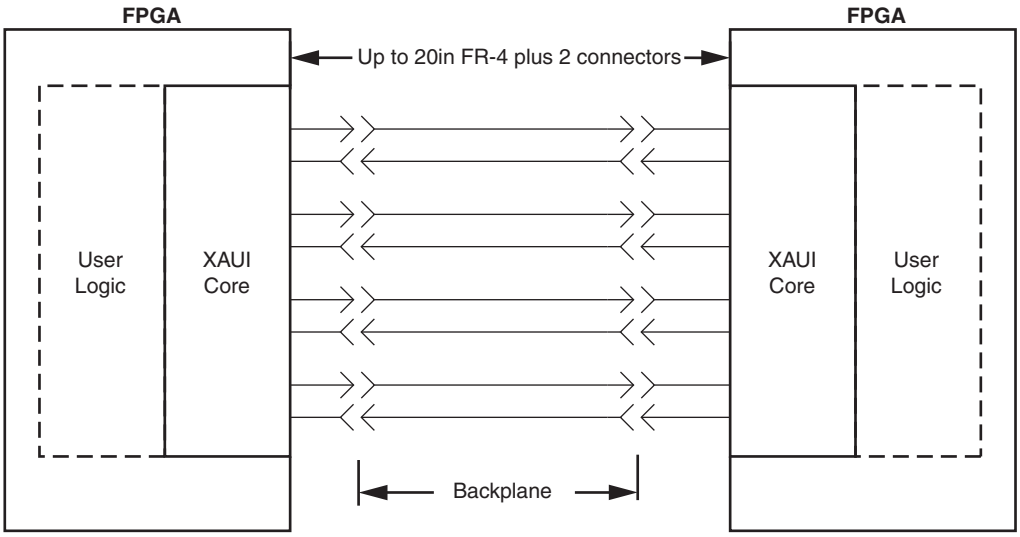

Figure 2: **Typical Backplane Application for XAUI**

Functional Description

Figure 3 shows a block diagram of the XAUI core implementation. The major functional blocks of the core include the following:

- **Transmit Idle Generation Logic** creates the code groups to allow synchronization and alignment at the receiver.
- **Synchronization State Machine (one per lane)** identifies byte boundaries in incoming serial data.
- **Deskew State Machine** de-skews the 4 received lanes into alignment.
- **Optional MDIO Interface** is a two-wire low-speed serial interface used to manage the core.
- **Four Device-Specific Transceivers** (integrated in the FPGAs) provide the high-speed transceivers as well as 8B/10B encode and decode and elastic buffering in the receive datapath.

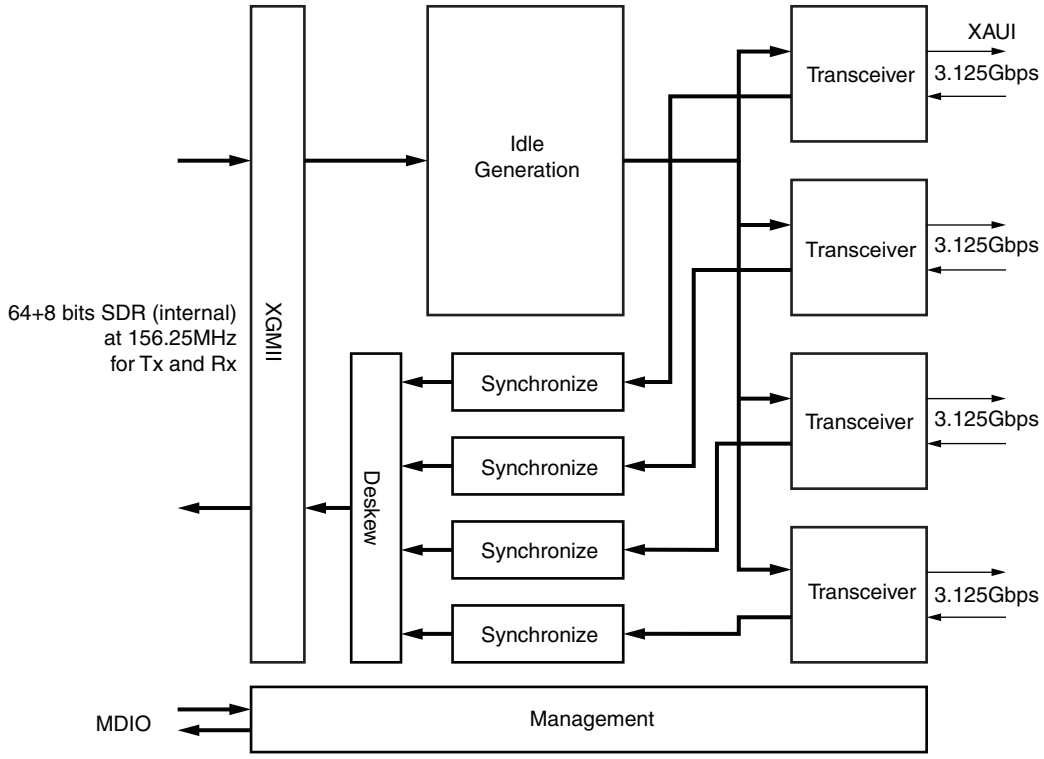

Figure 3: **Implementation of XAUI Core**

The core is implemented with the device-specific transceiver instantiations in the source code rather than in the netlist. This gives you more flexibility in a particular application to use additional device-specific transceiver features and resolve placement issues.

Core Interfaces

XAUI Interface

The XAUI interface consists of four differential transmit and receive pairs plus four low-speed control inputs to indicate the status of an attached optical module. The differential pairs are generated by the device-specific transceiver. The control input signals are connected directly to the core. These signals are described in Table 1.

Table 1: **XAUI Interface Ports**

Signal Name	Direction	Description
SIGNAL_DETECT[3:0]	IN	Signals from a 10GBASE-LX4 optical module indicating the optical receivers are illuminated by a signal. If unused, tie this bus to 1111.

Transceiver Interface

The device-specific transceiver interface is the internal connection between the XAUI core netlist and the serial transceivers that provide the XAUI interface. For detailed descriptions of the functions of these signals, see the transceiver user guides. Table 2 describes these signals.

Table 2: **Transceiver Interface Ports**

Signal Name	Direction	Description
MGT_TXDATA	OUT	Data to serial transceivers
MGT_TXCHARISK	OUT	Control to serial transceivers
MGT_RXDATA	IN	Data from serial transceivers
MGT_RXCHARISK	IN	Control from serial transceivers
MGT_CODEVALID	IN	Code error signals from each serial transceiver
MGT_CODECOMMA	IN	Code comma signals from each serial transceiver
MGT_ENABLE_ALIGN	OUT	Enable comma align signals to each serial transceiver
MGT_ENCHANSYNC	OUT	Enable channel sync signal to the serial transceivers
MGT_SYNCOK	IN	Sync OK signals from each serial transceiver
MGT_RXLOCK	IN	Receive lock signals from each serial transceiver
MGT_LOOPBACK	OUT	Loopback enable signal to each serial transceiver
MGT_POWERDOWN	IN	Power down signal to each serial transceiver

Client-Side Interface

The client-side interface is a 72-bit (64 data bits and 8 control bits) interface running at 156.25 MHz based on the XGMII standard. It is designed to be connected to either user logic within the FPGA.

Table 3: **Client-Side Interface Ports**

Name	Direction	Description
XGMII_TXD[63:0]	IN	Transmit data, 8 bytes wide
XGMII_TXC[7:0]	IN	Transmit control bits, one bit per transmit data byte.
XGMII_RXD[63:0]	OUT	Received data, 8 bytes wide
XGMII_RXC[7:0]	OUT	Receive control bits, one bit per received data byte.

Figure 4 illustrates transmitting a frame through the client-side interface.

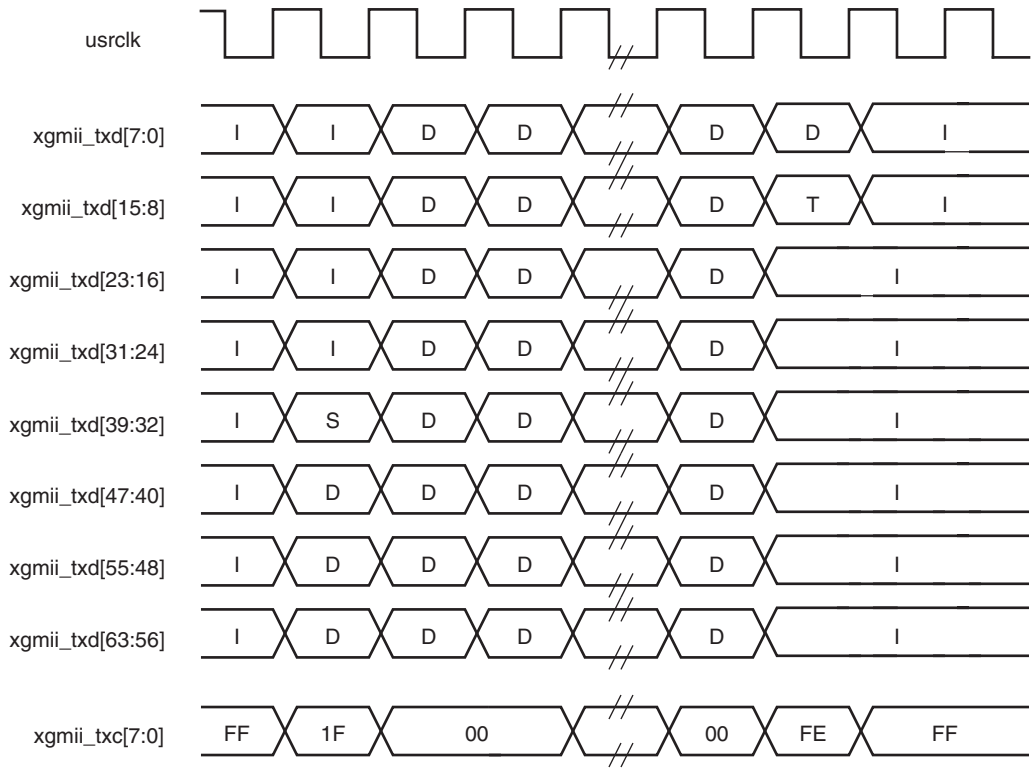

Figure 4: **Transmitting a Frame Through the Client-Side Interface**

Figure 5 illustrates receiving a frame through the client-side interface.

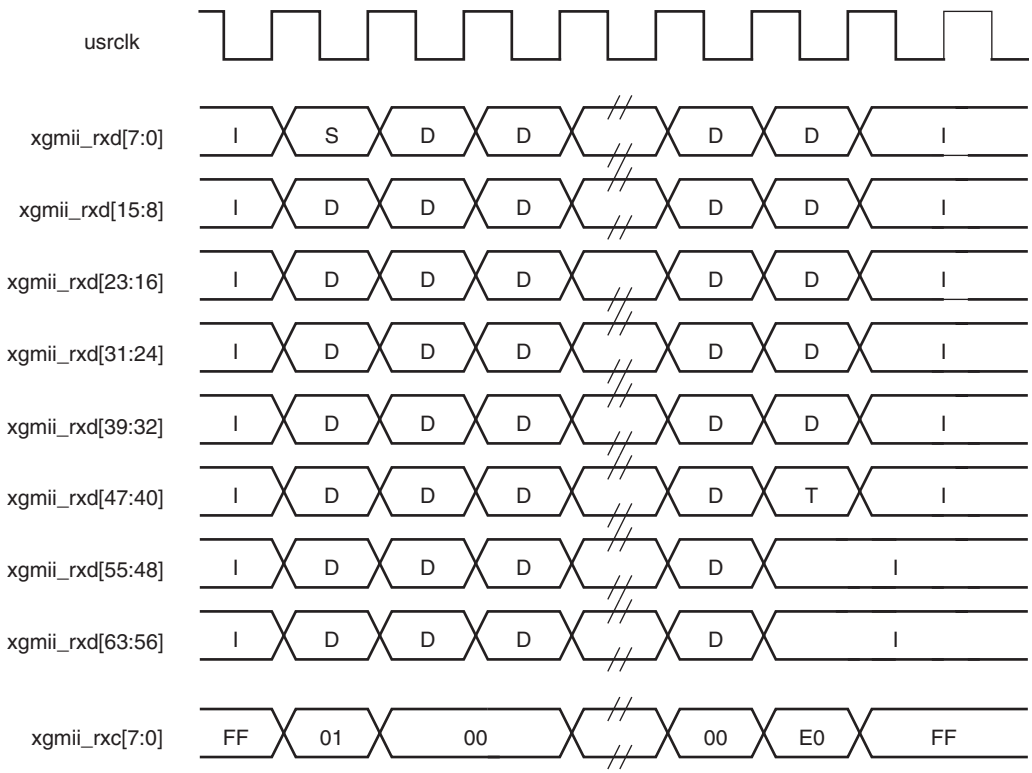

Figure 5: **Receiving a Frame Through the Client-Side Interface**

Management Interface (MDIO)

The MDIO interface is a simple low-speed two-wire interface for management of the XAUI core, consisting of a clock signal and a bidirectional data signal. The interface is defined in clause 45 of *IEEE 802.3-2008* standard.

In the XAUI core, the MDIO interface is an optional block. If implemented, the bidirectional data signal MDIO is implemented as three unidirectional signals. These can be used to drive a 3-state buffer either in the FPGA IOB or in a separate device.

There are additional signals that control the behavior of the core MDIO interface, specifically to set its position in the MDIO memory map.

Table 4: **MDIO Management Interface Ports**

Signal Name	Direction	Description
MDC	IN	Management clock
MDIO_IN	IN	MDIO input
MDIO_OUT	OUT	MDIO output
MDIO_TRI	OUT	MDIO 3-state. '1' disconnects the output driver from the MDIO bus.
TYPE_SEL[1:0]	IN	Type select. Determines which MDIO Register addresses the core responds to. type_sel = '00' or '01' – 10GBASE-X PCS type_sel = '10' – DTE XS type_sel = '11' – PHY XS See the *XAUI User Guide* for the MDIO Register addresses responded to in each case.
PRTAD[4:0]	IN	MDIO port address. When multiple MDIO-managed ports appear on the same bus, this address can be used to address each one individually.

Configuration and Status Signals

In addition to the pollable MDIO interface, the XAUI core continuously indicates its status on ports as defined in Table 5.

Table 5: **Configuration and Status Vector Ports**

Signal Name	Direction	Description
ALIGN_STATUS	OUT	'1' when the XAUI receiver is aligned across four lanes.
SYNC_STATUS[3:0]	OUT	Each pin is '1' when the respective XAUI lane receiver is synchronized to byte boundaries.
CONFIGURATION_ VECTOR[6:0]	IN	Configuration signals for the core. The bits are: Bit 0 - Loopback Bit 1 - Power down transceiver Bit 2 - Reset local fault status Bit 3 - Reset RX link status Bit 4 - Test Enable - '1' transmits test patterns on XAUI TX Bits 6:5 - Test pattern select For a more comprehensive description of these signals, consult the *XAUI User Guide*. This port only exists on the core if the MDIO interface is omitted.
STATUS_VECTOR[7:0]	OUT	Status indicators for the core. The bits are: Bit 0 - TX local fault Bit 1 - RX local fault Bit 5:2 - Synchronization - identical to SYNC_STATUS[3:0] Bit 6 - Alignment - identical to ALIGN_STATUS Bit 7 - RX link status For a more comprehensive description of these signals, consult the *XAUI User Guide*. This port only exists on the core if the MDIO interface is omitted.

Clock and Reset

Table 6 describes the clock and reset ports present on the core.

Table 6: **Clock and Reset Ports**

Name	Direction	Description
RESET	IN	Synchronous reset for core. The reference clock must be running for the core to emerge from the reset state.
USRCLK	IN	FPGA logic system clock.
MGT_TX_RESET	IN	Connect this to the same signal used to drive the serial transceiver TXRESET signal.
MGT_RX_RESET	IN	Connect this to the same signal used to drive the serial transceiver RXRESET signal.

MDIO Management Registers

The XAUI core, when generated with an MDIO interface, implements an MDIO Interface Register block. The core responds to MDIO transactions as either a 10GBASE-X PCS, a DTE XS, or a PHY XS depending on the setting of the `type_sel` port (see Table 4).

10GBASE-X PCS Registers

Table 7 shows the MDIO registers present when the XAUI core is configured as a 10GBASE-X PCS. For a more comprehensive description of the registers and their effect on core operation, see the *XAUI User Guide*.

Table 7: **10GBASE-X PCS/PMA MDIO Registers**

Register Address	Register Name
1.0	Physical Medium Attachment/Physical Medium Dependent (PMA/PMD) Control 1
1.1	PMA/PMD Status 1
1.2,1.3	PMA/PMD Device Identifier
1.4	PMA/PMD Speed Ability
1.5, 1.6	PMA/PMD Devices in Package
1.7	10G PMA/PMD Control 2
1.8	10G PMA/PMD Status 2
1.9	Reserved
1.10	10G PMD Receive Signal OK
1.11 to 1.13	Reserved
1.14, 1.15	PMA/PMD Package Identifier
1.16 to 1.65 535	Reserved
3.0	PCS Control 1
3.1	PCS Status 1
3.2, 3.3	PCS Device Identifier
3.4	PCS Speed Ability
3.5, 3.6	PCS Devices in Package
3.7	10G PCS Control 2
3.8	10G PCS Status 2
3.9 to 3.13	Reserved
3.14, 3.15	PCS Package Identifier
3.16 to 3.23	Reserved
3.24	10GBASE-X PCS Status
3.25	10GBASE-X Test Control
3.26 to 3.65 535	Reserved

DTE XS Registers

Table 8 shows the MDIO registers present when the XAUI core is configured as a DTE XS. For a more comprehensive description of the registers and their effect on core operation, see the *XAUI User Guide*.

Table 8: **DTE XS MDIO Registers**

Register Address	Register Name
5.0	DTE XS Control 1
5.1	DTE XS Status 1
5.2, 5.3	DTE XS Device Identifier
5.4	DTE XS Speed Ability
5.5, 5.6	DTE XS Devices in Package
5.7	Reserved
5.8	DTE XS Status 2
5.9 to 5.13	Reserved
5.14, 5.15	DTE XS Package Identifier
5.16 to 5.23	Reserved
5.24	10G DTE XGXS Lane Status
5.25	10G DTE XGXS Test Control

PHY XS Registers

Table 9 shows the MDIO registers present when the XAUI core is configured as a PHY XS. For a more comprehensive description of the registers and their effect on core operation, see the *XAUI User Guide*.

Table 9: **PHY XS MDIO Registers**

Register Address	Register Name
4.0	PHY XS Control 1
4.1	PHY XS Status 1
4.2, 4.3	PHY XS Device Identifier
4.4	PHY XS Speed Ability
4.5, 4.6	PHY XS Devices in Package
4.7	Reserved
4.8	PHY XS Status 2
4.9 to 4.13	Reserved
4.14, 4.15	PHY XS Package Identifier
4.16 to 4.23	Reserved
4.24	10G PHY XGXS Lane Status
4.25	10G PHY XGXS Test Control

10-Gigabit Fibre Channel Support

The 10-Gigabit Fibre Channel (10GFC) specification describes a XAUI interface similar to the 10-Gigabit Ethernet XAUI but operating at 2% higher line and data rates, equating to a line rate on each device-specific transceiver lane of 3.1875 Gb/s.

20-Gigabit XAUI (Double XAUI) Support

By running the XAUI interface at twice the normal clock and line rates, 20-Gigabit data rate can be achieved. For devices and speed grades, see Speed Grades. Consult the release notes for the core for the specific devices supported.

Verification

The XAUI core has been verified using both simulation and hardware testing.

Simulation

A highly parameterizable transaction-based simulation test suite was used to verify the core. Verification tests include:

- Register access over MDIO
- Loss and regain of synchronization
- Loss and regain of alignment
- Frame transmission
- Frame reception
- Clock compensation
- Recovery from error conditions

Hardware Verification

The core has been used in several hardware test platforms within Xilinx. In particular, the core has been used in a test platform design with the Xilinx® 10-Gigabit Ethernet MAC. This design comprises the MAC, XAUI, a *ping* loopback First In First Out (FIFO), and a test pattern generator all under embedded processor control. This design has been used for conformance and interoperability testing at the University of New Hampshire Interoperability Lab.

Speed Grades

The minimum device requirements for 10G and 20G operation are listed in the following table.

Table 10: **Speed Grades**

Device	XAUI (4x3.125G)	DXAUI (4x6.25G)
Virtex-7	-1	-1
Kintex-7	-1	-1[1]
Virtex-6 LXT/SXT/HXT	-1	-3
Virtex-6 CXT	-1	N/A
Spartan-6 LXT	-3	N/A
Virtex-5 FXT/LXT/SXT/TXT	-1	N/A
Virtex-4 FX	-10	N/A

1. For FFG packages only

Device Utilization

Virtex-7 FPGAs

Table 11 provides approximate slice counts for the various core options on Virtex-7 FPGAs.

Table 11: **Device Utilization – Virtex-7 FPGAs**

Parameter Values	Device Resources		
MDIO Interface	Slices	LUTs	FFs
No	324	532	553
Yes	388	683	648

Kintex-7 FPGAs

Table 12 provides approximate slice counts for the various core options on Kintex-7 FPGAs.

Table 12: **Device Utilization – Kintex-7 FPGAs**

Parameter Values	Device Resources		
MDIO Interface	Slices	LUTs	FFs
No	296	532	553
Yes	370	683	648

Virtex-6 FPGAs

Table 13 provides approximate slice counts for the various core options on Virtex-6 FPGAs.

Table 13: **Device Utilization – Virtex-6 FPGAs**

Parameter Values		Device Resources		
802.3ae State Machines	MDIO Interface	Slices	LUTs	FFs
No	No	301	676	644
No	Yes	375	826	745
Yes	No	359	798	712
Yes	Yes	423	947	807

Virtex-5 FPGAs

Table 14 and Table 15 provide approximate slice counts for the various core options on Virtex-5 FPGAs.

Table 14: **Device Utilization – Virtex-5 LXT/SXT FPGAs**

Parameter Values		Device Resources		
802.3ae State Machines	MDIO Interface	Slices	LUTs	FFs
No	No	432	564	652
No	Yes	518	715	753
Yes	No	551	712	718
Yes	Yes	644	863	815

Table 15: **Device Utilization – Virtex-5 FXT/TXT FPGAs**

Parameter Values		Device Resources[1]		
802.3ae State Machines	MDIO Interface	Slices	LUTs	FFs
No	No	1043	1189	1652
No	Yes	1116	1338	1753
Yes	No	1102	1349	1738
Yes	Yes	1204	1498	1835

1. All implementations require 4 block RAMs/FIFOs and 1 BUFG,

Virtex-4 FPGAs

Table 16 provides approximate slice counts for the various core options on Virtex-4 FPGAs.

Table 16: **Device Utilization – Virtex-4 FPGAs**

Parameter Values	Device Resources		
MDIO Interface	Slices	LUTs	FFs
No	1299	1417	1008
Yes	1635	1763	1105

Spartan-6 FPGAs

Table 17 provides approximate slice counts for the various core options on Spartan-6 FPGAs.

Table 17: **Device Utilization – Spartan-6 FPGAs**

Parameter Values		Device Resources		
802.3ae State Machines	MDIO Interface	Slices	LUTs	FFs
No	No	343	719	732
No	Yes	462	872	833
Yes	No	416	837	796
Yes	Yes	504	989	891

References

1. *IEEE Std. 802.3-2008*, Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications.
2. *IEEE Std. 802.3-2008*, Media Access Control (MAC) Parameters, Physical Layers, and Management Parameters for 10-Gb/s Operation.

Support

Visit www.xilinx.com/support for technical support. Xilinx provides technical support for this LogiCORE™ IP product when used as described in product documentation.

Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not listed in the documentation or if customized beyond that allowed in the product documentation, or if any changes are made in sections of the design marked *DO NOT MODIFY*.

Ordering Information

The LogiCORE IP XAUI core is provided free of charge under the terms of the Xilinx End User License Agreement. The core can be generated using the Xilinx ISE® Design Suite CORE Generator™ tool, which is a standard component of the Xilinx ISE Design Suite.

This version of the XAUI IP core does not require a license key. Previous versions of the XAUI IP core released in ISE Design Suite v11.2 and earlier did require a license key; see the version of the user guide for the version of the core you are using for information.

For more information, visit the XAUI product web page. Information about additional Xilinx LogiCORE IP modules is available at the Xilinx IP Center. For pricing and availability of other Xilinx LogiCORE IP modules and software, contact your local Xilinx sales representative.

Revision History

Date	Version	Revision
9/24/04	1.0	Initial Xilinx release in new data sheet format.
4/28/05	1.1	Document updated to support XAUI core v6.0 and Xilinx software v7.1i.
1/18/06	1.2	Updated dates, version number, and ISE tools 8.1i.
7/13/06	1.3	Updated core version to 6.2; Xilinx tools to 8.2i.
10/23/06	1.4	Updated core version to 7.0, added support for Virtex-5 LXT FPGAs.
2/15/07	1.5	Updated core version to 7.1; Xilinx tools to 9.1i.
8/8/07	1.6	Updated core version to 7.2; Xilinx tools to 9.2i.
3/24/08	1.7	Updated core version to 7.3; Xilinx tools to 10.1.
9/19/08	1.8	Updated core version to 7.4; added support for Virtex-5 TXT FPGAs.
4/24/09	1.9	Updated core version to 8.1; Xilinx tools to 11.1; added support for Virtex-6 FPGAs.
6/24/09	2.0	Updated core version to 8.2; Xilinx tools to 11.2; Added Virtex-6 CXT support.
09/16/09	2.1	Updated core version to 9.1; Xilinx tools to 11.3; Added Virtex-6 HXT, Virtex-6 Lower Power and Spartan-6 support.
12/02/09	2.1.1	Updated licensing information on page 15.
04/19/10	2.2	Updated core version to 9.2; Xilinx tools to 12.1
03/01/11	2.3	Updated core version to 10.1; Xilinx tools to 13.1
01/18/12	2.4	Summary of Core Changes Updated core version to 10.2; Xilinx tools to 13.4 Summary of Documentation Changes • Updated IP Facts table. Moved speed grades information to a new section and added speed grades for Virtex-7 and Kintex-7 devices • Updated Notice of Disclaimer and copyright notice • Replaced "MGT" with "serial transceiver" except when in signal names. • Removed two rows from Table 11 and 12. Removed four rows from Table 13. • Removed List of Acronyms. For the first occurrence of each acronym, spelled out occurrence followed by acronym. Example; Field Programmable Gate Array (FPGA)
04/24/12	2.5	Summary of Core Changes • Updated core version to 10.3; Xilinx tools to 14.1 • Added Supported S/W Drivers row to the IP Facts table • Removed External XGMII Interface

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